A 5.9 GHz DSRC Transmitter IC for Vehicle Wireless Communication System

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Abstract

This paper present a 5.9 GHz dedicated short range communication (DSRC) transmitter for wireless vehicular communication that satisfies specification of IEEE 802.11p standard mask c. The proposed transmitter consists of programmable gain amplifier (PGA), up-conversion mixer, drive amplifier, and synthesizer. Passive mixer, push-pull local oscillator (LO) buffer, and intermodulation distortion (IMD) canceller are applied to achieve high linearity and low power consumption. The transmitter is designed and fabricated on CMOS 0.18 μm process. The total power consumption is 63 mA at 1.8 V. A phase noise of synthesizer is -109.4 dBc/Hz at 1MHz offset. The transmitter total noise figure (NF) and adjacent channel leakage ratio (ACLR) are 14.2 dB and -53.6 dBc, respectively.

Keywords: DSRC, IEEE 802.11p, high linearity, power spectral density, passive mixer, noise figure (NF).

1. Introduction

For several decades, wireless vehicular communication (WVC) techniques have been rigorously developed for safety applications such as vehicle-to-vehicle (V2V) and vehicle-to-infrastructure (V2I) collisions in the United States. Dedicated short-range communication (DSRC) is particularly founded to be suited for WVC. The specific DSRC standards for WVC are developed and published in the IEEE 802.11p amendment [1], [2].

In order to meet the stringent transmitter spectral mask specification as shown in Figure 1, transmitter linearity specifications, OP1dB and OIP3, must be high enough to prevent harmonics from trespassing the mask [3]. This paper presents a high linearity 5.9 GHz DSRC transmitter that satisfies IEEE 802.11p standards transmit spectral mask c specification.

The remainder of the paper is organized as follows: Section 2, the topologies of the proposed transmitter important building sub-blocks are described, and each block's performance is also shown. In Section 3, chip fabrication and its performance measurements are displayed. The conclusion is written in Section 4

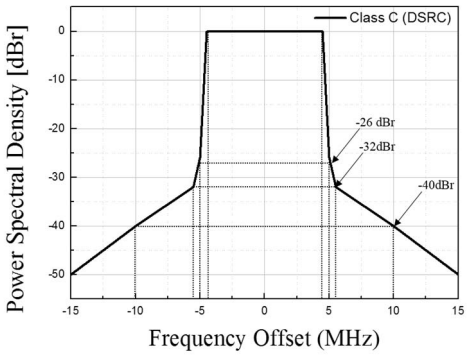

Fig. 1. Transmit Spectral Mask Class C (DSRC) in IEEE 802.11p

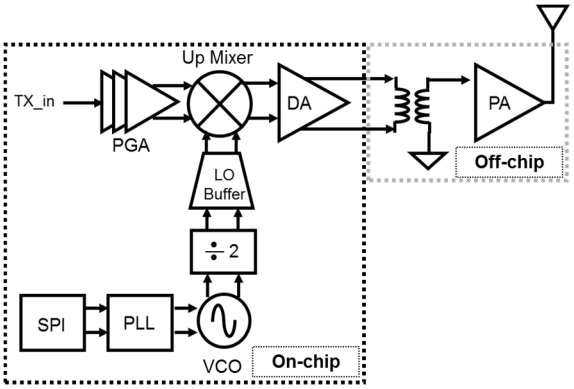

Fig. 2. Block Diagram of 5.9 GHz Transmitter for DSRC

2. Implementation of DSRC transmitter

Figure 2 shows the block diagram of the DSRC transmitter for the specification of IEEE 802.11p standard mask c. The transmitter consists of a programmable gain amplifier (PGA), a frequency up-converting mixer (UCM), a drive amplifier (DA), and a fractional-N PLL

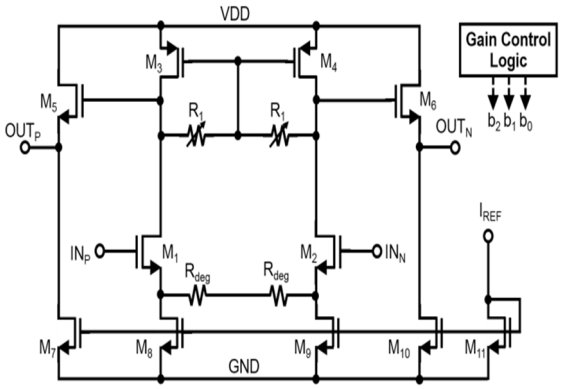

Fig. 3. Schematic of PGA

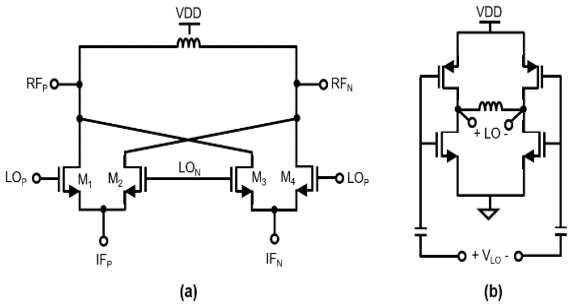

Fig. 4. Schematic of (a) Up-Conversion Passive Mixer and (b) Push-Pull LO Buffer

including a LO buffer. The voltage controlled oscillator (VCO) frequency is locked on 11.8 GHz, which leads 5.9 GHz frequency divider output. PGA is employed in DSRC transmitter in order to optimize the dynamic range of the IEEE 802.11p. The UCM and DA are designed to satisfy high linearity of transmit spectral mask c specification. In addition, the integrated fractional frequency synthesizer satisfies the specifications such as phase noise and spurious tone limitation in [4].

A. PGA

Figure 3 shows PGA schematic. The PGA is implemented differential degeneration architecture for precision gain step and good linearity. Furthermore, source follower buffers are used to drive relatively low passive mixer input impedance. The PGA differential gain is given by R1/Rdeg and is programmed by digitally changing R1 using Serial Peripheral Inter-face (SPI).

The PGA gain varies from 6 to 30 dB with 1 dB gain step. The transmitter total NF largely depends on the PGA NF, and the transmitter total noise floor can be defined as Equation (1). For an example, 14 dB transmitter total NF is required for 10 MHz bandwidth, 30 dB transmitter total gain, and -60 dBm transmitter output noise floor.

$$\overline{V_{n,out}^2}\big|_{dB} = NF_{dB} + 10\log A^2 + 4kTR_S|_{dB} + BW \quad (1)$$

B. Passive Mixer

A structure for a double balanced passive mixer is shown in Figure 4, which provides no power consumption and high linearity [5]. However, passive mixer requires higher LO swing amplitude than active mixer.

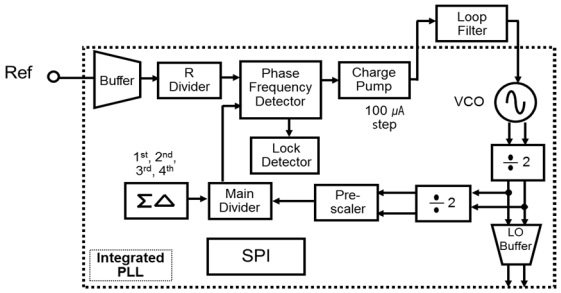

Fig. 5. Fractional-N PLL

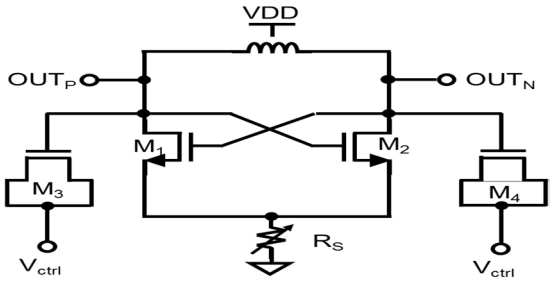

Fig. 6. Schematic of LC VCO

In order to optimize the passive mixer noise, the size of switch FETs (M1~M4) should be increased to reduce on-resistances, which, on the other hands, degrades the mixer gain and linearity [6]. In this paper, the size of the switch FETs is optimized for high linearity. In addition, a push-pull buffer (Figure 4 (b)) is introduced to get higher LO swing amplitude at given current, which enhance the mixer linearity [6]. Furthermore, the DC voltage of the LOp and LOn can be digitally programmed to achieve the best mixer linearity [7].

C. Frequency synthesizer

The fractional-N type PLL generates the 5.9 GHz LO signal with integrated LC-tank VCO and external 10 MHz reference oscillator. The PLL consists of phase frequency detector (PFD), charge pump (CP), VCO, pre-scaler, main divider, and delta-sigma modulator as shown in Figure 5. The CP current can be programmed from 100 μA to 1 mA with 100 μA current step. In addition, the delta-sigma modulator order can be programmed as 1st, 2nd, 3rd, and 4th for suppressing fractional spurious tones at different fractional numbers. The second frequency divider is implemented for lowering the 4/5 dual modulus pre-scaler input frequency.

The LC-tank VCO in this design is shown in Figure 6. The degeneration resistor (Rs), inductor, and active device size are properly chosen such that it reaches optimum performance. Using MOS varactors (M3 and M4), the VCO frequency is tuned to 11.8 GHz for avoiding DA or PA pulling. The VCO gain (Kvco) is 2 GHz/V, and noise and amplitude can be optimized by programming degeneration resistor, Rs, digitally [8]. The VCO consumes less than 2 mA.

3. Fabrication and measurement

The high linearity 5.9 GHz DSRC transmitter is implemented on 0.18μm 1P4M CMOS technology.

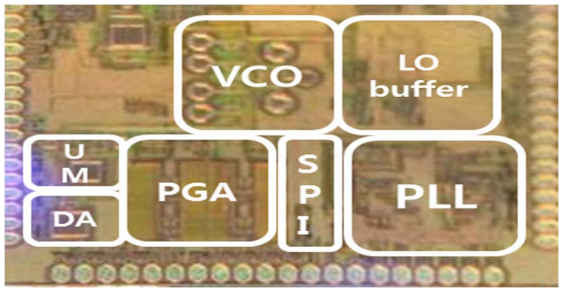

Fig. 7. Die Microphotograph of 5.9 GHz DSRC Transmitter

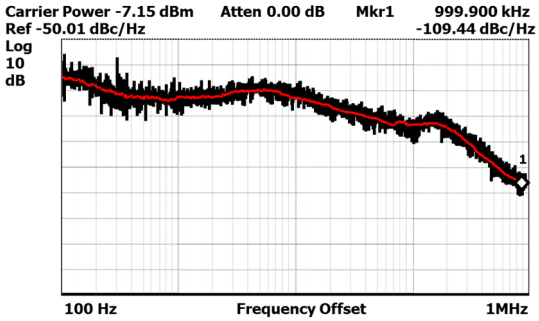

Fig. 8. PLL phase noise spectrum at 5.9 GHz

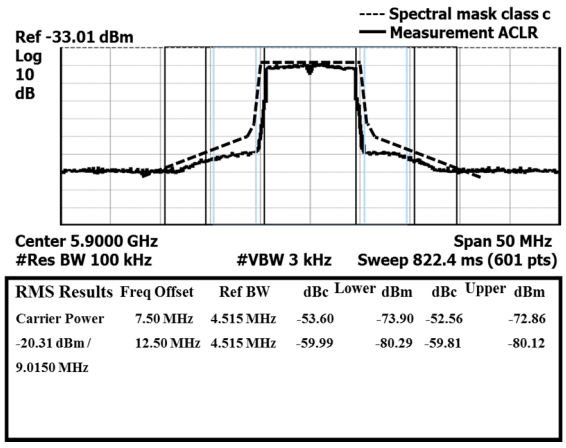

Fig. 9. Measurement Results of ACLR

Figure 7 shows the die microphotograph of fabricated transmitter with the total die size of 2400 µm X 1800 µm.

The PLL phase noise is -109.4 dBc/Hz at 1MHz offset (Figure 8). Transmitter total NF versus the PGA gain. The NF varies from 14.8 to 13.8 dB.

Figure 9 shows the ACLR spectrum of the DSRC transmitter. The ACLR of the transmitter was measured to be 53.6 dBc at 5.9 GHz signal with 10 MHz bandwidth, which satisfies IEEE 802.11p transmit spectral mask c specification. The overall performance of the 5.9 GHz DSRC transmitter is summarized in Table I.

4. Conclusion

This paper demonstrates a high linearity transmitter for the IEEE 802.11p standard applications. By employing IMD canceller structure for drive amplifier and passive mixer, low power consumption and high linearity can be achieved.

TABLE I: PERFORMANCE SUMMARY

Parameter	Unit	This work
Supply	V	1.8
Operating Frequency	GHz	5.9
Phase noise (△f=1MHz)	dBc/Hz	-109.4
ACLR	dBc	-53.6
TX Chain current	mA	53
Synthesizer current	mA	10
Noise Figure	dB	14.2

The proposed transmitter shows an ACLR lower than -53.6 dBc and an average total noise figure 14.2 dB is obtained. The PLL phase noise is -109.4 dBc/Hz at 1 MHz offset. The transmitter meets specifications for the wireless vehicular communication defined in IEEE 802.11p amendment.

Acknowledgement

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