Tutorial Introduction

PURPOSE:

- This tutorial describes concepts related to communication busses, including attributes, functions, and the different types of bus systems. The intent is to provide a baseline of knowledge related to the Freescale product line.

OBJECTIVES:

- Define basic terminology and concepts related to bus communication.
- Describe bus operations and the different types of communication.
- Identify the attributes of the main bus types.
- Match a bus type to application requirements.
- Describe Freescale's portfolio of bus ICs.

CONTENT:

- 48 pages
- 8 questions

LEARNING TIME:

- 90 minutes

This tutorial introduces concepts related to communication busses, including features, functions, and the different types of bus systems. We will examine the main bus types, identifying key attributes for each type. We will discuss how to prioritize bus attributes when selecting a bus for a specific application. Finally, we will introduce Freescale's portfolio of bus ICs.

Although there is no prerequisite for this tutorial, some experience with bus communication would be helpful.

Communication Bus

- A communication bus, or simply bus, is a one- or two-wire media onto which electrical devices are connected at points on the bus for the purpose of communicating.
  - The DSI bus, in addition to providing the communication media, also provides operational power for the bus device.
- The purpose of a bus is to minimize the wire necessary to pass data between two or more devices.

Let’s begin by defining a communication bus. For the purpose of this training, a communication bus, or simply a bus, relates to a one- or two-wire media onto which electrical devices are connected at points on the bus for the purpose of communicating. In the case of DSI, the bus also supplies power to the bus device. The purpose of a bus is to minimize the wire needed to pass data between two or more devices.

In this tutorial, we will present bus attributes to consider when matching a bus type to an application.

Some Bus Types

Bus Name	Bus Type
CAN (Controller Area Network)	Differential
DSI (Distributed System Interface)	Single Ended or Differential
ISO 9141 K-Line (International Standards Organization)	Single Ended
ISO 9141 K/L-Line (International Standards Organization)	Single Ended (Both K & L)
SAE J 1850 (Society of Automotive Engineers)	Single Ended or Differential
LIN (Local Interface Network)	Single Ended
SWCAN (Single Wire Controller Area Network)	Single Ended

There are many different types of wire busses used for communication, some of which are provided in the table. Each bus has a different performance and application, as we'll discuss later in this tutorial.

The Controller Area Network bus, or CAN bus, is normally a two-wire differential bus, but is capable of continued operation in a single ended fault tolerant mode.

The Distributed System Interface bus, or DSI bus, is either a single ended or differential bus.

The International Standards Organization ISO 9141 bus has two versions: a single ended K-Line bus, or two single ended K and L-Lines.

The Society of Automotive Engineers J 1850 specification, or SAE J 1850 bus, is either a single ended or a differential bus.

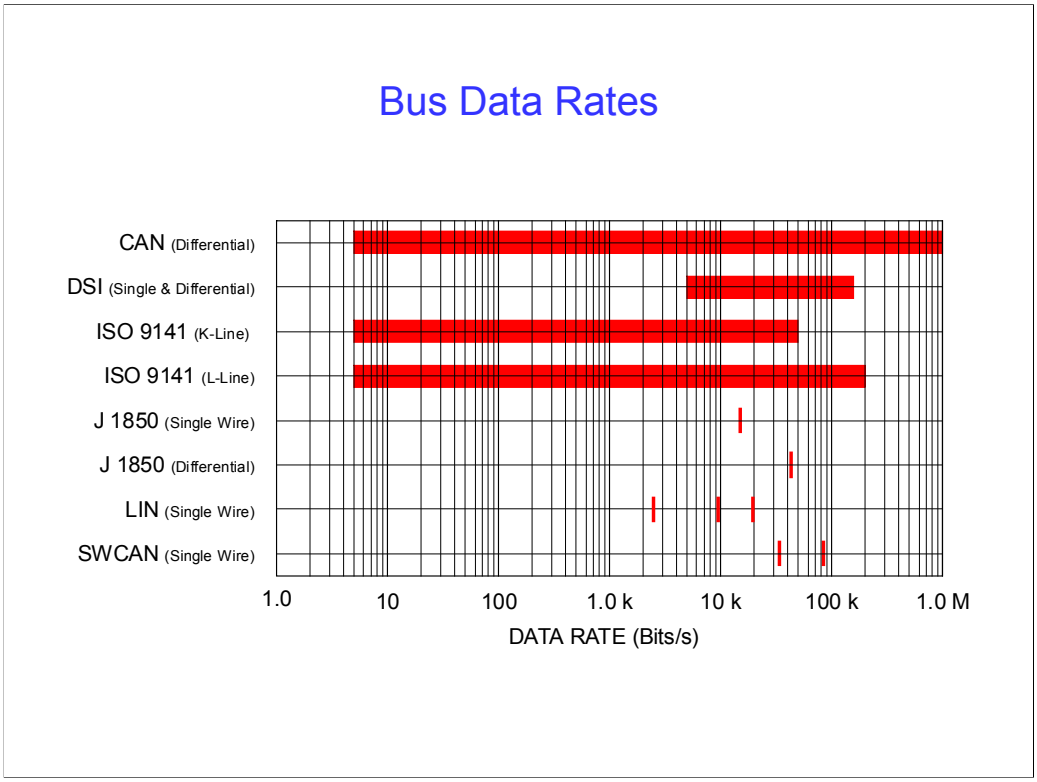
The Local Interface Network bus, or LIN bus, is a single ended bus.

The Single Wire Controller Area Network bus, or SWCAN bus, is a dedicated single ended bus.

Why Different Bus Types?

- **System Cost**
- Different bus data rates
- Single or multiple Microcontroller
- Unidirectional or Bi-Directional communication
- Simplex or Full Duplex
- Number of devices on the bus
- Physical Layer requirements
- Message error detection
- Message “through-put”
- Bus bandwidth efficiency
- Balanced or unbalanced line
- Differential or single-wire
- Radiated Electro-Magnetic Interference (EMI)
- Noise environment
- Noise immunity

The list of attributes for the various bus types is long, but as noted, the primary consideration is typically system cost, since this drives marketability. Every application will have specific requirements, yet if cost targets are not met for the application, all other attributes are secondary. Bus systems must be engineered so as to provide the performance necessary for the application at an affordable cost.



One of the most important bus attributes is the bus data rate. Some bus types, such as the J 1850 and SWCAN, define specific data rates that the bus is to operate at. Other busses are used over a broad range of data rates. As shown here, the CAN bus has the highest data rate, with the DSI and ISO 9141 K and L-Line busses as close seconds.

In addition to bus speed, each bus has many differentiating features and functions.

Physical Layer

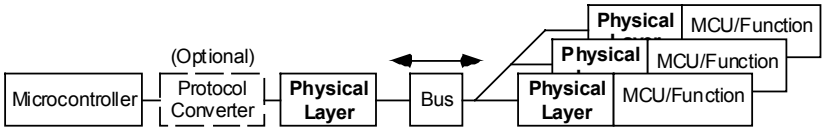
- A Physical Layer refers to circuitry that translates Microcontroller logic-level signals into bus-level voltage and current signals, and vice versa.
- Microcontroller defines the logic-level signals.
- Microcontrollers are designed for transmitting data short distances.
  - Inadequate for distant bus transmission, particularly in noisy environments
- Physical Layers convert Microcontroller signals to voltage and current signals appropriate for distant bus transmission.
- Physical layers are designed for single-wire or two-wire bus systems.

Logic level signals are defined by the system microcontroller. A Physical Layer refers to the circuitry that translates the microcontroller logic signals into bus voltage and current signals. In reverse fashion, the Physical Layer translates the bus voltage and current signals into logic signals for the microcontroller.

Microcontrollers have a lot of horsepower when it comes to computing, but they are only satisfactory for transmitting data short distances. This means that microcontrollers cannot deliver signals that need to be transmitted long distances, particularly in noisy environments. The Physical Layer fulfills this translation requirement for both Unidirectional and Bi-Directional bus communication needs.

Next, let’s examine how Physical Layers are used in a typical bus communication system.

Physical Layer Example



- A Microcontroller “talks” to the Physical Layer, which produces the appropriate signals for transmission over the bus.
  - Bus signals are received by the receive Physical Layer and passed to the Function
- The Physical Layer can include internal Waveshaping to reduce harmonic signal generation
- In Bi-directional systems, the Function “talks” to it’s Physical Layer circuit, which sends data back over the Bus to the Microcontroller
- An optional Protocol Converter:
  - Converts Microcontroller signals into bus protocol signals, and visa versa.
  - Can have memory buffers to off-load the protocol burden from the Microcontroller.

An example of how a Physical Layer is used in a typical bus communication system is shown here.

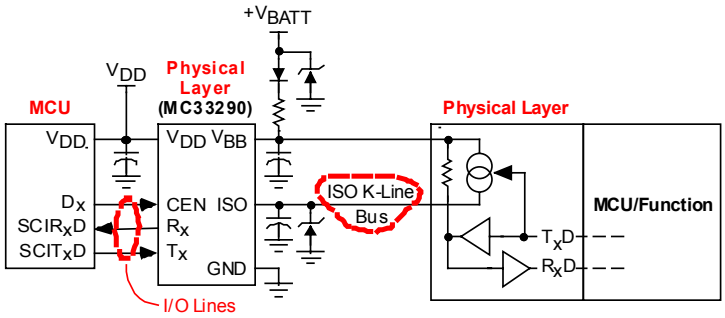
Disregarding the optional Protocol Converter, the Microcontroller “talks” to it’s Physical Layer circuit, which in turn produces the appropriate signals for transmission over the Bus. At the other end of the Bus, other similar Physical Layers convert the Bus signals back into signal levels to be used by a specific MCU/Function, for example a switch or a sensor. Typically each bus device associated with a Physical Layer has a name or address used for communication identification. This enables communication from the Microcontroller to be directed to a specific MCU/Function device.

In a Bi-Directional system, the opposite process occurs; a MCU/Function “talks-to” or “responds-back” to the Microcontroller.

The Physical Layer can have built-in wave-shaping circuits to control the slope of bus level transitions of voltage and current. Waveshaping greatly reduces the generation of unwanted harmonic signals. A very fast or abrupt bus level change in either voltage or current will generate high levels of harmonic signals, which can radiate to other devices or systems and cause interference. In contrast, slow changing sinusoidal signals generate lower levels of harmonic signals at higher frequencies where harmonic levels are most important.

In some instances, a Protocol Converter is placed between the Microcontroller and it’s associated Physical Layer. The purpose of the Protocol Converter is to convert the Microcontroller signals into bus protocol signals, and to convert the bus protocol signals back into signals that the Microcontroller can read. Often the Protocol Converter contains Bi-Directional memory buffers for temporary data storage. This greatly off-loads the messaging burden from the Microcontroller, thereby making the Microcontroller available for other tasks.

Physical Layer Control



- Physical Layer Control on the Microcontroller side
  - Data is sent and received by the Microcontroller to the Physical Layer
  - Generally implemented with parallel I/O lines for performance (speed) and simplicity of the Physical Layer circuitry (cost)
- Physical Layer control on the Function side
  - Typically integrated in the control front-end of the Function device to efficiently meet requirements and cost considerations
- Protocol Converter Control I/O is the same as the Physical Layer
  - Parallel I/O

Here is a specific example of Physical Layer control. The ISO 9141 K-Line bus is used with an MC33290 Physical Layer.

The Microcontroller interfaces with the Physical Layer for control and message handling using Microcontroller parallel I/O ports. Parallel control lines provide a simple means of control with optimal speed performance. This method is by far the most predominate means of connecting the two devices.

The ISO K-Line bus connects the two Physical Layers together for communication purposes. For simplicity, only two devices are shown, but it is important to note that many Physical Layers can be connected to the same bus.

At the other end, the Physical Layer is typically integrated into the front end of the MCU/Function device. By combining the Physical Layer with the MCU/Function, maximum performance at minimum cost is attained.

Bus Nodes

- A Node is a position on a bus where a Physical Layer resides.
- A bus typically has many Nodes.
- Nodes can be occupied by microcontrollers, sensors, or function control devices.
- Nodes are used to gain access to bus communication. Examples include:
  - Control motors, actuators, and trigger mechanisms
  - Report status
  - Any other activity requiring remote wired communication

A Node is a connection point on the bus where a Physical Layer resides. Typically, a bus has many Nodes. Nodes can be occupied by microcontrollers, sensors, or function control devices. They are located at the devices that require communication access to the bus.

As shown in the previous example, the Physical Layer can either stand alone or be integrated into a device MCU/Function. In general, Physical Layers used with microcontrollers stand alone due to the large disparity in voltages used by the two devices. Microcontrollers are typically low voltage devices, while Physical Layers involve relatively high voltages.

Mastering

- Masters are used to manage bus operations.
- There are Single and Multi-Master bus systems.
  - Each Master in a bus system typically requires a microcontroller.
  - Only one Master is allowed to assume Mastership of the bus at any time to eliminate bus contentions.
- Multi-Master system
  - Advantage
    - Ability to control the bus from more than one Node
  - Disadvantages
    - Bus access availability is dependent on activity.
    - Time critical systems have to be designed for very high speeds to guarantee message delivery in worst case time.
    - Multiple Masters increases the complexity of the system.

Next, let's discuss the concept of mastering. Mastering refers to devices that are used to manage bus operations. Bus systems can have multiple Masters, but only one is allowed to have control of the bus at any time. This eliminates bus contentions or bus messaging conflicts that can occur simultaneously between two or more Nodes. Typically, microcontrollers are used as Masters.

Although there can be an advantage in controlling the bus from different Nodes, there are also disadvantages. Access to the bus may be limited when there is high bus traffic. To guarantee that a message will be delivered in a worst case time requires that very high bus speeds be incorporated in order to handle all communication activity. In addition, the use of multiple Masters greatly increases the system's complexity and cost.

Bus Protocol

Bus Type	Protocol
CAN	Manchester type coding scheme with defined voltage levels and differential wire drivers
DSI	Bus power plus time high relative to time low at defined voltage and current levels
ISO 9141	Ground and battery levels with a defined Manchester type coding scheme
J 1850	Variable Pulse Width (VPW) and Pulse Width Modulation (PWM) at defined bus voltage levels
LIN	Protocol similar to Computer Com or SCI ports using RS-232
SWCAN	Same protocol as CAN except with a single wire driver

Bus Protocol refers to the systematic scheme employed to transfer data using voltage and/or current level wave shapes relative to time and/or each other. As shown in the table, each bus system uses a protocol unique to it's design and purpose.

The CAN bus uses a Manchester type of coding scheme with defined voltage levels and differential wire drivers.

DSI uses an entirely different scheme of supplying bus power plus time high relative to time low (or PWM) at defined voltage and current level signals.

ISO 9141 uses Ground and Battery level signals coupled with a defined Manchester type coding scheme.

J 1850 uses yet another scheme of Variable Pulse Width (or VPW) and Pulse Width Modulation signals at defined bus voltage levels.

LIN uses a protocol that is similar to that used in Computer Com or SCI ports using RS-232.

The SWCAN bus uses the same protocol as CAN except with a single wire driver.

Question

Which of the following is a TRUE statement about bus data rates? Click on your choice.

a) Differential CAN is only used for very high data transfer rates of 1.0 MBits/s.
b) Single Wire CAN is only used for very low data rate transfer applications.
c) ISO 9141 bus systems can only be used at defined data rates.
d) DSI is used for both high and low data rate applications.

Let's review what we've discussed so far with a couple of questions.
Consider this question about bus data rates.

Correct! Differential CAN buses are usable over a wide range of data rates, as are DSI, ISO 9141, and LIN busses. DSI is specifically designed to track the data rate of the Master and change data rates on a bit-by-bit basis making the system very desirable in applications having varying degrees of radiated EMI as the situation requires.

Question

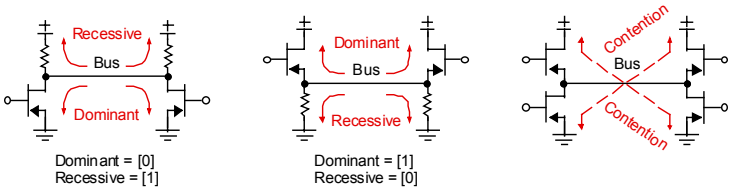
Which of the following statements defines Bus Protocol? Click on your choice.

a) The hierarchical method employed to recognize a specific node address on a bus for communication purposes
b) A systematic scheme used to transfer data using voltage and/or current level wave shapes relative to time and/or each other
c) A term relating to bus timing signals used to communicate over a bus media
d) An encoding and decoding method common to all bus communication

Here's another question for you.

Correct! Bus Protocol is the systematic scheme employed to transfer data using voltage and/or current level wave shapes relative to time and/or each other.

Dominant vs. Recessive



- Dominant and Recessive relate to how the High or Low voltage state of the communication bus is attained.
  - Dominant state: Bus voltage is pulled high or low by means of an active switch element
  - Recessive state: Bus is pulled high or low by means of a passive element
- Contention exists when the bus voltage is simultaneously challenged for opposing bus signal states by two or more Nodes using their active switch elements.
  - Contentions must be resolved before meaningful communication can occur.
  - Systems typically guard against and resolve Contention issues in software and/or hardware.
  - Dominant / Recessive contentions are resolved by the Dominant “over-powering” the Recessive.
  - Simultaneous Dominant High / Dominant Low contentions are not allowed by bus design (see diagram at right).

Let’s continue with a discussion of bus operations. The terms Dominant and Recessive refer to how the High or Low voltage state of the communication bus is attained.

A Dominant state is when the bus voltage is pulled high or low by means of an active switch element, such as a transistor. The transistor involvement is shown in the examples above. The bus can be pulled to ground by either transistor on the bus as shown in the left circuit, or to the positive rail by either transistor on the bus as shown in the middle circuit.

A Recessive state is when the bus is pulled high or low by means of a passive element, such as a resistor influencing the bus level when the active transistor element is switched OFF. When the transistors are switched OFF, the resistors pull the bus to the positive rail in the left circuit and to ground in the middle circuit.

When the bus voltage is simultaneously challenged for an opposing bus signal state by two or more Nodes using their active switch elements, a state of Contention exists. Contentions are analogous to the chaos created by a lot of people talking at the same time. For meaningful communication to occur, Contentions must be resolved as to who “talks” when and who “listens.” Bus communication is no different; order must be established. Systems normally guard against and resolve Contention issues through various software and/or hardware schemes. Dominant / Recessive contentions are resolved by the Dominant over-powering the Recessive.

Bus designs do not allow Dominant High / Dominant Low contentions as is shown in the right circuit. Contentions of this type are typically designed-out of the hardware by adopting a bus system using either the left or middle circuit but never the right circuit.

Collision Handling

- Ability to resolve simultaneous Dominant / Recessive signal collision conflicts
  - Advantages
    - Non-destructive collision
    - Allows prioritization of signals
    - No bus recovery time required
- Contention Back-Off
  - When two (or more) Node devices attempt simultaneous signaling, Contention occurs and is resolved by having all devices but one stop transmitting (back-off).
    - Resolution is solved in software programming.
    - Devices in contention back off per a pre-established priority system.
    - One device continues transmitting without loss of time.
  - Advantages
    - Higher data speeds are possible by using higher drive power.

Collision Handling is the ability of a system to resolve simultaneous Dominant/Recessive signal collisions. As was mentioned earlier, Dominant signals over-power Recessive signals in contention, and a device sending a Recessive signal while sensing a Dominant signal on the bus stops transmitting. This allows the device sending the Dominant signal to continue transmitting. The collision process is non-destructive and makes signal prioritization possible without occurring any loss in bus utilization.

Contention Back-Off is when two or more Node devices attempt simultaneous signaling; Contention occurs and is resolved by having all devices but one stop transmitting. The resolution is solved in the software program with the devices in contention backing off per a pre-established priority system, allowing one device to continue transmitting without any loss of time. The big advantage to this scheme is that it allows bus speeds to remain relatively low for a given through-put, making even higher bus speeds possible by using higher drive power.

Contention Back-Off resolution is a very powerful scheme that maintains efficient use of the bus and allows lower bus speeds. A detailed example of Contention Back-Off is provided on the next page.

Collision “Back-OFF”

Bit	1	2	3	4	5	6	7	
Node “A” Signal	1	0	1	1	0	1	1	Node “B” Senses a Conflict ([1] is Dominant, has Priority)
Node “B” Signal	1	0	1	0	1	0	0	Node “B” Ceases Transmission (“Backs-OFF”)
Resulting Bus Signal	1	0	1	1	0	1	1	Uninterrupted Node “A” Bus Signal

- Two simultaneous signals are sent from Nodes A and B.
- Also shown are the results of combining the two signals
  - A value of [1] has priority over [0] and is Dominant
- Both A & B signals agree with each other for bits 1, 2, and 3.
- Contention occurs for bit 4.
  - [1] wins over [0], so A signal is Dominant
  - Resulting bus signal is a [1] (same as Node A).
  - Node B backs-off.
  - Node A continues transmitting.
- Back-Off does not interrupt or delay the Node A transmission.
- Note: In contrast, Ethernet bus signals in contention require all Nodes to stop transmitting followed by a random wait and retry. This method incurs data transfer delays.

This example demonstrates how Collision Back-Off works. The example uses two signals, Nodes A and B, both attempting to send signals on the bus at the same time. To keep the system working, all Nodes operating on the bus must constantly monitor the bus status.

For bit 1, Node A sends a 1, as does Node B; the resulting bus signal is a 1.

For bit 2, Node A sends a 0, as does Node B; the resulting bus signal is a 0.

For bit 3, the Nodes are also in accord; the resulting bus signal is a 1.

For Bit 4, the Node signals differ**.** Node A sends a 1 while Node B sends a 0, and contention occurs. To resolve this contention, ground rules must be agreed upon. In this example, a 1 is dominant with priority over a 0. With Node A sending a 1 and Node B sending a 0, the resulting bus signal is a 1. Node B senses the 1 signal and realizes the presence of a Dominant on the bus.

At this point, Node B backs-off and immediately stops sending data. This allows Node A to continue sending data without any delay or interruption.

In contrast, an Ethernet bus, as commonly used in telecommunication systems, requires that all Nodes stop transmitting when a contention occurs and to wait a random time before attempting a retry. If a Node wins out on attempting a retry, the Node continues to transfer data. If though, another contention occurred, all the Nodes would again stop transmitting and again wait a random time before attempting a retry. This effectively becomes a signal game of chance. This process produces data transfer delays and does not fully utilize bus time as efficiently. As a result, a bus of this type must push for ever higher speeds to make-up for the time lost to guarantee that a message will be delivered within a specified time.

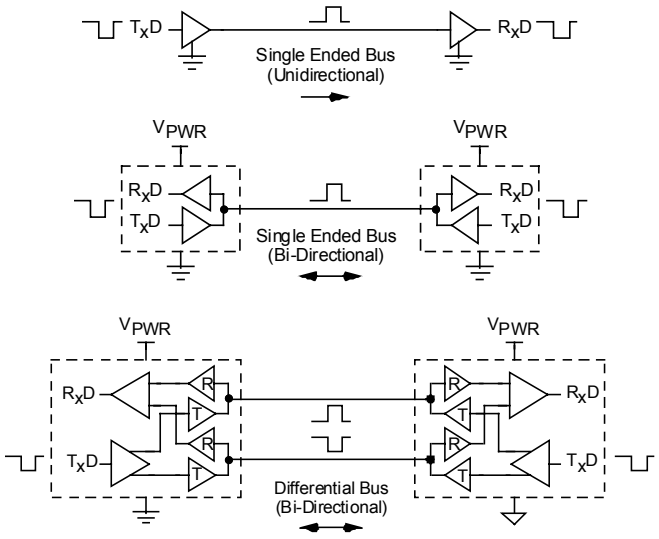
Determinism

- Determinism describes the degree of access a Master has to the bus at any particular time.
- Collision Handling greatly impacts the degree another Master has to the bus.
- If a Master is “talking”, a second Master must wait until the first Master either finishes transferring data, initiates a break, or in some other way recognizes and yields to the presence of the second Master
- Full Determinism is where a Master has immediate access to the bus at any time.

The term Determinism describes the degree of access a Master has to the bus at any particular time. Collision Handling greatly impacts the degree another Master has to gain control of the bus. If a Master is “talking”, a second Master will have to wait until the first Master either finishes transferring data, initiates a break, or in some other way recognizes and yields to the presence of the second Master.

Full Determinism is where a Master has immediate access to the bus at any time.

Single Ended and Differential Busses



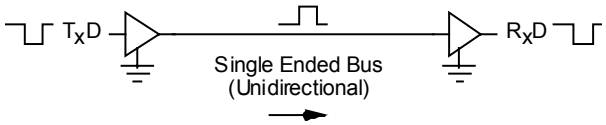
Next, let's examine the different types of bus systems. The main types are shown here.

There are two types of Single Ended bus systems, those that can transfer data in one direction only and those that can communicate in both directions. The Single Ended Bi-Directional bus has obvious advantages over the Unidirectional bus, but at a higher cost.

The Differential Bi-Directional bus provides the greatest performance in speed, but also costs the most.

Let's take a closer look at each bus system.

Unidirectional Bus

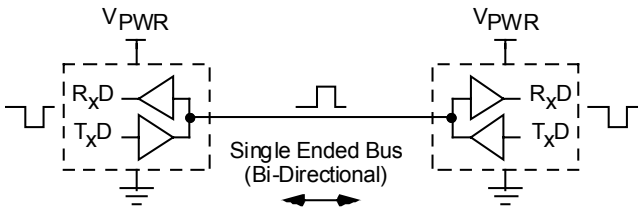


- Advantage
  - Minimal board space
  - Very simplistic system
  - Minimal system cost
- Disadvantage
  - One way communication only
    - Addressed Nodes are unable to communicate back
  - Difficult to have more than one “talker” on the bus
- Used in applications where one-way communication is acceptable

The Unidirectional Bus has the disadvantage of a sender not being able to receive a reply. The system does have the advantage of using devices that require little board space, are simple, and cost the least. Unidirectional Bus systems can have more than one “talker” on the bus, although this is difficult to manage efficiently.

Unidirectional systems are used in applications where one-way communication is acceptable.

Bi-Directional Bus

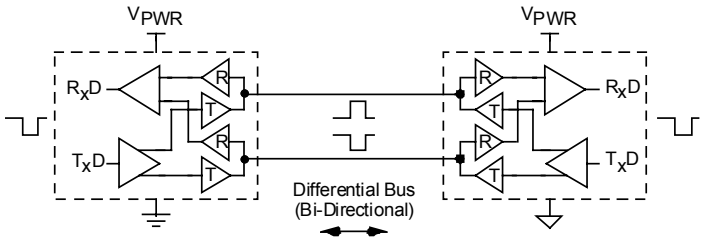


- Advantage
  - Two-way communication between Nodes
  - Simpler system than Differential Bi-directional Bus
- Disadvantage
  - Single Ended systems cannot tolerate large ground differences between Nodes.
    - Single Ended signal thresholds are referenced to ground.
- Used where Bi-directional communication is necessary and where desired data rates will not cause radiated EMI problems.

Shown is the Single Ended Bi-Directional Bus. It has the obvious advantage of being able to communicate in both directions, but it also requires more complex devices at a higher cost than those used in a Unidirectional system. Another disadvantages is that the system cannot tolerate large ground differences between Nodes. This is an important consideration, since the Single Ended Bus system relies solely on signals that are referenced to ground.

The single Ended Bi-directional Bus is used where two-way communication is necessary and where desired increases in data rates will not cause radiated EMI problems.

Differential Bi-Directional Bus



- Advantage
  - More tolerant of ground offset voltages between Nodes
    - Signaling thresholds are differentially referenced
  - Much higher bit rate capability with lower radiated EMI
- Disadvantage
  - Main disadvantages are higher cost and complexity.
- Used where two-way communication is needed for low to high speed communication in noisy or noise sensitive environments.

The Differential Bi-Directional Bus is capable of very high data rates and lower radiated Electro-Magnetic Interference, or EMI. The bus signals are differential, and, as a result, larger ground offset voltages are tolerated between Nodes. System cost is the main disadvantage brought about by the added wire, system complexity, speed, and low radiated EMI performance.

The Differential Bi-directional Bus is used where two-way communication is needed for low to high speed communication in noisy or noise sensitive environments.

Question

Complete the following statement: Collision "Back-Off" Resolution requires _____. Click on your choice.

a) Signals in contention to stop transmitting while allowing one remaining signal to continue transmitting without interruption or delay.

b) All parties to cease transmitting and to attempt a retry according to a pre-established software priority.

c) One transmitting device on the bus to Back-Off while the other re-transmits it's data.

d) The last signal to access the bus to Back-Off allowing the first signal to continue.

Let's review with a couple of questions. Consider this question about Collision Back-off Resolution.

Correct! When simultaneous independent signals sent from different bus nodes are in contention conflict with each other, the signal node or nodes in contention will sense the presence of other signals on the bus and cease transmitting. This allows the remaining node to continue transmitting without any interruption or delay in the data transfer.

Question

Which of the following statements about Single Ended Bi-Directional Bus systems is NOT true? Click on your choice.

a) They are simpler than Differential Bi-Directional Bus systems.
b) They provide two-way communication between multiple nodes.
c) They are more tolerant of ground differences than Differential Bus systems.
d) They are used where desired increased data rates will not cause radiated EMI problems.

Here's a question for you about Single Ended Bi-Directional Bus systems.

Correct! Single Ended Bi-Directional Bus systems solely reference their signals to ground, and for that reason they cannot tolerate the existence of large ground differences between Bus Nodes. Therefore, choice c is NOT true.

Simplex (Half-Duplex)

- Simplex, or Half-Duplex, describes a communication protocol relating to message sequencing.
- Simplex Bi-Directional communication is conducted in one direction at a time.
  - Only one “talker” at a time is allowed to communicate to one or more “listeners.”
  - For example, people usually communicate with one talker at a time.
  - If everyone talks at once, this can result in chaos and conflicts.
  - Conflicts must be resolved for meaningful communication.
- Simplex communication uses bus bandwidth less efficiently than Full-Duplex.

Let’s continue with a look at the main communication protocols.

Simplex, or Half-Duplex, describes a communication protocol related to message sequencing. Simplex Bi-Directional communication is conducted in one direction at a time. Since talking occurs in one direction at a time, the other talking direction is idle. As a result, Simplex communication utilizes bus bandwidth less efficiently as compared to systems that talk simultaneously in both directions.

Next, let’s look at Full-Duplex, which allows communication in two directions at once.

Full-Duplex

- Full-Duplex is simultaneous communication in two directions.
- Typically it incorporates a bi-modal voltage-current bus protocol.
  - Outgoing messaging: Voltage level signaling (as from Master to Node.
  - Incoming messaging: Current loading signals (as from Node to Master)
- Advantages
  - Twice as many bits can be transferred for a given bit rate.
  - Uses bus bandwidth very efficiently.
- Disadvantage
  - More complex system requiring more complex devices be used
- Full-Duplex is frequently used in applications where lower EMI is needed for a given data through-put.
  - Lower data rates tend to lower the radiated EMI.

Full-Duplex refers to simultaneous communication in two directions. Typically it uses a bi-modal voltage-current bus protocol to keep signals separated and to eliminate conflicts. An example might be for an outgoing messaging, say from a Master to a Node, to use voltage transitions for signaling, whereas a simultaneous incoming message, as from the Node to the Master, might use bus current loading levels for signaling.

The advantage of Full-Duplex is that twice as many bits of data can be transferred for any bit rate for any given duration. As a result, bus bandwidth is used more efficiently. Since bus bandwidth utilization is very high, data rates can often be reduced while still providing the specified through-put. This results in lower radiated EMI.

Compared with Half-Duplex, Full-Duplex requires a more complex system and requires more complex devices. Often, Full-Duplex is applied when lower radiated EMI is needed for a given data through-put.

Half- vs. Full-Duplex

- Half-Duplex (Sequenced two-way communication)
  - Less overhead burden for the Master microcontroller to support
  - Half the bits transferred for a given duration
  - Slower communication cycle through-put for a given bit rate
- Full-Duplex (Simultaneous two-way communication)
  - Faster communication cycle through-put with the same bit rate
  - Slightly higher system cost compared to Half-Duplex
  - Reduced bit rates and radiated EMI where through-puts are the same

A comparison of Half- and Full-Duplex is shown here.

Half-Duplex places less overhead on the Master microcontroller for support. It has half the number of bits transferred for a given duration, and slower communication cycle through-put for a given bit rate.

In comparison, Full-Duplex has faster communication cycle through-put with the same bit rate, and a slightly higher system cost. Where the through-puts are the same, data rates can be reduced, so as to realize lower radiated EMI.

Error Detection Types

- Cyclical Redundancy Check (CRC)
  - Error checking scheme capable of catching more than one bit in error
  - CRCs are more than one bit in length.
- Framing Error Check
  - Detects an incorrect number of bits in a frame (data field)
- Parity Error Check
  - Checking is performed on segmented data streams to determine the correctness of the data received.
  - The total number of binary 1's or 0's is always even or always odd.
  - Disadvantage: Might not signal an error if more than 1-bit of error exists.
    - For More than 1-bit error, correct only if there is an odd number of errors.
    - Incorrect if there are is an even number of total bits in error, meaning errors will go undetected.

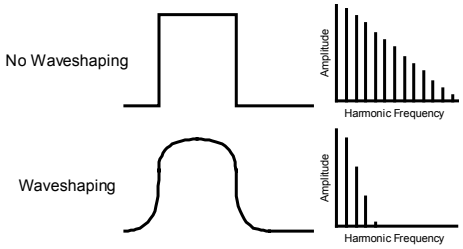
Next, let's discuss issues related to signal integrity and bus functions, beginning with error detection. The three principle types of error detection are described here.

Cyclical Redundancy Checking, or CRC, is capable of catching more than 1-bit in error.

Framing Error Checking counts to see if an incorrect number of bits has been received in a frame or data field.

Parity Error checks are performed on segmented data streams to determine the correctness of the data received. In this method of error detection, the total number of binary 1's or 0's is always even or always odd. The disadvantage of Parity Checking is that it is only accurate for detecting 1-bit of error, meaning multiple bit errors may go undetected.

Waveshaping



- Voltage and Current Waveshaping is a means controlling the signal slope to reduce the harmonic level of bus signals resulting from voltage and current signal transitions
  - Harmonic signals can interfere with the performance of other systems.
  - Pure sinusoidal signals do not generate harmonic signals.

As previously discussed, some Physical Layers implement waveshaping. Waveshaping is a means of controlling the slope of voltage and current signals sent over a bus, so as to reduce the harmonic content level of bus signals. Fast transitions of voltage or current are rich in harmonic content, equating to high levels of radiated EMI that can interfere with the performance of other systems. In contrast, a pure sinusoidal signal does not generate harmonic signals.

Shown here are two examples of signals, one with and one without waveshaping.

Wake-Up

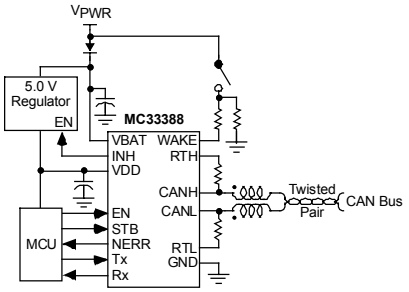
- Wake-Up associated with communication devices relates to a circuit or device that is in a limited operational state (sleep state) recognizing the presence of a signal and responding by becoming fully functional.
  - Typically, devices to go into a sleep state to conserve power either upon command or as a result inactivity occurring for some period of time.
  - Command sleep states are forced, and no activity sleep states are automatic.
- Device Wake-Up signals can come from different sources. Examples include:
  - Serial Peripheral Interface (SPI) inputs from the microcontroller
  - Dedicated parallel inputs with signals from the microcontroller or other circuitry
  - Activity signals present on the bus
  - Special bus voltage levels or signals

For communication devices, wake-up refers to a circuit or device in a limited operational state or sleep state. When the device recognizes the presence of a signal, it responds, or “wakes-up”, by becoming fully functional. Devices enter a sleep state to conserve power, either on command or as a result of inactivity. Command sleep states are forced, and inactivity sleep states are automatic.

Device Wake-Up signals can come from many different sources. Example sources include: Serial Peripheral Interface (SPI) inputs from the microcontroller; Dedicated parallel inputs with signals from the microcontroller or other circuitry; sensed bus signals being present; and Special bus voltage levels or signals.

Inhibit Output

- Inhibit output: function associated with a signal to activate or turn-ON another device or circuit
- The MC33388 is a prime example.
  - CAN communication device with a sleep mode feature
  - A Wake-Up signal deactivates the Inhibit signal.
  - The deactivated Inhibit signal can, as shown in this case, be used to enable a voltage regulator.
- Useful for applications critical of power conservation



An Inhibit output is a function associated with a signal to activate or turn-ON another device or circuit. An Inhibit feature is very useful for applications requiring power conservation.

The example shown uses the MC33388. The MC33388 is a CAN communication device with a sleep mode feature. When the MC33388 is in a sleep state, a Wake-Up signal received via the bus or the dedicated Wake input will deactivate the Inhibit signal.

This signal can be used to enable a voltage regulator to provide full operation power to the MC33388 and the controlling microcontroller.

Shared Power and Data Bus

- Bus systems can be designed to supply both power for remote bus devices and to conduct communication operations.
  - Supplies enough power for small sensors, indicators, and control devices.
  - Reduces wiring and power conditioning.
- Example: DSI Bus design
  - Supplies operational power to remote Nodes, from the Host Microcontroller Physical Layer.
  - Provides Full-Duplex Bi-Directional communication.

A Shared Power and Data Bus system can be designed to supply both power for remote bus devices and conduct communication operations. This type of system can provide enough power for small sensors, indicators, and control devices. Also, this system greatly reduces wiring and power conditioning requirements.

An example is the DSI Bus. This bus is designed to supply operational power to remote Nodes, from the Host Microcontroller Physical Layer, and provide Full-Duplex Bi-directional communication.

Question

Which of the following is a TRUE statement? Select all that apply and then click Done.

Half-Duplex is sequenced two-way communication.

Full-Duplex is simultaneous two-way communication.

Half-Duplex has slow communication cycle “through-put” for a given bit rate as compared to a Full-Duplex system.

Full-Duplex has slow communication cycle “through-put” for a given bit rate as compared to a Half-Duplex system.

Done

Consider this question about Half-Duplex and Full-Duplex communication. Can you identify the true statements?

Correct! The first three statements are true, and the last statement is false. The main advantage of Full-Duplex is that it can conduct simultaneous two-way communication and as a result has a faster cycle “through-put” of data for the same bit rate as that of a Half-Duplex system.

Question

Which of the following statements is NOT true? Click on your choice.

a) Waveshaping is a term applied to controlling the slope of voltage and current signals.
b) A transmitted square wave signal has a very high harmonic frequency content.
c) A transmitted sinusoidal signal has a very high harmonic frequency content.
d) Harmonic signals can cause interference with other systems.

Here's another question for you. Can you identify which statement is NOT true?

Correct! This statement is NOT true, since a sinusoidal signal contains the fundamental frequency only and does not generate any harmonic signals.

CAN Bus

- Used where high data transfer speed performance is paramount.
- Data rate
  - 5.0 Bits/s to 1.0 MBits/s (dynamic range)
- Bi-Directional Half-Duplex communication
- Manchester type of signal coding
- Differential Bus (two-wire bus)
  - Requires more expensive bus wire
  - Bus is EMI affected by the wire used
  - Includes signal waveshaping
- Fault tolerant capability
  - If one of the bus wires is lost, continues to function with increased radiated EMI.
- Error detection
  - CRC
  - Parity
  - Framing
- Dominant / Recessive Contention Handling
  - Collision Back-Off
- Supports Multi-Masters (microcontrollers).

Now that we have discussed the main concepts, features, and functions related to communication busses, let's examine the key attributes of each type of bus, beginning with the CAN bus.

The CAN bus is used primarily in high speed data transfer applications. It is a high performance Bi-directional Half-Duplex bus that is capable of differential data rates up to 1.0 MBit/s using a Manchester type of signal coding. The CAN bus will perform equally well at data rates down to 5.0 Bits/s.

Signal waveshaping is incorporated to attain the higher data rates and reduce the radiated EMI levels. The CAN requires a higher cost twisted pair bus wire to be used for the higher data rates for minimized radiated EMI.

The bus is fault tolerant of one bus wire "opening"; that is, the communication process will continue if one of the bus wires becomes disabled, but with an increase in the radiated EMI as a result of the unbalanced bus operation.

The CAN bus has good error detection with the capability to perform CRC, Parity, and Framing error checks.

In addition, the CAN bus has Dominant/Recessive Contention Handling with Collision Back-Off, and supports the use of multiple Masters.

DSI Bus

- Data rates
  - 5 Kilobits/s to 150 Kilobits/s
- Full-Duplex communication
- Pulse Width Modulated (PWM) Signal Coding
- Automatic data rate tracking
  - Bit-to-bit automatic adjusting to Master
- Supports a Single Master (microcontroller)
  - Full Determinism
    - Immediate access availability by the Master to communicate on the bus
- Signaling and power to Nodes on the same wire
- Single Ended and Differential Bus
  - Differential Bus
    - Lower radiated EMI
    - Fault tolerant
      - If one bus wire is lost, bus continues to function with increased radiated EMI.
- Signal waveshaping for lower EMI
- Error detection
  - 4-Bit CRC
  - Framing

The Distributed Serial Interface (DSI) bus is a high performance Full-Duplex Bi-Directional bus capable of data transfer rates of 5 Kilobits/s to 150 Kilobits/s. The Full Duplex operation means the DSI uses bus bandwidth efficiently.

The DSI bus is unique in several ways. The Pulse Width Modulated signal coding affords all devices operating on the bus the ability to self-adjust to abrupt bit-to-bit changes in the data rate. Data can be sent at a slow rate for remedial routine operations and can immediately change to a high data rate for time sensitive critical operations. Aiding this performance is Full Determinism, where the DSI Master microcontroller has immediate access to communicate on the bus at whatever data rate the situation requires. Another unique capability of the DSI bus is to provide operational power for the Node devices in addition to providing a communication media.

The DSI bus can fully operate in either the Single Ended Bus mode or the Differential Bus mode. The Differential mode exhibits a lower radiated EMI than the single ended mode of operation. Signal waveshaping is incorporated to minimize the radiated EMI.

4-Bit CRC and Framing error checks are supported.

ISO 9141

- ISO Bus Specification for vehicle to diagnostic tester communication
- First communication standard adopted by California Air Resources Board (CARB).
  - Other states have adopted similar legislation.
- Clean air legislation requirements mandate on-board diagnostic systems.
  - The standard affects all new cars sold in those states.
  - ISO 9141 and J 1850 are now approved standards for these requirements.
- Single-Ended K-Line
  - Bi-Directional
  - Used to transfer data and address information between the tester and the vehicle's microcontroller initialization.
- L-Line
  - Unidirectional and optional
  - Used to download data to the vehicle's microcontroller at a high speed during system initialization.
- The ISO 9141 bus has many industrial heavy equipment applications outside of automotive.

ISO 9141 is an International Standard Organization bus specification for vehicle to diagnostic tester communication. This standard was initially adopted by the California Air Resources Board, or CARB, mandating on-board diagnostic systems to meet clean air legislation requirements. The standard has been adopted in other states, and effects all new cars sold in those states. The J 1850 specification is another bus system used to meet clean air legislation requirements.

The ISO 9141 specification supports two different K and L-Lines. The Single-Ended K-Line is used to transfer Bi-directional data and address information during initialization between the tester and the vehicle's microcontroller. The L-Line is unidirectional and optional, and is used to download data to the vehicle's microcontroller at a high speed for initialization purposes. The features of the ISO9141 K-Line and L-Line are described on the following pages.

Please note that The ISO 9141 bus has many industrial heavy equipment applications outside of automotive.

ISO 9141 (K-Line)

- Data rates
  - 5 Bits/s to 50 Kilobits/s (K-Line)
- Bi-Directional Half-Duplex bus communication
- Manchester type of signal coding
- Single Ended Bus
  - Signal waveshaping
- Dominant / Recessive Contention Handling
  - Collision Back-Off
- Error detection
  - 8-bit CRC
  - Parity
  - Framing
- Supports Multi-Masters (microcontrollers)

The ISO 9141 K-Line is a Bi-Directional Half-Duplex bus capable of data transfer rates of 5 Bits/s to 50 Kilobits/s using a Manchester type of signal coding. The K-Line provides Signal waveshaping and Dominant/Recessive Contention Handling with Collision Back-Off. Three types of error checking are implemented: 8-bit CRC, Parity, and Framing error checks. In addition, multiple Masters are supported.

ISO 9141 (L-Line)

- Data rates
  - 5 Bits/s to 200 Kilobits/s (L-Line)
- Unidirectional Communication
- Manchester type of signal coding
- Single Ended Bus
  - No signal waveshaping
- Dominant / Recessive Contention Handling
  - Collision Back-Off
- Error detection
  - 8-bit CRC
  - Parity
  - Framing
- Supports Multi-Masters (microcontrollers)

The ISO 9141 L-Line is Unidirectional and capable of data transfer rates of 5 Bits/s to 200 Kilobits/s using a Manchester type of signal coding. The L-Line is very useful for high speed downloading purposes. The L-Line uses Dominant/Recessive Contention Handling with Collision Back-Off.

As with the K-Line, the L-Line provides three error detection types and supports multiple Masters.

J 1850

- Data rates
  - Single Wire: 10.4 Kilobits/s Variable Pulse Width (VPW) Coding
  - Differential Wire: 41.6 Kilobits/s Pulse Width Modulated (PWM) Coding
- Bi-Directional Half-Duplex communication
- Differential Bus (two-wire bus)
  - Bus is EMI sensitive to the wire used
    - High quality twisted-pair reduces radiated EMI
  - Signal waveshaping
- Fault tolerant capability
  - If one bus wire is lost, bus continues to function with increased radiated EMI.
- Dominant / Recessive Contention Handling
  - Collision Back-Off
- Error detection
  - 8-Bit CRC
- Supports Multi-Masters (microcontrollers)
- J 1850 is an SAE standard specification for on-board diagnostic communication to meet clean air standards legislation required of U.S. vehicles.
- The J 1850 bus has many industrial heavy equipment applications outside of automotive.

J 1850 is both a Bi-Directional Half-Duplex Single and Differential wire bus. Single wire operation uses Variable Pulse Width coding at 10.4 Kilobits/s. Differential operation uses Pulse Width Modulation coding at 41.6 Kilobits/s.

Signal waveshaping is incorporated to reduce the amount of radiated EMI. Differential operation keeps the radiated EMI to minimum levels as does the use of high quality twisted-pair lines.

The bus is fault tolerant, meaning the communication process will continue if one bus wire opens, but with an increase in the radiated EMI as a result of the unbalanced bus operation.

The J 1850 bus has Dominant/Recessive Collision Handling with Contention Back-Off, provides 8-Bit CRC error detection, and will support the use of multiple Masters.

Like the ISO 9141, the J 1850 bus standard specification for on-board diagnostic communication to meet clean air standards legislation required of U.S. vehicles. Also, the J 1850 bus has industrial heavy equipment applications outside of automotive.

LIN

- Data rates
  - 2.4, 9.6, and 19.2 Kilobits/s
- Bi-Directional Half-Duplex Communication
- Coding is similar to standard UART Serial Communication Interface (SCI)
- Single Ended Bus
  - Signal waveshaping
- Dominant / Recessive Contention Handling
  - Collision Back-Off
- Error Detection
  - 1-byte checksum field
- Supports Single Master (microcontroller)

The Local Interconnect Network, or LIN, bus transfers data at suggested rates of 2.4, 9.6, or 19.2 Kilobits/s in a Bi-Directional Half-Duplex manner over a single wire. The LIN uses a coding scheme that is similar to that used with a standard UART Serial Communication Interface (SCI).

The bus has signal waveshaping to reduce radiated EMI, Doninant/Recessive Contention Handling with Collision Back-Off. The LIN bus also uses a one byte checksum field for detecting errors, and supports a single Master.

SWCAN

- Data rates
  - 33.3 Kilobits/s and 83.3 Kilobits/s
- Manchester type of signal coding
- Bi-Directional Half-Duplex Communication
- Single Ended Bus
  - Signal waveshaping
- Error detection
  - CRC
  - Parity
  - Framing
- Dominant / Recessive Contention Handling
  - Collision Back-Off
- Supports Multi-Masters (microcontrollers)

The last bus type we'll examine is the Single Wire Controller Area Network, or SWCAN. This bus is a single Bi-Directional Half-Duplex bus for 33.3 Kilobits/s and 83.3 Kilobits/s communication using a Manchester type of signal coding. Waveshaping is incorporated to keep radiated EMI to a minimum.

The SWCAN bus offers good error detection, with the capability of performing CRC, Parity, and Framing error checks. In addition, the SWCAN bus has Dominant/Recessive Contention Handling with Collision Back-Off. The bus also supports the use of multiple Masters.

Bus Summary

	Type					Data Rate							Features											Coding			
	Single Ended Bus	Differential Bus	Unidirectional	Half-Duplex	Full-Duplex	5 Bit/s to 1.0 MBits/s	5 Bits/s to 20 kBits/s	5 Bits/s to 200 kBits/s	5 kBits/s to 150 kBits/s	10.4 kBits/s	41.3 k Bits/s	5 Bits/s to 20 kBits/s	33.3 kBits/s & 83.3 kBits/s	Supports Multiple Masters	Node Operating Power Supplied over Bus	Automatic Variable Data Rate Tracking	Bus Signal Waveshaping	Fault Tolerant Capable	Dominant / Recessive Contention Handling	Contention Back-Off Ability	Full Determinism	CRC Error Checking	Parity Error Checking	Framing Error Checking	Manchester Type Coding	Variable Pulse Width Coding	Pulse Width Modulation Coding	SCI / UART Type Coding
CAN		●		●	●	●								●			●	●	●	●		●	●	●	●			
DSI	●	●			●				●						●	●	●	●	n/a	n/a	●	●					●	
ISO 9141 K-Line	●			●			●							●			●		●	●		●	●	●	●			
ISO 9141 L-Line	●		●					●						●					●	●		●	●	●	●			
SAE J 1850	●	●		●						●	●			●			●	●	●	●		●				●	●	
LIN	●			●								●		●			●		●	●			●	● [1]				●
SWCAN	●			●									●	●			●		●	●		●	●	●	●			

NOTES:
1. 1 byte checksum field

This table shows the various buses along with their associated type and data rates. Please note that you can access additional information about bus features and coding using the Features button at the top of the course page.

Note that Dominant/Recessive Collision Handling and Back-Off Collision Handling are not applicable for the DSI bus. This bus typically uses a single Master with Full Determinism, meaning the Master has instant access to the bus at any time. This capability is very important for time critical applications, for example automotive airbag deployment applications. Also note that the DSI is the only bus in the matrix that has Full-Duplex communication.

The ISO 9141 K-L-Line bus is a two-wire bus, but it is not a differential bus. The K and L-Lines are used for separate protocols. As previously noted, the K-Line is for Bi-Directional Half-Duplex communication, while the L-Line is for Unidirectional communication.

Question

Which of the following statements describes the CAN bus? Select all that apply and then click Done.

Differential bus supporting Bi-directional communication at data rates up to 1.0 MBits/s

Supports multi-masters and has Dominant / Recessive Contention Handling

Designed for high data rates only and for that reason is more expensive

Has CRC, Parity, and Framing Error capability

Done

Let's review key bus attributes with a couple of questions. Consider this question about the CAN Bus.

Correct! The CAN bus is a two-wire differential Half-Duplex Bi-directional bus supporting data rates of 5 kBits/s to 1.0 MBits/s. It supports multi-masters and has Dominant / Recessive Contention Handling. It has good error detection, supporting CRC, Parity, and Framing Error capability.

Question

Which of the following are attributes of the J 1850 bus? Select all that apply and then click Done.

Low EMI Unidirectional bus system
Supports multiple Masters (microcontrollers)
Dominant/Recessive Contention handling capability
Has both 8-Bit CRC and Parity error detection capability
Supports data rate of 10.4 kBits/s using Variable Pulse Width coding

Done

Here's another question for you. Can you identify which of the items listed are attributes of the J 1850 bus?

Correct! The J 1850 is a Bi-directional Half-Duplex one- or two-wire bus having low radiated EMI. It supports multiple Masters and Dominant/Recessive Contention handling with Collision Back-Off. When using Variable Pulse Width coding, the J1850 supports a data rate of 10.4 kBits/s.

Note that the J 1850 supports only 8-bit CRC error detection (not Parity).

EMI Considerations

- Electro-Magnetic Interference (EMI)
  - Radiated EMI can cause electronic devices and systems to malfunction or degrade in performance.
- Faster bus transitions cause higher spectral frequency components, which increases the radiated EMI.
- Slower bus transitions reduce the bus data rate possible.
- Low pass filters used to filter out EMI must have their cut-off frequency high enough to allow the bus communication signal to pass through.
  - Some unwanted RF energy might get into the IC and cause interference.
  - Higher capacitance filtering requires the bus drive power to be increased to maintain a given level of performance.
  - Larger capacitors are less effective above their SRF, and actually become inductive at higher frequencies.

EMI considerations impact the selection of a bus system, since radiated EMI from the bus can cause other electronic devices and systems to malfunction or degrade in performance. Some of the factors related to EMI are described here.

Faster bus transitions cause higher spectral frequency components, which increase the radiated EMI. Yet, slower bus transitions reduce the bus data rate.

Low pass filters can be used to filter out the EMI, although these components introduce other considerations. Low pass filters must have their cut-off frequency high enough to allow the bus communication signal to pass through. Even with filters, some unwanted RF energy may still get into the IC and cause interference. Higher capacitance filtering requires the bus drive power to be increased to maintain a given level of performance. The use of larger capacitors is less effective above their self resonant frequency, or SRF, and these components can actually become inductive at higher frequencies. The reason for this is beyond the scope of this training. The important thing to note is that larger capacitors used at high frequencies do not necessarily bypass as well as smaller capacitors.

Selection Considerations

1. System cost
2. Through-put data rate requirement
    - High or low data rate
3. Unidirectional or Bi-Directional communication requirement
4. Balanced Differential (2-wire) or Unbalanced (single wire) Bus
    - EMI
    - Fault tolerance level
5. Number of Masters on the bus
    - Dominant / Recessive Collision Handling
    - Back-Off Collision Handling
    - Level of Determinism
        - Level of access to bus communication
    - Level of error checking
6. Shared Node operating power supply and signaling over the bus

Shown is an approach one might consider when selecting a bus system. The consideration priorities might change depending on the application.

First and foremost, you should always keep an eye on the overall system cost.

Next in importance is usually the rate of data through-put, followed by the type of communication. Should the system provide Unidirectional or Bi-Directional communication?

Would a single-wire system be adequate? Or is a differential system needed for reasons of high speed, low radiated EMI, or fault-tolerant operation?

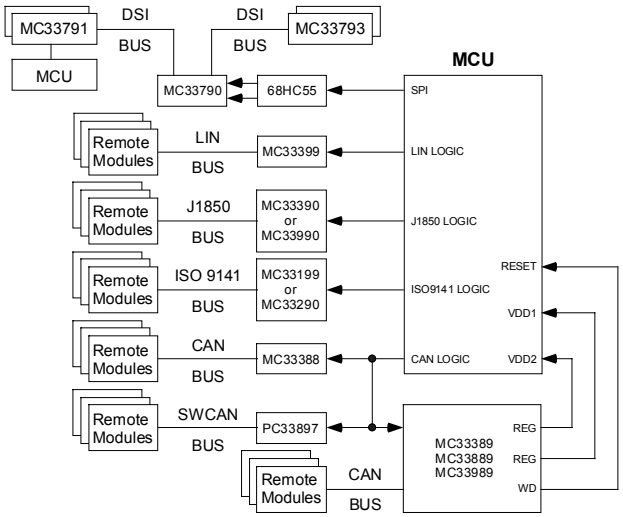
Another consideration is how many Masters are required on the bus? Will one Master suffice, or are multiple Masters needed? If one Master is required, Dominant/Recessive Collision Handling and Back-Off Collision Handling considerations can be eliminated. Also, in the case of one Master, data rates can possibly be reduced by using the Full-Duplex DSI bus having full Determinism.

What level of error checking is required? Will 1-bit error checking suffice, or are 4, 8, or 16 bits required? Note that higher levels of error checking add to system management and system cost.

Does it make sense to supply operational power over the bus line along with data?

Please note that the order of priority of these selection considerations is not fixed. In general, once you've addressed the issues of data rate and whether bi-directional communication is required, the other considerations tend to fall into line.

Freescale Offered Bus Systems



Shown here is the family of bus systems and devices offered by Freescale, along with some of their associated peripheral devices and how they connect to various microcontrollers.

Please note that you can access a detailed summary of the device attributes on the following page. The tables provide a more detailed comparison of the various wired communication devices.

Device Attributes

Wired Communication

Device Application/Function/Protection/Feature/Control Cross Reference

Device	Com Protocol: LIN	SAE J1850 Class B	ISO 9141	CAN	DSI	Voltages: Operating Voltage (V)	5.0 V V_{DD} Required	Bus Output: ISO K-Line	Differential CAN	Single Ended	Bi-Directional Half-Duplex	Bi-Directional Full-Duplex	Data Rate: 10.4 kBits/s	10 kBits/s to 125 kBits/s	>50 k Bits/s (max)	<83.333 kBits/s	<20 kBits/s	120 kBits/s	<500 kBits/s	5 to 150 kBits/s Bit-to-Bit Variable
MC33290			•			8.0 to 18	•	•		•					•					
MC33388				•		5.5 to 27	•		•		•			•						
MC33389				•		5.5 to 27			•					•						
MC33390		•				9.0 to 16				•	•		•				•			
MC33394				•		3.5 to 26.5			•		•								•	
MC33399	•					7.0 to 27				•							•			
MC33790					•	8.0 to 25	•			•		•								•
MC33793					•	7.0 to 30				•		•								•
MC33794			•			7.0 to 27		•		•								•		
MC33889				•		5.5 to 27			•		•			•						
PC33897				•		7.0 to 18	•			•						•				
MC33990		•				9.0 to 16				•	•		•				•			

Device	Reg. Supply Out: 5.0 V V_{DD}	5.0 V	Switched V_{PWR}	Current Limiting	Overtemperature Shutdown	Protection: Bus - Short Circuit Protected	Current Limiting	Overtemperature Shutdown	Undervoltage Shutdown	Open Ground Shutdown	Features: Sleep and/or Standby Mode	Wake-Up Output	Inhibit Output	Automatic Single/Differential Bus Modes	Supports Unshielded Twisted Wire Bus	Bus Signal Waveshaping	Undervoltage Detection	Watch-Dog	Reset or Interrupt Output	Status or Fault Reporting	Input Control: Enable Input	Wake-Up Inputs	Binary Mode Select	SPI Mode Select	SPI Input Control	Parallel Input Control
MC33290						•		•			•					•					•					•
MC33388						•		•			•		•	•	•	•	•			•	•	•	•			•
MC33389	•	•	•			•		•	•		•			•	•	•	•	•	•			•		•		•
MC33390						•		•		•						•										•
MC33394						•		•				•		•	•	•	•			•					•	
MC33399							•	•					•			•					•	•				•
MC33790							•	•								•										•
MC33793		•							•							•										
MC33794		•														•										
MC33889	•	Adj	•	•	•	•					•			•	•	•	•	•	•	•		•			•	•
PC33897						•		•	•	•	•	•				•					•					•
MC33990						•	•	•			•					•				•	•			•		•

Content for pg 47

Tutorial Completion

BUS type

- CAN
- DSI
- ISO 9141 K-line
- ISO 9141 K/L-line
- SAE J 1850
- LIN
- SWCAN

Selection Criteria

- System cost
- Data through-put
- Unidirectional or Bi-Directional communication
- Single-wire bus or Differential (two-wire) bus (two-wire)
- Number of Masters on the bus
- Error checking
- Node operating power and signaling over the bus

Note: Additional information is provided in the device Fact Sheets. These sheets can be found in the Communication section of the Analog ICs Integrated Solutions Marketing “Pitch Pak.”

This concludes our tutorial on communication busses. In this tutorial, we introduced concepts related to busses, including features, functions, and operations. We examined the different types of busses and discussed their distinguishing characteristics. We also introduced Freescale’s portfolio of bus ICs.

To further your understanding of Freescale’s Wired Communications portfolio, we recommended that you read the Fact Sheets for the different devices. The device Fact Sheets can be found in the Communication section of the Analog ICs Integrated Solutions Marketing “Pitch Pak.”

We hope this training module has expanded your knowledge of wired bus communications, and has acquainted you with the product line. Thank you for your time, dedication, and diligence, and above all, Happy Communicating!