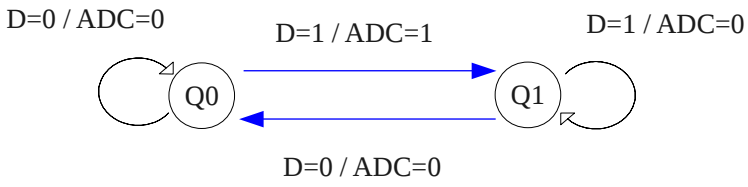
FreeMCAn - programmable logic array configuration

V-I: Edge to level trigger w. extra cycle glitch cancellation

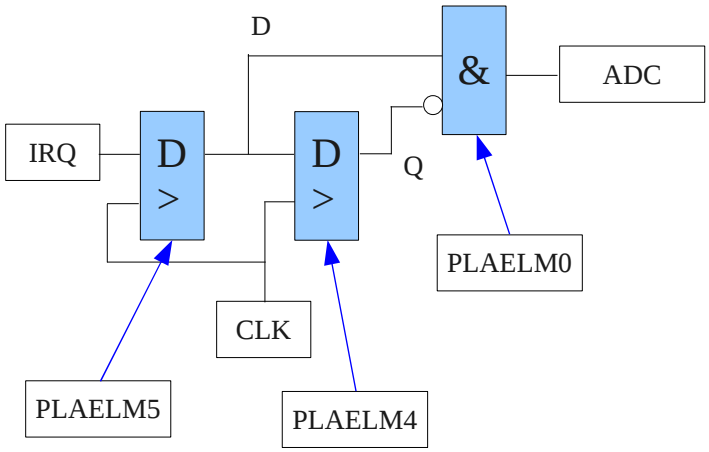
Karnaugh map No	Verbal	D[n]	Q[n]	ADC[n]	Q[n+1]
0		0	0	0	0
1		0	1	0	0
2		1	0	1	1
3		1	1	0	1

D[n] = Debounce (IRQ[n])
Q[n+1] = D[n]
ADC[n] = [D*NOT(Q)][n]
FALSCH
FALSCH
WAHR
FALSCH



ADC[n]

D[n] \ Q[n]	0	1
0	0 (0)	0 (1)
1	1 (2)	0 (3)



Legend:

IRQ:	AD–conversion trigger. Rising / falling edge configurable (PLAELM5)
ADC:	PLA output trigger for ADC module (1 = convert)
CLK:	Use HCKL (for freeMCAn with divider = 41.78 Mhz)

Timing:

HCLK	41780000	Hz
PLA clks delay & jitter	2	
ADC prescaler	2	
ADC Acquisition time	8	
ADC Bit trial+WR	19	
Total:	1,39	us
Track & hold only	0,48	us

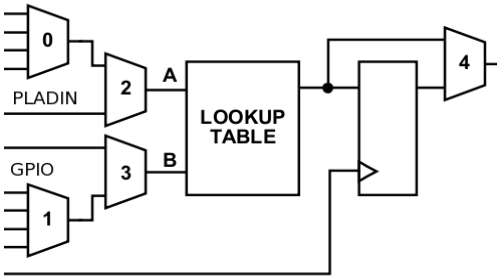
Feedback Configuration

PLAELMx Bit No	Value	PLAELM 0		PLAELM 1 to 7		PLAELM 8		PLAELM 9 to 15	
10:9 (MUX0)	00	Element	15	Element	0	Element	7	Element	8
	01	Element	2	Element	2	Element	10	Element	10
	10	Element	**4**	Element	4	Element	12	Element	12
	11	Element	6	Element	6	Element	14	Element	14
8:7 (MUX1)	00	Element	1	Element	1	Element	9	Element	9
	01	Element	3	Element	3	Element	11	Element	11
	10	Element	**5**	Element	**5**	Element	13	Element	13
	11	Element	7	Element	7	Element	15	Element	15

ADC trigger

Pin selection on MUX3 and MUX2 input and MUX4 output

	PLA Block 0		PLA Block 1		
Element	Input	Output	Element	Input	Output
0	P1.0	P1.7	8	P3.0	P4.0
1	P1.1	P0.4	9	P3.1	P4.1
2	P1.2	P0.5	10	P3.2	P4.2
3	P1.3	P0.6	11	P3.3	P4.3
4	P1.4	P0.7	12	P3.4	P4.4
5	**P1.5**	P2.0	13	P3.5	P4.5
6	P1.6	P2.1	14	P3.6	P4.6
7	P0.0	P2.2	15	P3.7	P4.7

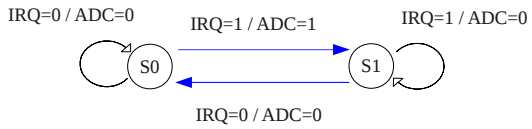


		Configuration			
Port	Pin	00	01	10	11
0	P0.0	GPIO	CMP	MS0	PLAI[7]
	P0.1	GPIO	PWM2H	BLE	
	P0.2	GPIO	PWM2L	BHE	
	P0.3	GPIO	TRST	A16	ADCBUSY
	P0.4	GPIO/IRQ0	PWMTRIP	MS1	PLAO[1]
	P0.5	GPIO/IRQ1	ADCBUSY	MS2	PLAO[2]
	P0.6	GPIO/T1	MRST		PLAO[3]
	P0.7	GPIO	ECLK/XCLK	SIN	PLAO[4]
1	P1.0	GPIO/T1	SIN	SCL0	PLAI[0]
	P1.1	GPIO	SOUT	SDA0	PLAI[1]
	P1.2	GPIO	RTS	SCL1	PLAI[2]
	P1.3	GPIO	CTS	SDA1	PLAI[3]
	P1.4	GPIO/IRQ2	RI	CLK	PLAI[4]
	P1.5	GPIO/IRQ3	DCD	MISO	PLAI[5]
	P1.6	GPIO	DSR	MOSI	PLAI[6]
	P1.7	GPIO	DTR	CSL	PLAO[0]
2	P2.0	GPIO	CONVSTART	SOUT	PLAO[5]
	P2.1	GPIO	PWM0H	WS	PLAO[6]
	P2.2	GPIO	PWM0L	RS	PLAO[7]
	P2.3	GPIO		AE	
	P2.4	GPIO	PWM0H	MS0	
	P2.5	GPIO	PWM0L	MS1	
	P2.6	GPIO	PWM1H	MS2	
	P2.7	GPIO	PWM1L	MS3	
3	P3.0	GPIO	PWM0H	AD0	PLAI[8]
	P3.1	GPIO	PWM0L	AD1	PLAI[9]
	P3.2	GPIO	PWM1H	AD2	PLAI[10]
	P3.3	GPIO	PWM1L	AD3	PLAI[11]
	P3.4	GPIO	PWM2H	AD4	PLAI[12]
	P3.5	GPIO	PWM2L	AD5	PLAI[13]
	P3.6	GPIO	PWMTRIP	AD6	PLAI[14]
	P3.7	GPIO	PWMSYNC	AD7	PLAI[15]
4	**P4.0**	GPIO		AD8	PLAO[8]
	P4.1	GPIO		AD9	PLAO[9]
	P4.2	GPIO		AD10	PLAO[10]
	P4.3	GPIO		AD11	PLAO[11]
	P4.4	GPIO		AD12	PLAO[12]
	P4.5	GPIO		AD13	PLAO[13]
	P4.6	GPIO		AD14	PLAO[14]
	P4.7	GPIO		AD15	PLAO[15]

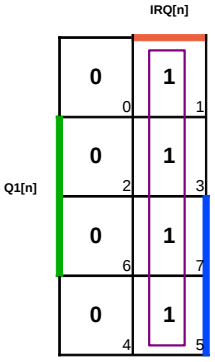
V-II: Alternate MOORE implementation / one cycle (non prefered solution)

Truth table MOORE – State machine (Folgeschaltverhalten)

Karnaugh map	Verbal	$Q0^n$	$Q1^n$	IRQ^n	$Q0^{n+1}$	$Q1^{n+1}$	
0		0	0	0	0	0	Q1[n+1]=Not(Q0[n])*IRQ[n]
1		0	0	1	1	1	FALSCH
2		0	1	0	0	0	WAHR
3		0	1	1	1	1	FALSCH
4		1	0	0	0	0	WAHR
5		1	0	1	1	0	FALSCH
6		1	1	0	0	0	FALSCH
7		1	1	1	1	0	FALSCH

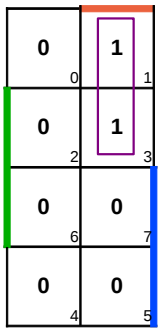


Q0[n+1]



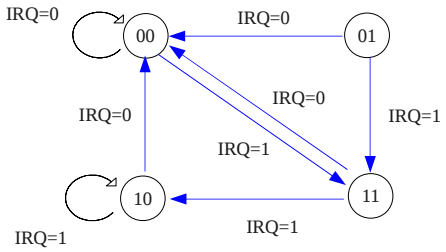
Q0[n+1]=IRQ[n]

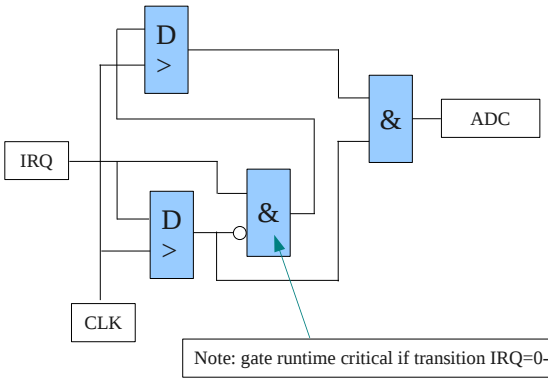
Q1[n+1]



Q1[n+1]=Not(Q0[n])*IRQ[n]

1.) Alle ADC = 0/1 über Pfeilenden in die Zustände schreiben
2.) Zustände auftrennen und Pfeilenden verteilen
3.) Pfeilanfang aufteilen
4.) Knotennotation (Q0Q1); Ausgabe ADC=1 im Zustand 11 (beim Moore nur vom Zustand abhängig)





D-Flipflop
$Q^{n+1}=D^n$

$Q0^{n+1}=IRQ^n$
$Q1^{n+1}=(Not(Q0)*IRQ)^n$

ADC=Q0*Q1 (1 in state 11)