



KC705 MIG Design Creation

June 2014

XTP196

Revision History

Date	Version	Description
06/09/14	9.0	Regenerated for 2014.2.
05/02/14	8.1	Minor update.
04/16/14	8.0	Regenerated for 2014.1.
12/18/13	7.0	Regenerated for 2013.4.
10/23/13	6.0	Regenerated for 2013.3.
07/30/13	5.1	Added missing files to RDF0186.
06/19/13	5.0	Regenerated for 2013.2
04/03/13	4.0	Regenerated for 2013.1. AR53420 fixed. Added AR55531.
02/22/13	3.1	Added AR53420.
12/18/12	3.0	Regenerated for 2012.4. Added AR53392.
10/23/12	2.0	Regenerated for 2012.3. Added AR52368.
07/25/12	1.0	Regenerated for 14.2. Added Vivado Flow. Added AR50886.

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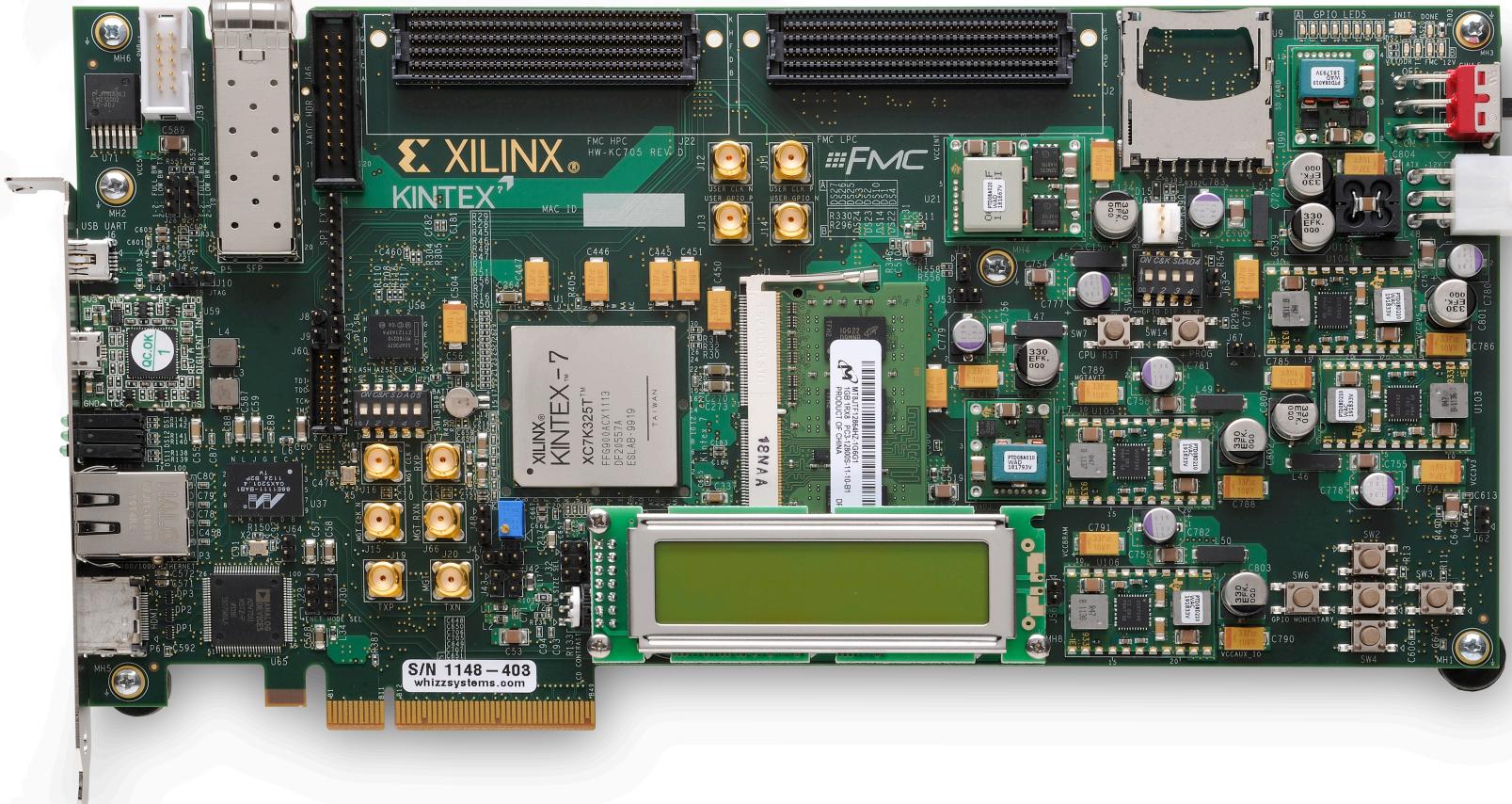
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Overview

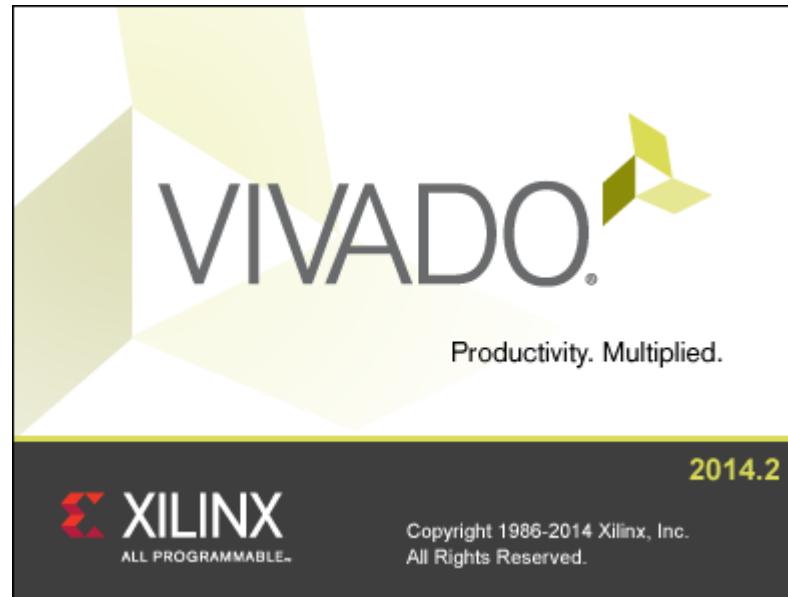
- Xilinx KC705 Board
- Software Requirements
- Generate MIG Example Design
- Modifications to Example Design
- Compile Example Design
- KC705 Setup
- Run MIG Example Design
 - Adjust Data Pattern using VIO Console
- References

Xilinx KC705 Board



Vivado Software Requirements

- Xilinx Vivado Design Suite 2014.2, Design Edition

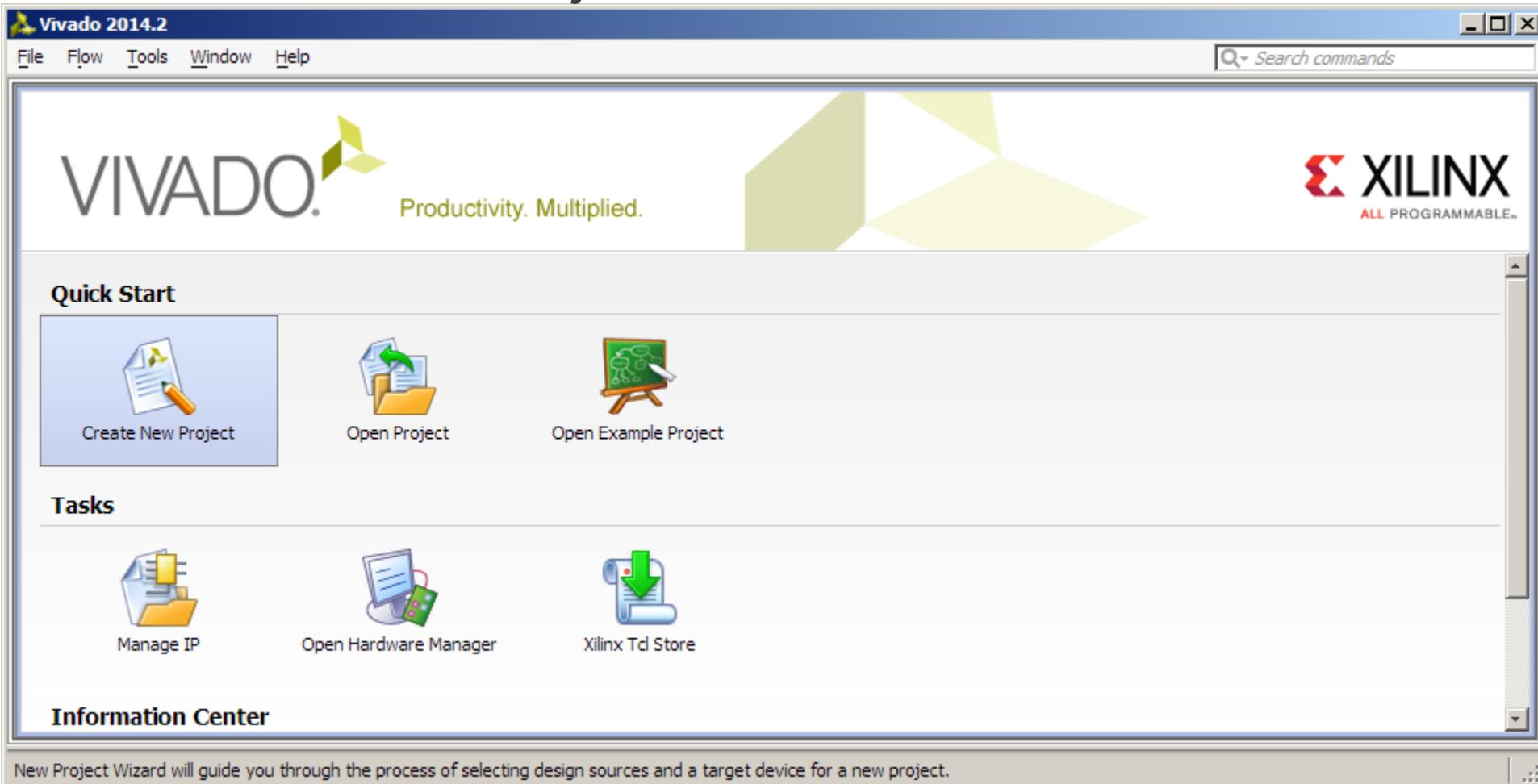


Generate MIG Example Design

► Open Vivado

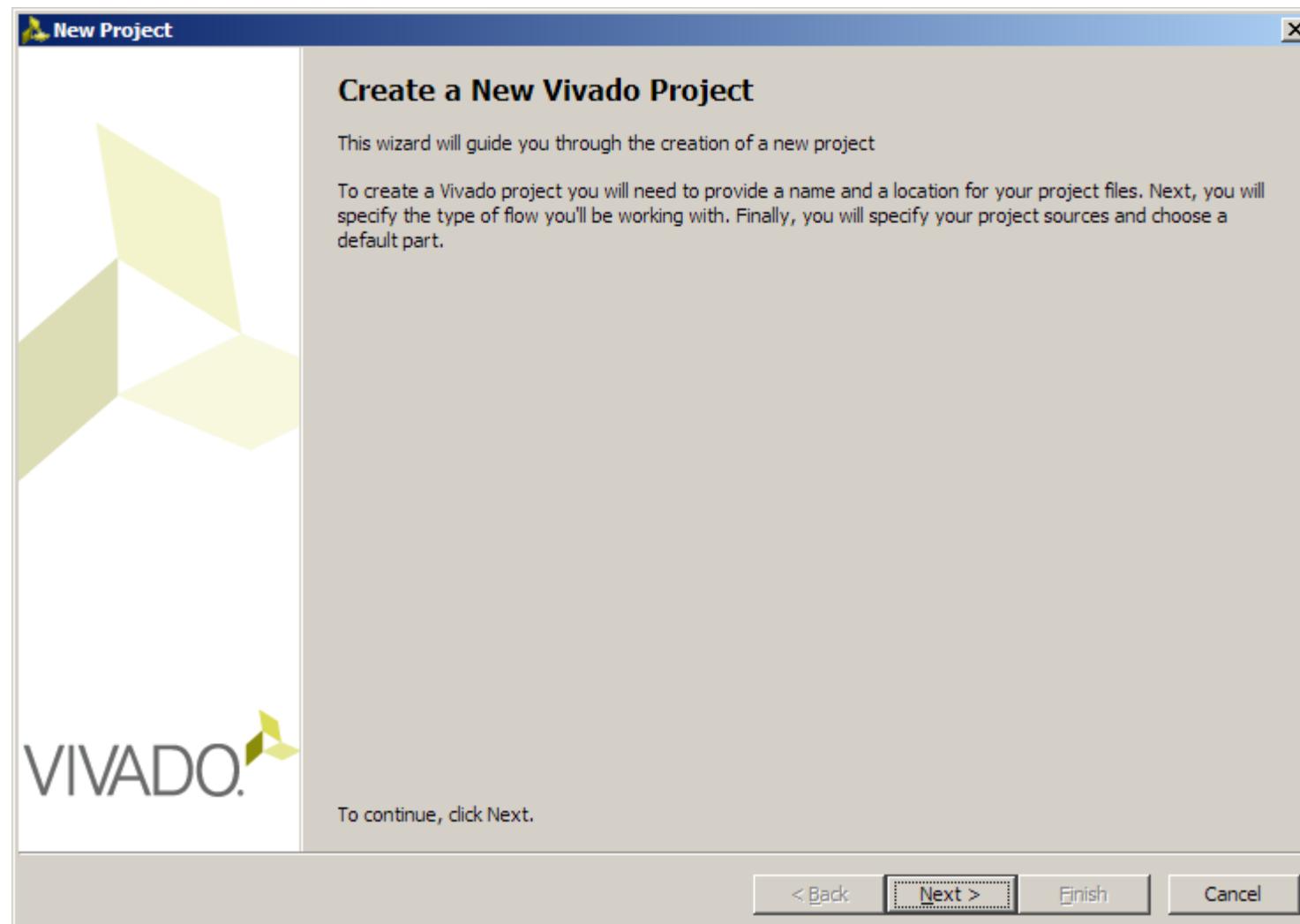
Start → All Programs → Xilinx Design Tools → Vivado 2014.2 → Vivado

► Select Create New Project



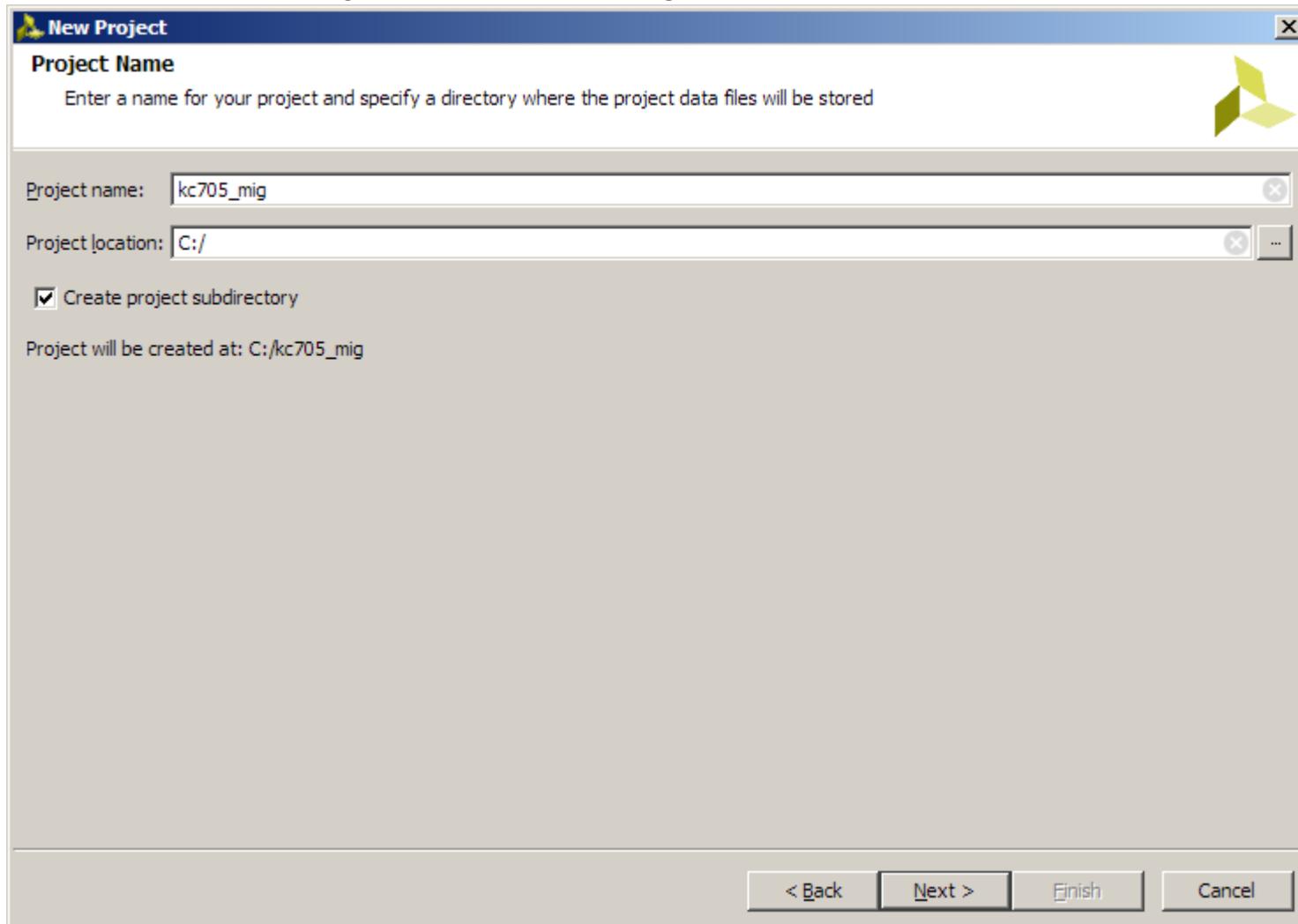
Generate MIG Example Design

► Click Next



Generate MIG Example Design

- Set the Project name and location to **kc705_mig** and **C:**
 - Check **Create project subdirectory**



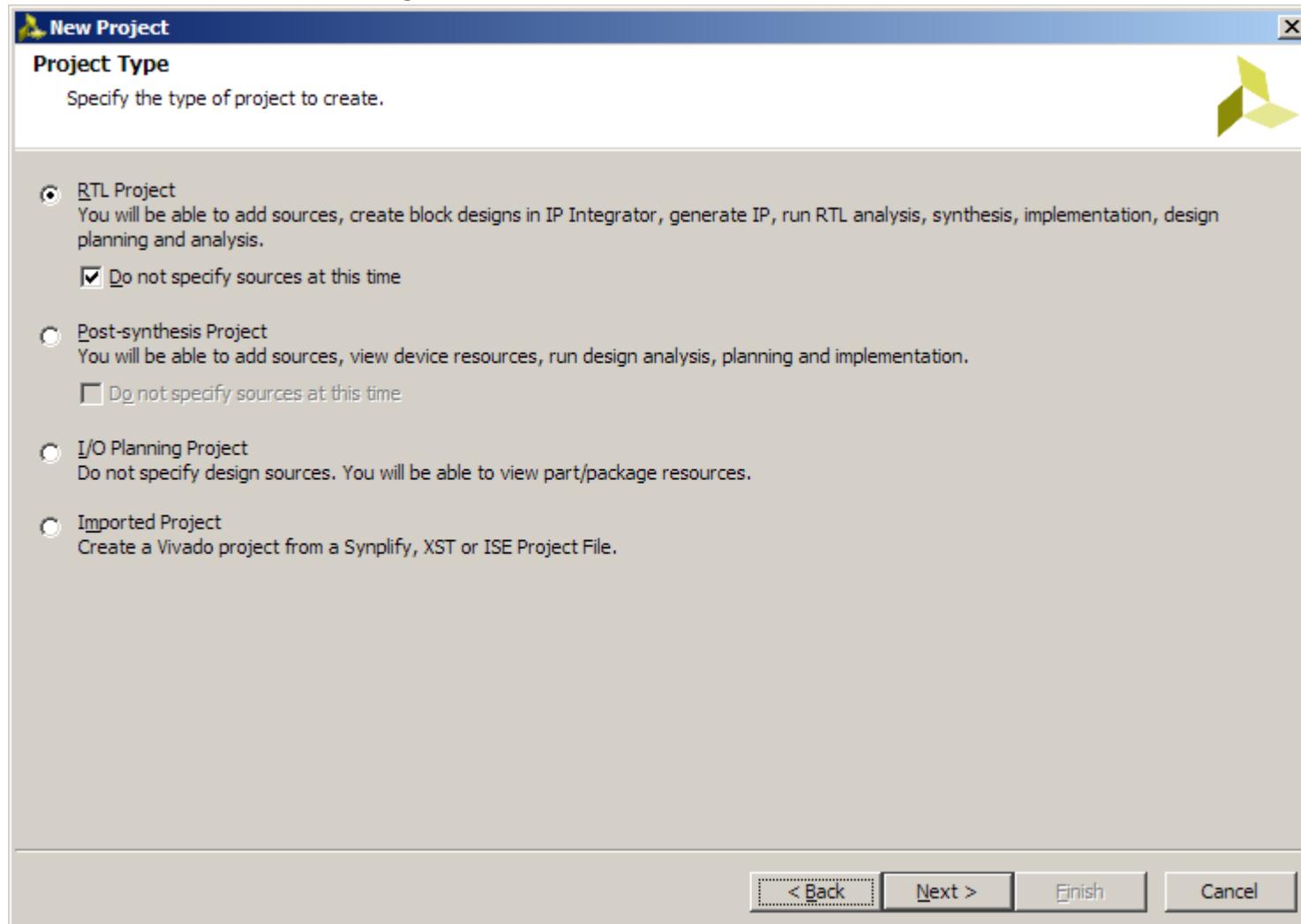
Note: Vivado generally requires forward slashes in paths

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Generate MIG Example Design

► Select RTL Project

- Select **Do not specify sources at this time**



Generate MIG Example Design

► Select the KC705 Board

The screenshot shows the 'New Project' dialog with the title 'Default Part'. It prompts the user to choose a default Xilinx part or board for their project, stating that this can be changed later. The interface includes a 'Specify' section with tabs for 'Parts' (selected) and 'Boards' (highlighted with a blue border). A 'Filter' section contains dropdown menus for 'Vendor' (All), 'Display Name' (All), and 'Board Rev' (Latest), along with a 'Reset All Filters' button. Below these is a search bar with a magnifying glass icon and a dropdown arrow. The main area displays a table of evaluation boards:

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version	Avail IOBs
MicroZed Board	em.avnet.com	e	xc7z010clg400-1	400	1.0	100
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1	484	1.0	200
Artix-7 AC701 Evaluation Platform	xilinx.com	1.0	xc7a200tfgb676-2	676	1.0	400
Kintex-7 KC705 Evaluation Platform	xilinx.com	1.1	xc7k325tffg900-2	900	1.0	500
Virtual-ZC707 Evaluation Platform	xilinx.com	1.1	xc7vx485tffg1761-2	1,761	1.0	700
Virtual-ZC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2	1,761	1.0	850
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020clg484-1	484	1.0	200
ZYNQ-7 ZC706 Evaluation Board	xilinx.com	1.1	xc7z045ffg900-2	900	1.0	362

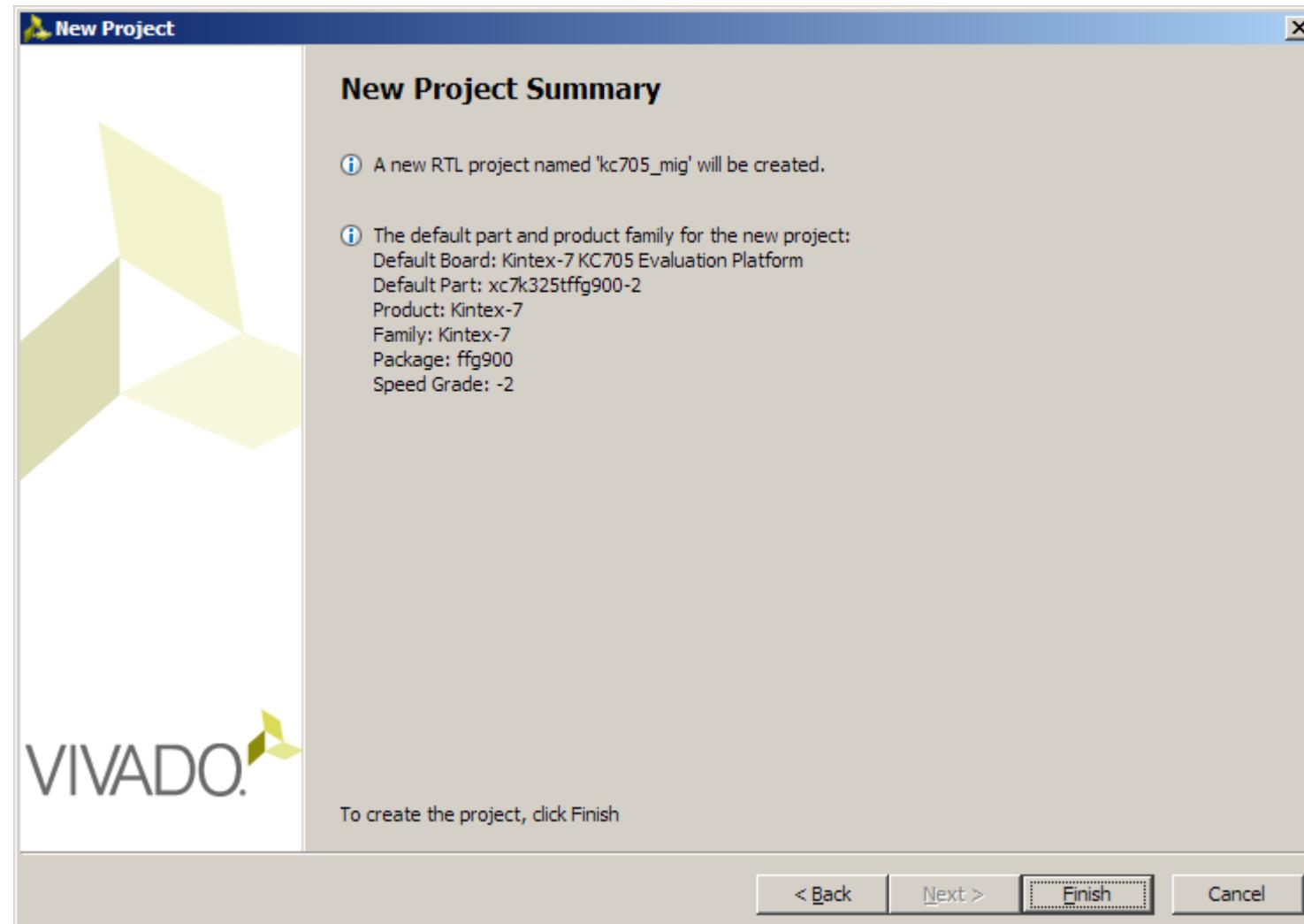
At the bottom are navigation buttons: '< Back', 'Next >', 'Finish', and 'Cancel'.

Note: Presentation applies to the KC705

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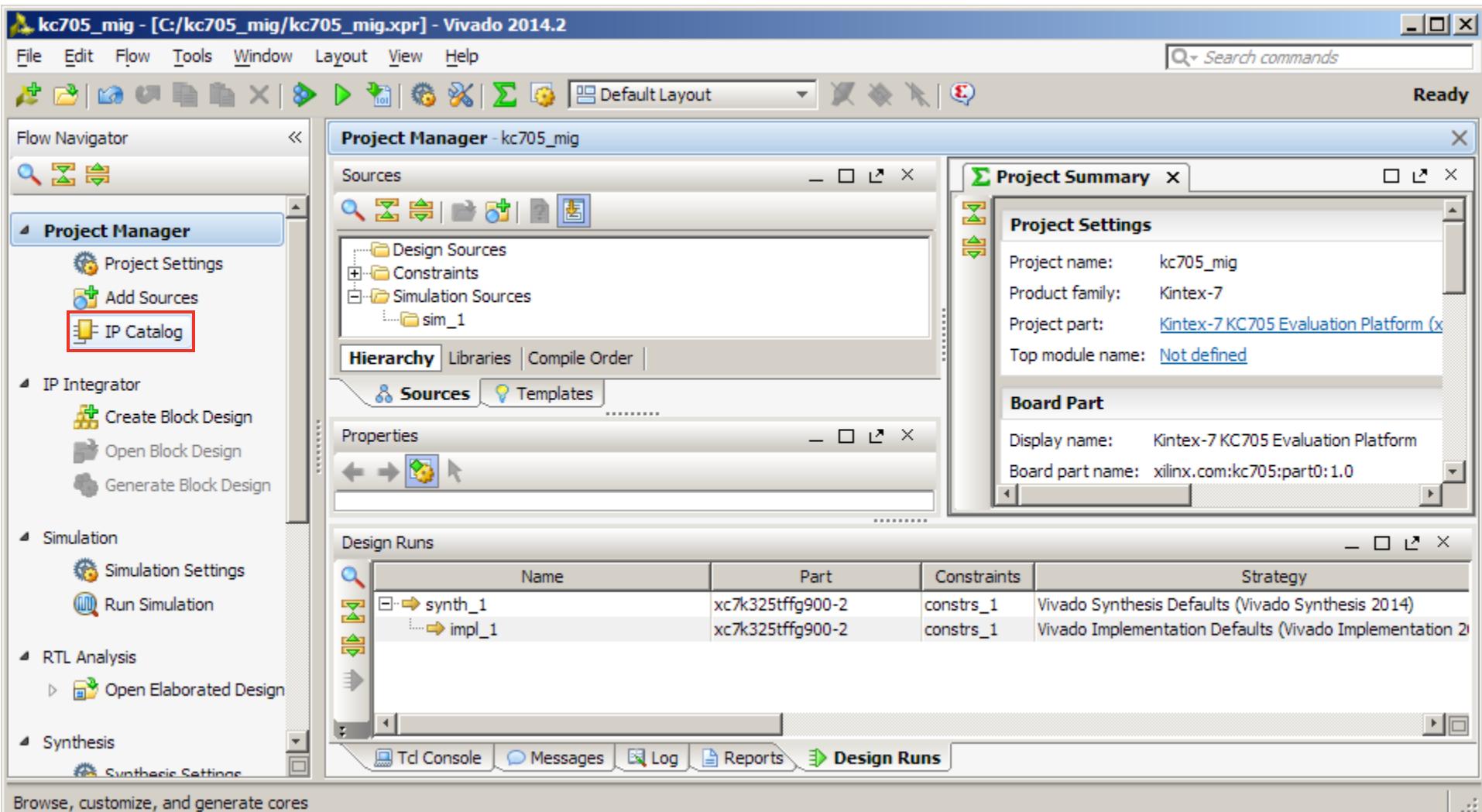
Generate MIG Example Design

► Click Finish



Generate MIG Example Design

► Click on IP Catalog

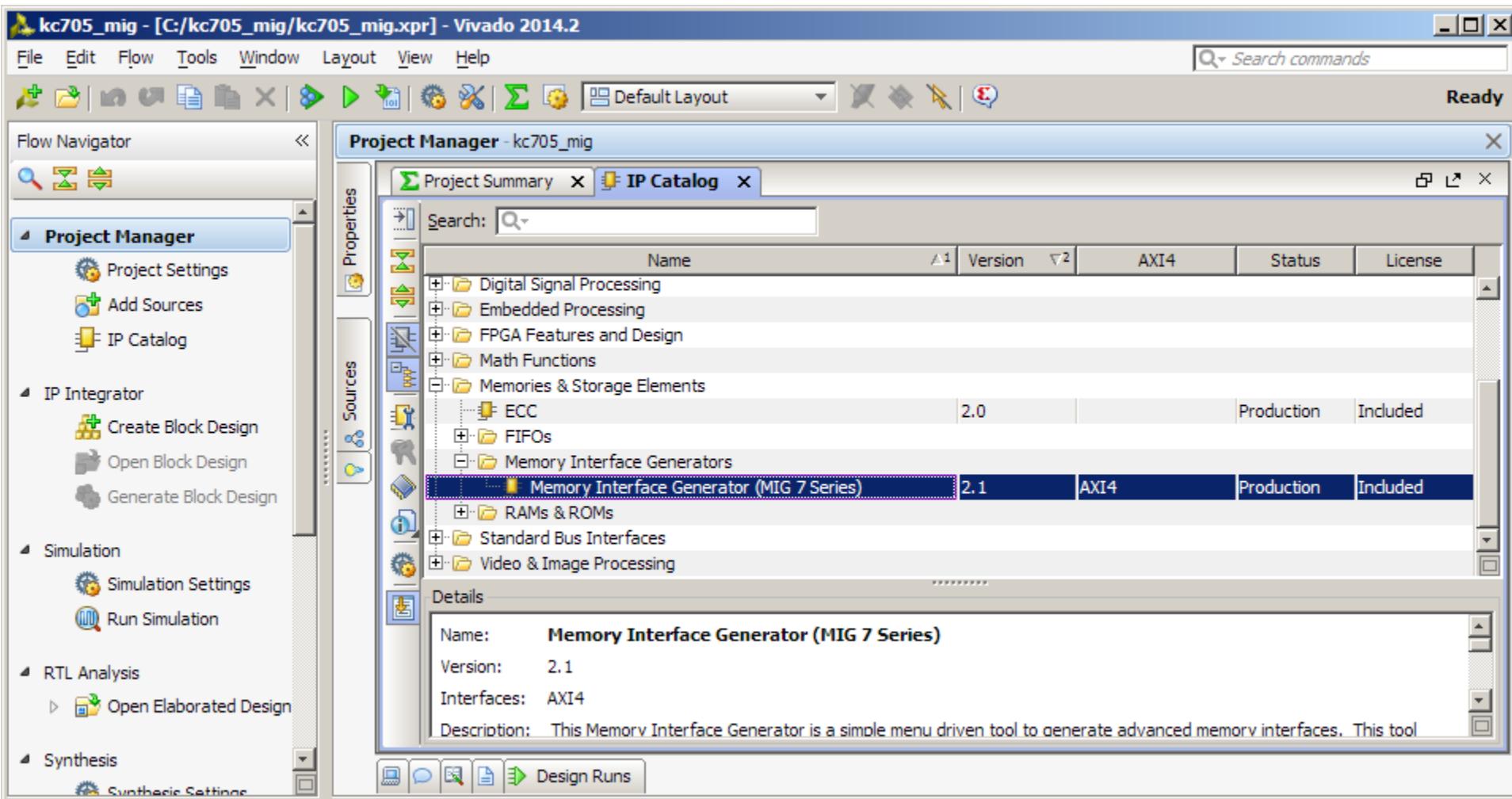


Note: Presentation applies to the KC705

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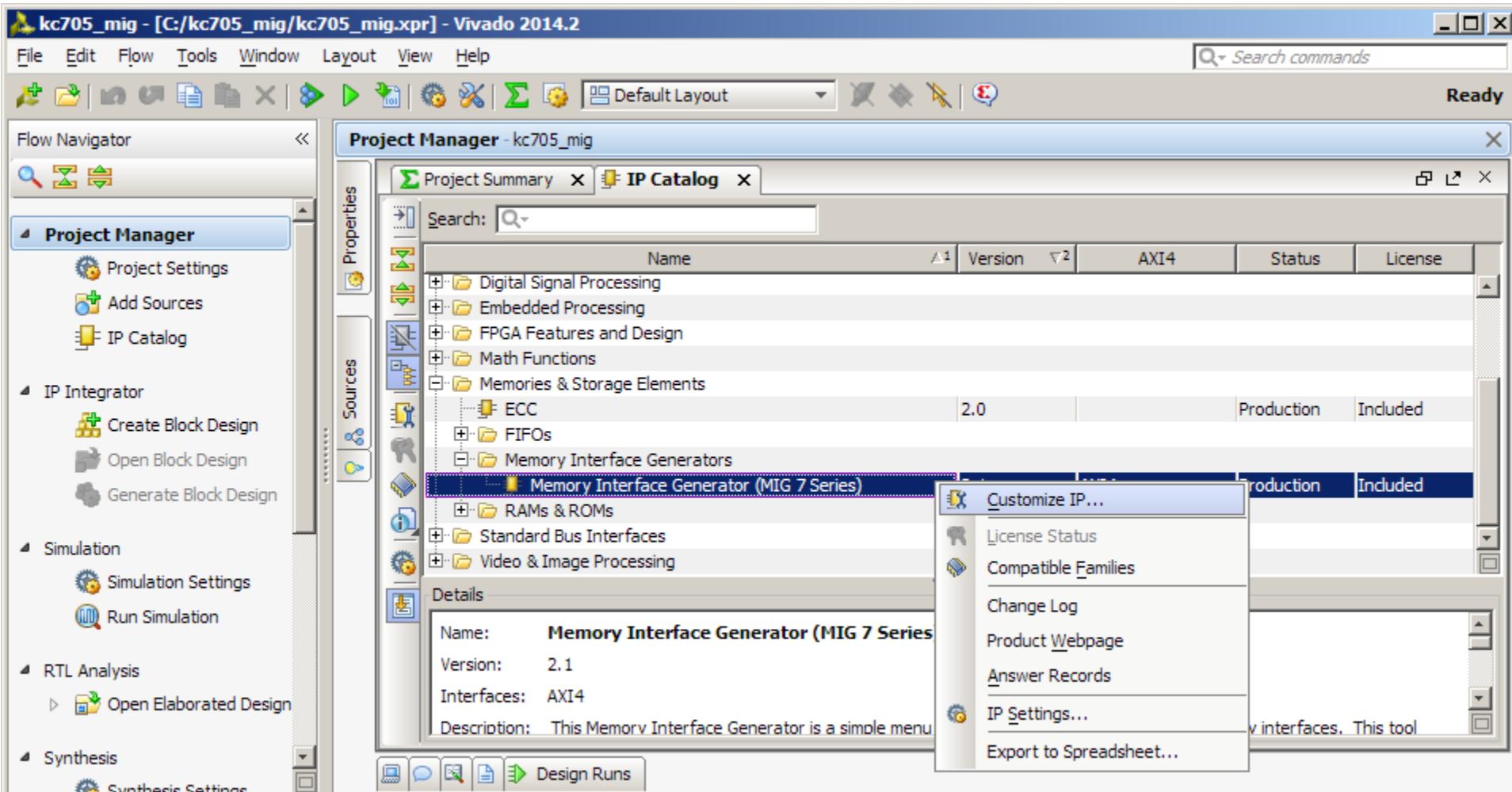
Generate MIG Example Design

► Select MIG 7 Series, v2.1 under Memory Interface Generators



Generate MIG Example Design

- Right click on MIG 7 Series
 - Select Customize IP

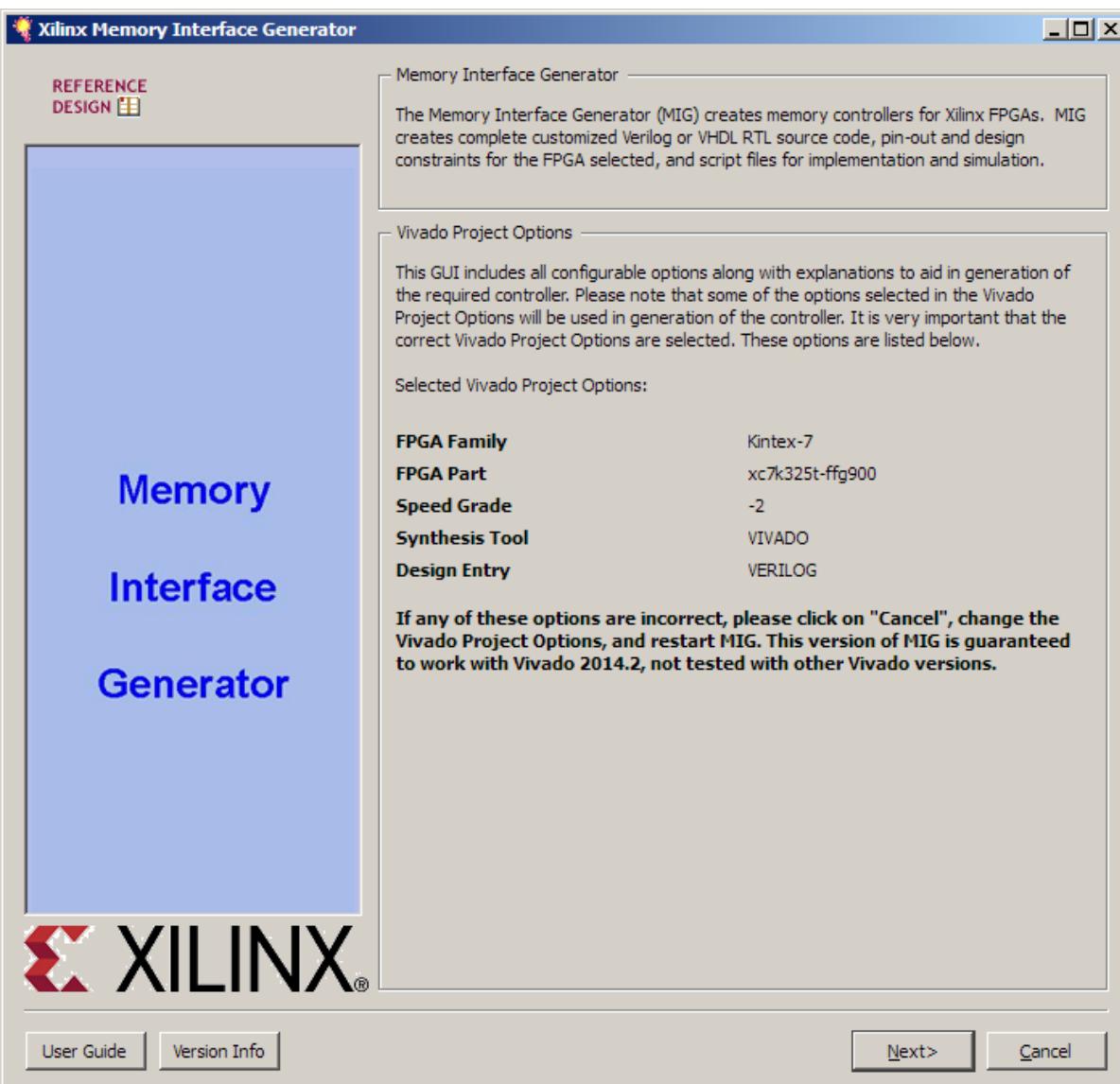


Customize the selected core

Note: Presentation applies to the KC705

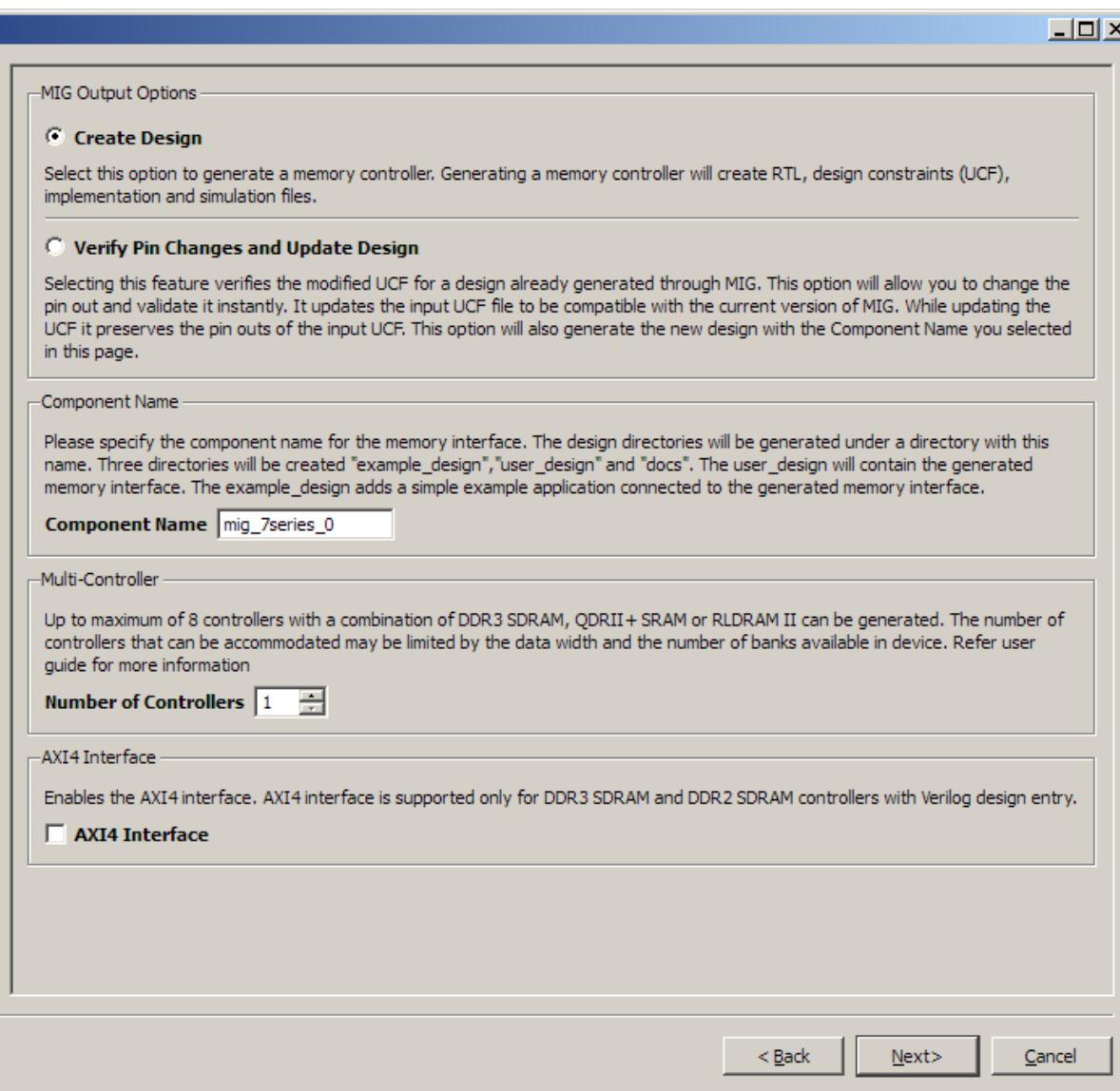
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Generate MIG Example Design



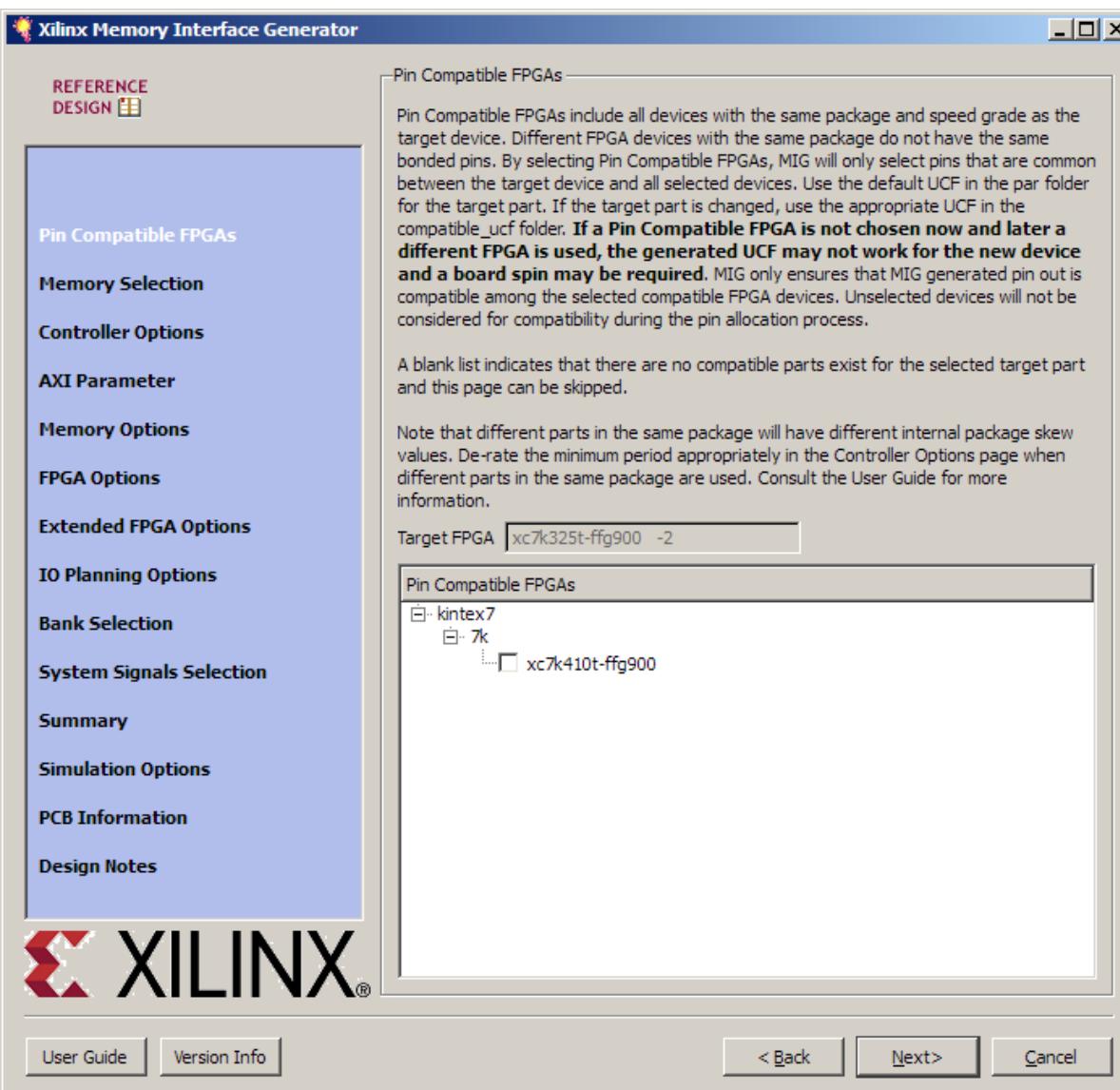
➤ Leave this page as is
– Click Next

Generate MIG Example Design



➤ Leave this page as is
– Click Next

Generate MIG Example Design



➤ Leave this page as is
– Click Next

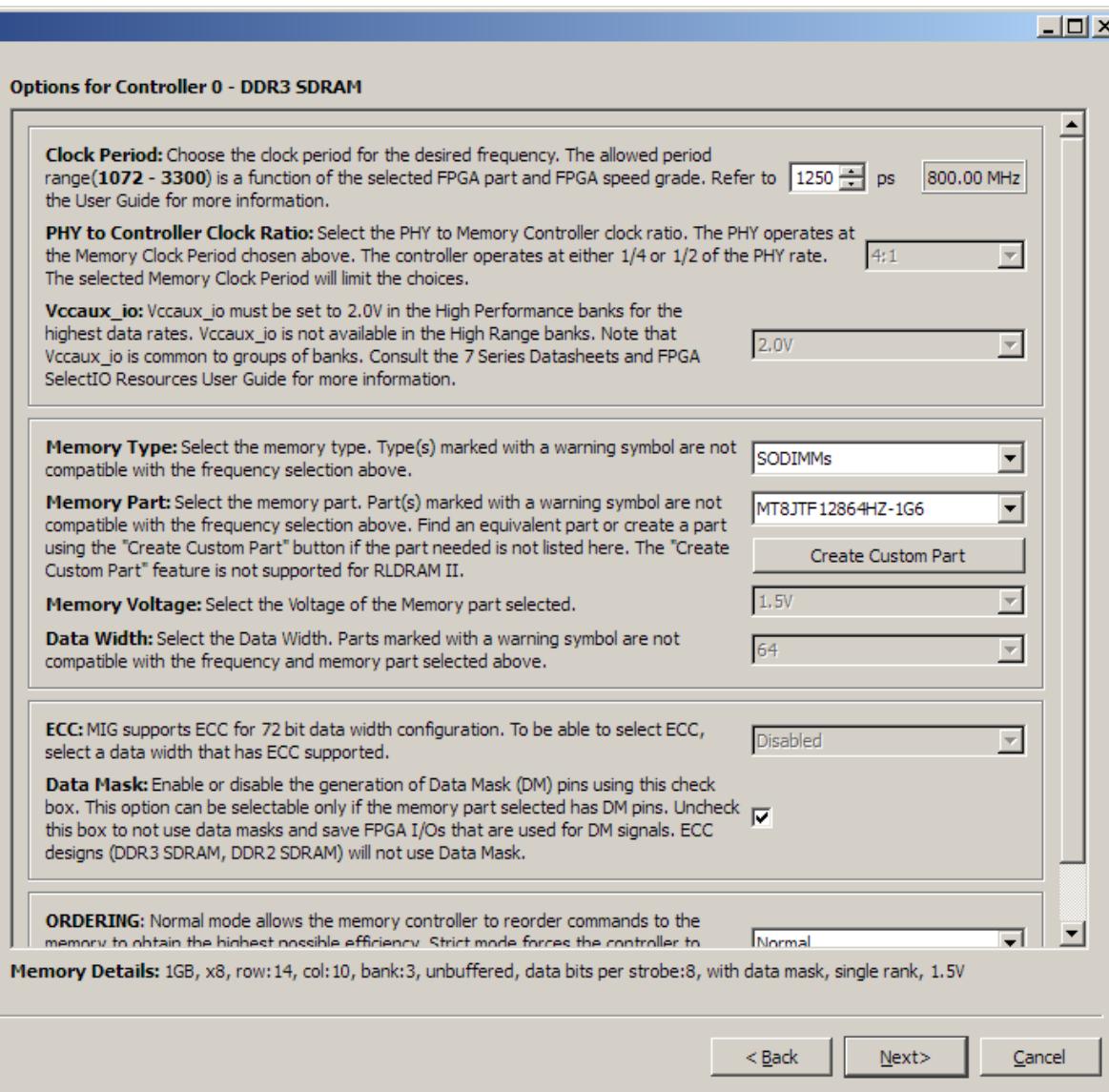
Generate MIG Example Design



► Select Memory Type

- DDR3 SDRAM
- Click Next

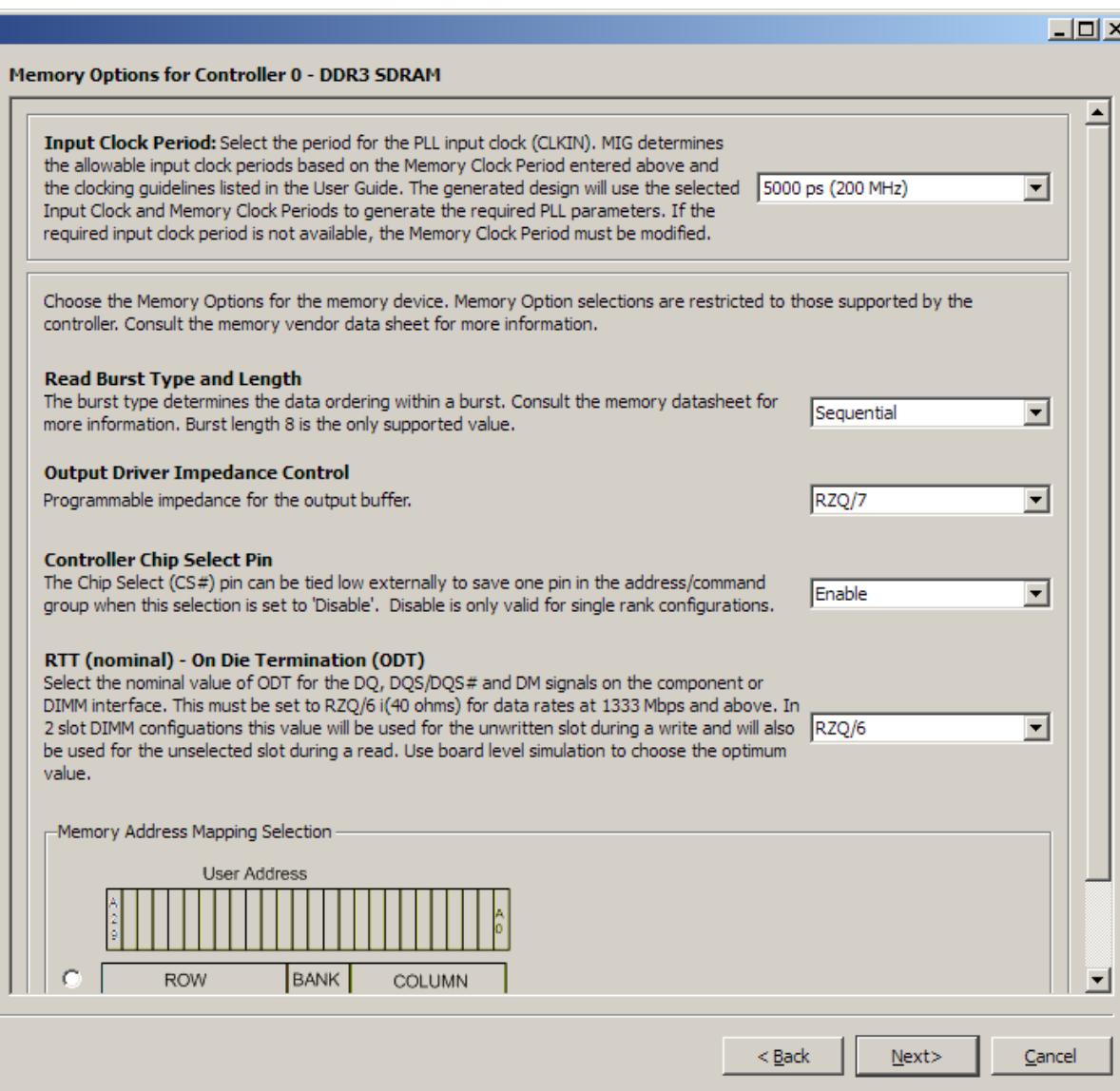
Generate MIG Example Design



► Select

- Clock Period: 1250 ps
- Type: SODIMMs
- Part: MT8JTF12864HZ-1G6
- Data Mask: Checked
- Click Next

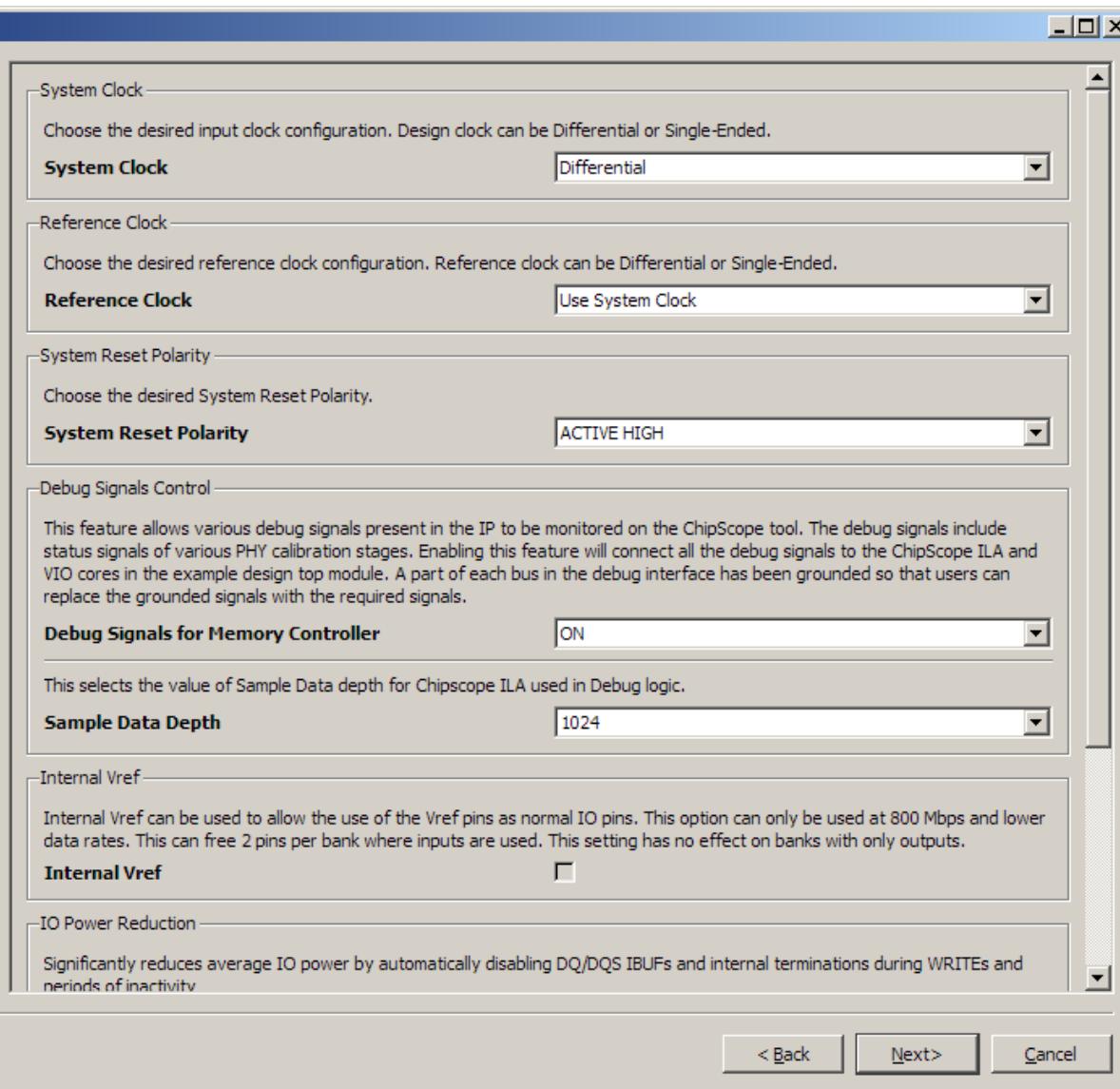
Generate MIG Example Design



► Select:

- Input Clock Period: **5000 ps**
- RTT: **RZQ/6**
- Click Next

Generate MIG Example Design



► Select

- Reference Clock: **Use System Clock**
- System Reset: **ACTIVE HIGH**
- Debug: **ON**
- Click Next

Generate MIG Example Design



► Select

- DCI Cascade: **Checked**
- Click Next

Generate MIG Example Design

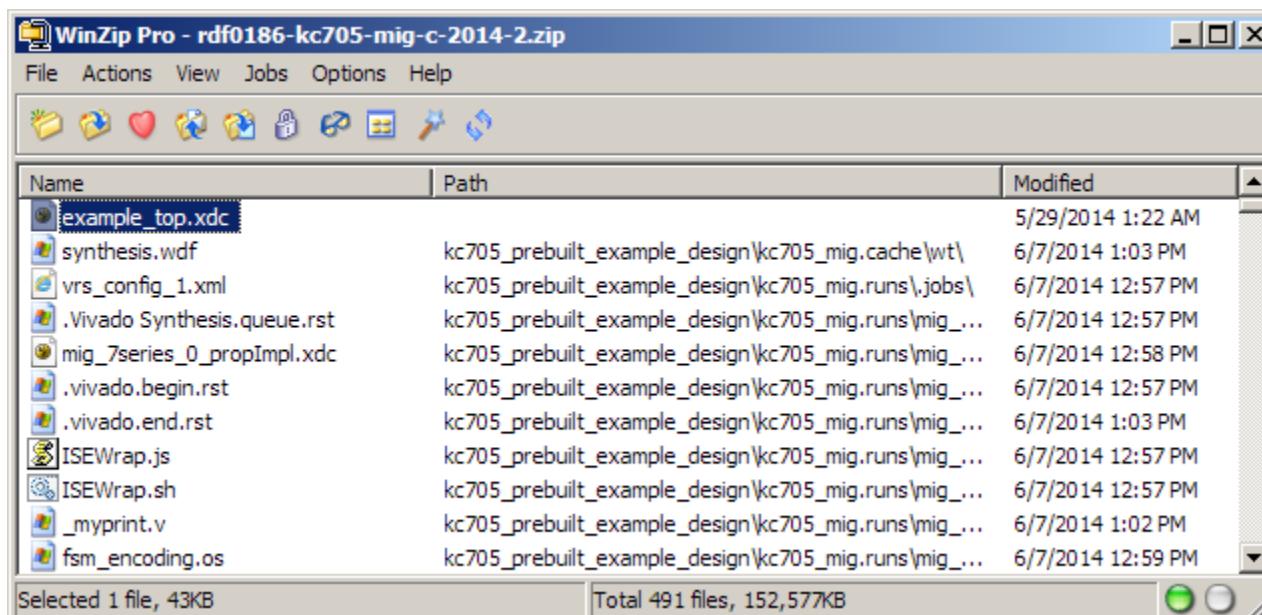


► Select Fixed Pin Out
– Click Next

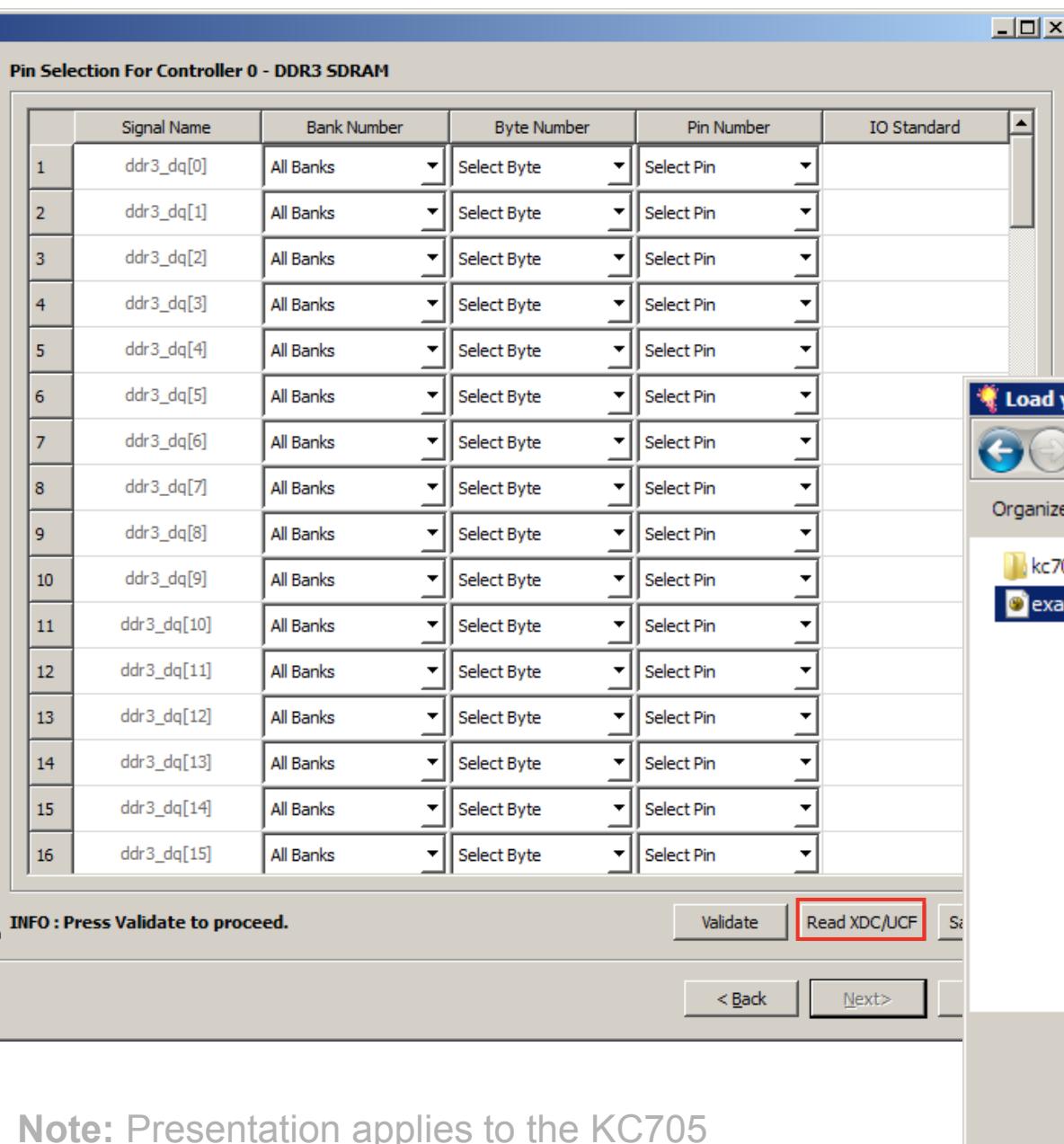
Modifications to Example Design

► Open the RDF0186 - KC705 MIG Design Files (2014.2 C) zip file

- Available through <http://www.xilinx.com/kc705>
- Extract the file, “**example_top.xdc**” *only* to C:\kc705_mig
- Contains the XDC constraints needed for KC705 MIG design
- This zip file will be needed later in the presentation

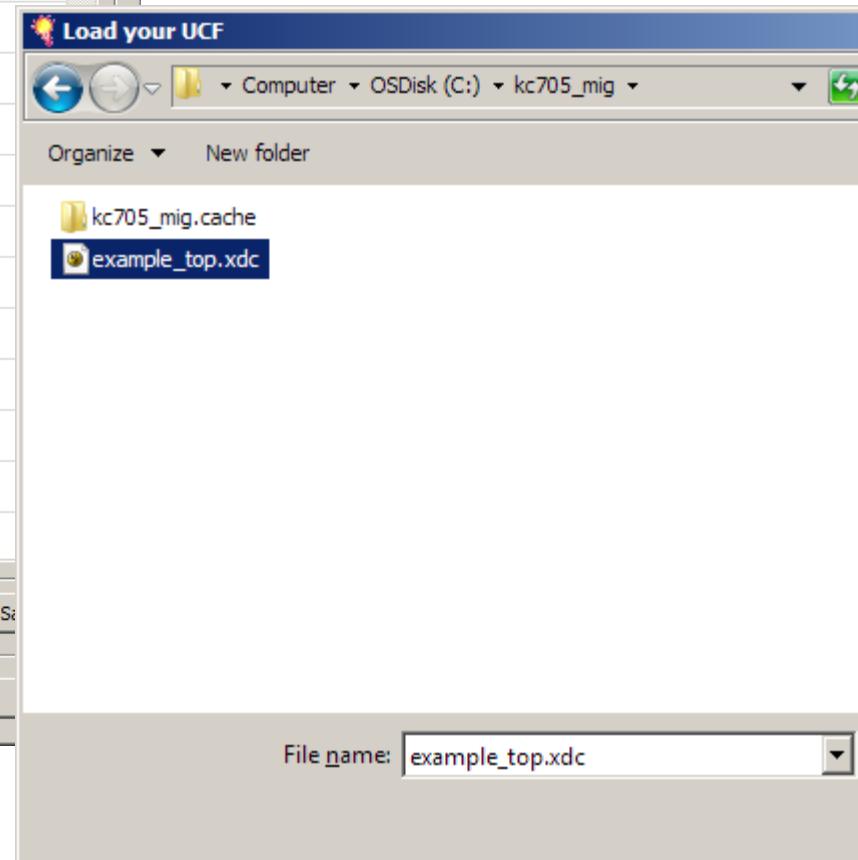


Generate MIG Example Design

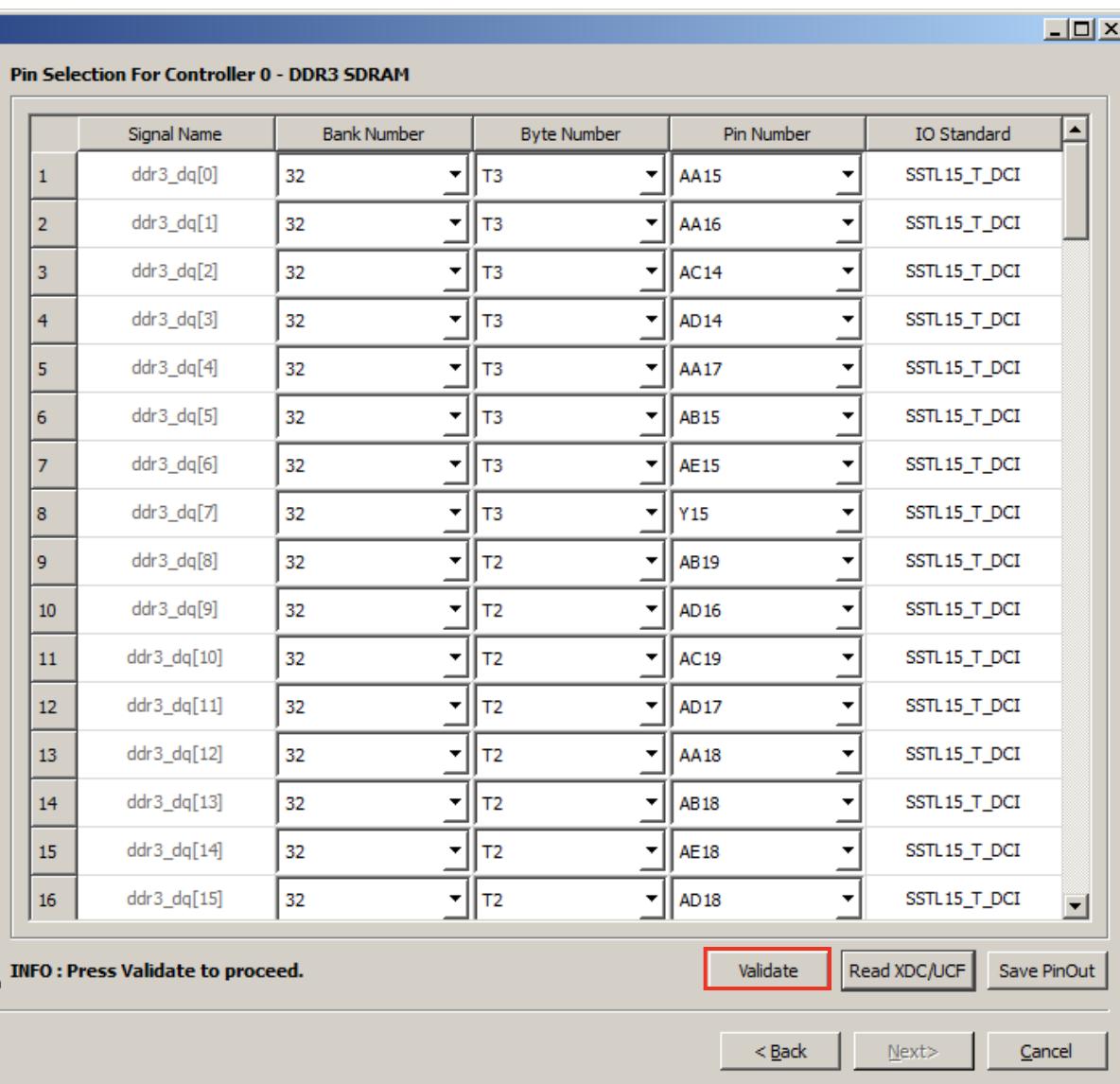


► Select Read XDC/UCF

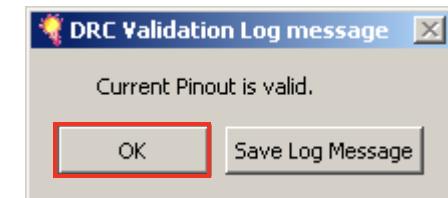
- Open the file:
example_top.xdc



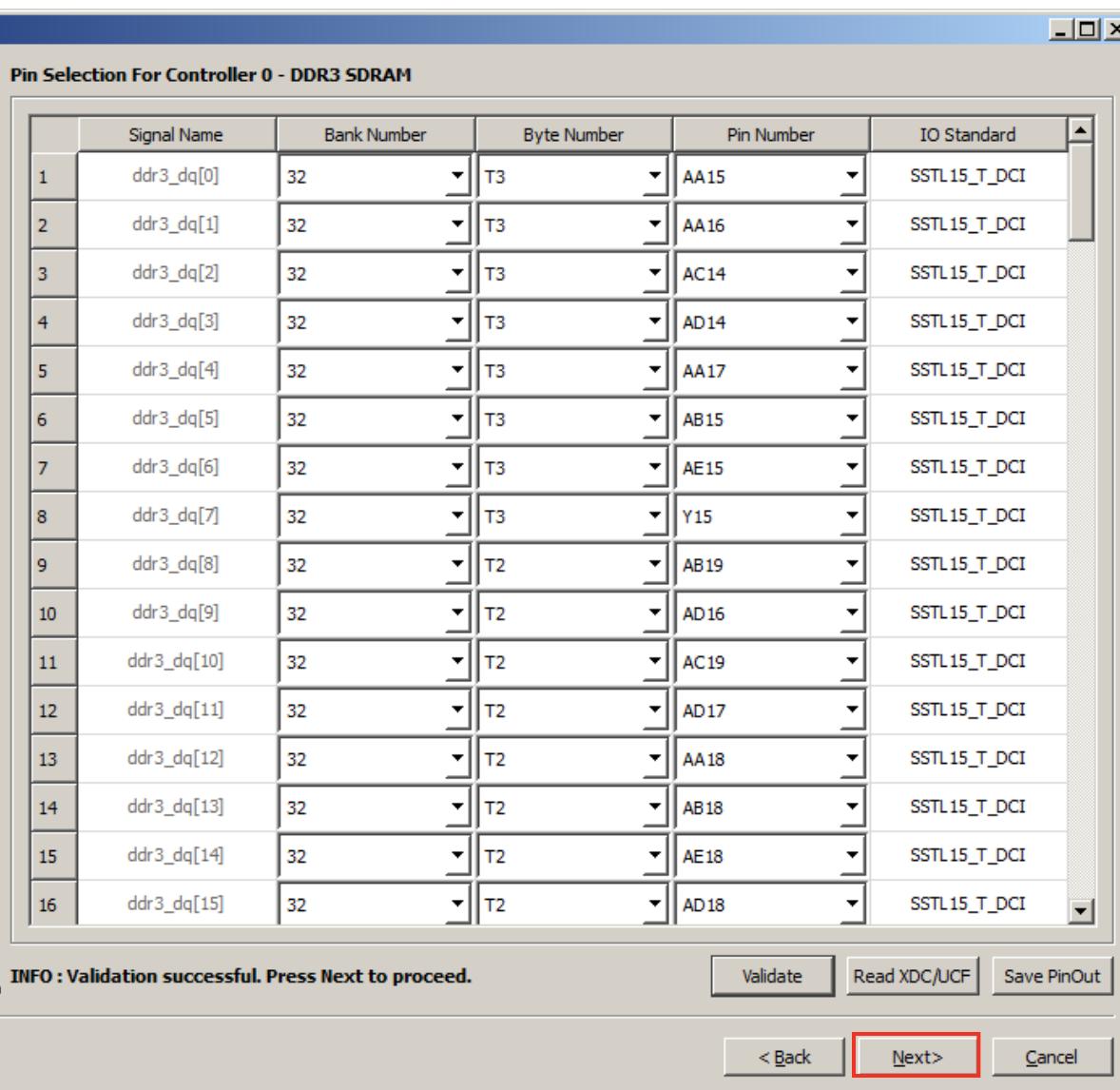
Generate MIG Example Design



- Once it finishes reading in the XDC, click Validate
 - Click OK

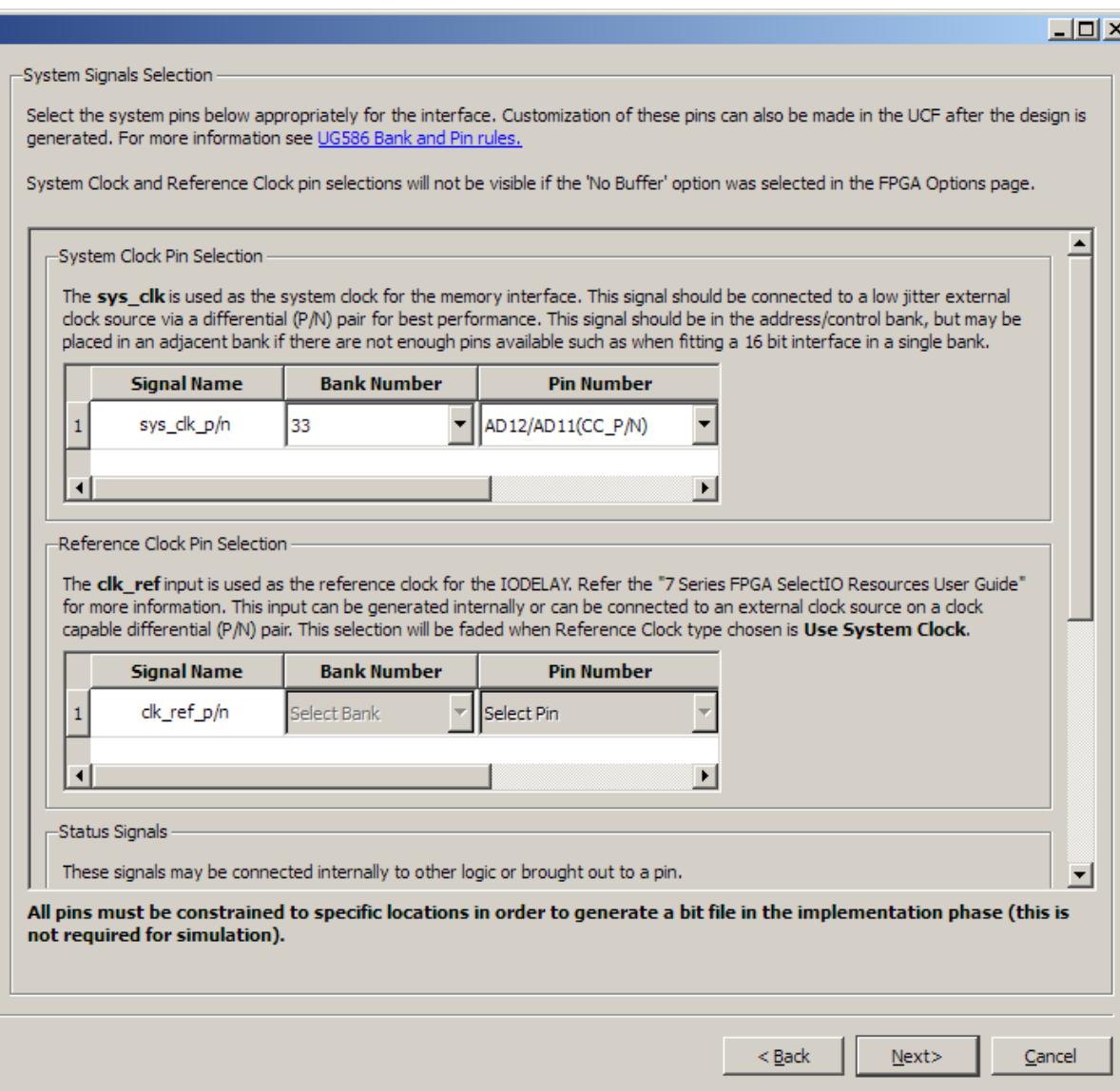


Generate MIG Example Design



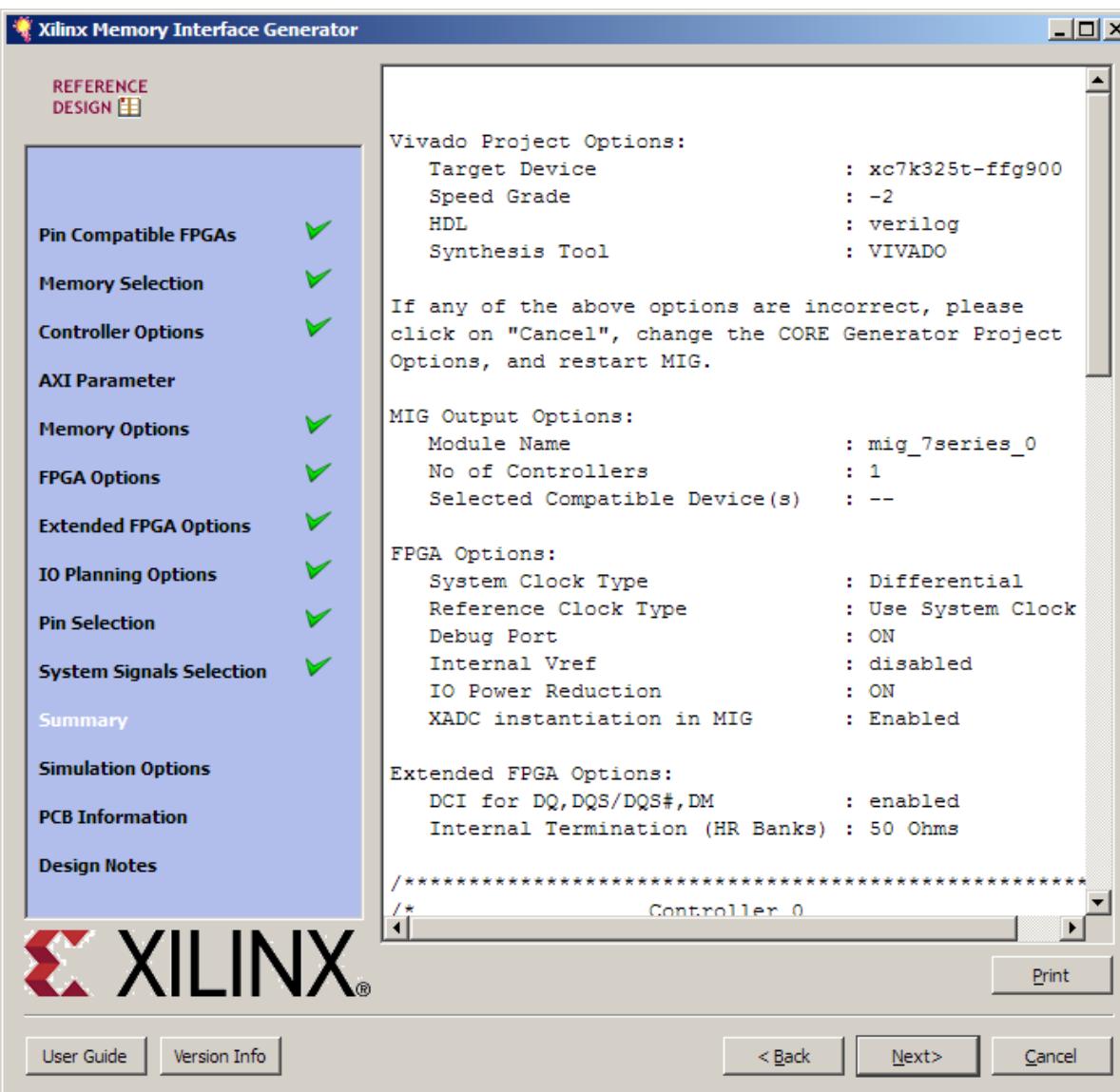
- The Next button is enabled once the pinout is validated.
 - Click Next

Generate MIG Example Design



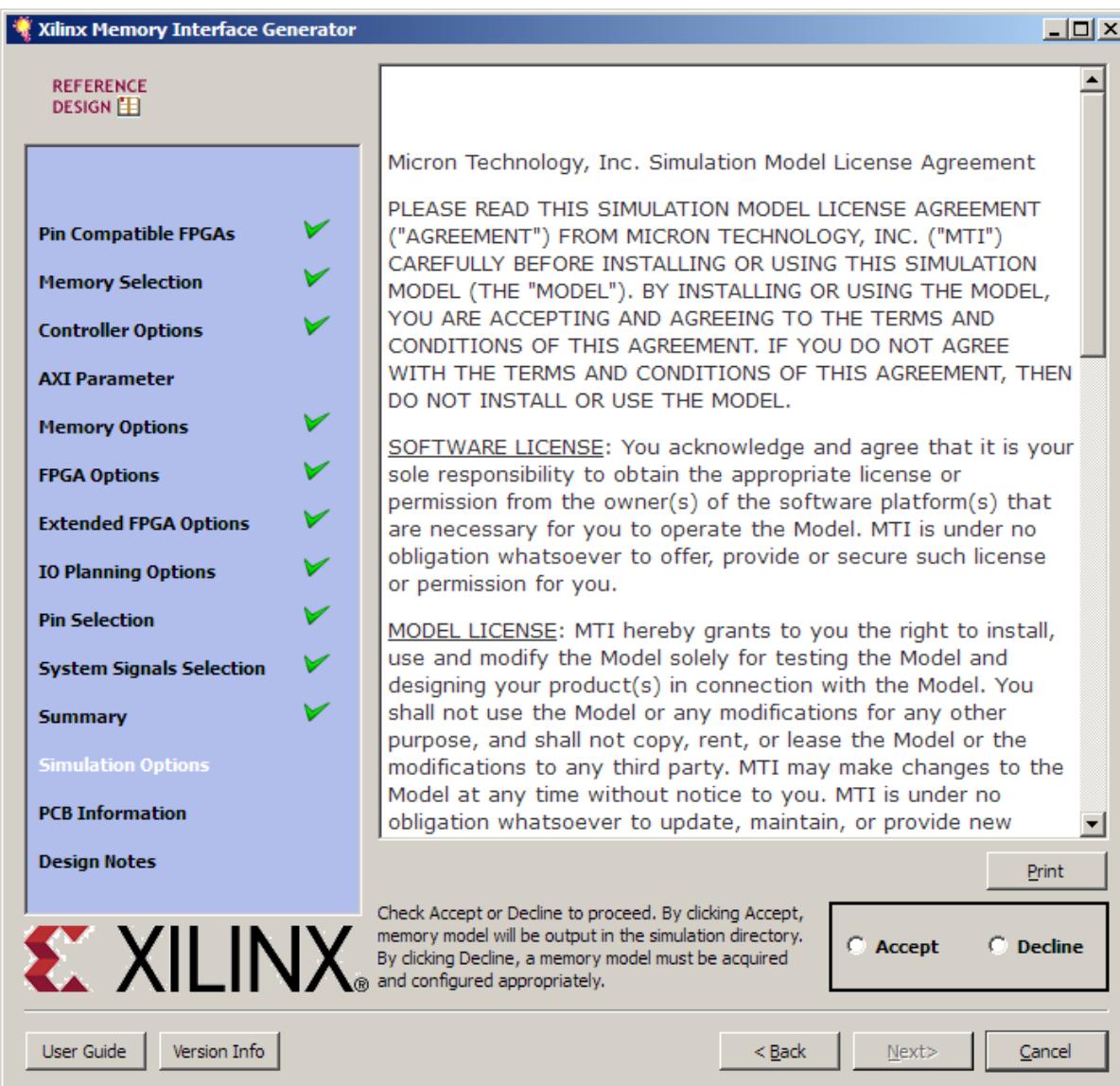
➤ Leave this page as is
– Click Next

Generate MIG Example Design



➤ Leave this page as is
– Click Next

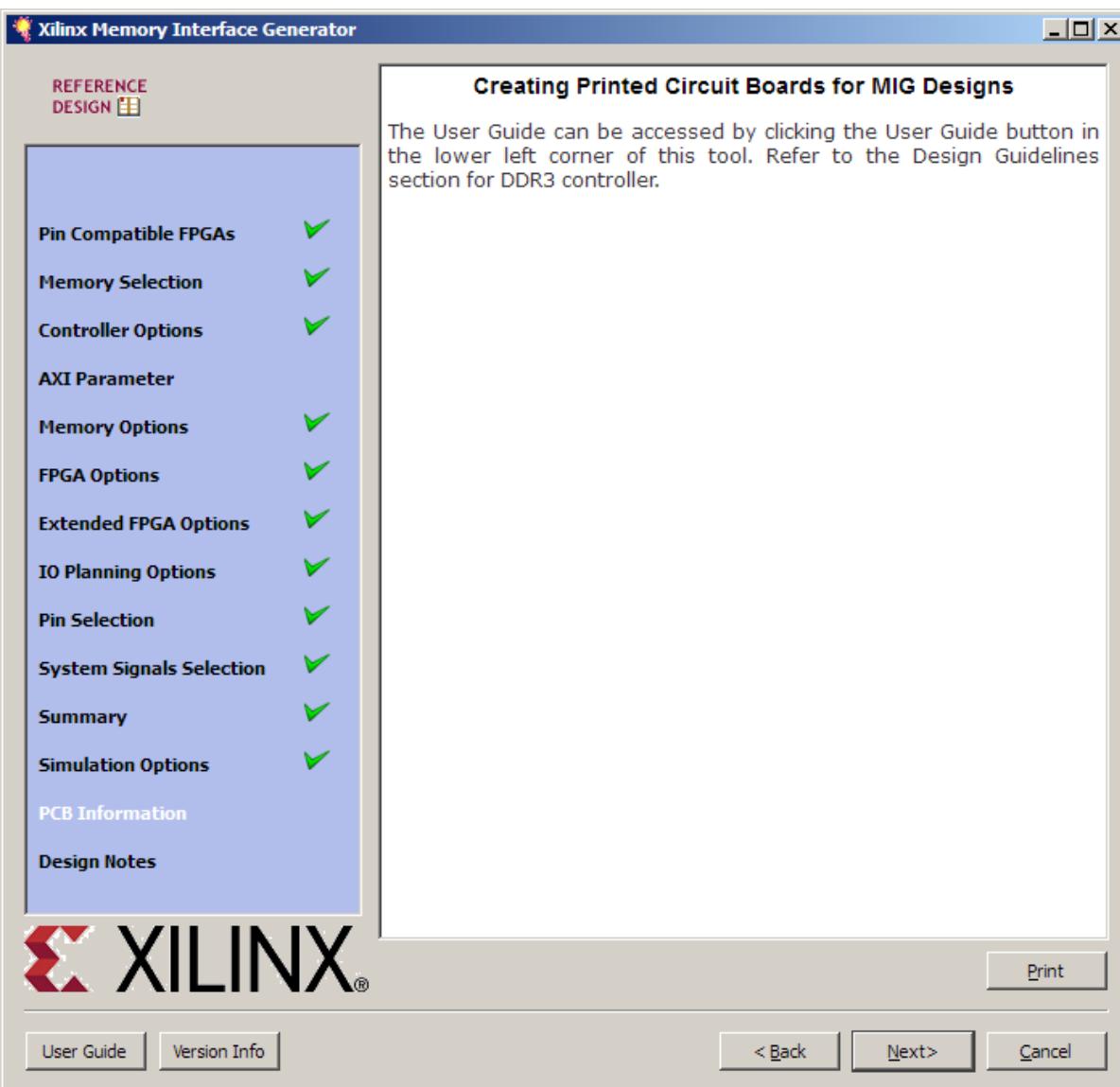
Generate MIG Example Design



➤ Accept Simulation license, if desired

- Otherwise, Decline license
- Click Next

Generate MIG Example Design



➤ Leave this page as is
– Click Next

Generate MIG Example Design

Xilinx Memory Interface Generator

REFERENCE DESIGN

Pin Compatible FPGAs ✓

Memory Selection ✓

Controller Options ✓

AXI Parameter

Memory Options ✓

FPGA Options ✓

Extended FPGA Options ✓

IO Planning Options ✓

Pin Selection ✓

System Signals Selection ✓

Summary ✓

Simulation Options ✓

PCB Information ✓

Design Notes

DDR3 SDRAM Design for Kintex-7 FPGAs

Design Notes

1. This design is tested with Vivado 2014.2 version
2. This design is simulated with Questa SIM 10.2a version, VCS I-2014.03 version, and IES 13.20.005 version
3. Components, RDIMMs, UDIMMs and SODIMMs are supported
4. If fly by delays are simulated, they must be limited to 1.2ns
5. Consult the Version Info for known limitations

Key Enhancements for MIG 2.1 - 2014.2 release

1. DDR3 Clocking Scheme changes
2. DDR3 read path calibration algorithm changes

Key Enhancements for MIG 2.0 - 2014.1 release

1. Extended IES and VCS support to Multi-Controller and Multi-Interface designs

Key Enhancements for MIG 2.0 - 2013.4

Print

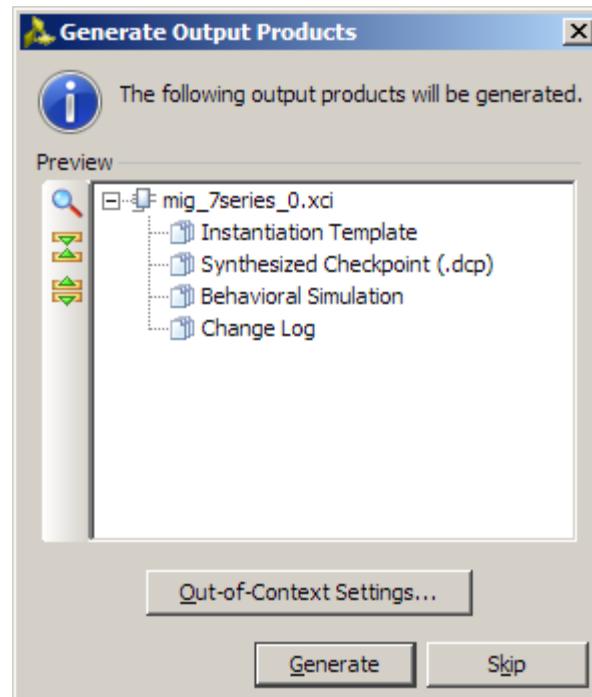
< Back Generate Cancel

XILINX

Click Generate

Generate MIG Example Design

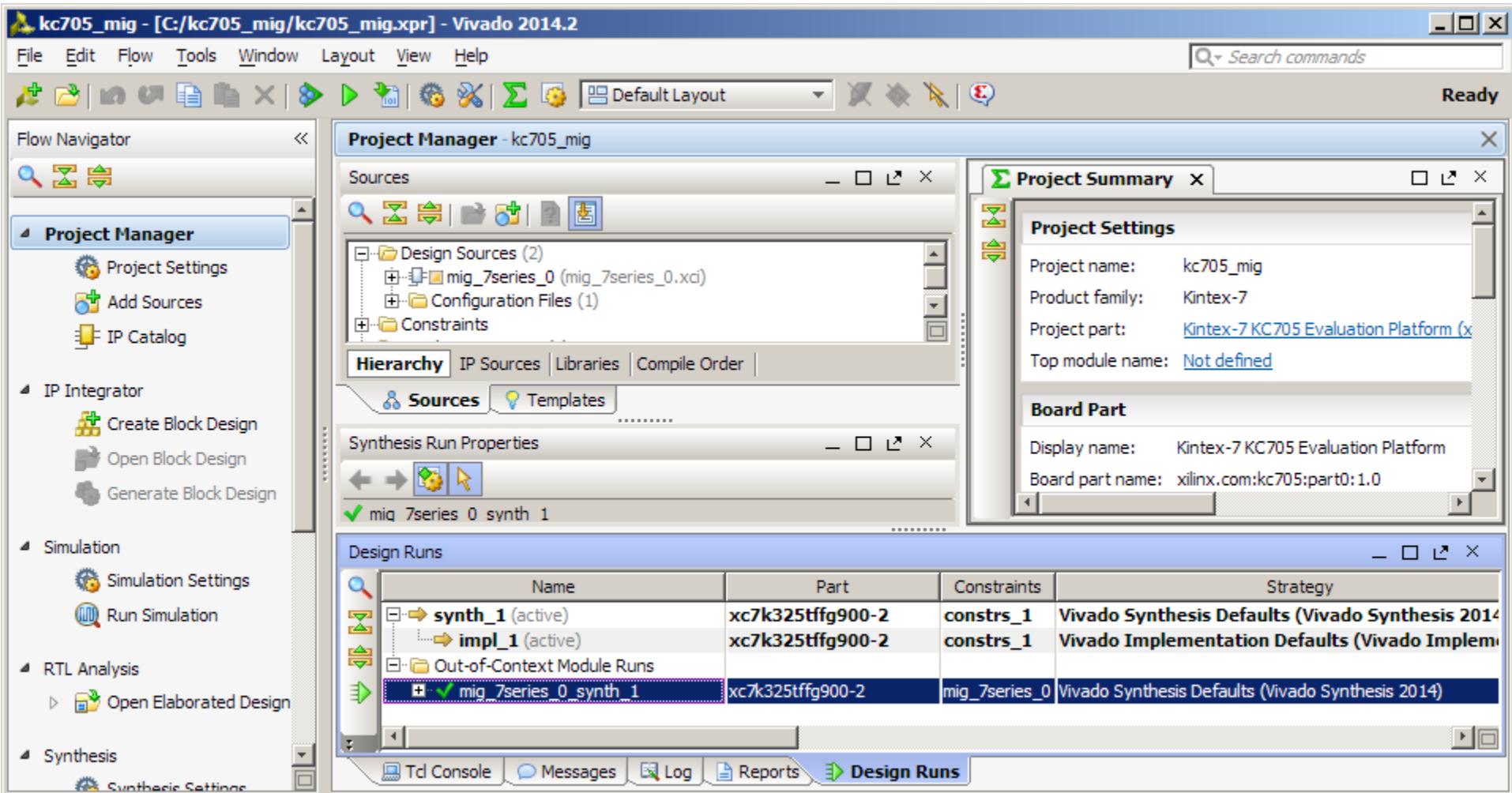
► Click Generate



Generate MIG Example Design

► MIG design appears in Design Sources

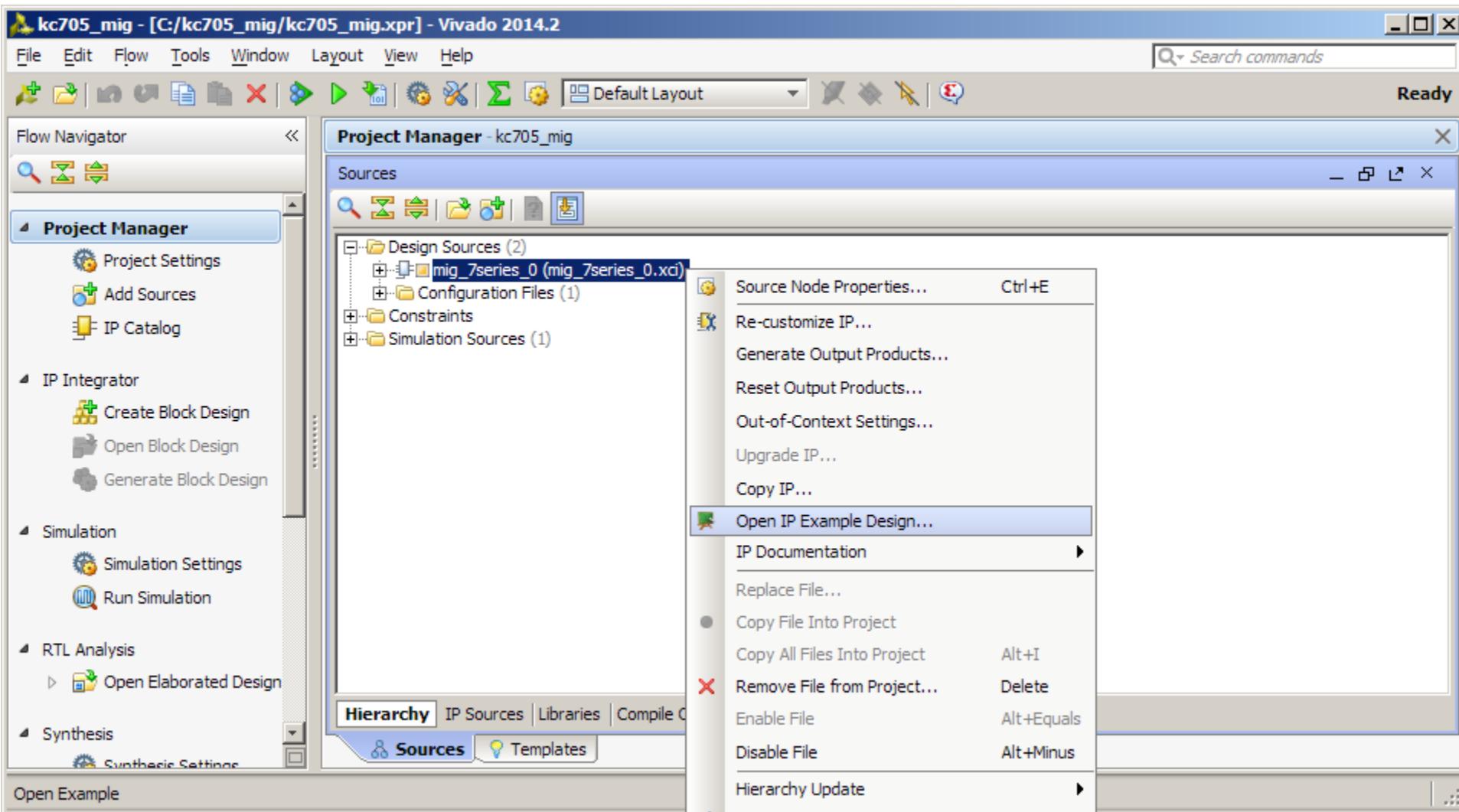
- Wait until checkmark appears on mig_7series_0_synth_1



Synthesis Run: mig_7series_0_synth_1

Compile Example Design

► Right click on mig_7series_0 and select Open IP Example Design...

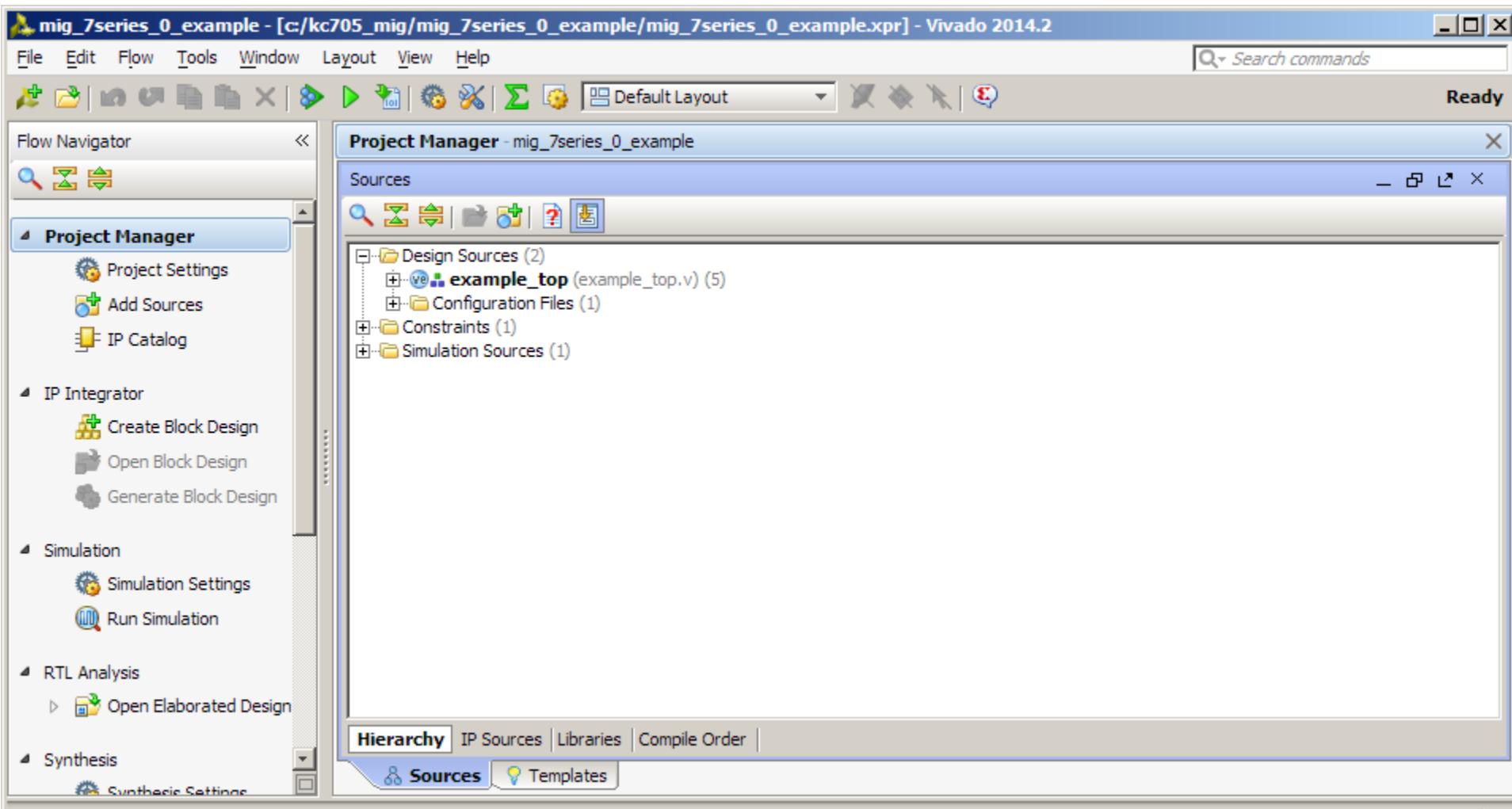


Note: Presentation applies to the KC705

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Compile Example Design

- A new project is created under <design path>/

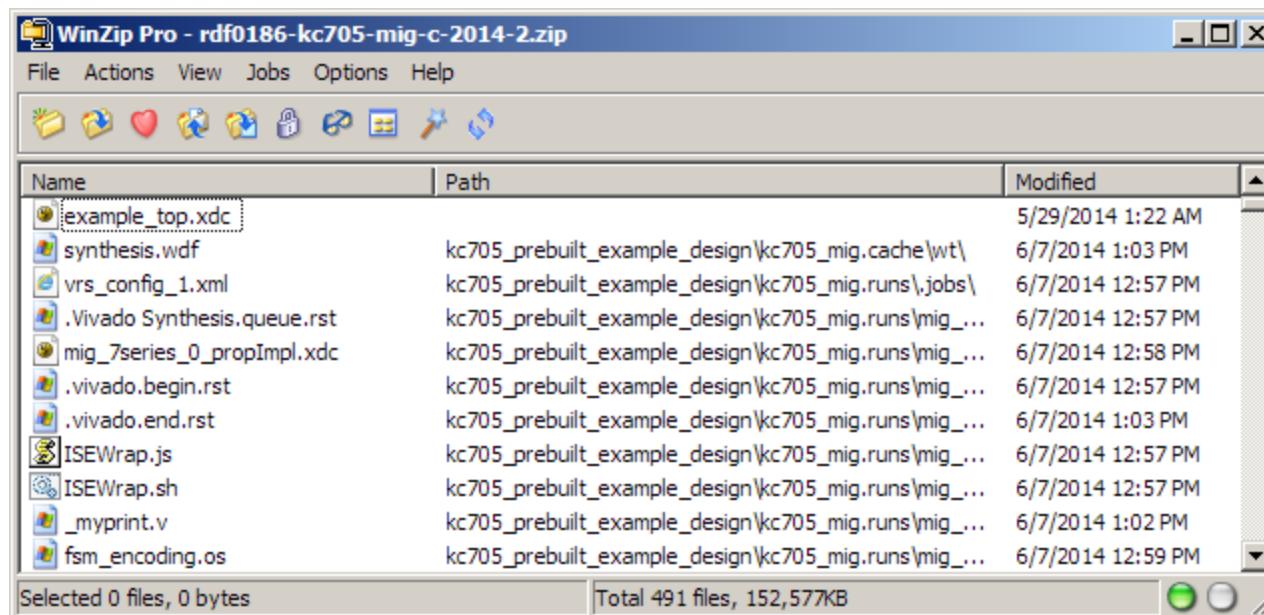


Note: The original project window can be closed

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Modifications to Example Design

- Unzip the RDF0186 - KC705 MIG Design Files (2014.2 C) zip file to your C:\kc705_mig directory
 - Contains several changes needed to support Kintex-7 devices with MIG
 - Do this **after** creating the Example Design; changes only affect the Example Design



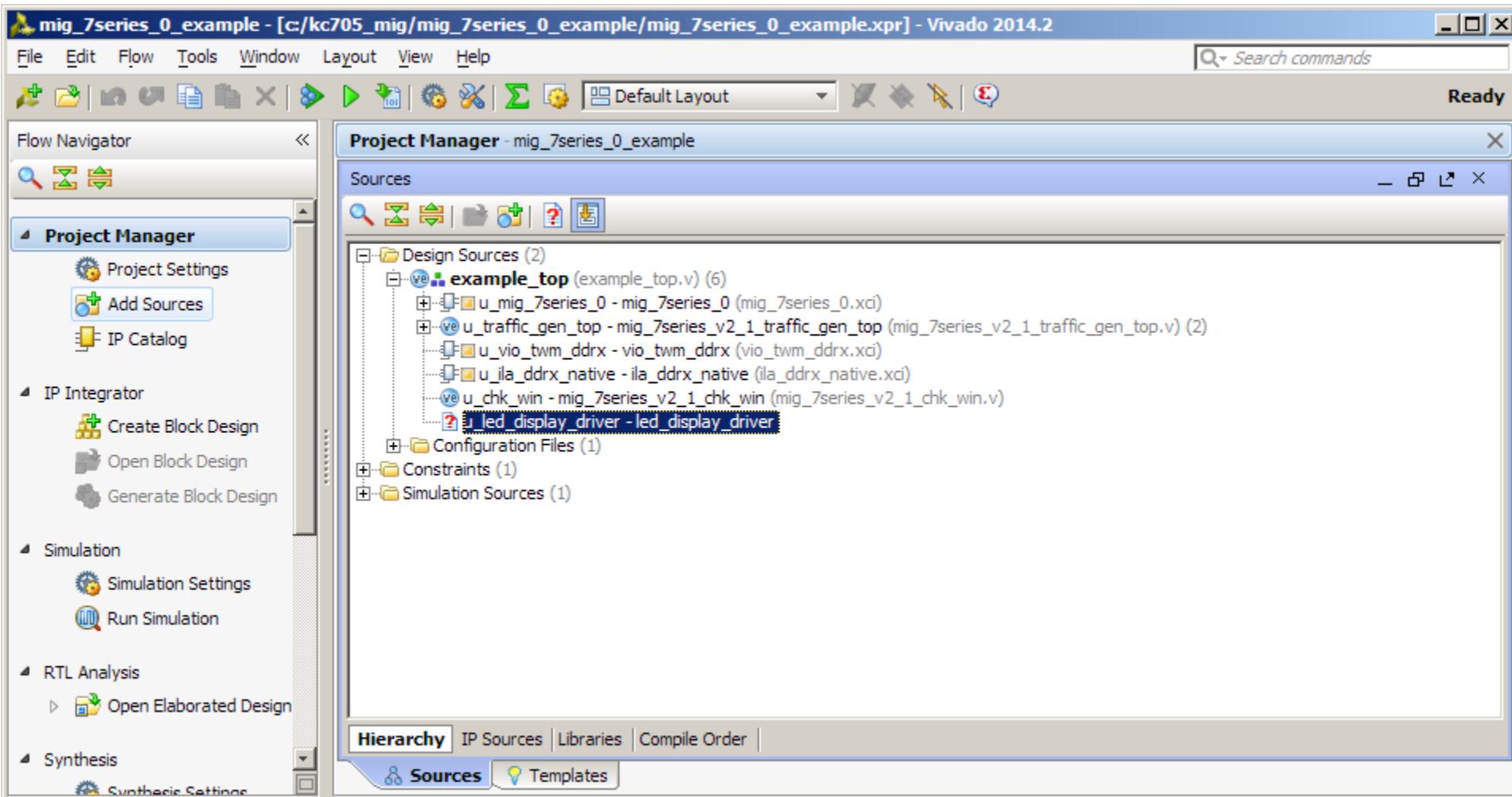
Modifications to Example Design

► Modifications to the example design

- Added RTL and XDC modifications to drive LEDs
- Added DCI Cascade constraints to XDC; for more information on using the DCI Cascade constraints for 7 Series refer to [UG899](#)

Modifications to Example Design

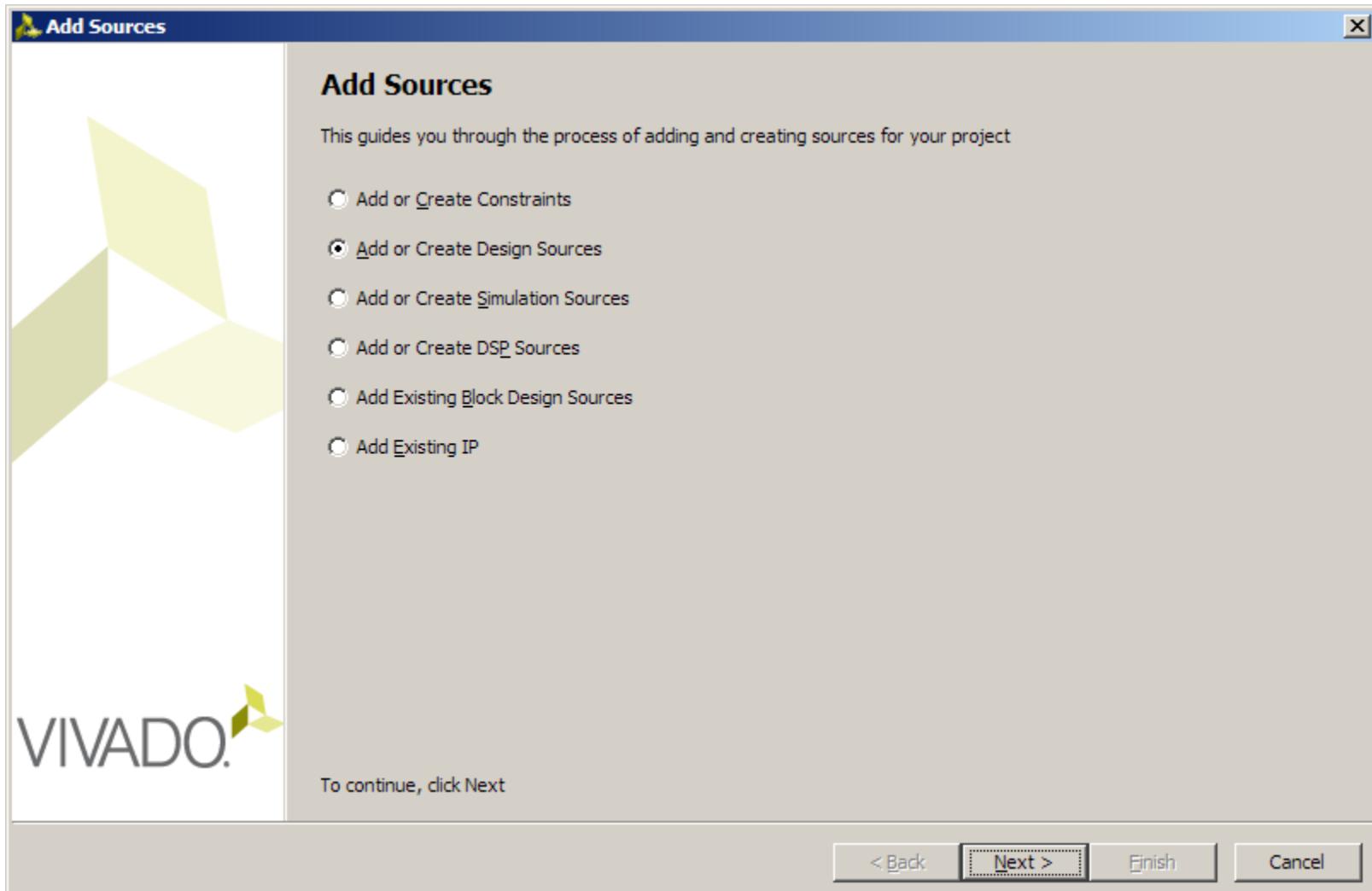
- The LED Display driver RTL file needs to be added manually
- Click on Add Sources



Specify and/or create source files to add to the project

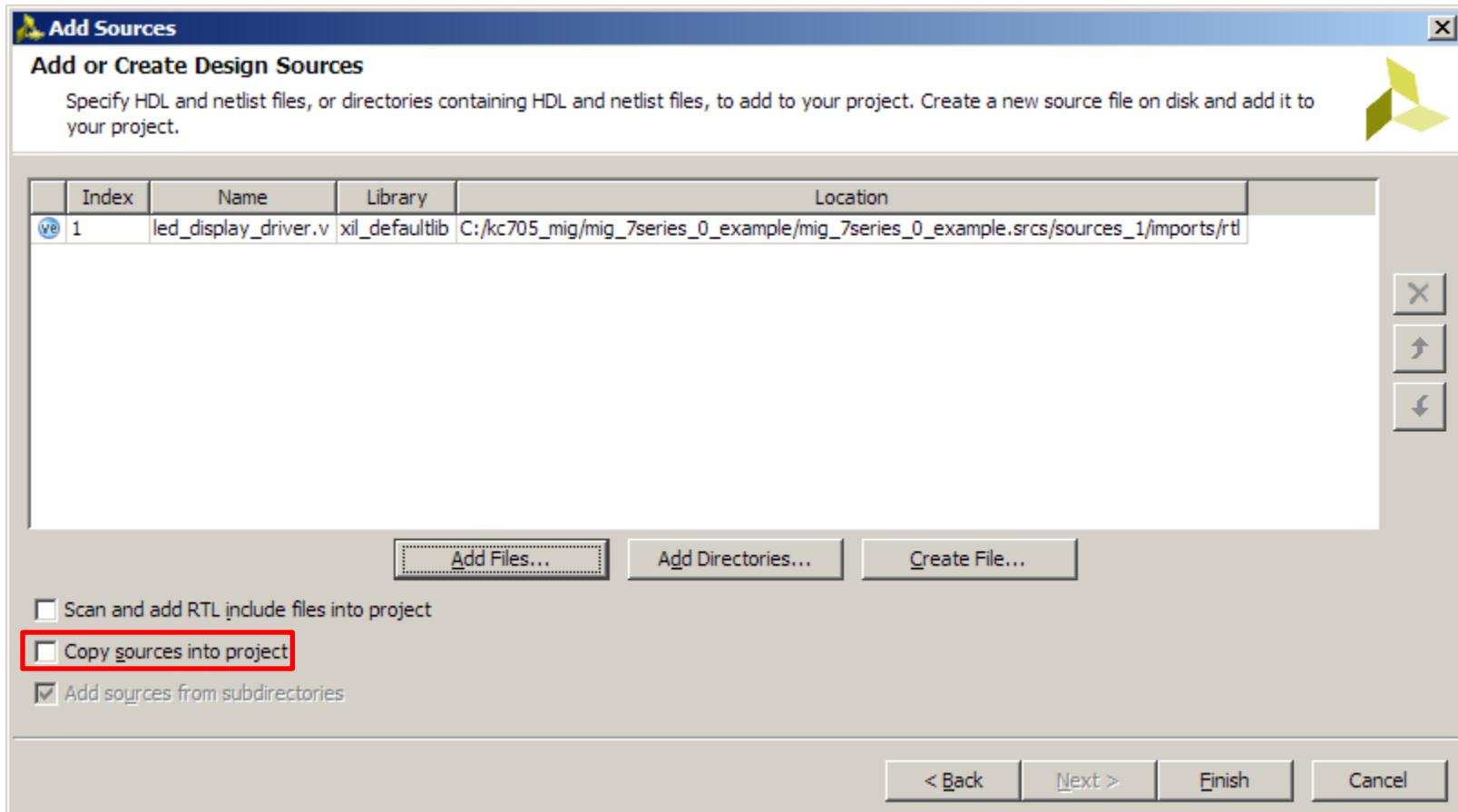
Modifications to Example Design

► Select Add or Create Design Sources and click Next



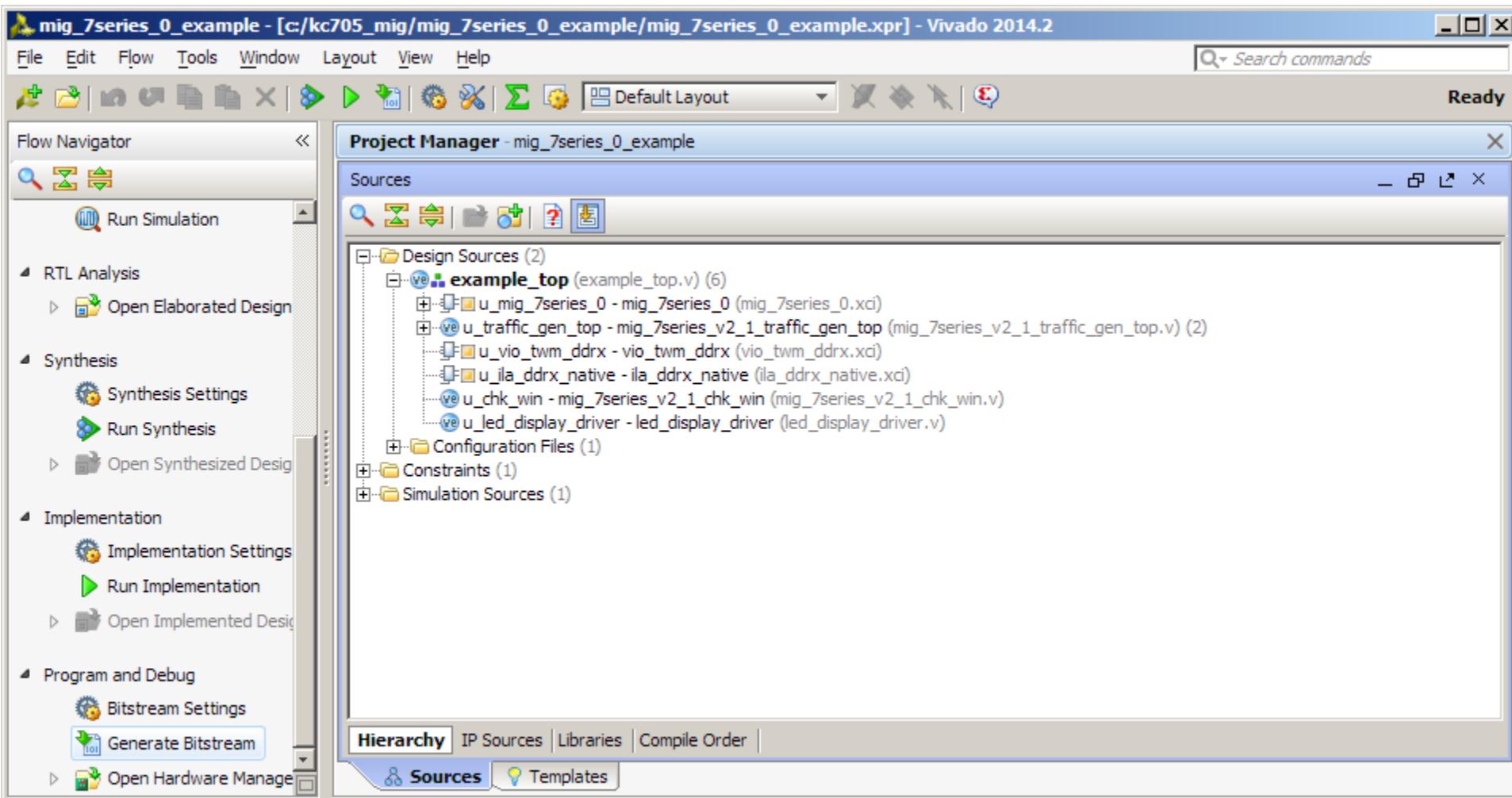
Modifications to Example Design

- Add led_display_driver.v from the example project
- Make sure Copy sources into project is deselected
- Click Finish



Compile Example Design

► Click on Generate Bitstream



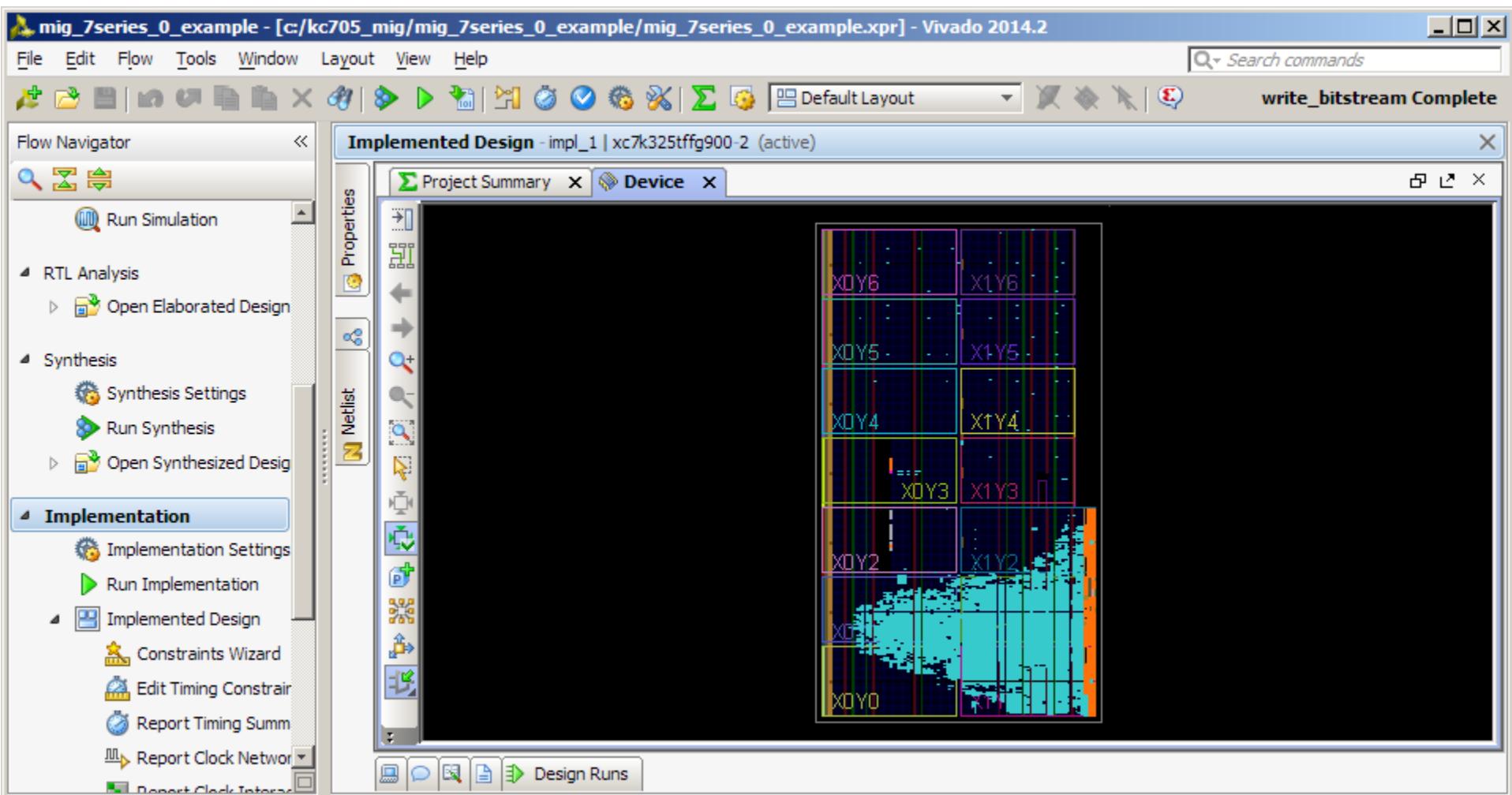
Generate a programming file after implementation

Note: Presentation applies to the KC705

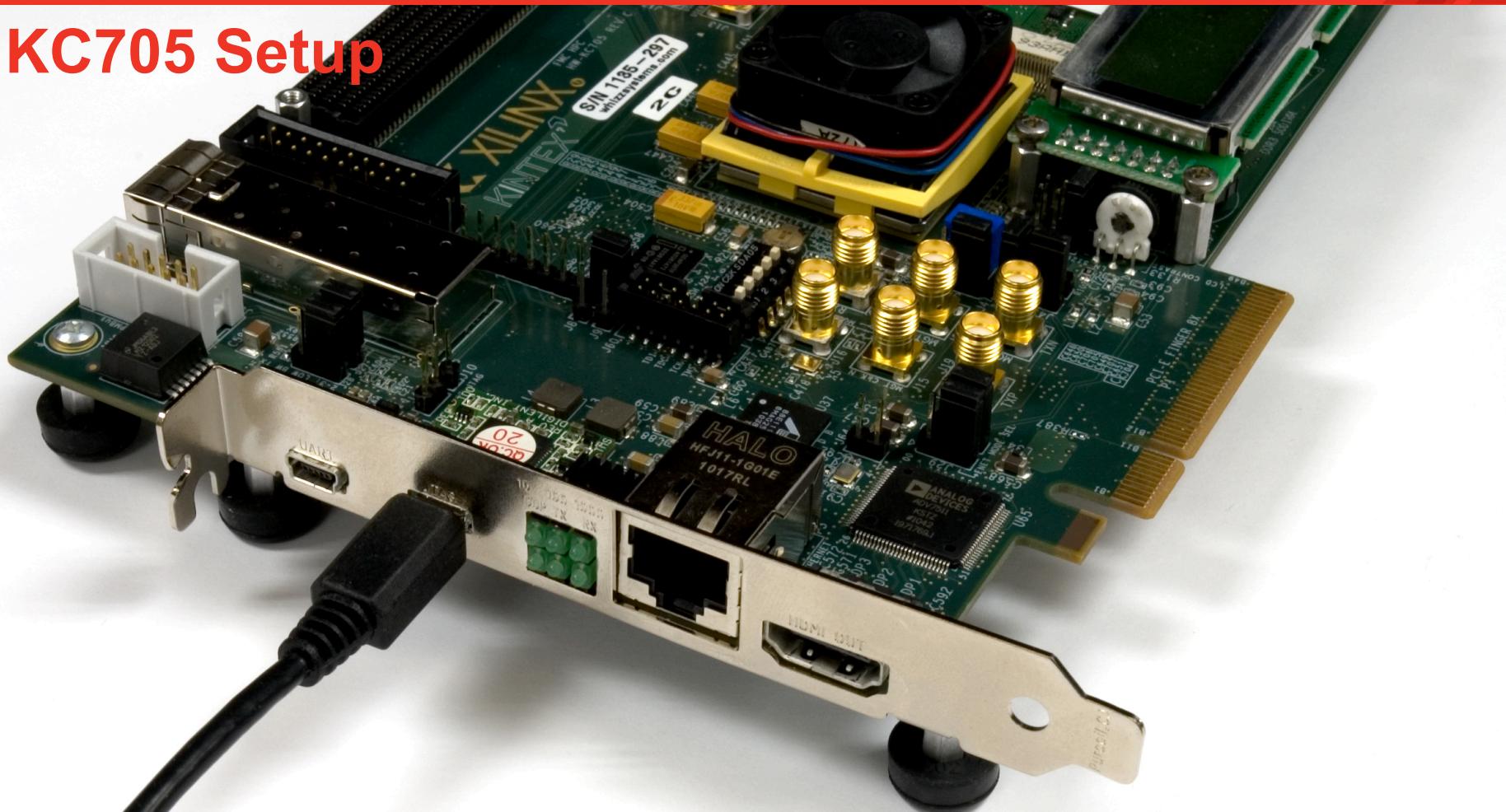
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Compile Example Design

► Open and view the Implemented Design



KC705 Setup

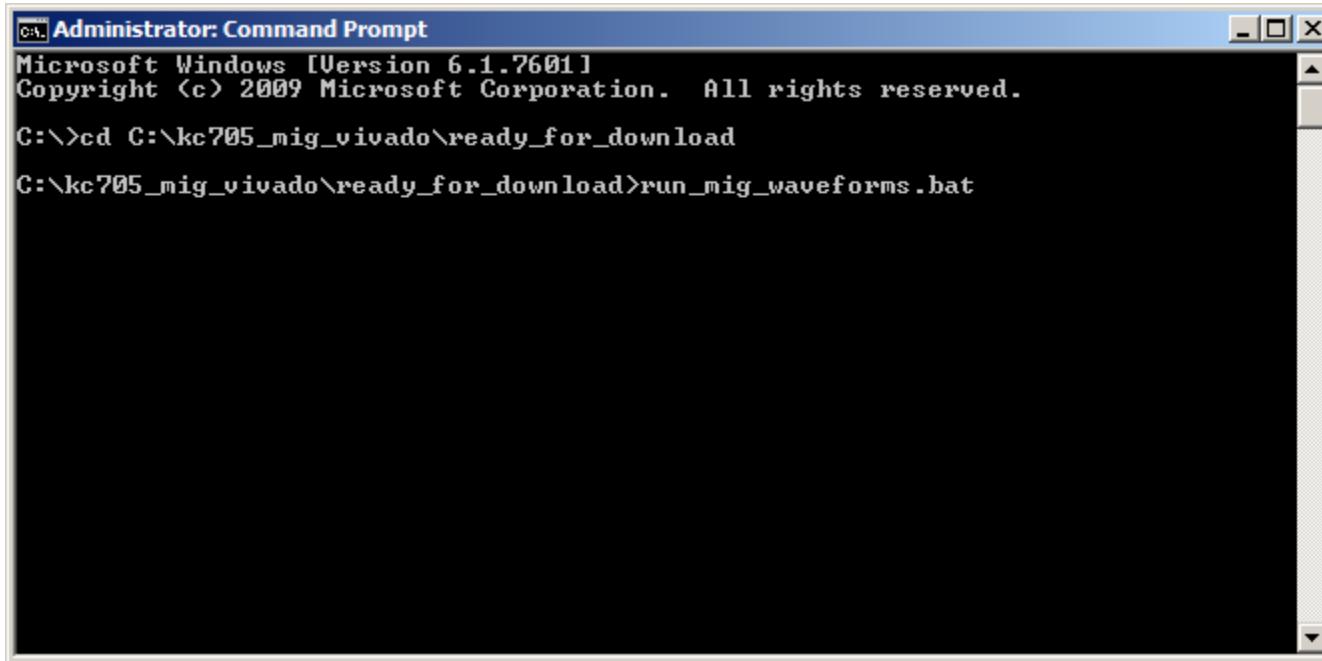


- **Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the KC705 board**
 - Connect this cable to your PC
 - Power on the KC705 board

Run MIG Example Design

- ▶ From a Command Prompt, type:

```
cd C:\kc705_mig\ready_for_download  
run_mig_waveforms.bat
```



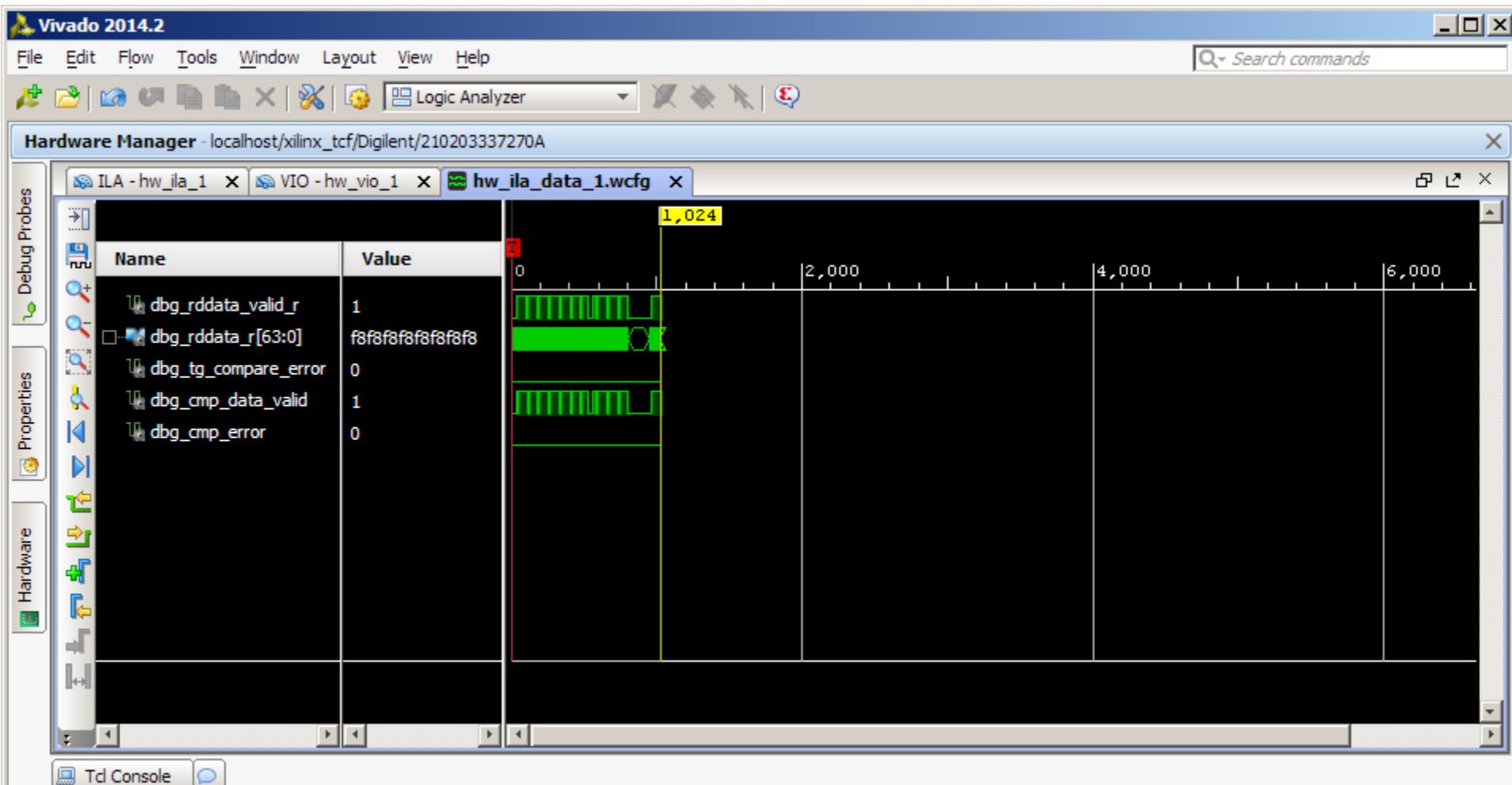
The screenshot shows a Windows Command Prompt window with the title bar 'Administrator: Command Prompt'. The window displays the following text:

```
Microsoft Windows [Version 6.1.7601]
Copyright <c> 2009 Microsoft Corporation. All rights reserved.

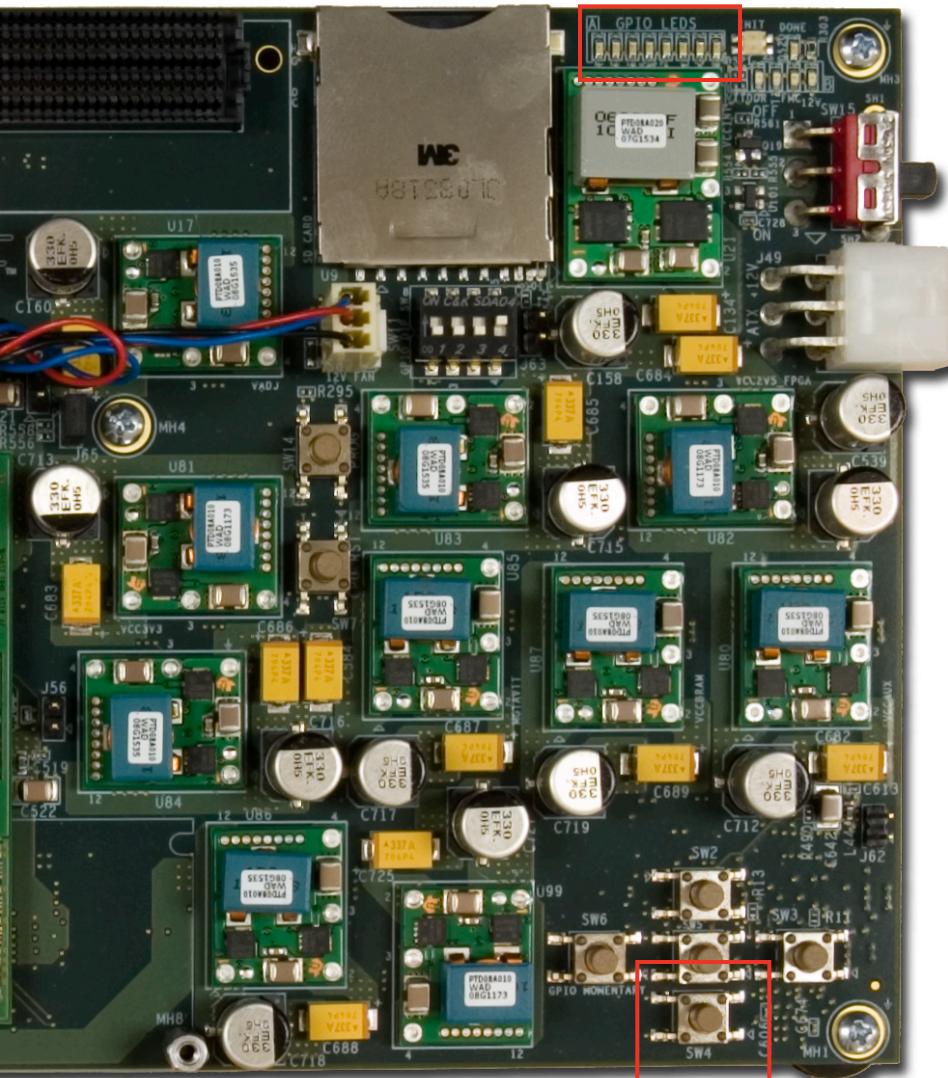
C:>cd C:\kc705_mig_vivado\ready_for_download
C:\kc705_mig_vivado\ready_for_download>run_mig_waveforms.bat
```

Run MIG Example Design

- ▶ Under Tcl script control, Vivado opens, loads the bitstream and generates a MIG waveform



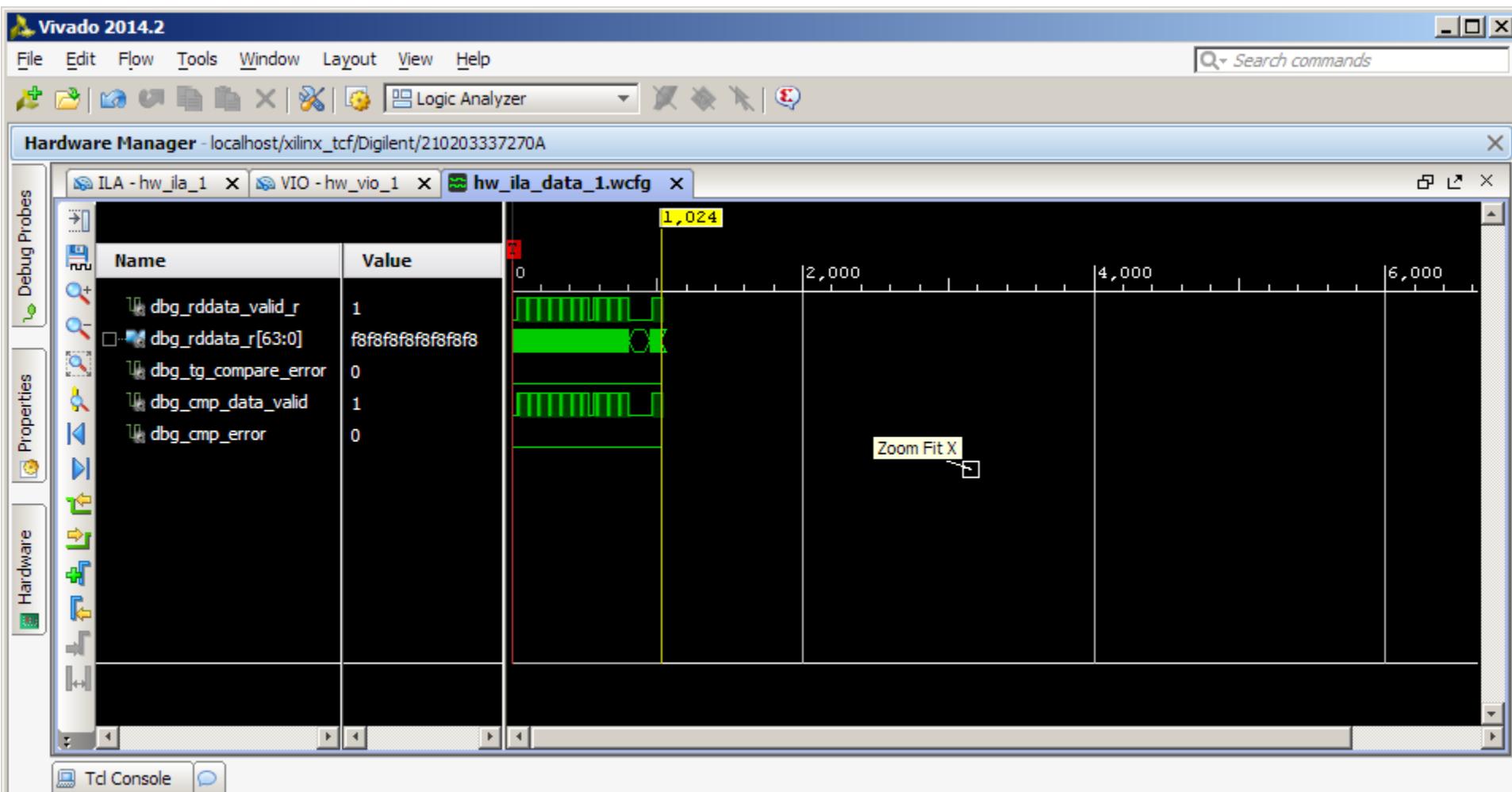
Run MIG Example Design



- After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- LED 3 will light and stay on
 - This indicates Calibration has completed
- If an error occurs, LED 0 will go out and LED 2 will light
 - The “South” button, SW4, is the reset

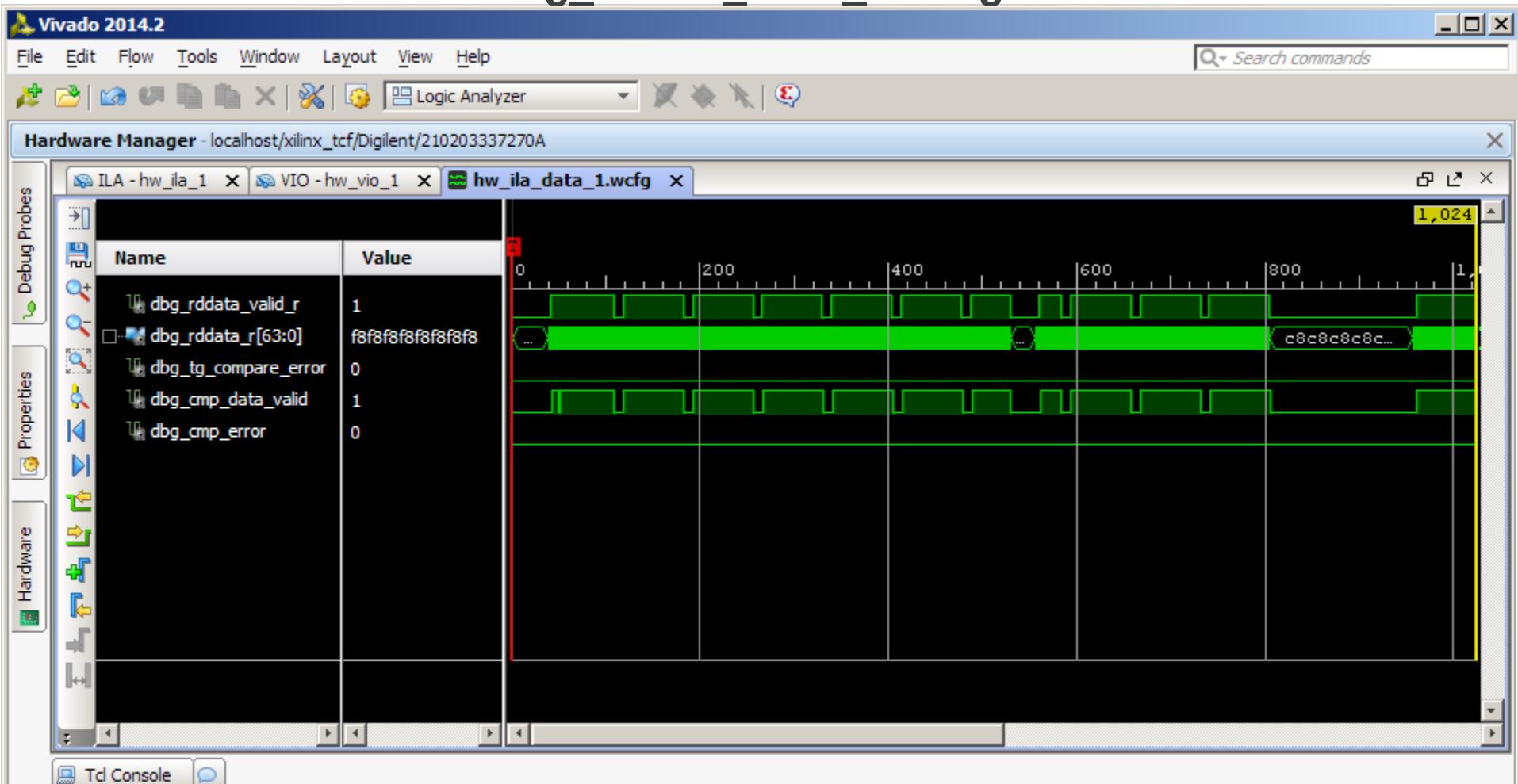
Run MIG Example Design

► Click and drag to the left to expand the waveform



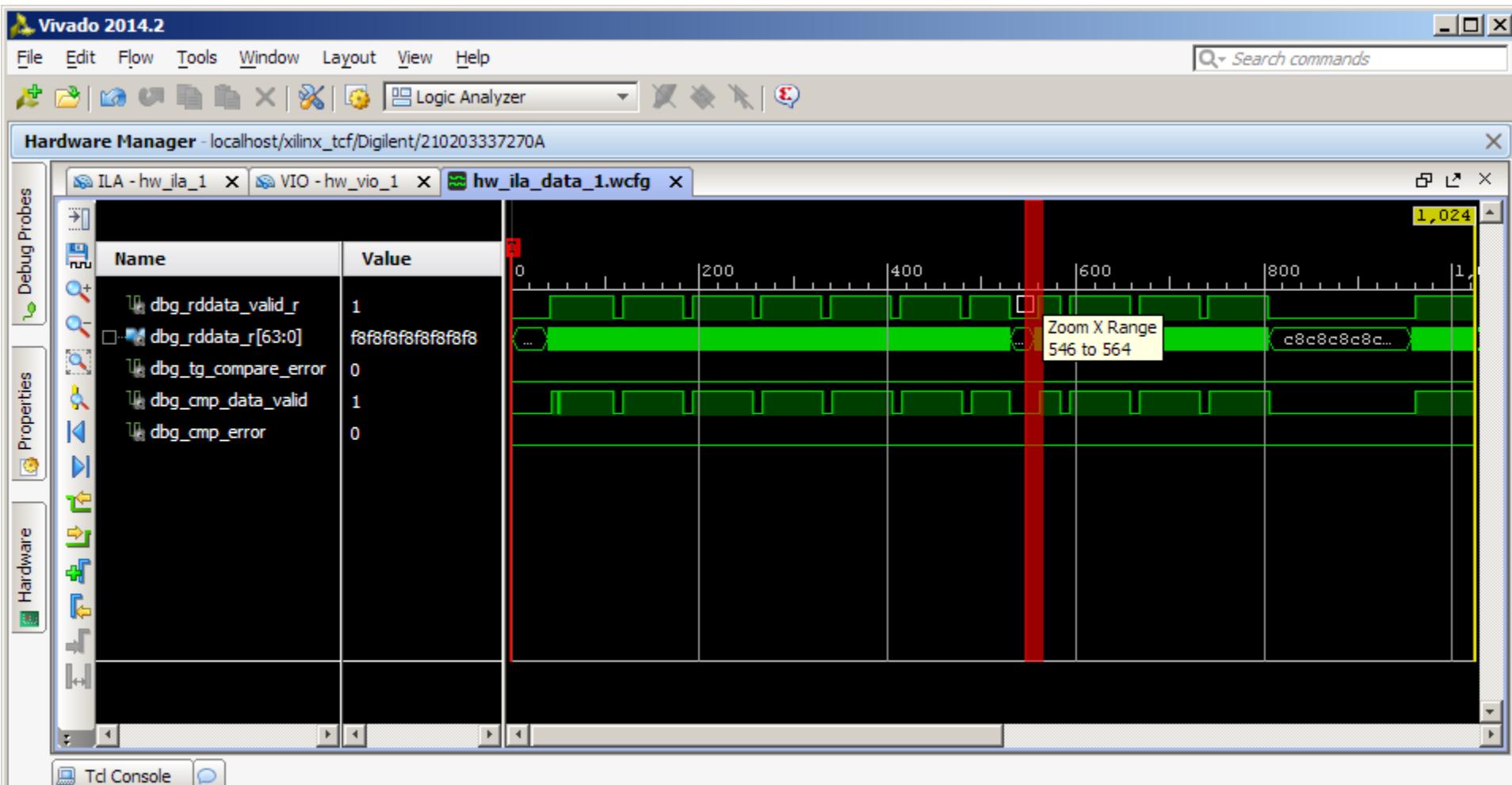
Run MIG Example Design

- View waveforms
- Data is valid when `dbg_rddata_valid_r` is high



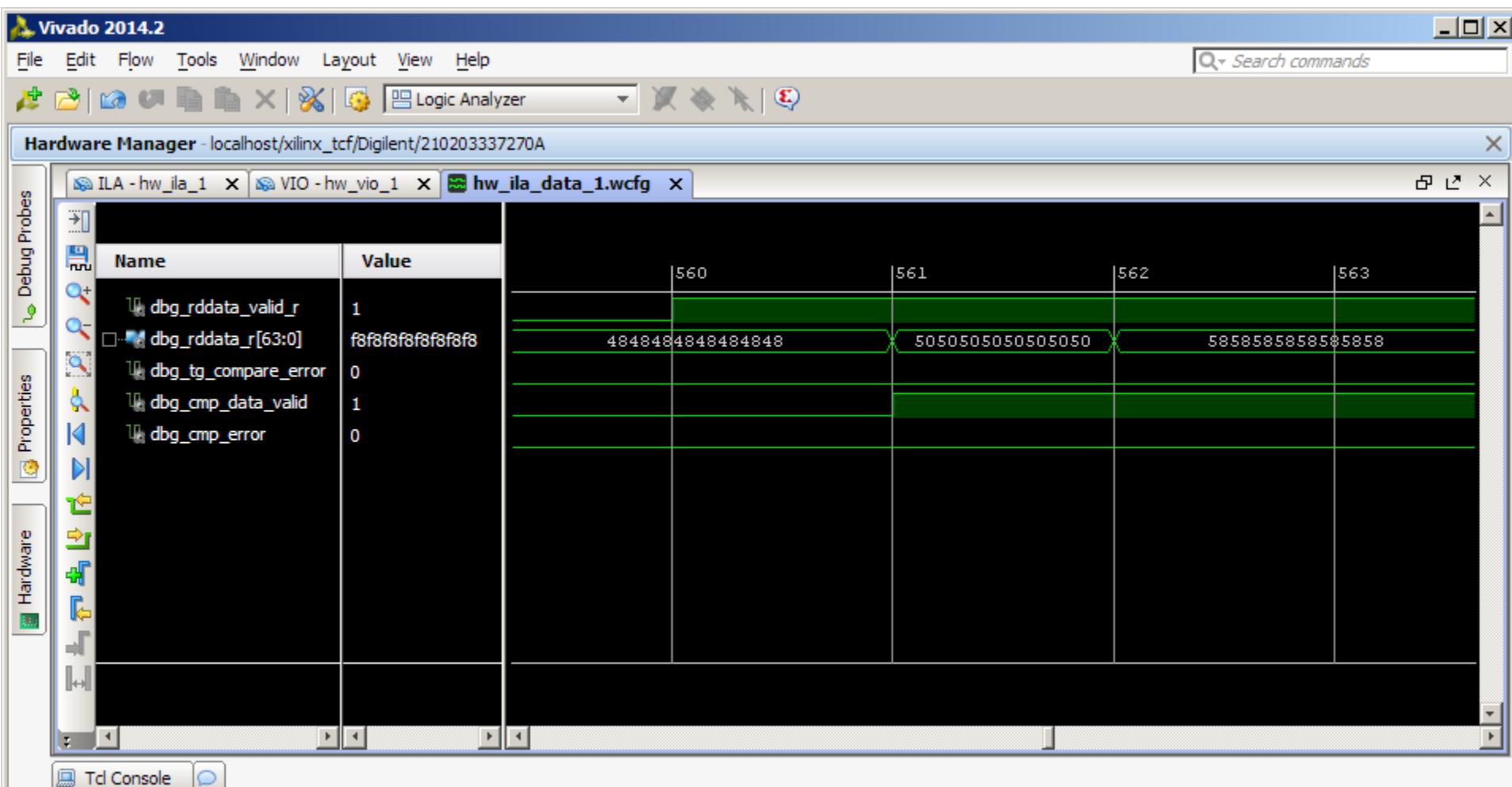
Run MIG Example Design

► Click and drag to the right to zoom in



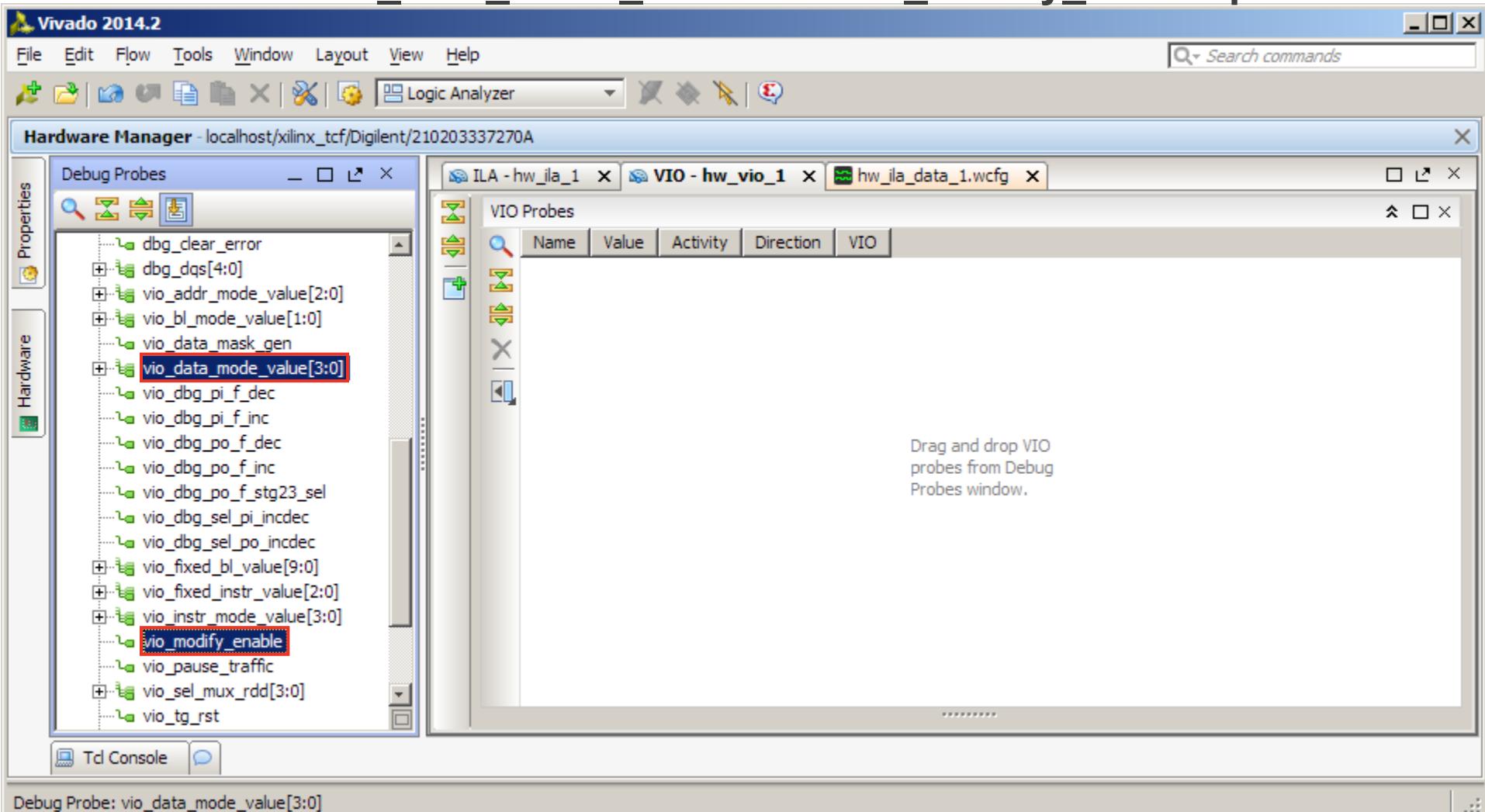
Run MIG Example Design

► View waveform details



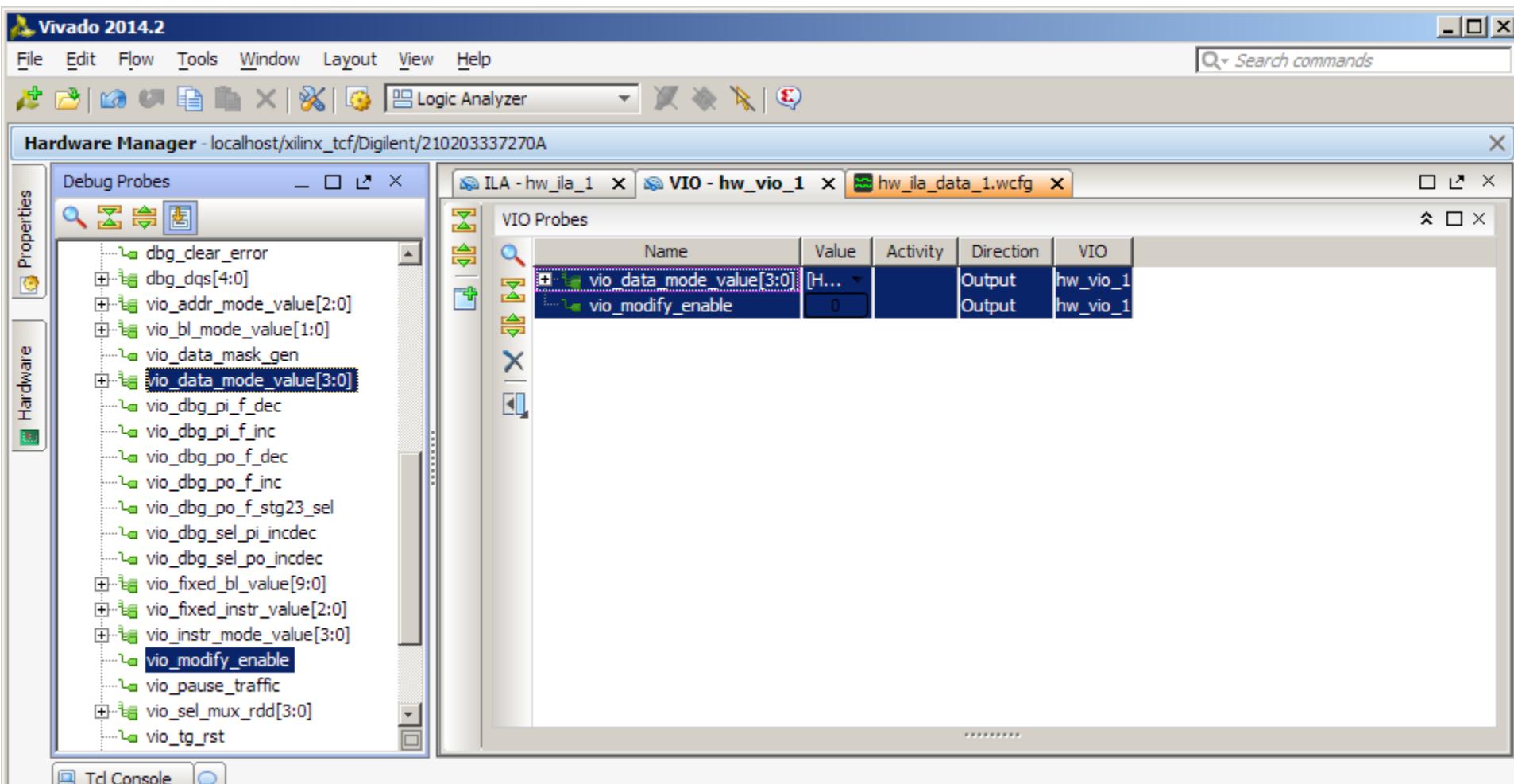
Adjust Data Pattern using VIO Console

- Open the Debug Probes tab and select the VIO – hw_vio_1 tab
- Select the vio_data_mode_value and vio_modify_enable probes



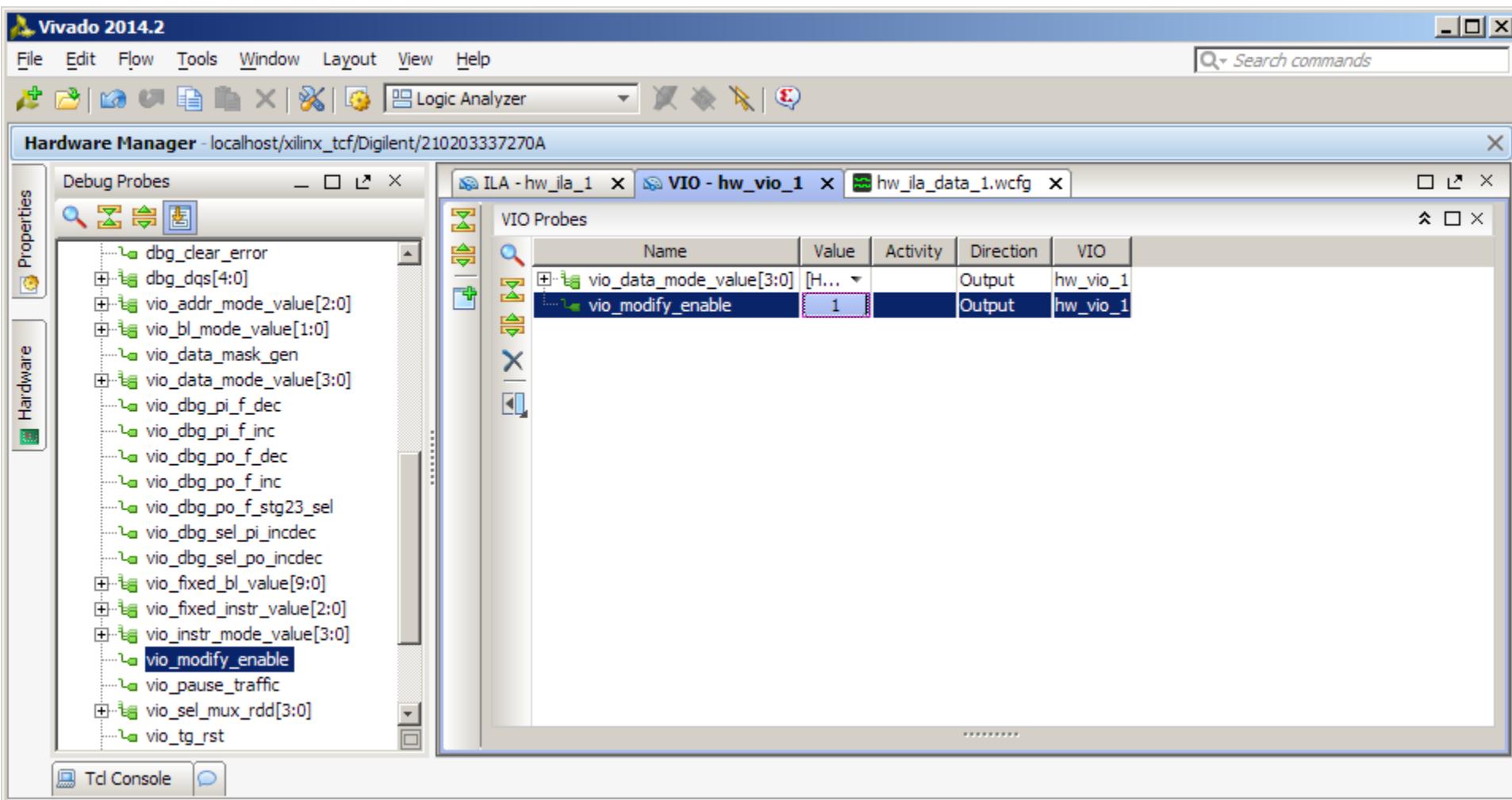
Adjust Data Pattern using VIO Console

► Drag these probes to the VIO – hw_vio_1 tab

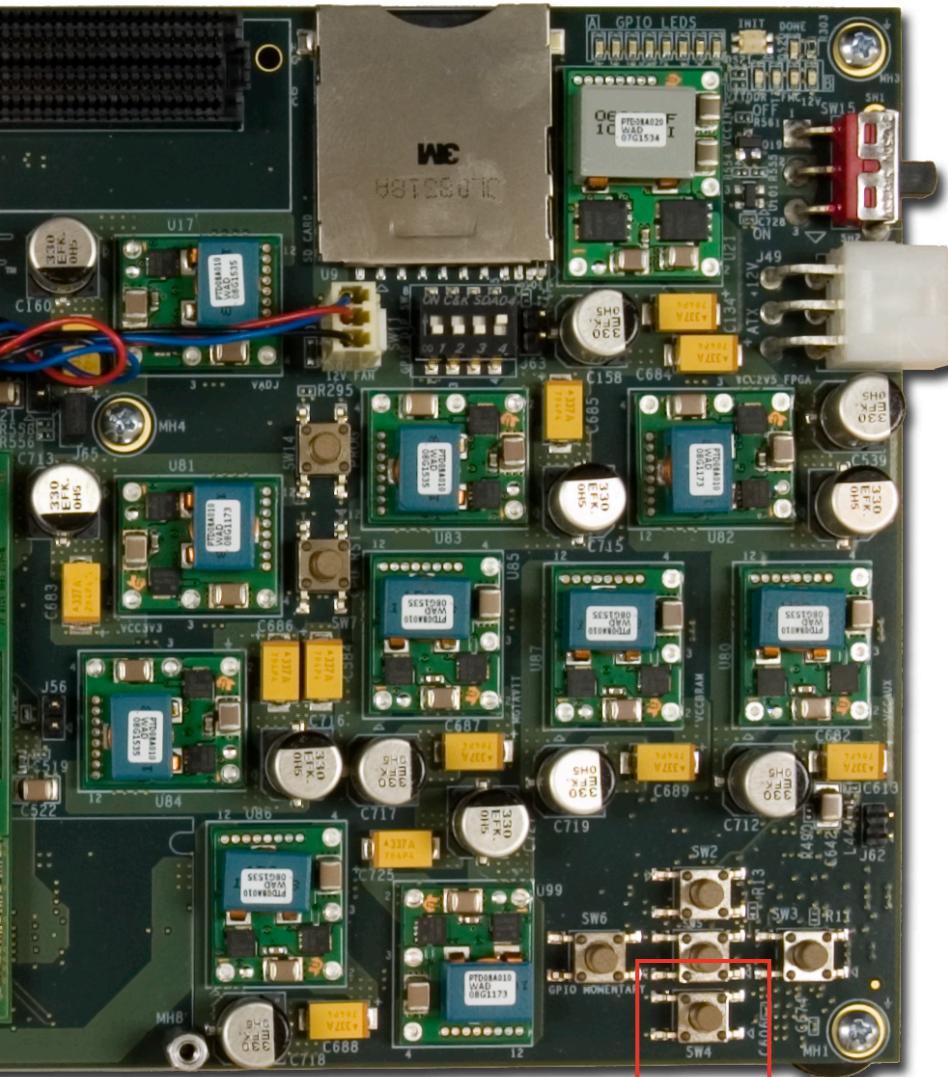


Adjust Data Pattern using VIO Console

- Toggle the vio_modify_enable button to “1”



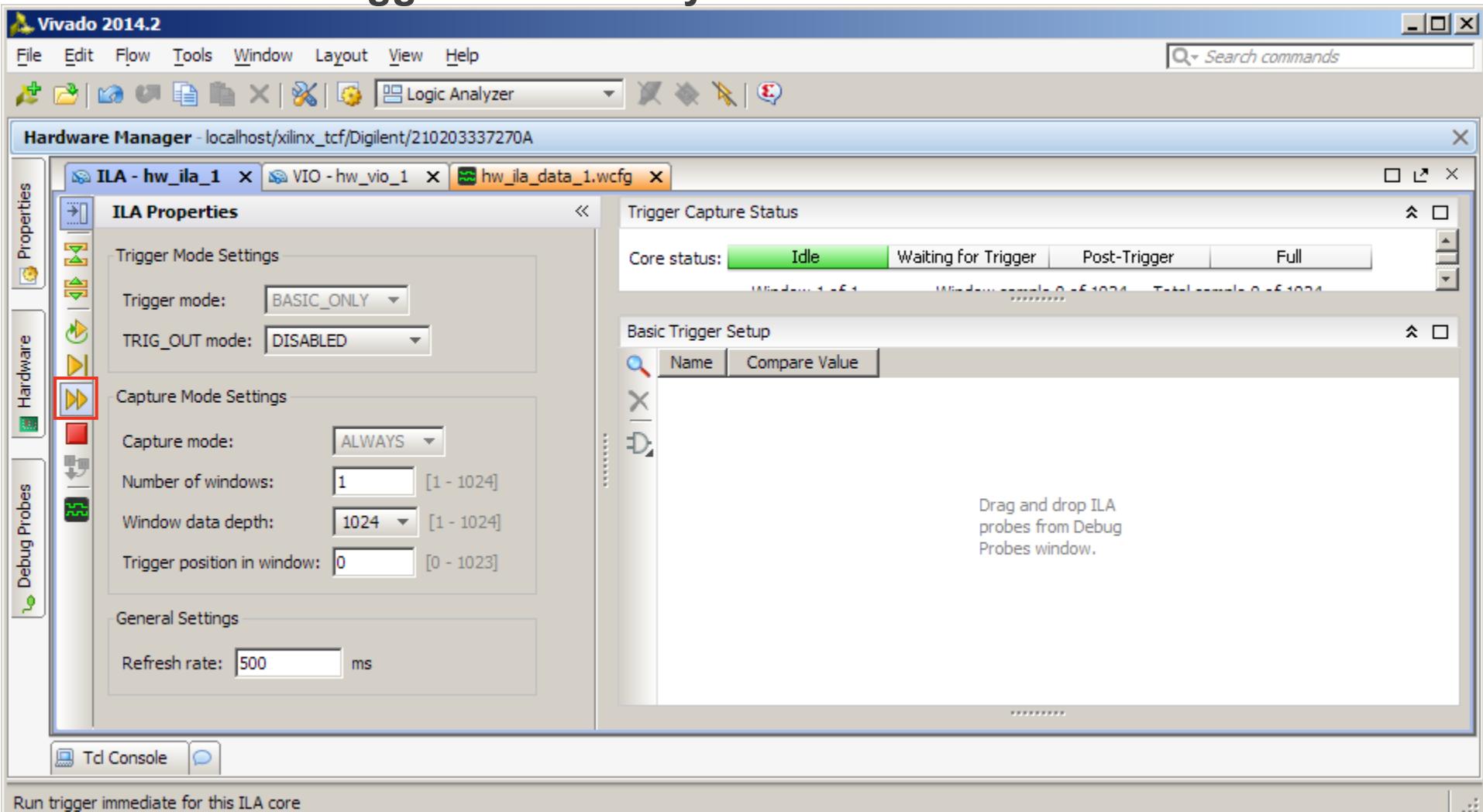
Adjust Data Pattern using VIO Console



► Press and release the CPU RESET switch, SW4, after each change to `vio_modify_enable` or `vio_data_mode_value`

Adjust Data Pattern using VIO Console

- Select the ILA – hw_ilा_1 tab
- Click Run Trigger Immediately



Adjust Data Pattern using VIO Console

- Select the hw_ilab_data_1.wcfg tab
- View PRBS data

The screenshot shows the Vivado 2014.2 Hardware Manager window. The title bar reads "Vivado 2014.2". The menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. A search bar at the top right says "Search commands". The toolbar below the menu has icons for New, Open, Save, Close, Logic Analyzer, and others. The main area is titled "Hardware Manager - localhost/xilinx_tcf/Digilent/210203337270A". There are three tabs open: "ILA - hw_ilab_1", "VIO - hw_vio_1", and "hw_ilab_data_1.wcfg" (which is the active tab). On the left, there are tabs for Properties, Hardware, and Debug Probes. The central pane displays a table with columns "Name" and "Value". The table rows are:

Name	Value
dbg_rddata_valid_r	1
dbg_rddata_r[63:0]	e5cb962c59b265ca
dbg_tg_compare_error	0
dbg_cmp_data_valid	1
dbg_cmp_error	0

Below the table, there are several green horizontal bars representing memory or data segments. The bottom of the window has buttons for Tcl Console and a message center.

References

References

► Kintex-7 Memory

- 7 Series FPGAs Memory Interface Solutions User Guide – UG586
 - http://www.xilinx.com/support/documentation/ip_documentation/mig_7series/v2_1/ug586_7Series_MIS.pdf

► Vivado Programming and Debugging

- Vivado Design Suite Programming and Debugging User Guide
 - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_2/ug908-vivado-programming-debugging.pdf

Documentation

Documentation

► Kintex-7

- Kintex-7 FPGA Family
 - <http://www.xilinx.com/products/silicon-devices/fpga/kintex-7/index.htm>
- Design Advisory Master Answer Record for Kintex-7 FPGAs
 - <http://www.xilinx.com/support/answers/42946.htm>

► KC705 Documentation

- Kintex-7 FPGA KC705 Evaluation Kit
 - <http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm>
- KC705 Getting Started Guide
 - http://www.xilinx.com/support/documentation/boards_and_kits/kc705/2013_2/ug883_K7_KC705_Eval_Kit.pdf
- KC705 User Guide
 - http://www.xilinx.com/support/documentation/boards_and_kits/kc705/ug810_KC705_Eval_Bd.pdf