KC705 MultiBoot Design

June 2014

XTP201

Revision History

Date	Version	Description
06/09/14	9.0	Recompiled for 2014.2. AR44635 and AR60411 fixed.
04/25/14	6.1	Added AR44635 and AR60411.
04/16/14	6.0	Recompiled for 2014.1.
12/18/13	5.0	Recompiled for 2013.4.
10/23/13	4.0	Recompiled for 2013.3. Added AR58291.
07/01/13	3.1	Minor updates.
06/19/13	3.0	Recompiled for 2013.2. AR55431 fixed.
04/03/13	2.0	Recompiled for 2013.1. Added AR55431.
12/18/12	1.0	Initial version. Added AR53392.

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Overview

- Kintex-7 MultiBoot Capability
- Overview of 7 Series Fallback MultiBoot
- Xilinx KC705 Board
- Software Requirements
- KC705 Setup
- Compiling the MultiBoot Design
- Run MultiBoot Design
- Kintex-7 MultiBoot Details
- References

Note: This presentation applies to the KC705

Kintex-7 MultiBoot Capability

- **What is MultiBoot?**
  - The MultiBoot feature allows the FPGA application to load two or more FPGA bitstreams under the control of the FPGA application. The FPGA application triggers a MultiBoot operation, causing the FPGA to reconfigure from a different configuration bitstream. After a MultiBoot operation is triggered, the FPGA restarts its configuration process as usual.
  - More details can be found in UG470
- **MultiBoot Capability**
  - FPGA application controlled configuration
  - Bitstream selection of multiple applications
- **Safe Update**
  - Golden bitstream
  - Upgradeable bitstream
  - Failure recovery
    - Possible Triggers (CRC error, IDCODE error, WDT timeout)

Note: Presentation applies to the KC705

Kintex-7 MultiBoot Capability

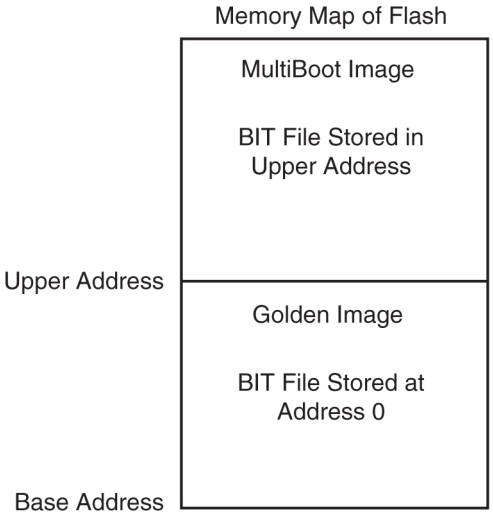
- **Overview of 7 Series Fallback MultiBoot**
  - The 7 series FPGAs MultiBoot and fallback features support updating systems in the field. Bitstream images can be upgraded dynamically in the field. The FPGA MultiBoot feature enables switching between images on the fly. When an error is detected during the MultiBoot configuration process, the FPGA can trigger a fallback feature that ensures a known good design can be loaded into the device.
  - The MultiBoot feature allows the FPGA application to load two or more FPGA bitstreams under the control of the FPGA application. The FPGA application triggers a MultiBoot operation, causing the FPGA to reconfigure from a different configuration bitstream. After a MultiBoot operation is triggered, the FPGA restarts its configuration process as usual.
- **Reference Design Source and Application**
  - RDF0191 - KC705 MultiBoot Design Files (2014.2 C) zip file
  - Available through http://www.xilinx.com/kc705

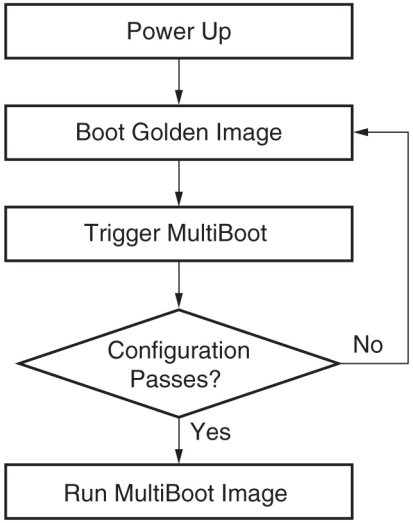
Note: Presentation applies to the KC705

KC705 MultiBoot Design Description

- **Description**
  - Design consists of three bitstreams, golden_iprog_spi.bit, multiboot.bit, and corrupted.bit loaded in the PROM at 0x0, 0x400000, and 0x800000
  - The golden_iprog_spi.bit has software to allow a reboot to the second or third bitstreams with certain switch settings
  - The multiboot.bit is compiled with this property set:

    set_property BITSTREAM.CONFIG.CONFIGFALLBACK Enable [current_design]
  - The corrupted.bit is a multiboot.bit with one byte changed to force a CRC error when loaded
- **This diagram shows the general process**
  - Since the corrupted.bit doesn't pass configuration, the Golden Image is booted





Note: Presentation applies to the KC705

Upgrade Example

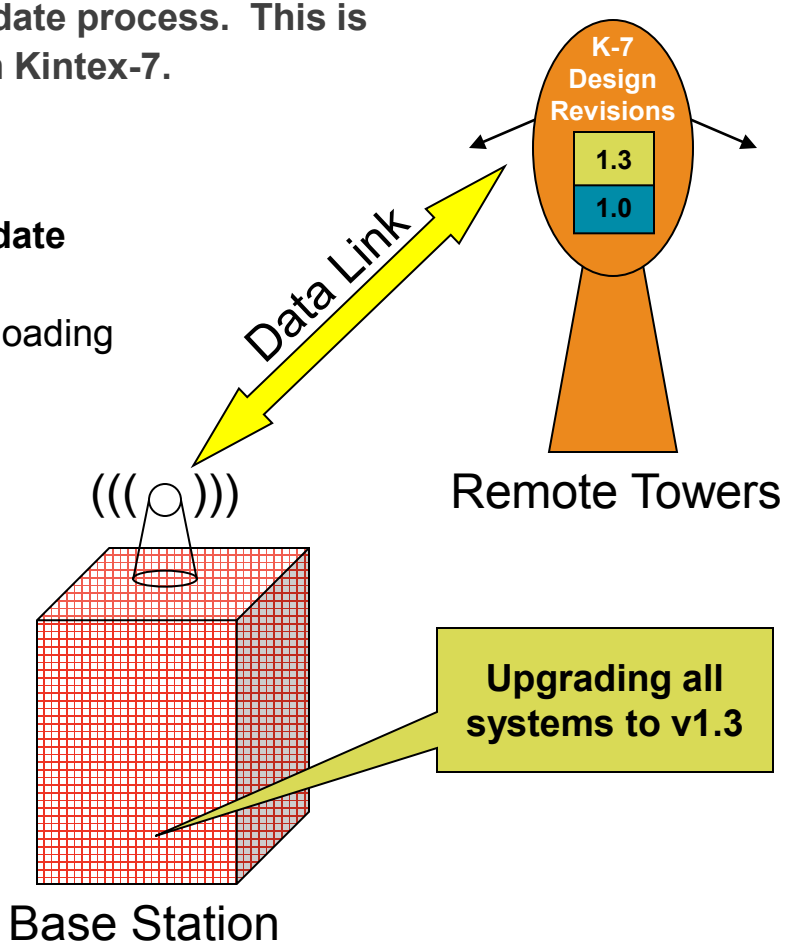
- **MultiBoot:** **Process by which the FPGA selectively reprograms and reloads its bitstream from an attached external memory.**
- **Safe update:** **Field updating bitstream storage with a new bitstream in such a manner to prevent any failure due to a failure in the update process. This is accomplished with the enhanced MultiBoot available in Kintex-7.**

Can a multi-boot system be implemented without safe update design considerations?

Yes – If there are no potential for disruptions during flash loading

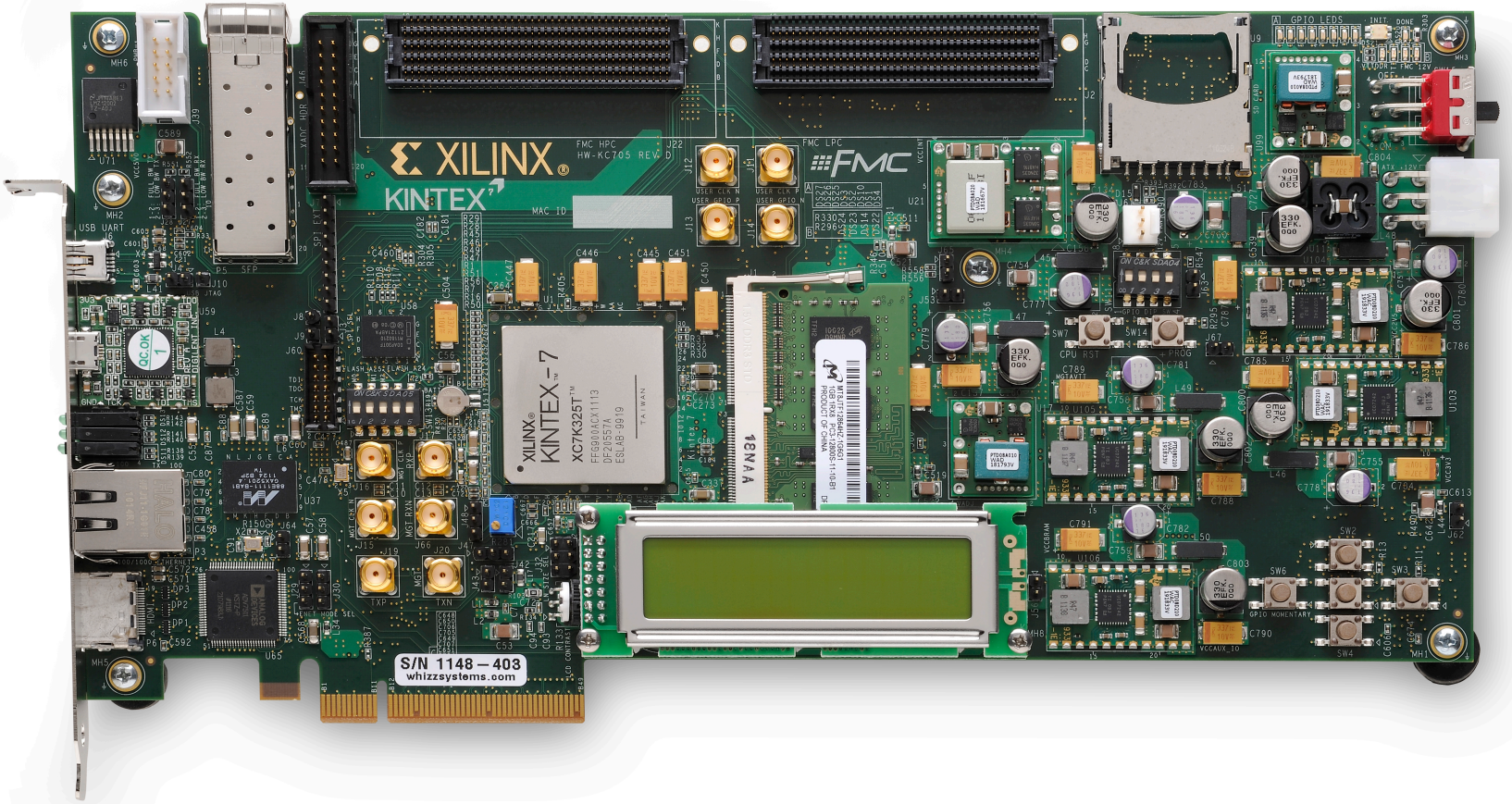
How is a system upgraded?

1. New multi-boot image is created
2. System setup to receive the new image
3. User application erases section of Flash
4. The new image is delivered into the system's Flash
5. User application resets system



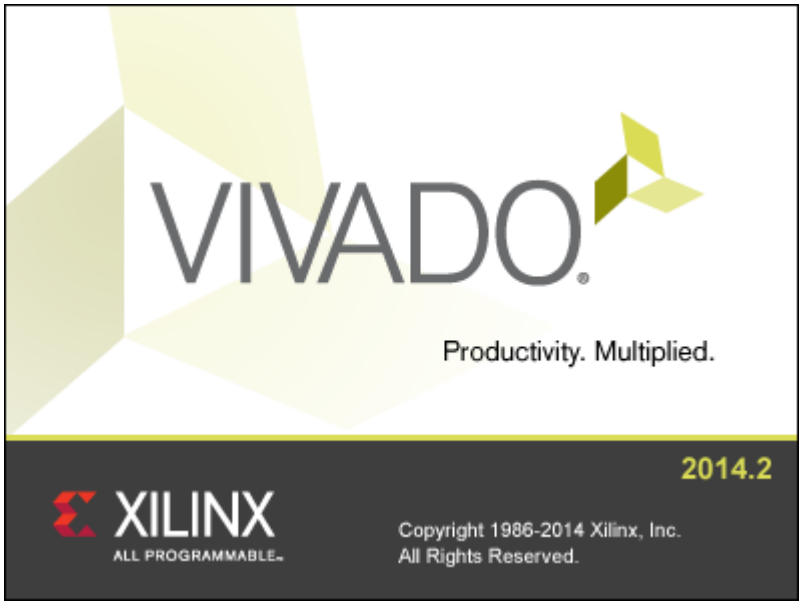
Note: Presentation applies to the KC705

Xilinx KC705 Board



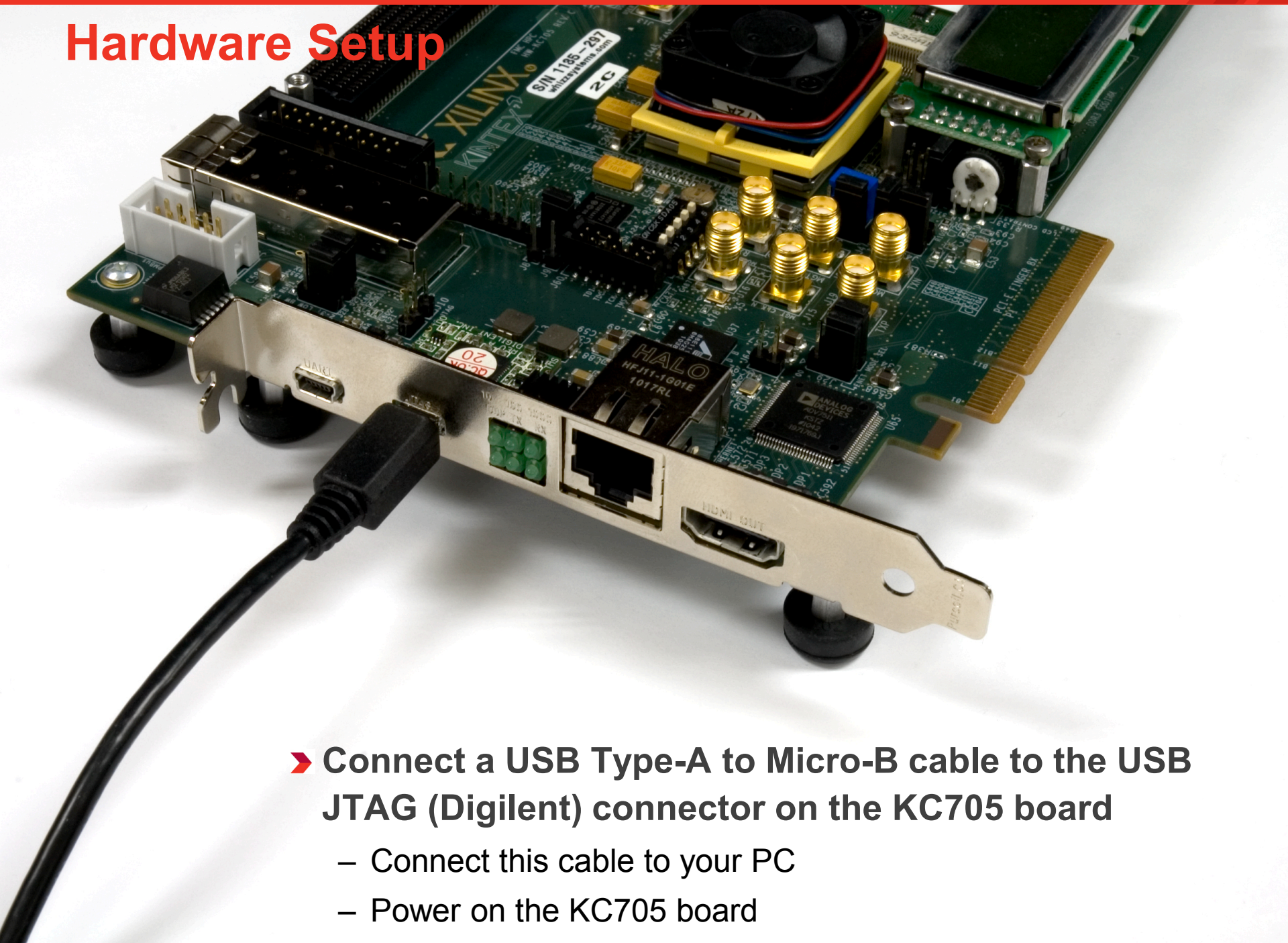
Vivado Software Requirements

- **Xilinx Vivado Design Suite 2014.2, Design Edition + SDK**
  - Combined installer



Note: Presentation applies to the KC705

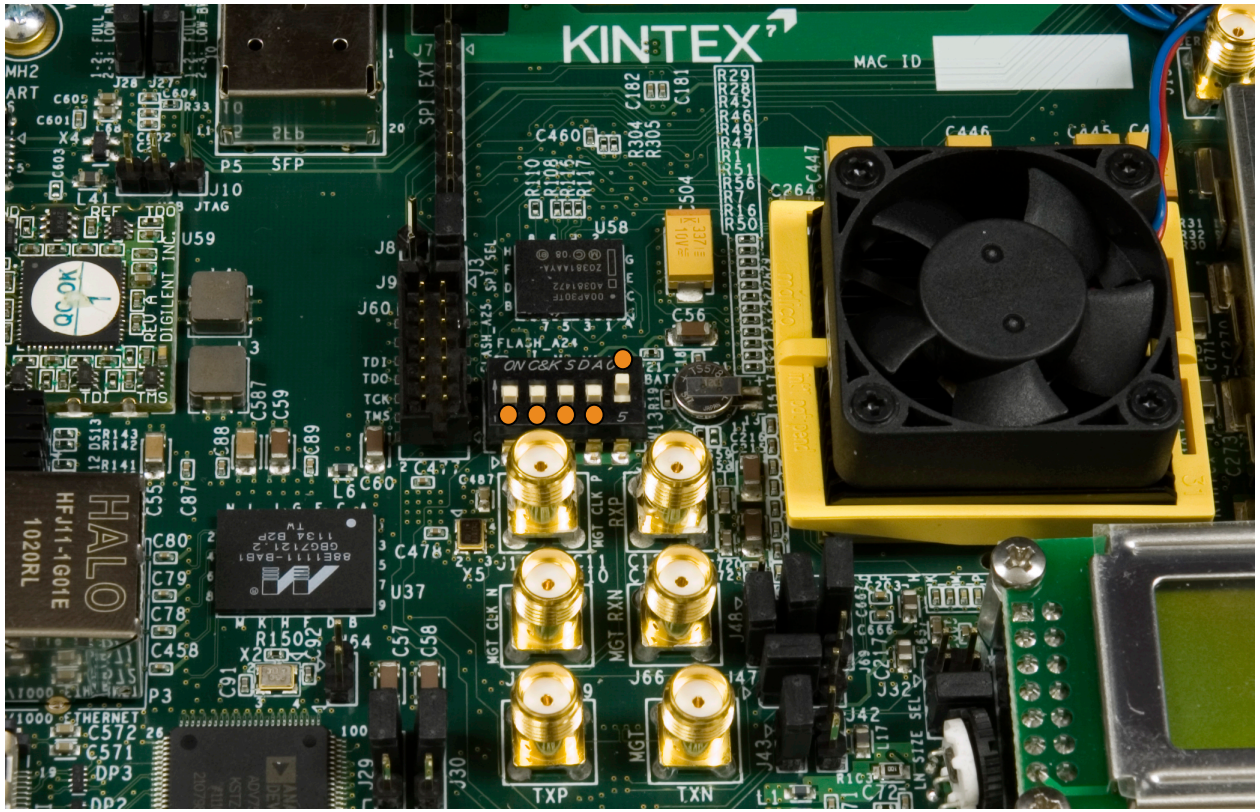
Hardware Setup



- **Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the KC705 board**
  - Connect this cable to your PC
  - Power on the KC705 board

Hardware Setup

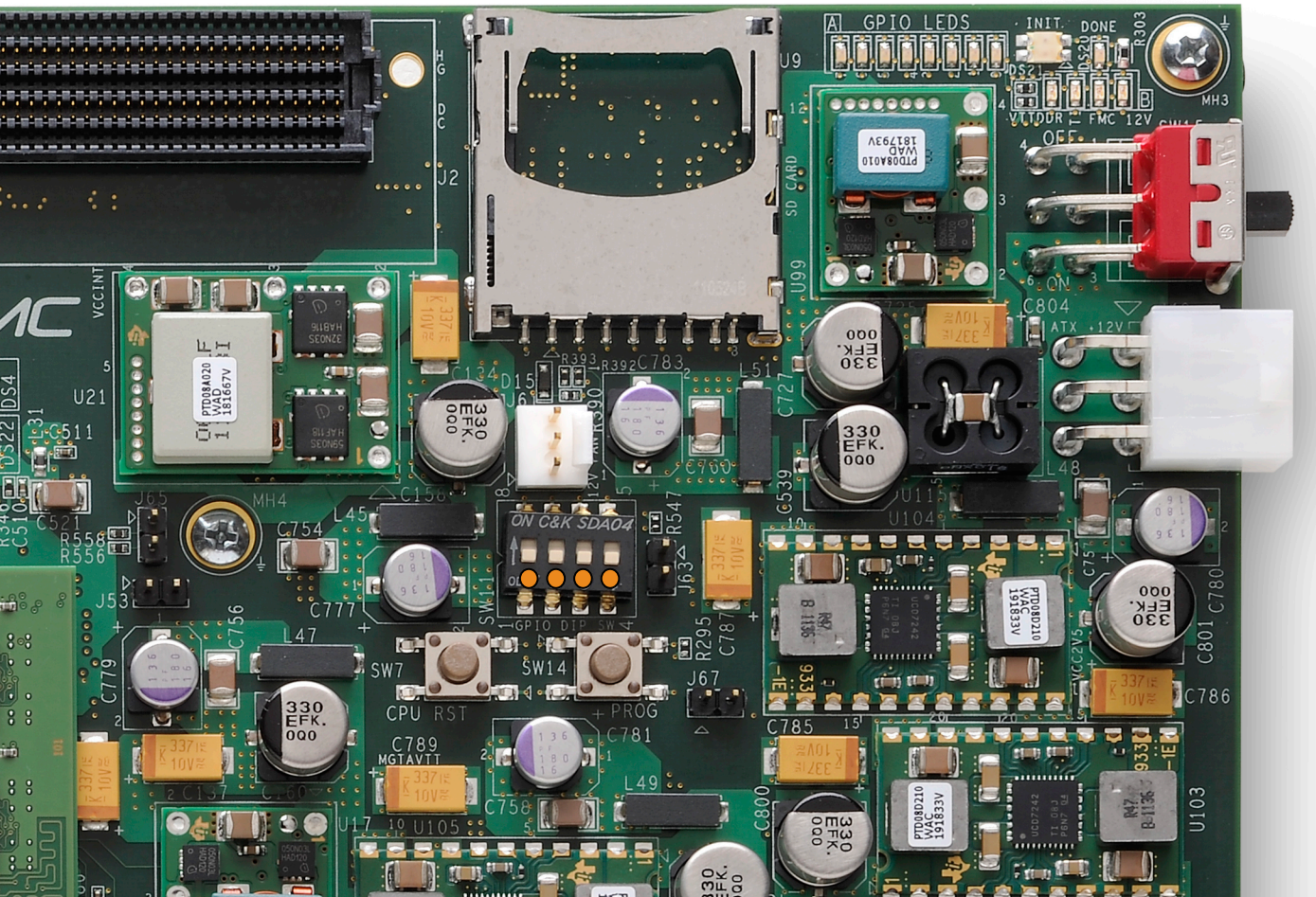
- **Set S13 to 00001 (1 = on, Position 1 → Position 5)**
  - This enables Master SPI configuration from the QSPI Flash
    - Flash A25, A24 = 00
    - FPGA mode pins M[2:0] = 001



Note: Presentation applies to the KC705

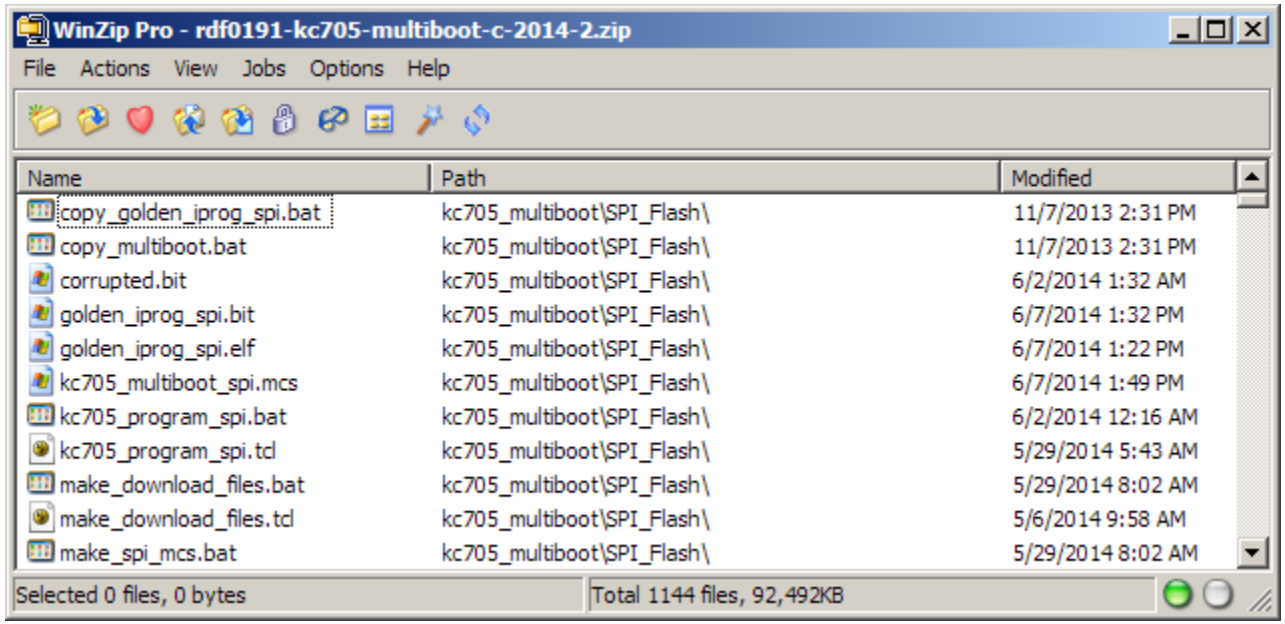
Hardware Setup

- **Set S11 to 0000 (1 = on, Position 1 → Position 4)**
  - This sets the MultiBoot functions to off



Program SPI MultiBoot Design

- **Unzip the RDF0191 - KC705 MultiBoot Design Files (2014.2 C) zip file**
  - Available through http://www.xilinx.com/kc705
  - AR44635 has been applied to this design

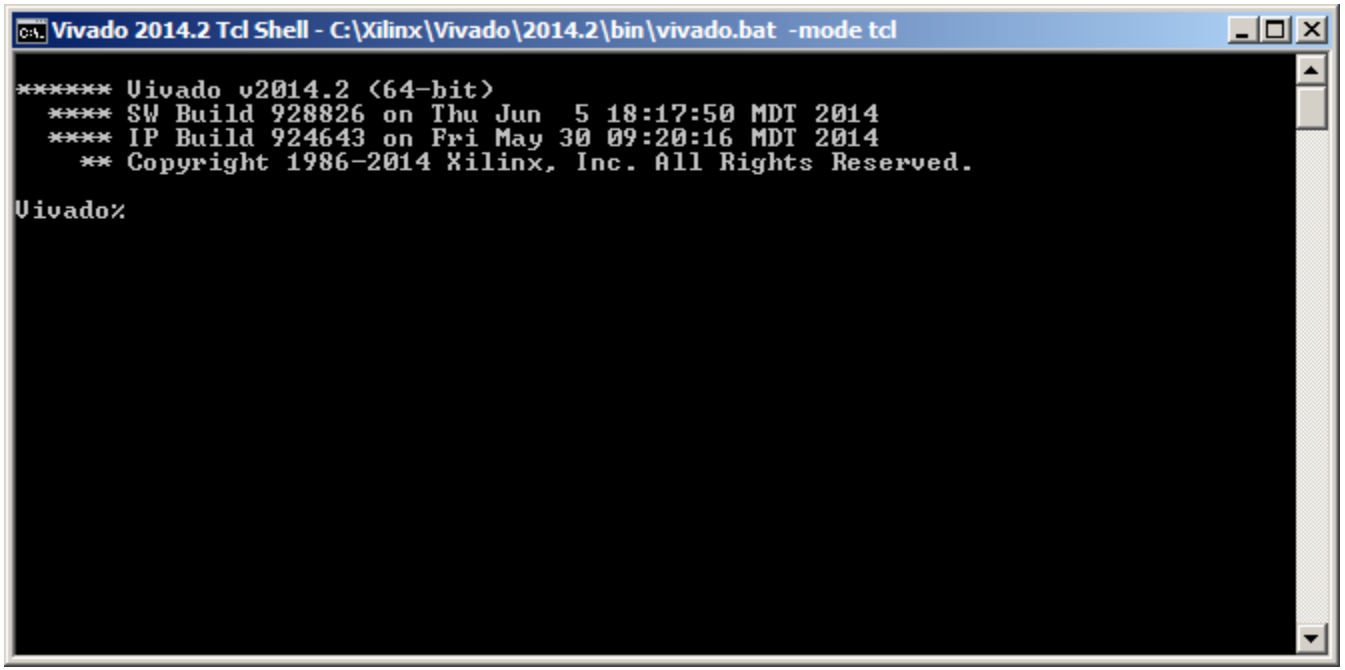


Note: Presentation applies to the KC705

Program SPI MultiBoot Design

- Open a Vivado Tcl Shell:

  Start → All Programs → Xilinx Design Tools → Vivado 2014.2 → Vivado 2014.2 Tcl Shell



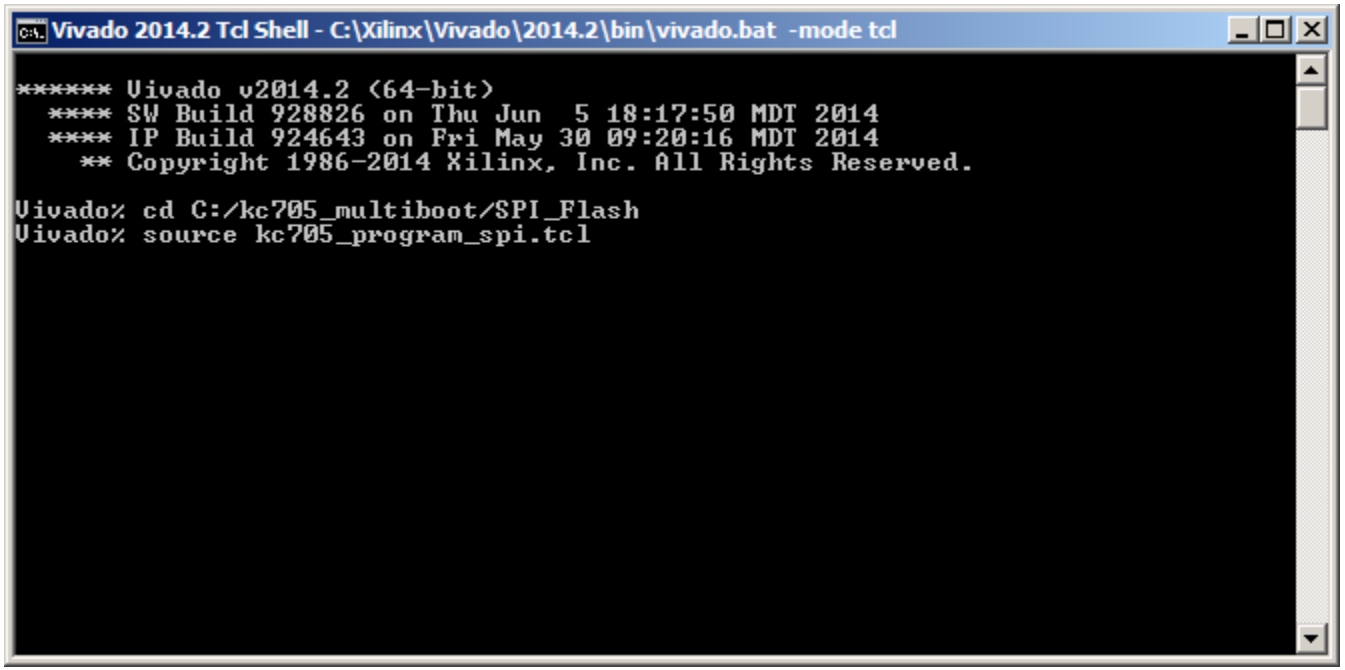
Note: Presentation applies to the KC705

Program SPI MultiBoot Design

- In the Vivado Tcl Shell type:

  cd C:/kc705_multiboot/SPI_Flash

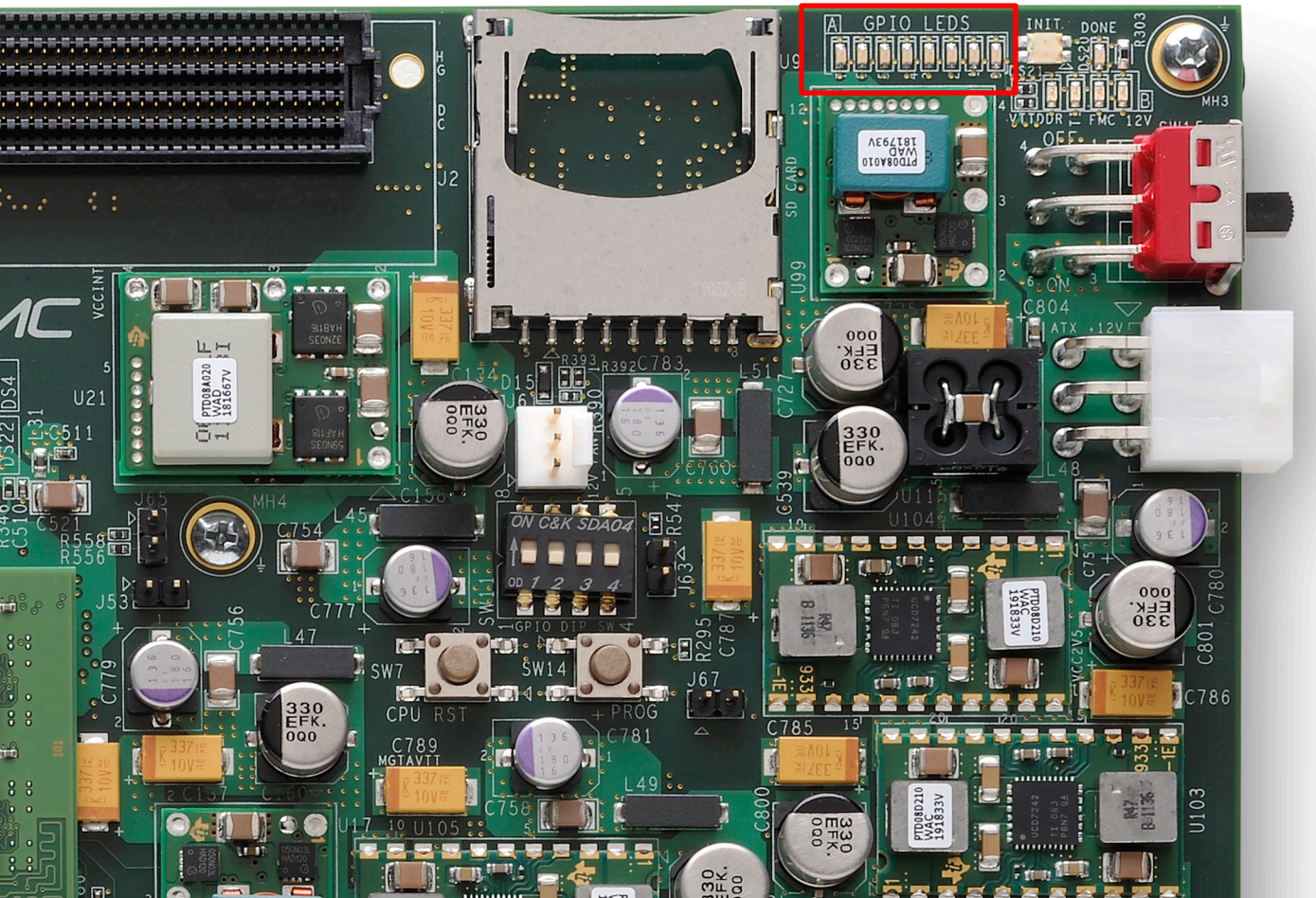
  source kc705_program_spi.tcl



Note: Takes about 10 minutes

Run MultiBoot Design

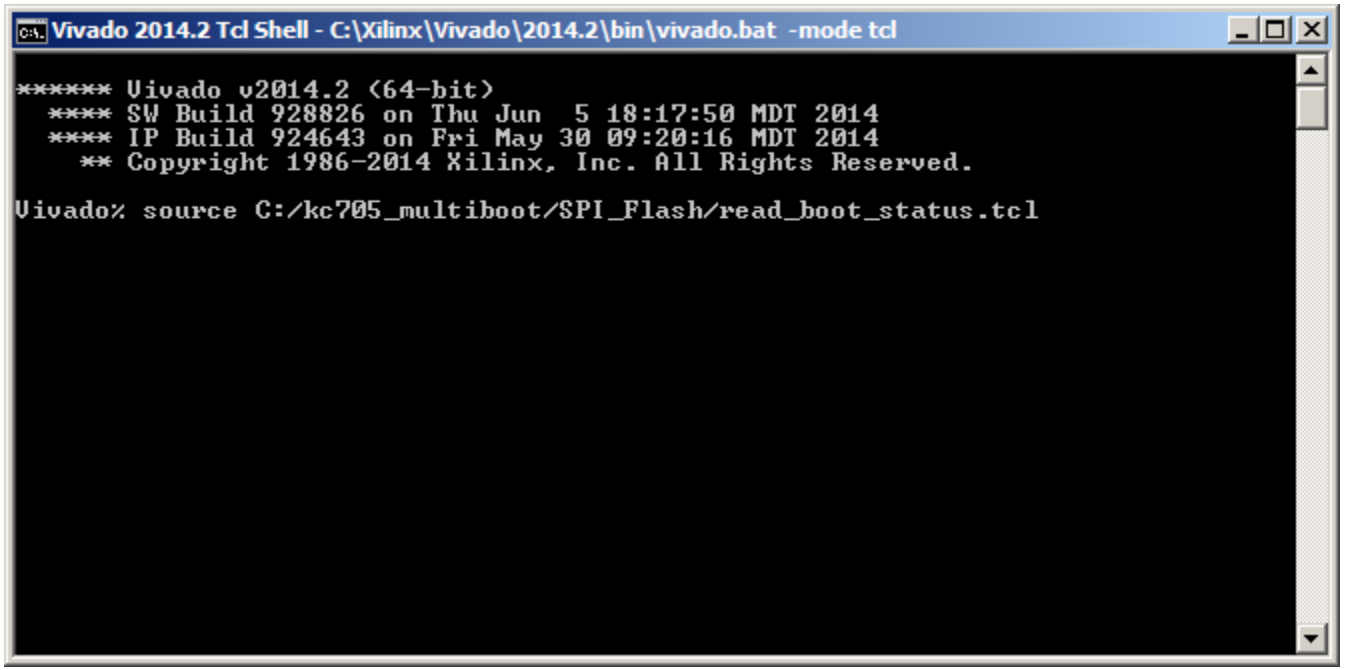
- The initial design, “golden_iprog_spi.bit”, shows a cycling LED pattern on the GPIO LEDs



Run MultiBoot Design

- In a Vivado Tcl Shell type:

  source C:/kc705_multiboot/SPI_Flash/read_boot_status.tcl



Note: Presentation applies to the KC705

Run MultiBoot Design

- View the “REGISTER.BOOT_STATUS.BIT00_0_STATUS_VALID”
- Since this was a regular boot, only “0_STATUS_VALID” is set

Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Logic Analyzer

Hardware Manager - localhost/xilinx_tcf/Digilent/210203337270A

There are no debug cores. Program device Refresh device

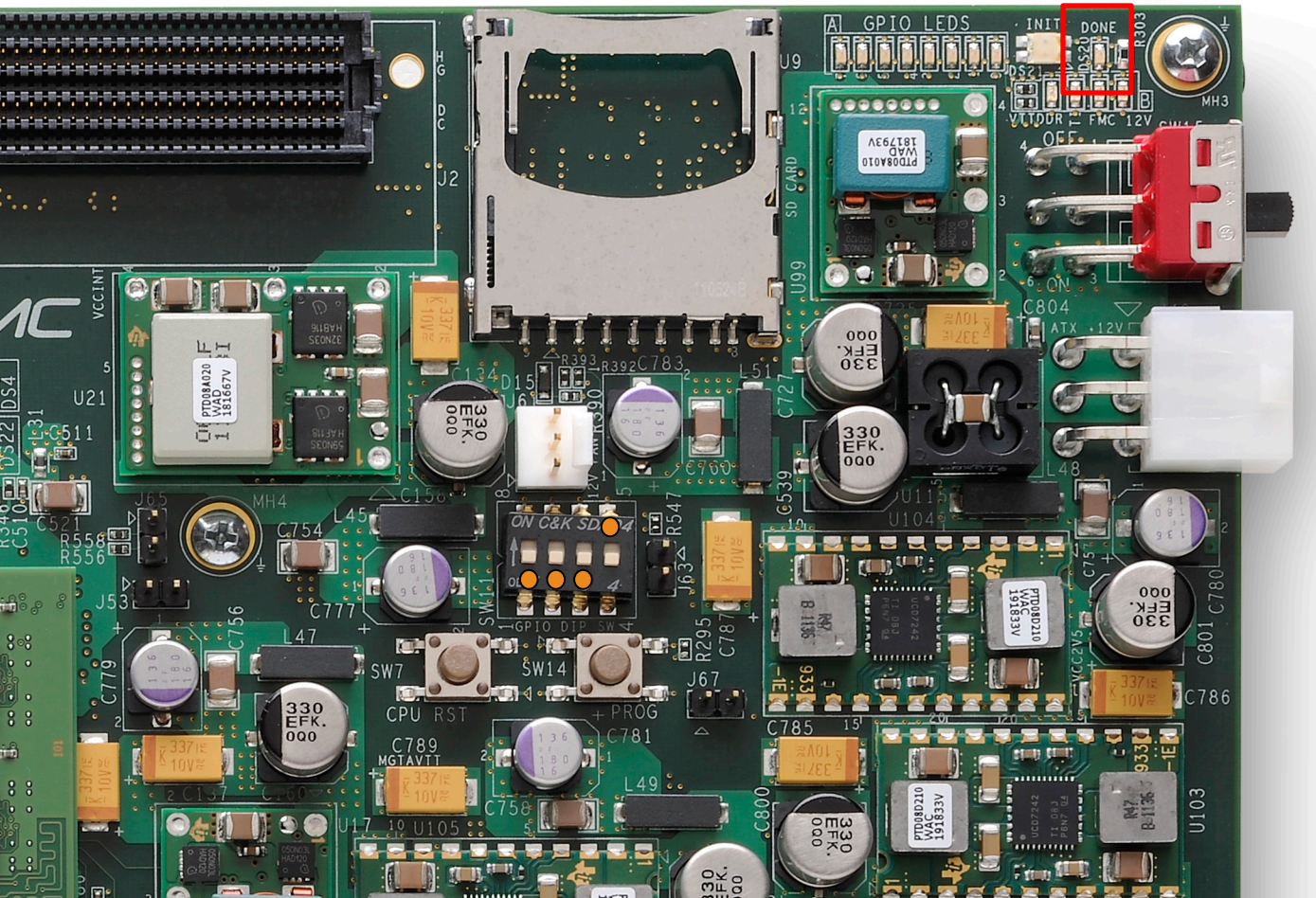
Tcl Console

```
REGISTER.BOOT_STATUS.BIT00_0_STATUS_VALID           string  true    1
REGISTER.BOOT_STATUS.BIT01_0_FALLBACK               string  true    0
REGISTER.BOOT_STATUS.BIT02_0_INTERNAL_PROG          string  true    0
REGISTER.BOOT_STATUS.BIT03_0_WATCHDOG_TIMEOUT_ERROR string  true    0
REGISTER.BOOT_STATUS.BIT04_0_ID_ERROR               string  true    0
REGISTER.BOOT_STATUS.BIT05_0_CRC_ERROR              string  true    0
REGISTER.BOOT_STATUS.BIT06_0_WRAP_ERROR             string  true    0
REGISTER.BOOT_STATUS.BIT07_RESERVED                 string  true    0
REGISTER.BOOT_STATUS.BIT08_1_STATUS_VALID           string  true    0
REGISTER.BOOT_STATUS.BIT09_1_FALLBACK               string  true    0
REGISTER.BOOT_STATUS.BIT10_1_INTERNAL_PROG          string  true    0
REGISTER.BOOT_STATUS.BIT11_1_WATCHDOG_TIMEOUT_ERROR string  true    0
REGISTER.BOOT_STATUS.BIT12_1_ID_ERROR               string  true    0
REGISTER.BOOT_STATUS.BIT13_1_CRC_ERROR              string  true    0
REGISTER.BOOT_STATUS.BIT14_1_WRAP_ERROR             string  true    0
REGISTER.BOOT_STATUS.BIT15_RESERVED                 string  true    0000000000000000
```

Tcl Console Messages

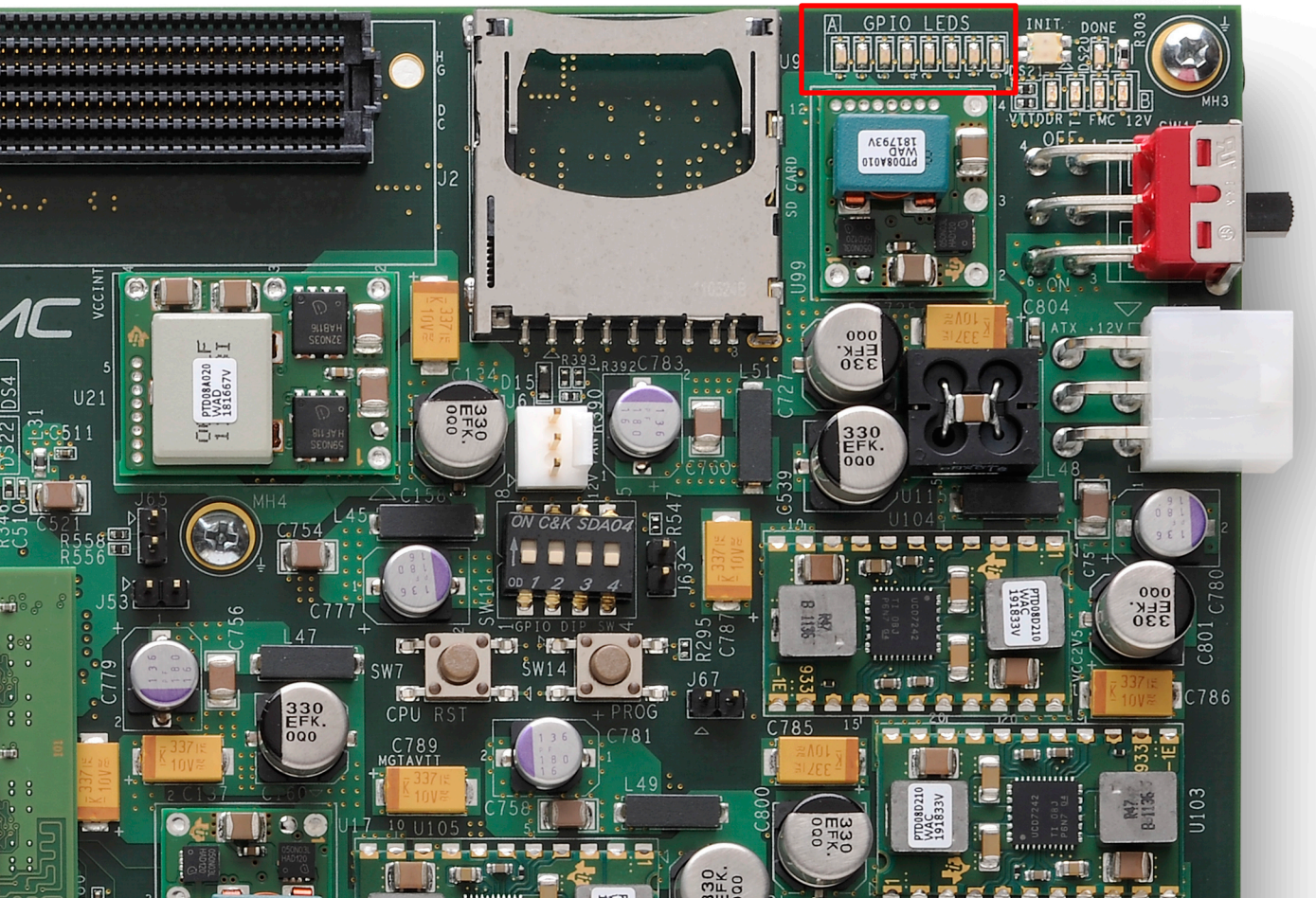
Run MultiBoot Design

- **Set S11 to 0001 (1 = on, Position 1 → Position 4)**
  - Issues an IPROG command to re-configure from a good MultiBoot bitstream
  - Set it back to 0000 when the DONE LED goes out



Run MultiBoot Design

- The MultiBoot design, “multiboot.bit”, shows a rapid blinking LED pattern on the GPIO LEDs



Run MultiBoot Design

- The script adds a procedure “refresh_boot_status”
- Type refresh_boot_status and press Enter

Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Logic Analyzer

Hardware Manager - localhost/xilinx_tcf/Digilent/210203337270A

There are no debug cores. Program device Refresh device

Tcl Console

```
REGISTER.BOOT_STATUS.BIT00_0_STATUS_VALID            string  true    1
REGISTER.BOOT_STATUS.BIT01_0_FALLBACK                string  true    0
REGISTER.BOOT_STATUS.BIT02_0_INTERNAL_PROG           string  true    0
REGISTER.BOOT_STATUS.BIT03_0_WATCHDOG_TIMEOUT_ERROR  string  true    0
REGISTER.BOOT_STATUS.BIT04_0_ID_ERROR                string  true    0
REGISTER.BOOT_STATUS.BIT05_0_CRC_ERROR               string  true    0
REGISTER.BOOT_STATUS.BIT06_0_WRAP_ERROR              string  true    0
REGISTER.BOOT_STATUS.BIT07_RESERVED                  string  true    0
REGISTER.BOOT_STATUS.BIT08_1_STATUS_VALID            string  true    0
REGISTER.BOOT_STATUS.BIT09_1_FALLBACK                string  true    0
REGISTER.BOOT_STATUS.BIT10_1_INTERNAL_PROG           string  true    0
REGISTER.BOOT_STATUS.BIT11_1_WATCHDOG_TIMEOUT_ERROR  string  true    0
REGISTER.BOOT_STATUS.BIT12_1_ID_ERROR                string  true    0
REGISTER.BOOT_STATUS.BIT13_1_CRC_ERROR               string  true    0
REGISTER.BOOT_STATUS.BIT14_1_WRAP_ERROR              string  true    0
REGISTER.BOOT_STATUS.BIT15_RESERVED                  string  true    0000000000000000
```

```
refresh_boot_status
```

Tcl Console | Messages

Run MultiBoot Design

- The following status register messages are now set:
  - INTERNAL_PROG and 1_STATUS_VALID

Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Logic Analyzer

Hardware Manager - localhost/xilinx_tcf/Digilent/210203337270A

There are no debug cores. Program device Refresh device

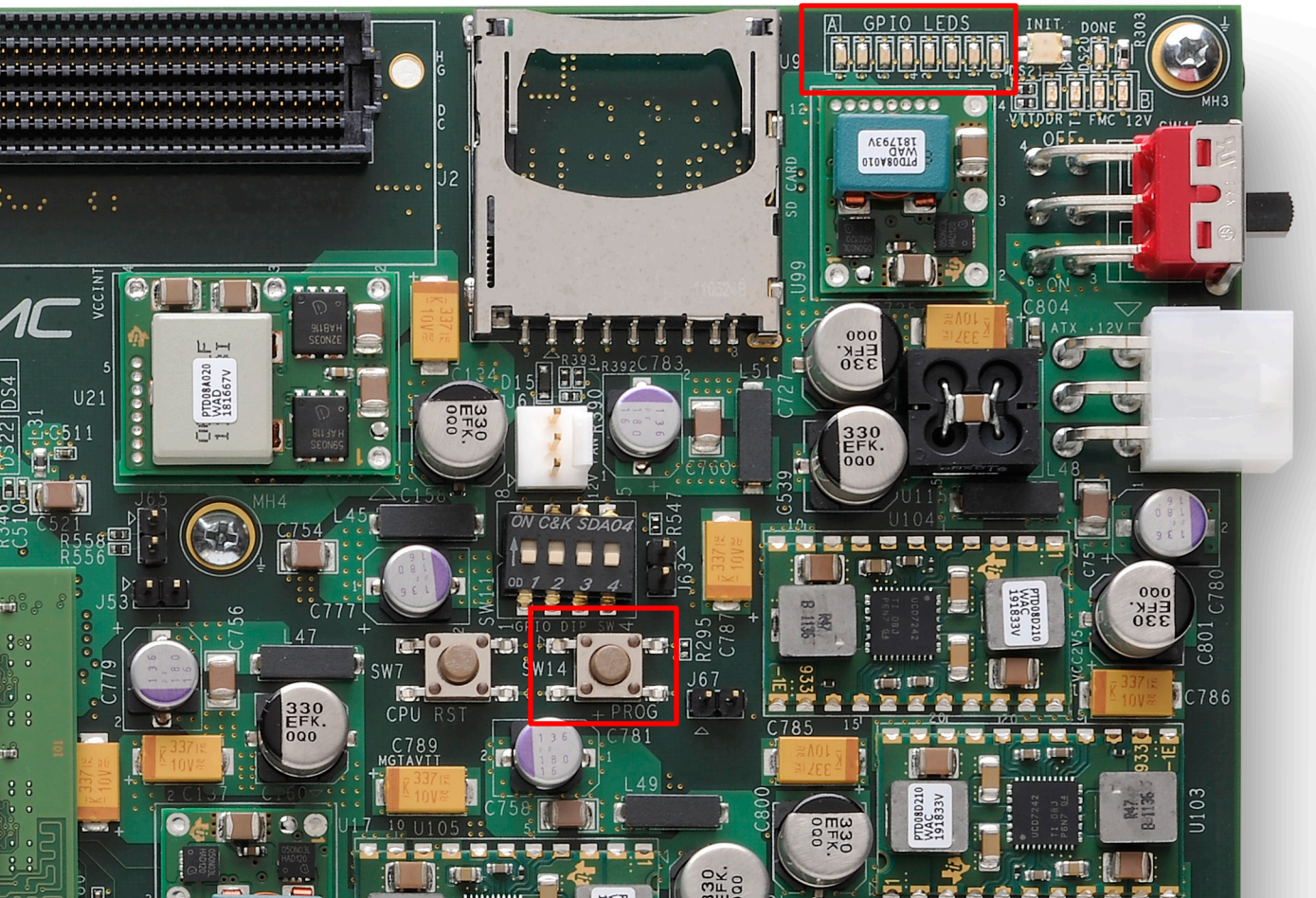
Tcl Console

```
REGISTER.BOOT_STATUS.BIT00_0_STATUS_VALID            string  true    1
REGISTER.BOOT_STATUS.BIT01_0_FALLBACK                string  true    0
REGISTER.BOOT_STATUS.BIT02_0_INTERNAL_PROG           string  true    1
REGISTER.BOOT_STATUS.BIT03_0_WATCHDOG_TIMEOUT_ERROR  string  true    0
REGISTER.BOOT_STATUS.BIT04_0_ID_ERROR                string  true    0
REGISTER.BOOT_STATUS.BIT05_0_CRC_ERROR               string  true    0
REGISTER.BOOT_STATUS.BIT06_0_WRAP_ERROR              string  true    0
REGISTER.BOOT_STATUS.BIT07_RESERVED                  string  true    0
REGISTER.BOOT_STATUS.BIT08_1_STATUS_VALID            string  true    1
REGISTER.BOOT_STATUS.BIT09_1_FALLBACK                string  true    0
REGISTER.BOOT_STATUS.BIT10_1_INTERNAL_PROG           string  true    0
REGISTER.BOOT_STATUS.BIT11_1_WATCHDOG_TIMEOUT_ERROR  string  true    0
REGISTER.BOOT_STATUS.BIT12_1_ID_ERROR                string  true    0
REGISTER.BOOT_STATUS.BIT13_1_CRC_ERROR               string  true    0
REGISTER.BOOT_STATUS.BIT14_1_WRAP_ERROR              string  true    0
REGISTER.BOOT_STATUS.BIT15_RESERVED                  string  true    0000000000000000
```

Tcl Console Messages

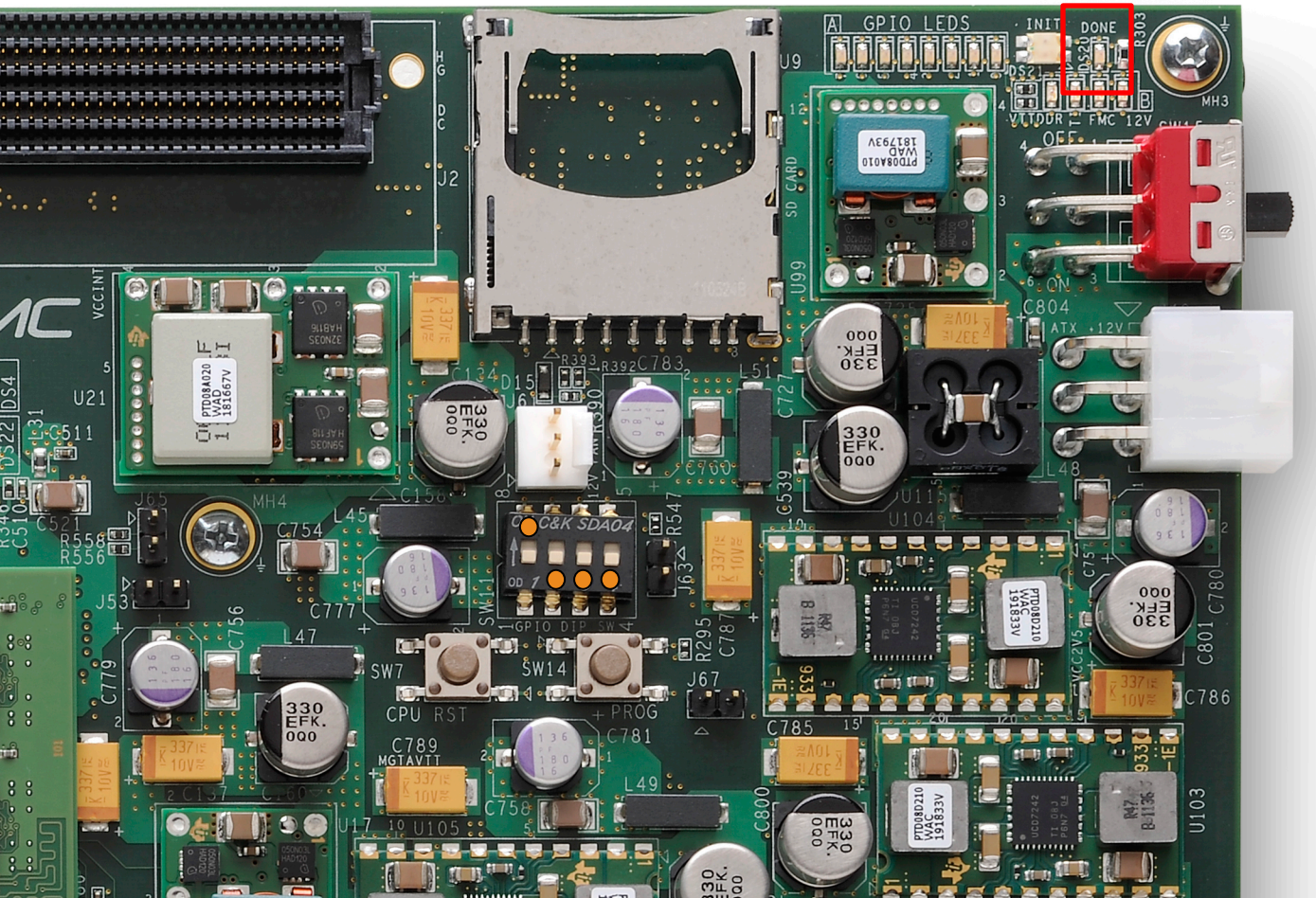
Run MultiBoot Design

- Press PROG to return to the golden bitstream
- Wait until you see the cycling pattern on the LEDs



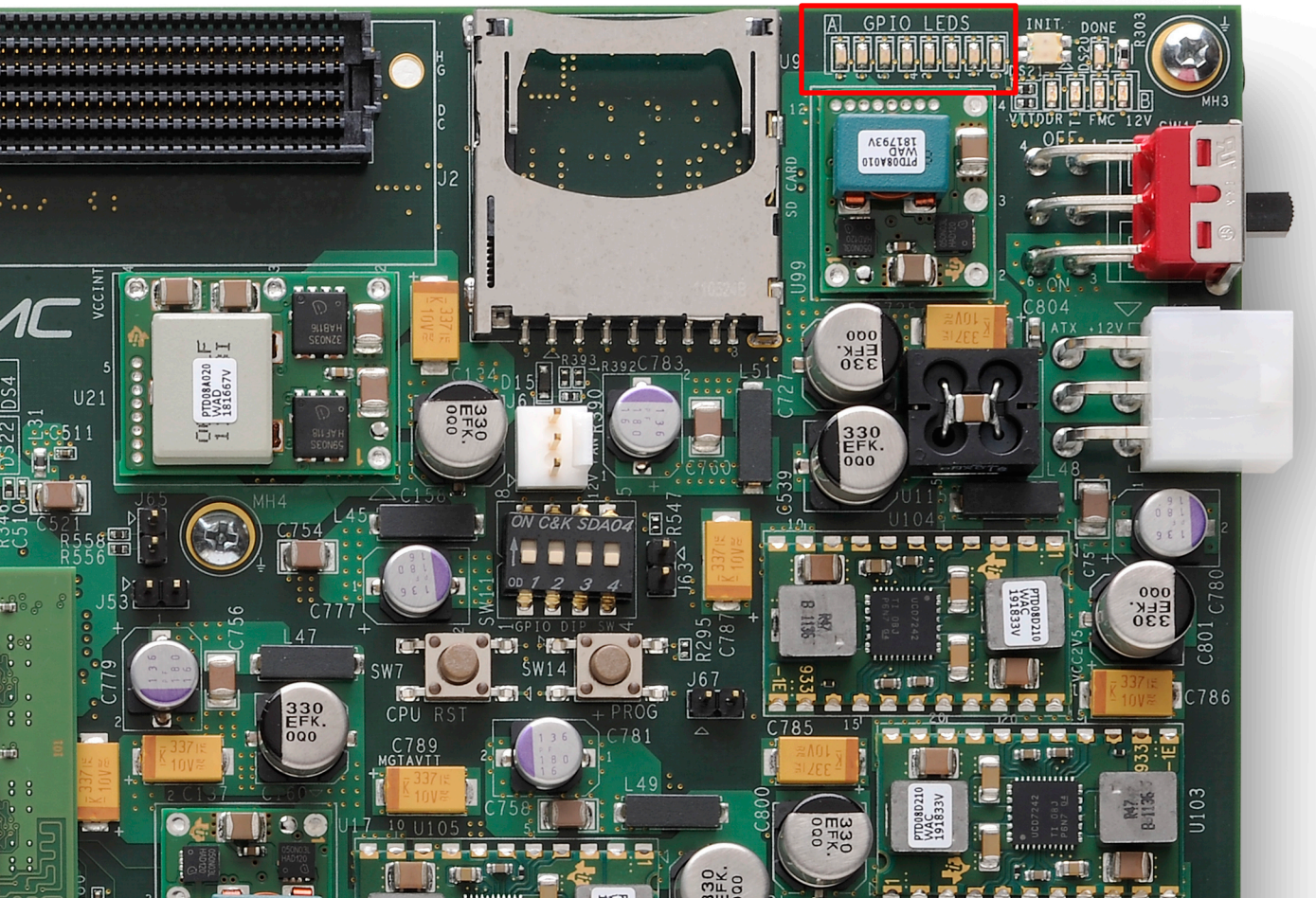
Run MultiBoot Design

- **Set S11 to 1000 (1 = on, Position 1 → Position 4)**
  - Issues an IPROG command to re-configure from a corrupted MultiBoot bitstream
  - Set it back to 0000 when the DONE LED goes out



Run MultiBoot Design

- The corrupted.bit generates a CRC error and cannot load the FPGA
- The FPGA falls back to the golden bitstream with a cycling LED pattern



Run MultiBoot Design

- Type refresh_boot_status and press Enter

Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Logic Analyzer

Hardware Manager - localhost/xilinx_tcf/Digilent/210203337270A

There are no debug cores. Program device Refresh device

Tcl Console

```
REGISTER.BOOT_STATUS.BIT00_0_STATUS_VALID            string  true    1
REGISTER.BOOT_STATUS.BIT01_0_FALLBACK                string  true    0
REGISTER.BOOT_STATUS.BIT02_0_INTERNAL_PROG           string  true    1
REGISTER.BOOT_STATUS.BIT03_0_WATCHDOG_TIMEOUT_ERROR  string  true    0
REGISTER.BOOT_STATUS.BIT04_0_ID_ERROR                string  true    0
REGISTER.BOOT_STATUS.BIT05_0_CRC_ERROR               string  true    0
REGISTER.BOOT_STATUS.BIT06_0_WRAP_ERROR              string  true    0
REGISTER.BOOT_STATUS.BIT07_RESERVED                  string  true    0
REGISTER.BOOT_STATUS.BIT08_1_STATUS_VALID            string  true    1
REGISTER.BOOT_STATUS.BIT09_1_FALLBACK                string  true    0
REGISTER.BOOT_STATUS.BIT10_1_INTERNAL_PROG           string  true    0
REGISTER.BOOT_STATUS.BIT11_1_WATCHDOG_TIMEOUT_ERROR  string  true    0
REGISTER.BOOT_STATUS.BIT12_1_ID_ERROR                string  true    0
REGISTER.BOOT_STATUS.BIT13_1_CRC_ERROR               string  true    0
REGISTER.BOOT_STATUS.BIT14_1_WRAP_ERROR              string  true    0
REGISTER.BOOT_STATUS.BIT15_RESERVED                  string  true    0000000000000000
```

```
refresh_boot_status
```

Tcl Console | Messages

Run MultiBoot Design

- The following status register messages are now seen:
  - IPROG_0 is no longer active
  - 0_FALLBACK, 1_INTERNAL_IPROG, and 1_CRC_ERROR are now active

Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Logic Analyzer

Hardware Manager - localhost/xilinx_tcf/Digilent/210203337270A

There are no debug cores. Program device Refresh device

Tcl Console

```
REGISTER.BOOT_STATUS.BIT00_0_STATUS_VALID            string  true    1
REGISTER.BOOT_STATUS.BIT01_0_FALLBACK                string  true    1
REGISTER.BOOT_STATUS.BIT02_0_INTERNAL_PROG           string  true    0
REGISTER.BOOT_STATUS.BIT03_0_WATCHDOG_TIMEOUT_ERROR  string  true    0
REGISTER.BOOT_STATUS.BIT04_0_ID_ERROR                string  true    0
REGISTER.BOOT_STATUS.BIT05_0_CRC_ERROR               string  true    0
REGISTER.BOOT_STATUS.BIT06_0_WRAP_ERROR              string  true    0
REGISTER.BOOT_STATUS.BIT07_RESERVED                  string  true    0
REGISTER.BOOT_STATUS.BIT08_1_STATUS_VALID            string  true    1
REGISTER.BOOT_STATUS.BIT09_1_FALLBACK                string  true    0
REGISTER.BOOT_STATUS.BIT10_1_INTERNAL_PROG           string  true    1
REGISTER.BOOT_STATUS.BIT11_1_WATCHDOG_TIMEOUT_ERROR  string  true    0
REGISTER.BOOT_STATUS.BIT12_1_ID_ERROR                string  true    0
REGISTER.BOOT_STATUS.BIT13_1_CRC_ERROR               string  true    1
REGISTER.BOOT_STATUS.BIT14_1_WRAP_ERROR              string  true    0
REGISTER.BOOT_STATUS.BIT15_RESERVED                  string  true    0000000000000000
```

Tcl Console Messages

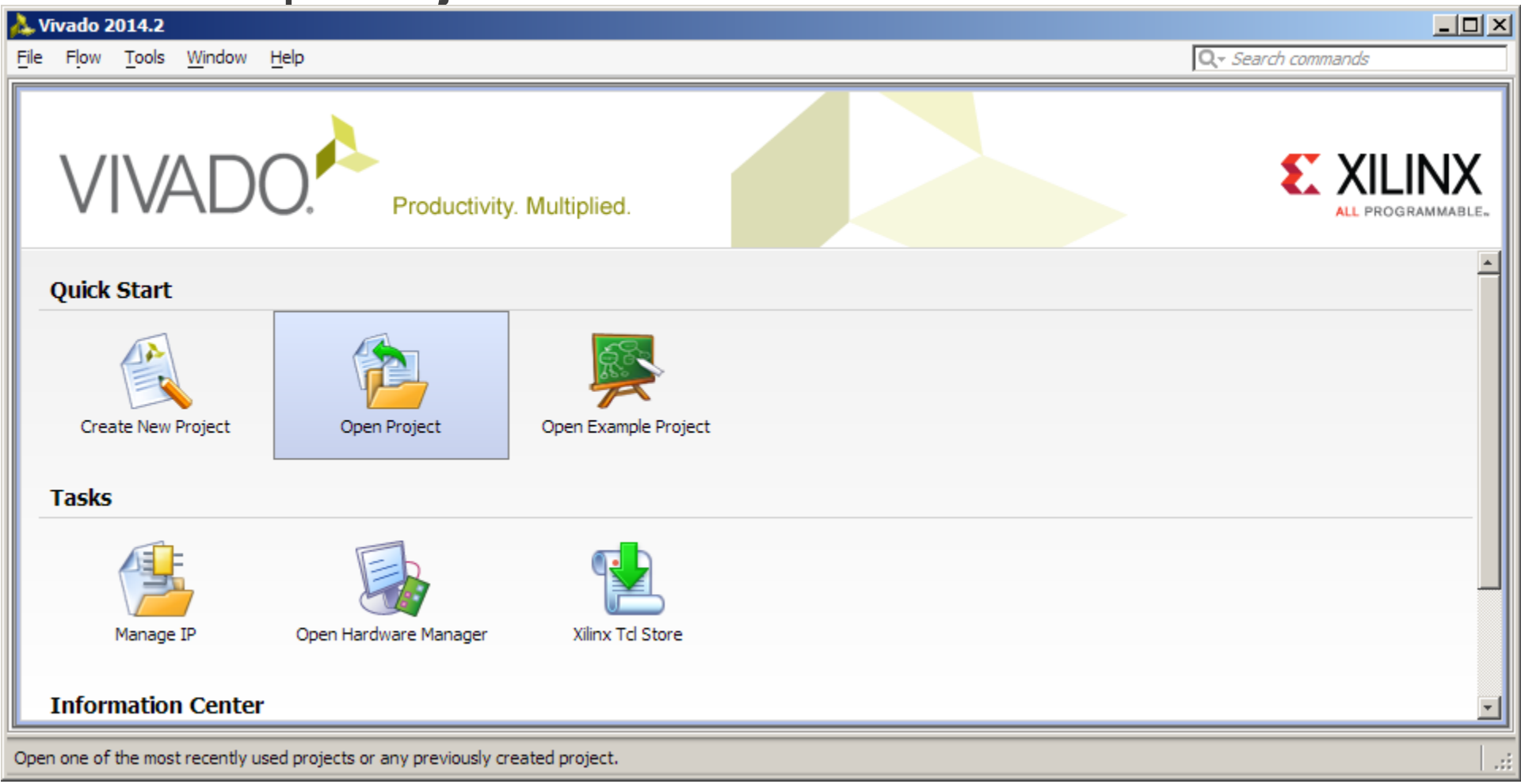
Compile KC705 MultiBoot Design

Compile KC705 MultiBoot Design

- Open Vivado

  Start → All Programs → Xilinx Design Tools → Vivado 2014.2 → Vivado

- Select Open Project



Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- Open the KC705 Design:
  - <Design Name>\kc705_multiboot.xpr

kc705_multiboot - [C:/kc705_multiboot/kc705_multiboot.xpr] - Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Default Layout

write_bitstream Complete

Flow Navigator

Project Manager
- Project Settings
- Add Sources
- IP Catalog

IP Integrator
- Create Block Design
- Open Block Design
- Generate Block Design

Simulation
- Simulation Settings
- Run Simulation

RTL Analysis
- Open Elaborated Design

Synthesis
- Synthesis Settings

Project Manager - kc705_multiboot

Sources

Design Sources (1)
- system_wrapper (system_wrapper.v) (1)

Constraints (1)

Simulation Sources (1)

Hierarchy | IP Sources | Libraries | Compile Order

Sources | Templates

Properties

Project Summary

Project Settings

Project name:	kc705_multiboot
Product family:	Kintex-7
Project part:	Kintex-7 KC705 Evaluation Platform (x
Top module name:	system_wrapper

Board Part

Display name:	Kintex-7 KC705 Evaluation Platform
Board part name:	xilinx.com:kc705:part0:1.0

Design Runs

Name	Part	Constraints	Strategy
synth_1	xc7k325tffg900-2	constrs_1	Vivado Synthesis Defaults (Vivado Synthesis 2014)
impl_1	xc7k325tffg900-2	constrs_1	Vivado Implementation Defaults (Vivado Implementation 2

Tcl Console | Messages | Log | Reports | Design Runs

Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- **The design is fully implemented; you can recompile, or export to SDK**
  - To recompile, right-click **synth_1**, select **Reset Runs** then **Generate Bitstream**

kc705_multiboot - [C:/kc705_multiboot/kc705_multiboot.xpr] - Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Default Layout

write_bitstream Complete

Flow Navigator

Run Simulation

RTL Analysis

Open Elaborated Design

Synthesis

Synthesis Settings

Run Synthesis

Open Synthesized Desig

Implementation

Implementation Settings

Run Implementation

Open Implemented Desig

Program and Debug

Bitstream Settings

Generate Bitstream

Open Hardware Manage

Project Manager - kc705_multiboot

Sources

Design Sources (1)

system_wrapper (system_wrapper.v) (1)

Constraints (1)

Simulation Sources (1)

Hierarchy IP Sources Libraries Compile Order

Sources Templates

Synthesis Run Properties

synth_1

Design Runs

Name

synth_1

impl_1

Tcl Console Messages Log

Project Summary

Project Settings

Project name: kc705_multiboot

Product family: Kintex-7

Project part: Kintex-7 KC705 Evaluation Platform (x

Top module name: system_wrapper

Board Part

Kintex-7 KC705 Evaluation Platform

xilinx.com:kc705:part0:1.0

Strategy

esis Defaults (Vivado Synthesis 2014)

mentation Defaults (Vivado Implementation 2

Synthesis Run Properties... Ctrl+E

Delete Delete

Make Active

Change Run Settings...

Save As Strategy...

Open Run

Launch Runs...

Reset Runs

Launch Next Step

Reset to Previous Step: synth_design

Generate Bitstream

Generate a programming file after implementation

Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- Once done, both the Synthesis and Implementation will have green check marks

kc705_multiboot - [C:/kc705_multiboot/kc705_multiboot.xpr] - Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Default Layout

write_bitstream Complete

Flow Navigator

Project Manager
- Project Settings
- Add Sources
- IP Catalog

IP Integrator
- Create Block Design
- Open Block Design
- Generate Block Design

Simulation
- Simulation Settings
- Run Simulation

RTL Analysis
- Open Elaborated Design

Synthesis
- Synthesis Settings

Project Manager - kc705_multiboot

Sources

Design Sources (1)
- system_wrapper (system_wrapper.v) (1)

Constraints (1)

Simulation Sources (1)

Hierarchy | IP Sources | Libraries | Compile Order

Sources | Templates

Properties

Project Summary

Project Settings

Project name:	kc705_multiboot
Product family:	Kintex-7
Project part:	Kintex-7 KC705 Evaluation Platform (x
Top module name:	system_wrapper

Board Part

Display name:	Kintex-7 KC705 Evaluation Platform
Board part name:	xilinx.com:kc705:part0:1.0

Design Runs

Name	Part	Constraints	Strategy
synth_1	xc7k325tffg900-2	constrs_1	Vivado Synthesis Defaults (Vivado Synthesis 2014)
impl_1	xc7k325tffg900-2	constrs_1	Vivado Implementation Defaults (Vivado Implementation 2

Tcl Console | Messages | Log | Reports | Design Runs

Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- The MultiBoot Design has been implemented with IP Integrator (IPI)
- Click Open Block Design

kc705_multiboot - [C:/kc705_multiboot/kc705_multiboot.xpr] - Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Default Layout

write_bitstream Complete

Flow Navigator

- Project Manager
  - Project Settings
  - Add Sources
  - IP Catalog
- IP Integrator
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- Simulation
  - Simulation Settings
  - Run Simulation
- RTL Analysis
  - Open Elaborated Design
- Synthesis
  - Synthesis Settings

Project Manager - kc705_multiboot

Sources

- Design Sources (1)
  - system_wrapper (system_wrapper.v) (1)
- Constraints (1)
- Simulation Sources (1)

Hierarchy | IP Sources | Libraries | Compile Order

Sources | Templates

Properties

Project Summary

Project Settings

Project name:	kc705_multiboot
Product family:	Kintex-7
Project part:	Kintex-7 KC705 Evaluation Platform (x
Top module name:	system_wrapper

Board Part

Display name:	Kintex-7 KC705 Evaluation Platform
Board part name:	xilinx.com:kc705:part0:1.0

Design Runs

Name	Part	Constraints	Strategy
synth_1	xc7k325tffg900-2	constrs_1	Vivado Synthesis Defaults (Vivado Synthesis 2014)
impl_1	xc7k325tffg900-2	constrs_1	Vivado Implementation Defaults (Vivado Implementation 2

Tcl Console | Messages | Log | Reports | Design Runs

Open an IP subsystem from the current project

Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- All the IP Blocks used in the design can be seen in this view

kc705_multiboot - [C:/kc705_multiboot/kc705_multiboot.xpr] - Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Default Layout

write_bitstream Complete

Flow Navigator

Project Manager
- Project Settings
- Add Sources
- IP Catalog

IP Integrator
- Create Block Design
- Open Block Design
- Generate Block Design

Simulation
- Simulation Settings
- Run Simulation

RTL Analysis
- Open Elaborated Design

Synthesis
- Synthesis Settings

Block Design - system

Diagram | Address Editor

system

MicroBlaze

Design Hierarchy

Properties

Tcl Console

Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- To export to SDK, the Block and Implemented designs must be open
- Click Open Implemented Design

kc705_multiboot - [C:/kc705_multiboot/kc705_multiboot.xpr] - Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Default Layout

write_bitstream Complete

Flow Navigator

Run Simulation

RTL Analysis

Open Elaborated Design

Synthesis

Synthesis Settings

Run Synthesis

Open Synthesized Desig

Implementation

Implementation Settings

Run Implementation

Open Implemented Desig

Program and Debug

Bitstream Settings

Generate Bitstream

Open Hardware Manage

Block Design - system

Diagram

Address Editor

system

MicroBlaze

Design Hierarchy

Properties

Tcl Console

Analyze and constrain an Implemented Design

Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- View Implemented Design

kc705_multiboot - [C:/kc705_multiboot/kc705_multiboot.xpr] - Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Default Layout

write_bitstream Complete

Flow Navigator

Run Simulation

RTL Analysis

Open Elaborated Design

Synthesis

Synthesis Settings

Run Synthesis

Open Synthesized Desig

Implementation

Implementation Settings

Run Implementation

Implemented Design

Constraints Wizard

Edit Timing Constrair

Report Timing Summ

Report Clock Networ

Implemented Design - xc7k325tffg900-2 (active)

Properties

Netlist

Project Summary

Device

X0Y6 X1Y6

X0Y5 X1Y5

X0Y4 X1Y4

X0Y3 X1Y3

X1Y2

X0Y1 X1Y1

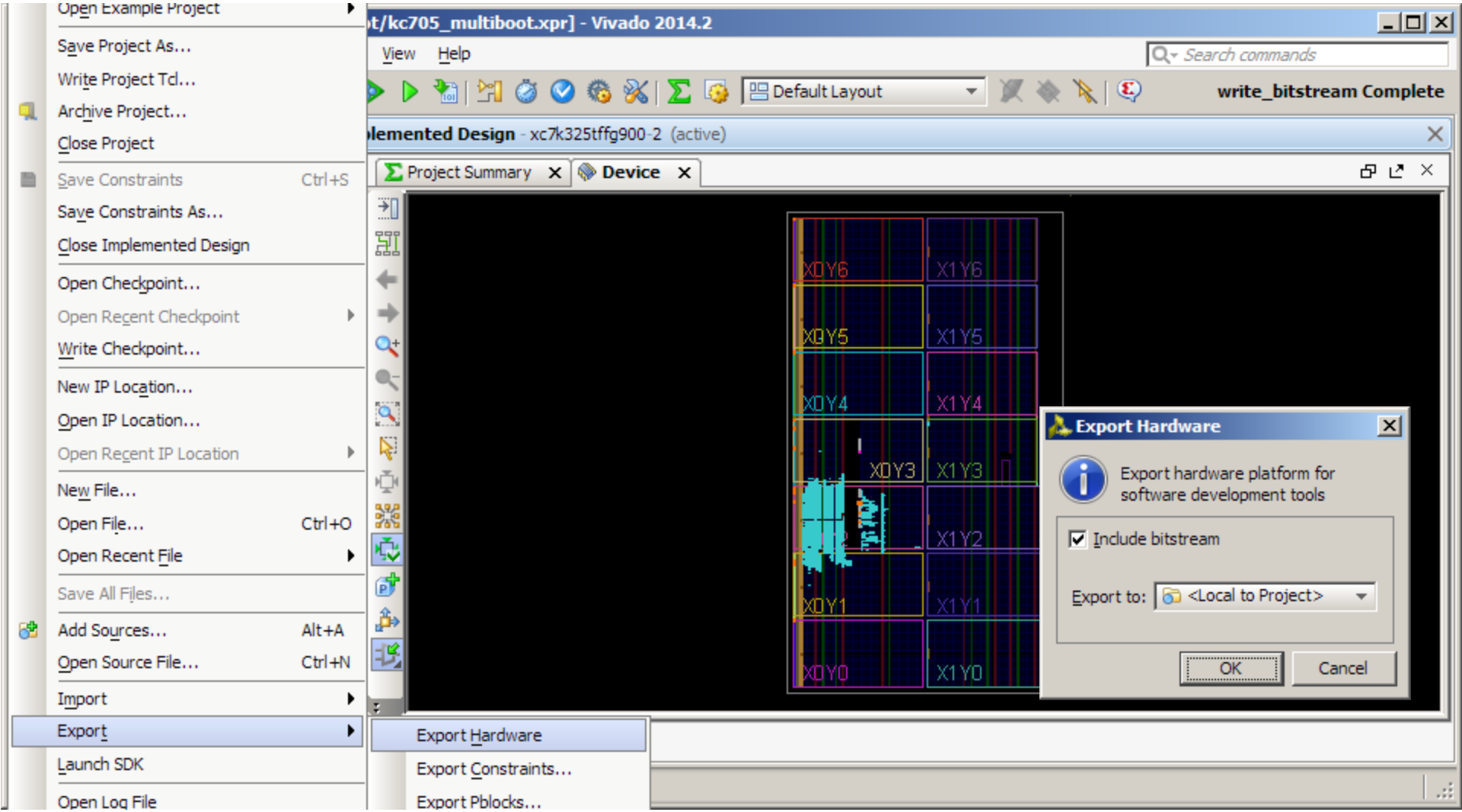
X0Y0 X1Y0

Design Runs

Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

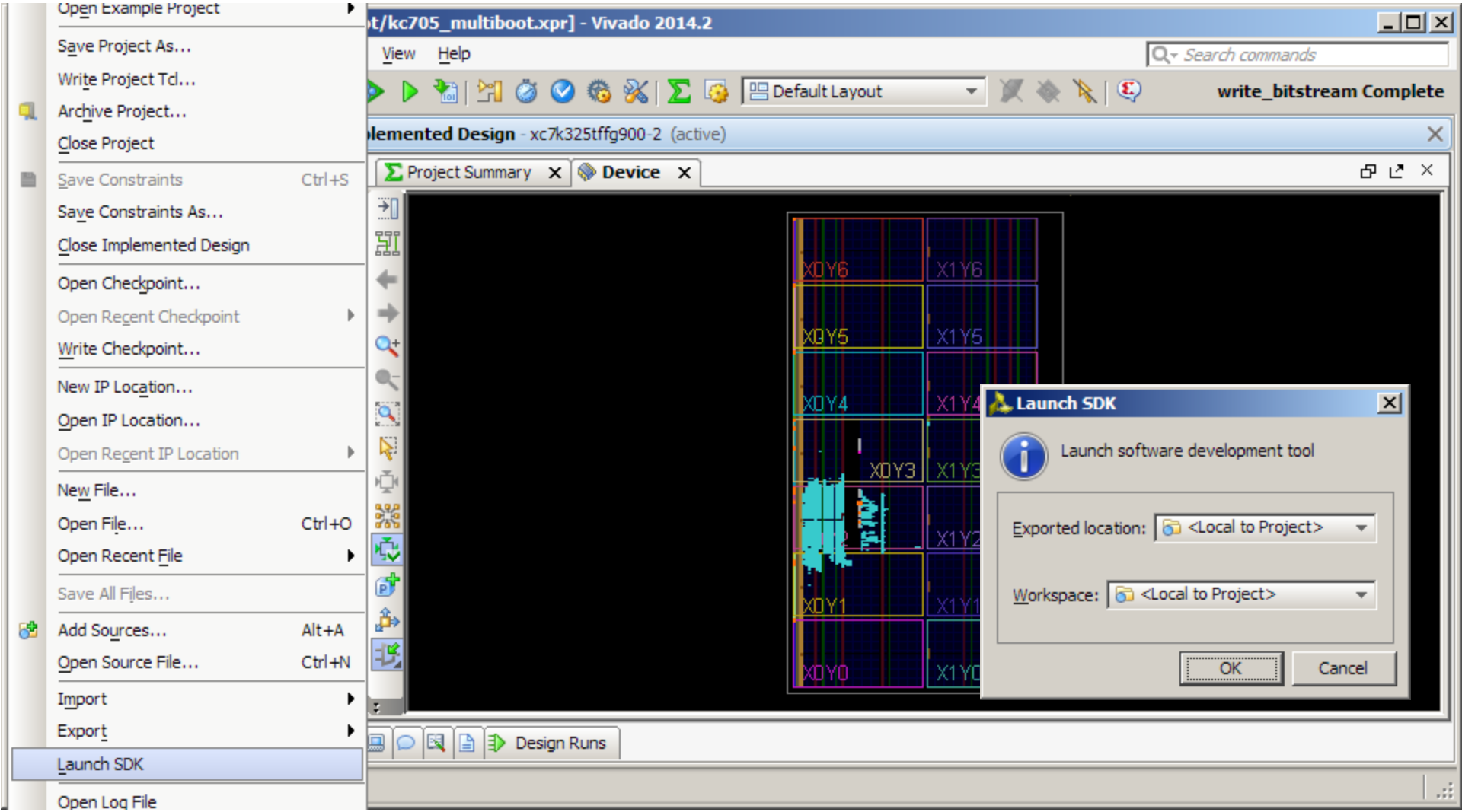
- Select File → Export → Export Hardware
- Click OK



Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- Select File → Launch SDK
- Click OK



Note: Presentation applies to the KC705

Compile KC705 Software in SDK

- **SDK Software Compile - Build ELF files in SDK**
  - Project builds automatically
  - When done, close SDK and return to Vivado

C/C++ - Xilinx SDK

File Edit Source Refactor Navigate Search Run Project Xilinx Tools Window Help

Project Explorer

- golden_iprog_spi
- multiboot
- standalone_bsp_0
- system_wrapper_hw_platform_0

Problems | Tasks | Console | Properties | Terminal

CDT Build Console [golden_iprog_spi]

```
mb-gcc -Wl,-T -Wl,../src/lscript.ld -L../../standalone_bsp_0/microblaze_0/lib -mlittle-endian
-mxl-barrel-shift -mcpu=v9.3 -mxl-soft-mul -Wl,--no-relax -Wl,--gc-sections -o
"golden_iprog_spi.elf"  ./src/golden.o ./src/xgpio_tapp_example.o
./src/xhwicap_low_level_example.o   -Wl,--start-group,-lxil,-lgcc,-lc,--end-group
'Finished building target: golden_iprog_spi.elf'
' '
'Invoking: MicroBlaze Print Size'
mb-size golden_iprog_spi.elf  |tee "golden_iprog_spi.elf.size"
   text    data     bss     dec     hex filename
   8209     428    2131   10768    2a10 golden_iprog_spi.elf
'Finished building: golden_iprog_spi.elf.size'
' '

02:01:43 Build Finished (took 2s.61ms)
```

Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- **With Vivado, a special flow is used for compressed embedded designs**
  - SDK can only program an ELF file into an uncompressed bitstream
  - Compression is used here to fit the three MultiBoot bitstreams into a smaller area for programming the SPI flash
- **After SDK has compiled the ELF files, they must be associated with the design**
  - To do this, we will use the **Add Sources** command, followed by the **Associate ELF** command

Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- Select Add Sources

kc705_multiboot - [C:/kc705_multiboot/kc705_multiboot.xpr] - Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Default Layout

write_bitstream Complete

Flow Navigator

Project Manager
- Project Settings
- Add Sources
- IP Catalog

IP Integrator
- Create Block Design
- Open Block Design
- Generate Block Design

Simulation
- Simulation Settings
- Run Simulation

RTL Analysis
- Open Elaborated Design

Synthesis
- Synthesis Settings

Implemented Design - xc7k325tffg900-2 (active)

Sources

- Design Sources (1)
  - system_wrapper (system_wrapper.v) (1)
- Constraints (1)
- Simulation Sources (1)

Hierarchy | IP Sources | Libraries | Compile Order

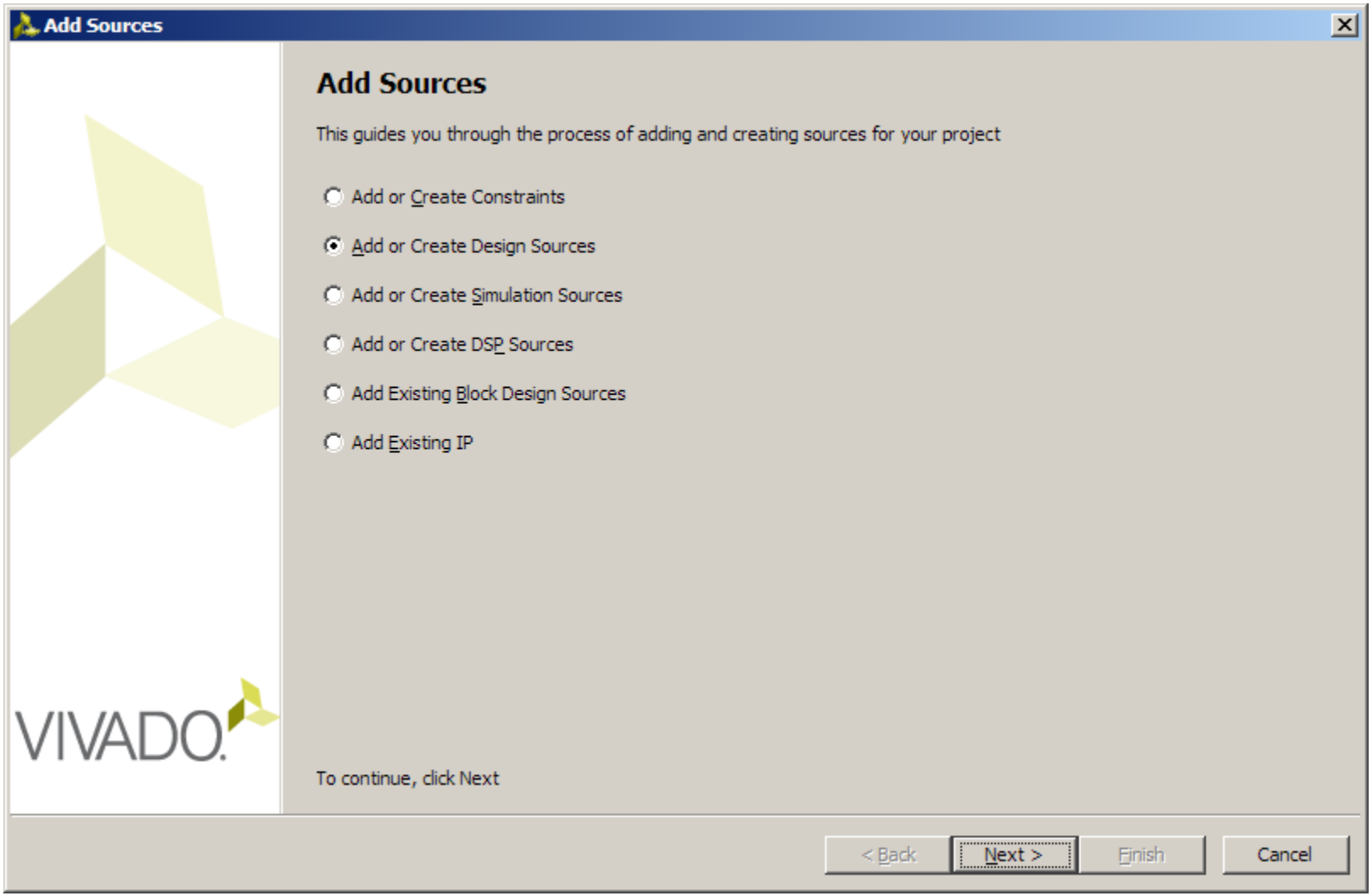
Sources | Netlist

Specify and/or create source files to add to the project

Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

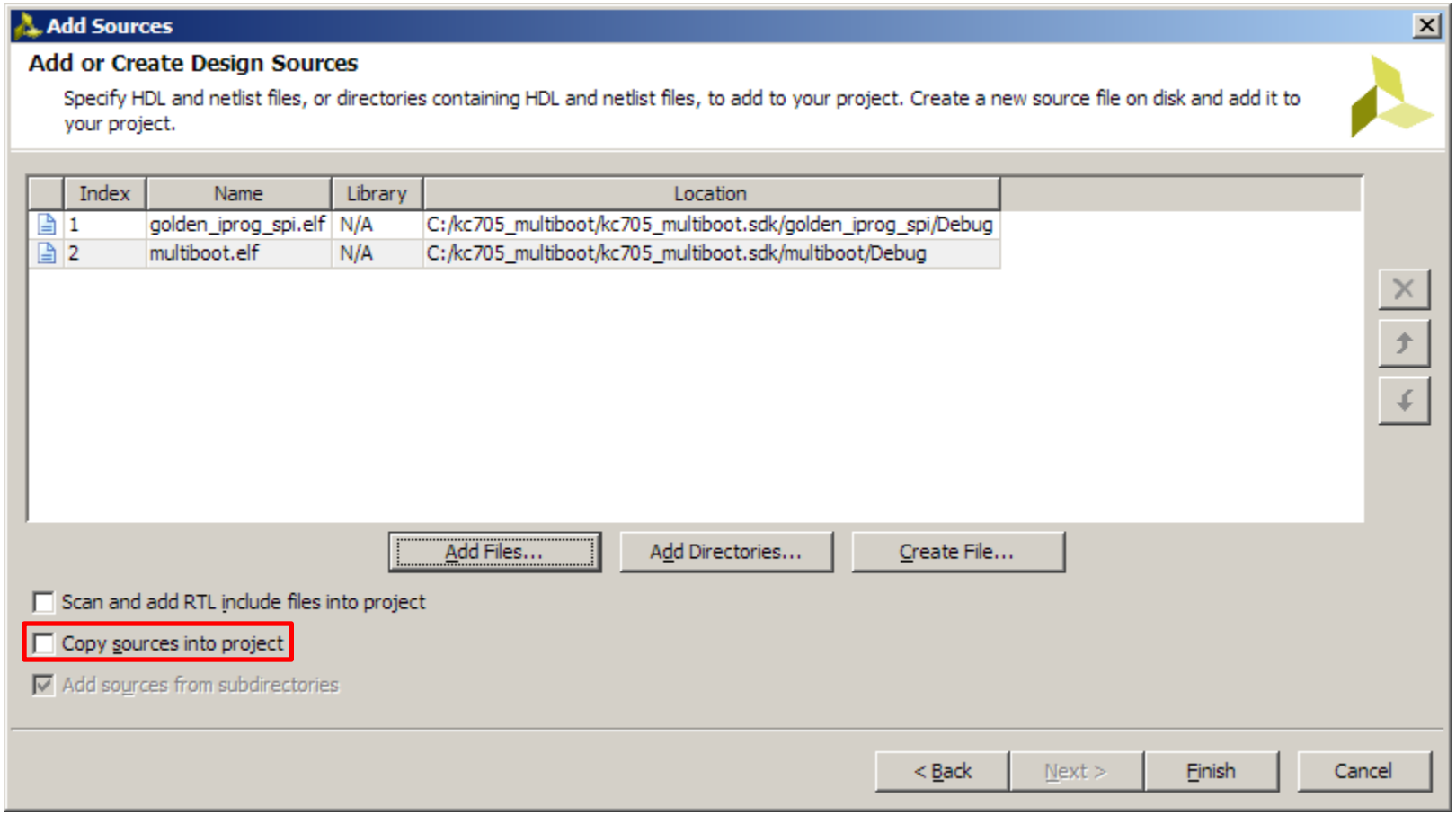
- Select Add or Create Design Sources



Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- Add golden_iprog_spi.elf and multiboot.elf from the SDK tree
- Make sure Copy sources into project is deselected
  - This eliminates the need to re-Associate the ELF each time it is recompiled
- Click Finish



Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- Right-click on one of the ELF files and select Associate ELF files

kc705_multiboot - [C:/kc705_multiboot/kc705_multiboot.xpr] - Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Default Layout

write_bitstream Complete

Flow Navigator

Project Manager
- Project Settings
- Add Sources
- IP Catalog

IP Integrator
- Create Block Design
- Open Block Design
- Generate Block Design

Simulation
- Simulation Settings
- Run Simulation

RTL Analysis
- Open Elaborated Design

Synthesis
- Synthesis Settings

Implemented Design - xc7k325tffg900-2 (active)

Sources

Design Sources (3)
- system_wrapper
- ELF (2)
  - golden_iprog_spi.elf
  - multiboot.elf

Constraints (1)

Simulation Sources (3)
- sim_1 (3)
  - system_wrappe
  - ELF (2)
    - golden_iprog_sp
    - multiboot.elf

Hierarchy | IP Sources | Libraries

Sources | Netlist

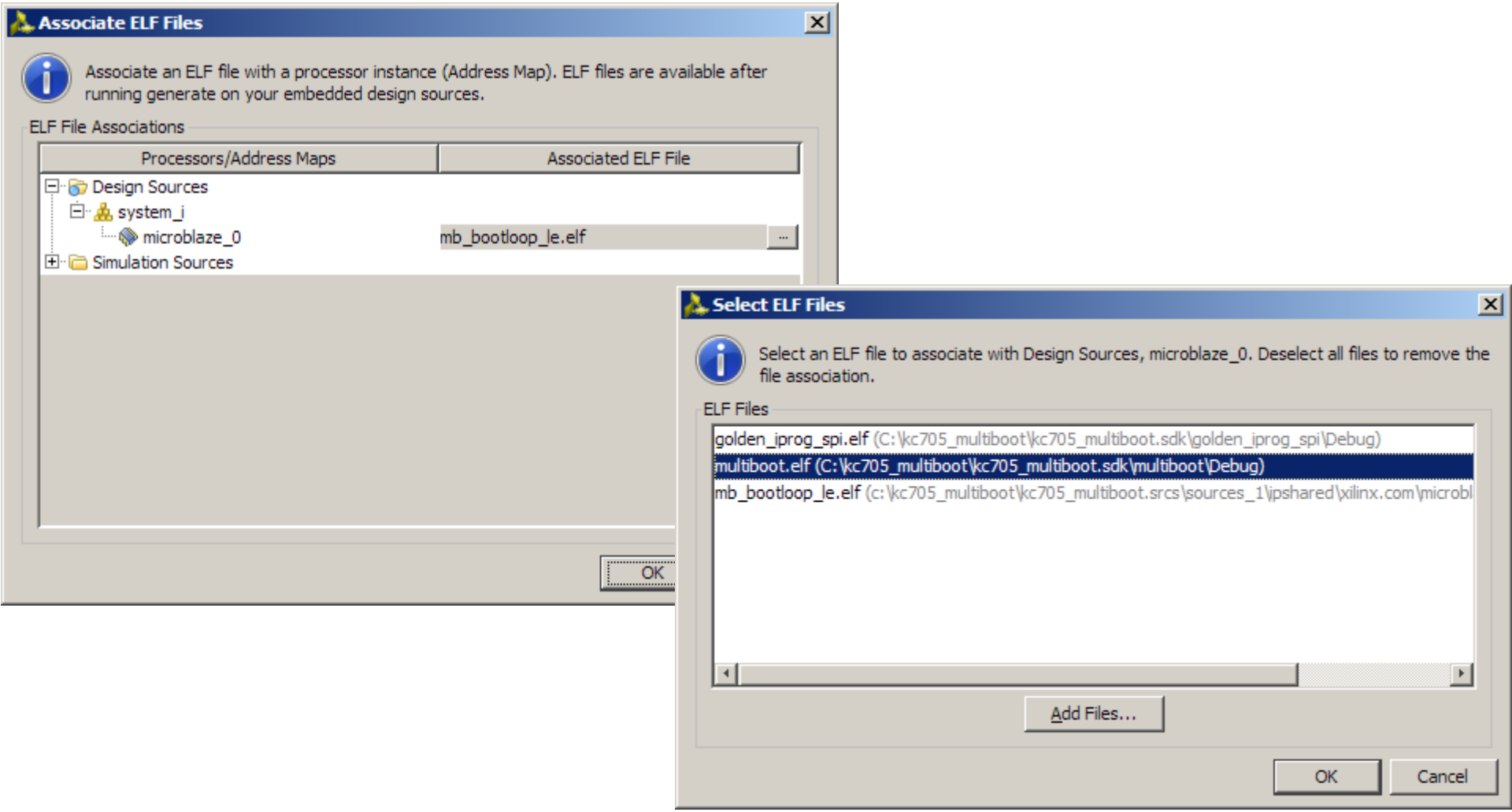
Source File Properties...	Ctrl+E
Open File	Alt+O
Replace File...	
Copy File Into Project	
Copy All Files Into Project	Alt+I
Remove File from Project...	Delete
Enable File	Alt+Equals
Disable File	Alt+Minus
Hierarchy Update	▸
Refresh Hierarchy	
IP Hierarchy	▸
Set as Top	
Set File Type...	
Set Used In...	
Edit Constraints Sets...	
Edit Simulation Sets...	
Associate ELF Files...	

ELF File Association

Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- Click the button to the right; select the multiboot.elf then click OK twice



Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- Right-click on impl_1 and select Force Up-to-Date

kc705_multiboot - [C:/kc705_multiboot/kc705_multiboot.xpr] - Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Default Layout

Implementation Out-of-date more info

Flow Navigator

Project Manager
- Project Settings
- Add Sources
- IP Catalog

IP Integrator
- Create Block Design
- Open Block Design
- Generate Block Design

Simulation
- Simulation Settings
- Run Simulation

RTL Analysis
- Open Elaborated Design

Synthesis
- Synthesis Settings

Implemented Design - xc7k325tffg900-2 (active)

Sources

Design Sources (3)
- system_wrapper (system_wrapper.v) (1)
- ELF (2)
  - golden_iprog_spi.elf
  - multiboot.elf

Hierarchy | IP Sources | Libraries | Compile

Sources | Netlist

Implementation Run Properties

impl_1

Design Runs

Name	Strategy
synth_1	is Defaults (Vivado Synthesis 2014)
impl_1	ntation Defaults (Vivado Implementation 2

Tcl Console | Messages | Log

Project Summary | Device

Project Settings

Project name: kc705_multiboot

Product family: Kintex-7

Kintex-7 KC705 Evaluation Platform

e: system_wrapper

Kintex-7 KC705 Evaluation Platform

e: xilinx.com:kc705:part0:1.0

Implementation Run Properties... Ctrl+E

Delete Delete

Make Active

Change Run Settings...

Set Incremental Compile...

Save As Strategy...

Open Run

Launch Runs...

Reset Runs

Launch Next Step

Reset to Previous Step: write_bitstream

Force Up-to-Date

Generate Bitstream

Export Bitstream File...

Display Run Log

Force the selected run up-to-date

Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- Select Generate Bitstream

kc705_multiboot - [C:/kc705_multiboot/kc705_multiboot.xpr] - Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Default Layout

write_bitstream Complete

Flow Navigator

Implementation
- Implementation Settings
- Run Implementation
- Implemented Design
  - Constraints Wizard
  - Edit Timing Constrair
  - Report Timing Summ
  - Report Clock Networ
  - Report Clock Interac
  - Report DRC
  - Report Noise
  - Report Utilization
  - Report Power

Program and Debug
- Bitstream Settings
- Generate Bitstream
- Open Hardware Manage

Implemented Design - xc7k325tffg900-2 (active)

Sources

Design Sources (3)
- system_wrapper (system_wrapper.v) (1)
- ELF (2)
  - golden_iprog_spi.elf
  - multiboot.elf

Hierarchy | IP Sources | Libraries | Compile Order

Sources | Netlist

Implementation Run Properties

impl_1

Project Summary | Device

Project Settings

Project name:	kc705_multiboot
Product family:	Kintex-7
Project part:	Kintex-7 KC705 Evaluation Platform
Top module name:	system_wrapper

Board Part

Display name:	Kintex-7 KC705 Evaluation Platform
Board part name:	xilinx.com:kc705:part0:1.0

Design Runs

Name	Part	Constraints	Strategy
synth_1	xc7k325tffg900-2	constrs_1	Vivado Synthesis Defaults (Vivado Synthesis 2014)
impl_1	xc7k325tffg900-2	constrs_1	Vivado Implementation Defaults (Vivado Implementation 2

Tcl Console | Messages | Log | Reports | Design Runs

Generate a programming file after implementation

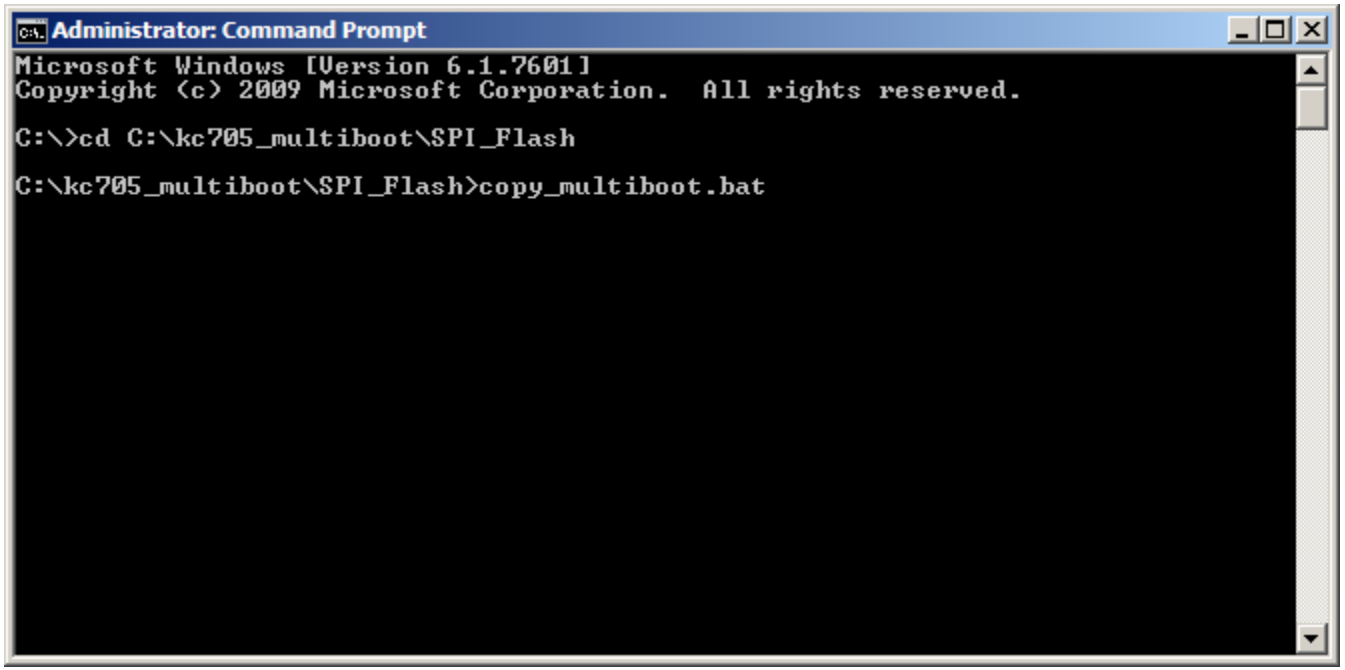
Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- Once the write_bitstream command finishes, open a Windows Prompt and enter these commands:

  cd C:\kc705_multiboot\SPI_Flash

  copy_multiboot.bat



Compile KC705 MultiBoot Design

- Now associate the second ELF file
- Right-click one of the ELF files and select Associate ELF files

kc705_multiboot - [C:/kc705_multiboot/kc705_multiboot.xpr] - Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Default Layout

write_bitstream Complete

Flow Navigator

Run Simulation

RTL Analysis
- Open Elaborated Design

Synthesis
- Synthesis Settings
- Run Synthesis
- Open Synthesized Desig

Implementation
- Implementation Settings
- Run Implementation
- Open Implemented Desig

Program and Debug
- Bitstream Settings
- Generate Bitstream
- Open Hardware Manage

Project Manager - kc705_multiboot

Sources

Design Sources (3)
- system_wrapper (s
- ELF (2)
  - golden_iprog_spi.elf
  - multiboot.elf

Constraints (1)

Simulation Sources (3)
- sim_1 (3)
  - system_wrappe
  - ELF (2)
    - golden_iprog_sp
    - multiboot.elf

Hierarchy | IP Sources | Libraries

Sources | Templates

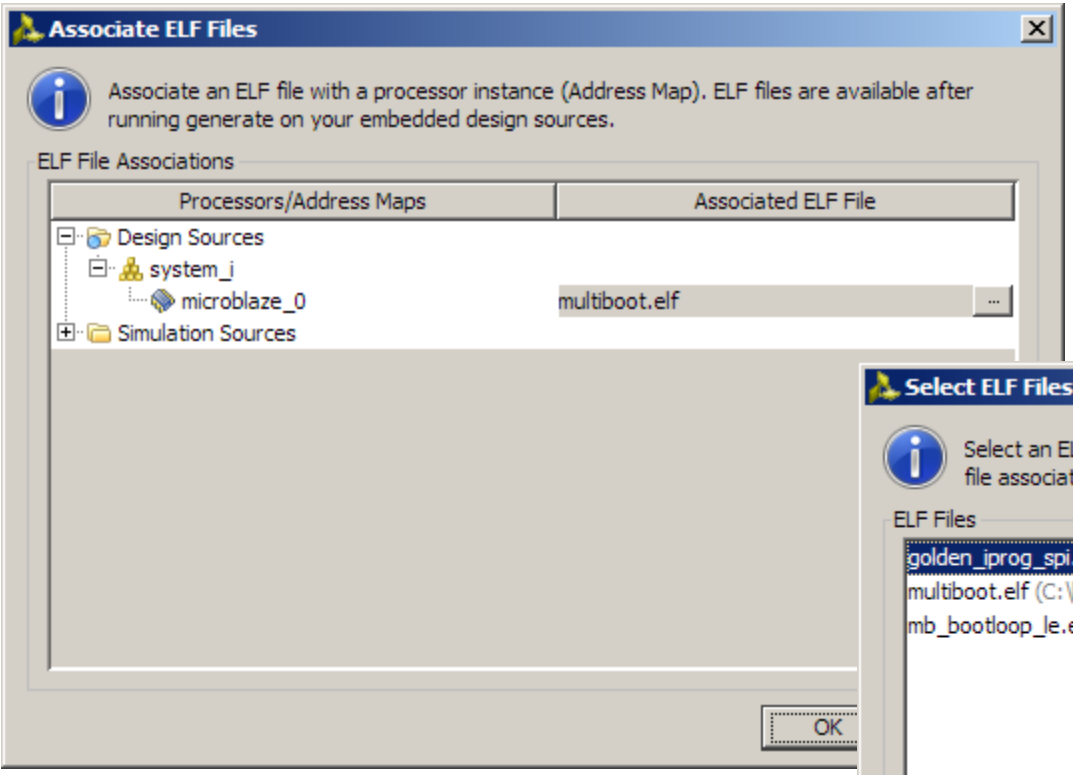
Source File Properties...	Ctrl+E
Open File	Alt+O
Replace File...	
Copy File Into Project	
Copy All Files Into Project	Alt+I
Remove File from Project...	Delete
Enable File	Alt+Equals
Disable File	Alt+Minus
Hierarchy Update	▸
Refresh Hierarchy	
IP Hierarchy	▸
Set as Top	
Set File Type...	
Set Used In...	
Edit Constraints Sets...	
Edit Simulation Sets...	
Associate ELF Files...	

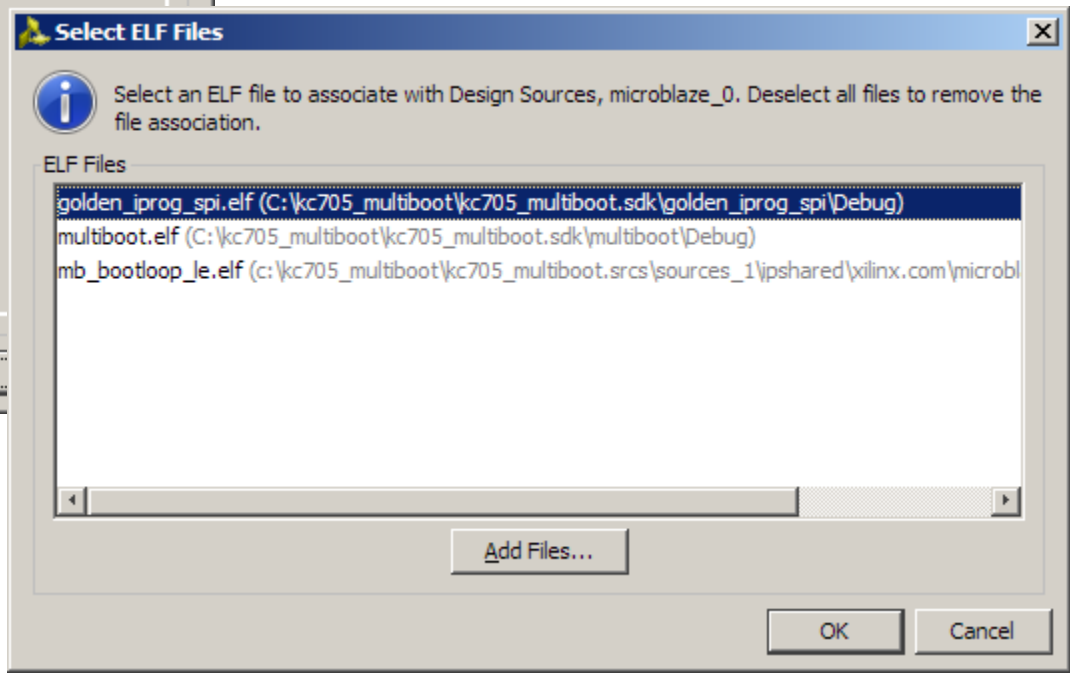
ELF File Association

Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- Click the button to the right of the multiboot.elf; select the golden_iprog_spi.elf then click OK twice





Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- Right-click on impl_1 and select Force Up-to-Date

kc705_multiboot - [C:/kc705_multiboot/kc705_multiboot.xpr] - Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Default Layout

Implementation Out-of-date more info

Flow Navigator

Project Manager
- Project Settings
- Add Sources
- IP Catalog

IP Integrator
- Create Block Design
- Open Block Design
- Generate Block Design

Simulation
- Simulation Settings
- Run Simulation

RTL Analysis
- Open Elaborated Design

Synthesis
- Synthesis Settings

Implemented Design - xc7k325tffg900-2 (active)

Sources

Design Sources (3)
- system_wrapper (system_wrapper.v) (1)
- ELF (2)
  - golden_iprog_spi.elf
  - multiboot.elf

Hierarchy | IP Sources | Libraries | Compile

Sources | Netlist

Implementation Run Properties

impl_1

Design Runs

Name	Strategy
synth_1	is Defaults (Vivado Synthesis 2014)
impl_1	ntation Defaults (Vivado Implementation 2

Tcl Console | Messages | Log

Project Summary | Device

Project Settings

Project name: kc705_multiboot

Product family: Kintex-7

Kintex-7 KC705 Evaluation Platform

e: system_wrapper

Kintex-7 KC705 Evaluation Platform

e: xilinx.com:kc705:part0:1.0

Implementation Run Properties... Ctrl+E

Delete Delete

Make Active

Change Run Settings...

Set Incremental Compile...

Save As Strategy...

Open Run

Launch Runs...

Reset Runs

Launch Next Step

Reset to Previous Step: write_bitstream

Force Up-to-Date

Generate Bitstream

Export Bitstream File...

Display Run Log

Force the selected run up-to-date

Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- Select Generate Bitstream

kc705_multiboot - [C:/kc705_multiboot/kc705_multiboot.xpr] - Vivado 2014.2

File Edit Flow Tools Window Layout View Help

Search commands

Default Layout

write_bitstream Complete

Flow Navigator

Implementation
- Implementation Settings
- Run Implementation
- Implemented Design
  - Constraints Wizard
  - Edit Timing Constrair
  - Report Timing Summ
  - Report Clock Networ
  - Report Clock Interac
  - Report DRC
  - Report Noise
  - Report Utilization
  - Report Power

Program and Debug
- Bitstream Settings
- Generate Bitstream
- Open Hardware Manage

Implemented Design - xc7k325tffg900-2 (active)

Sources

Design Sources (3)
- system_wrapper (system_wrapper.v) (1)
- ELF (2)
  - golden_iprog_spi.elf
  - multiboot.elf

Hierarchy | IP Sources | Libraries | Compile Order

Sources | Netlist

Implementation Run Properties

impl_1

Project Summary | Device

Project Settings

Project name:	kc705_multiboot
Product family:	Kintex-7
Project part:	Kintex-7 KC705 Evaluation Platform
Top module name:	system_wrapper

Board Part

Display name:	Kintex-7 KC705 Evaluation Platform
Board part name:	xilinx.com:kc705:part0:1.0

Design Runs

Name	Part	Constraints	Strategy
synth_1	xc7k325tffg900-2	constrs_1	Vivado Synthesis Defaults (Vivado Synthesis 2014)
impl_1	xc7k325tffg900-2	constrs_1	Vivado Implementation Defaults (Vivado Implementation 2

Tcl Console | Messages | Log | Reports | Design Runs

Generate a programming file after implementation

Note: Presentation applies to the KC705

Compile KC705 MultiBoot Design

- From the Command Prompt type:

  copy_golden_iprog_spi.bat

```
Administrator: Command Prompt
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation.  All rights reserved.

C:\>cd C:\kc705_multiboot\SPI_Flash

C:\kc705_multiboot\SPI_Flash>copy_multiboot.bat

C:\kc705_multiboot\SPI_Flash>copy /Y ..\kc705_multiboot.runs\impl_1\system_wrapp
er.bit .\multiboot.bit
        1 file(s) copied.

C:\kc705_multiboot\SPI_Flash>copy_golden_iprog_spi.bat
```

Note: Presentation applies to the KC705

Generate KC705 MultiBoot PROM File

- From the Command Prompt type:

  make_spi_mcs.bat

Administrator: Command Prompt

```
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation.  All rights reserved.

C:\>cd C:\kc705_multiboot\SPI_Flash

C:\kc705_multiboot\SPI_Flash>copy_multiboot.bat

C:\kc705_multiboot\SPI_Flash>copy /Y ..\kc705_multiboot.runs\impl_1\system_wrapp
er.bit .\multiboot.bit
        1 file(s) copied.

C:\kc705_multiboot\SPI_Flash>copy_golden_iprog_spi.bat

C:\kc705_multiboot\SPI_Flash>copy /Y ..\kc705_multiboot.runs\impl_1\system_wrapp
er.bit .\golden_iprog_spi.bit
        1 file(s) copied.

C:\kc705_multiboot\SPI_Flash>make_spi_mcs.bat
```

Note: Presentation applies to the KC705

Kintex-7 MultiBoot Details

MultiBoot Register Setup & Command

- **Below are the values programmed into the ICAP via IPROG**
  - This table is from UG470, 7 Series FPGAs Configuration User Guide

Table 7-1: **Example Bitstream for IPROG through ICAP**

Configuration Data (hex)	Explanation
FFFFFFFF	Dummy Word
AA995566	Sync Word
20000000	Type 1 NO OP
30020001	Type 1 Write 1 Words to WBSTAR
00000000	Warm Boot Start Address (Load the Desired Address)
30008001	Type 1 Write 1 Words to CMD
0000000F	IPROG Command
20000000	Type 1 NO OP

Note: Presentation applies to the KC705

MultiBoot Register Setup & Command

- IPROG command issued via the software in xhwicap_low_level_example.c

UltraEdit - [C:\kc705_multiboot\kc705_multiboot.sdk\SDK\SDK_Export\golden_iprog_spi\src\xhwicap_low_level_example.c]

File Edit Search Insert Project View Format Column Macro Scripting Advanced Window Help

```c
// Reusing IDCODE array and code to send IPROG
// From UG470 p. 126, Table 7-1
static u32 ReadId[HWICAP_EXAMPLE_BITSTREAM_LENGTH] =
{
  0xFFFFFFFF, /* Dummy Word */
  0xAA995566, /* Sync Word*/
  0x20000000, /* Type 1 NO OP */
  0x30020001, /* Write WBSTAR cmd */
  0x00400000, /* Addr in SPI Flash of Multiboot bitstream */
  0x30008001, /* Write CMD */
  0x0000000F, /* Write IPROG */
  0x20000000, /* Type 1 NO OP  */
};
```

Note: Presentation applies to the KC705

References

References

- **IP Integrator Documentation**
  - Vivado Design Suite Tcl Command Reference Guide
    - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_2/ug835-vivado-tcl-commands.pdf
  - Designing IP Subsystems Using IP Integrator
    - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_2/ug994-vivado-ip-subsystems.pdf
- **7 Series Configuration**
  - 7 Series FPGAs Configuration User Guide
    - http://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf

Documentation

Documentation

- **Kintex-7**
  - Kintex-7 FPGA Family
    - http://www.xilinx.com/products/silicon-devices/fpga/kintex-7/index.htm
  - Design Advisory Master Answer Record for Kintex-7 FPGAs
    - http://www.xilinx.com/support/answers/42946.htm
- **KC705 Documentation**
  - Kintex-7 FPGA KC705 Evaluation Kit
    - http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm
  - KC705 Getting Started Guide
    - http://www.xilinx.com/support/documentation/boards_and_kits/kc705/2013_2/ug883_K7_KC705_Eval_Kit.pdf
  - KC705 User Guide
    - http://www.xilinx.com/support/documentation/boards_and_kits/kc705/ug810_KC705_Eval_Bd.pdf