



# KC705 GTX IBERT Design Creation

June 2014

XTP200

# Revision History

Date	Version	Description
06/09/14	9.0	Regenerated for 2014.2.
04/16/14	8.0	Regenerated for 2014.1.
12/18/13	7.0	Regenerated for 2013.4.
10/23/13	6.0	Regenerated for 2013.3.
06/19/13	5.0	Regenerated for 2013.2. AR55738 fixed.
04/03/13	4.0	Regenerated for 2013.1. Added AR55738.
12/18/12	3.0	Regenerated for 2012.4. Added AR53392.
10/23/12	2.0	Regenerated for 2012.3. Added AR52368.
08/20/12	1.0	Initial version. Added AR50886.

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# KC705 IBERT Overview

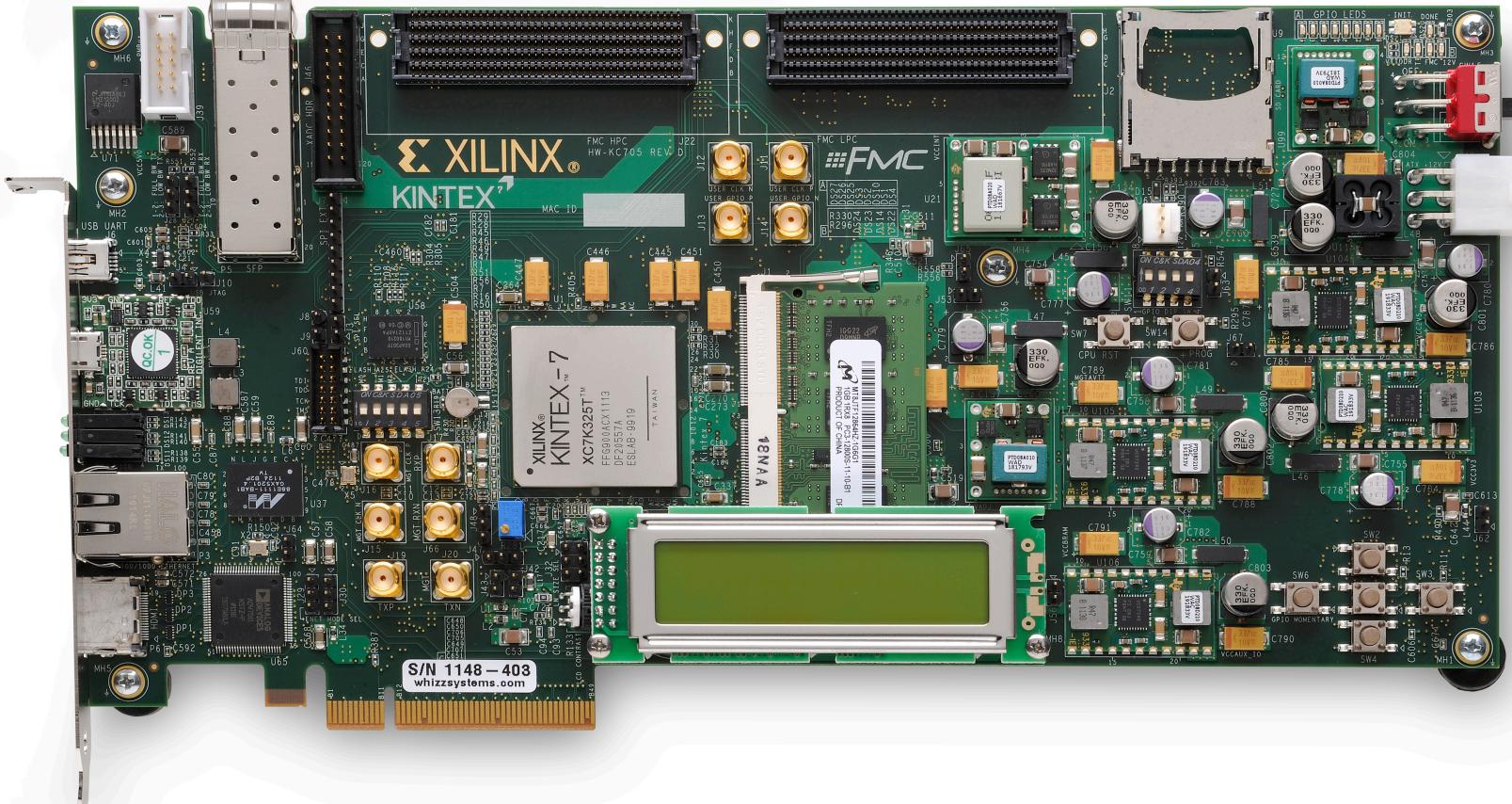
## ► Description

- The LogiCORE Integrated Bit Error Ratio (IBERT) core is used to create a pattern generation and verification design to exercise the Kintex-7 GTX transceivers. A graphical user interface is provided through the Vivado Hardware Manager.

## ► Reference Design IP

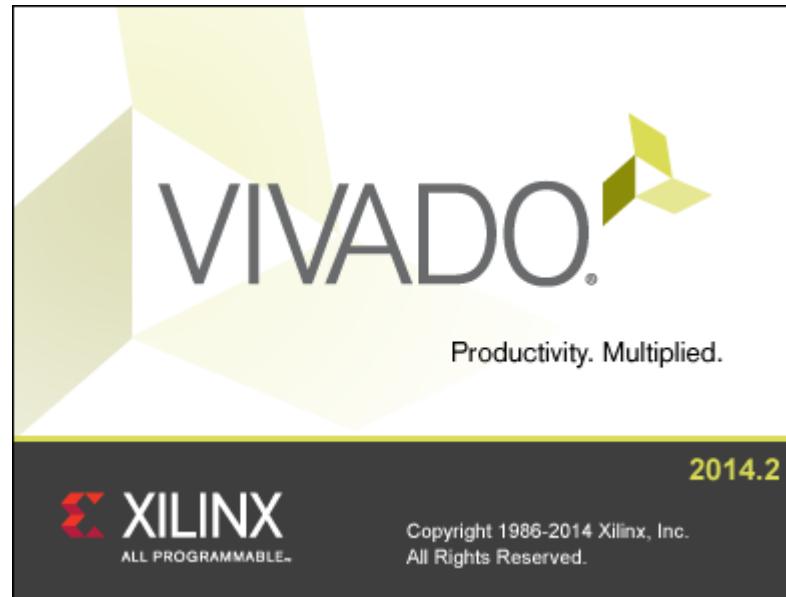
- LogiCORE IBERT Example Designs

# Xilinx KC705 Board



# Vivado Software Requirements

- Xilinx Vivado Design Suite 2014.2, Design Edition

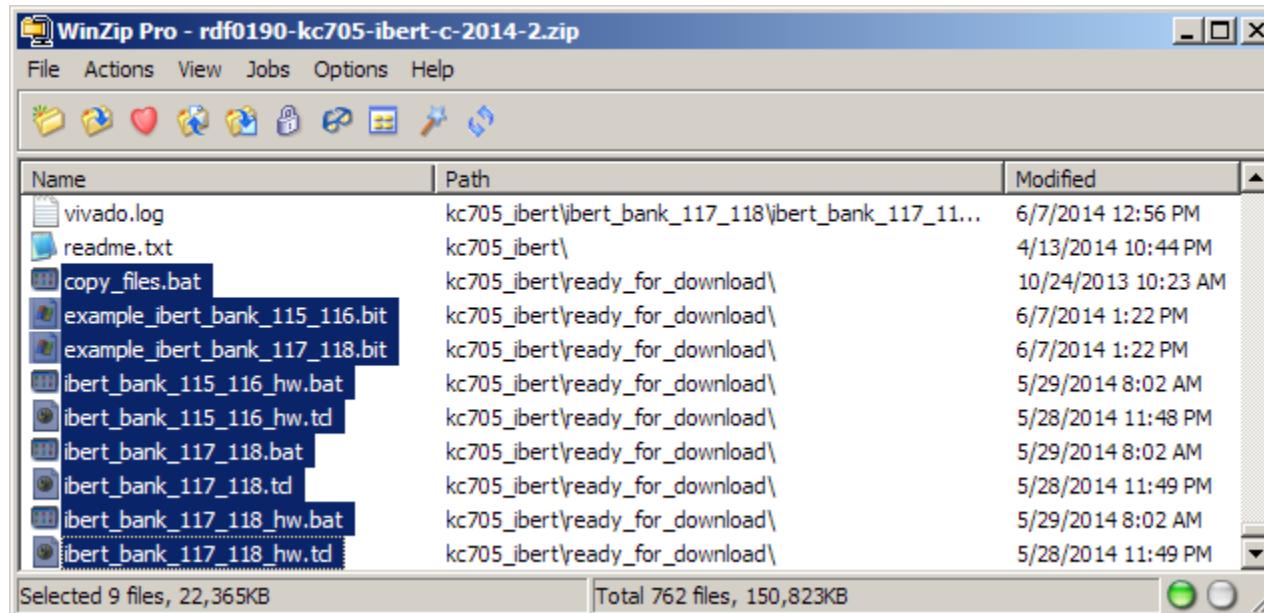


# **Setup for the KC705 IBERT Designs**

# Setup for the KC705 IBERT Designs

► Open the RDF0190 - KC705 GTX IBERT Design Files (2014.2 C) zip file, and extract these files to your C:\ drive:

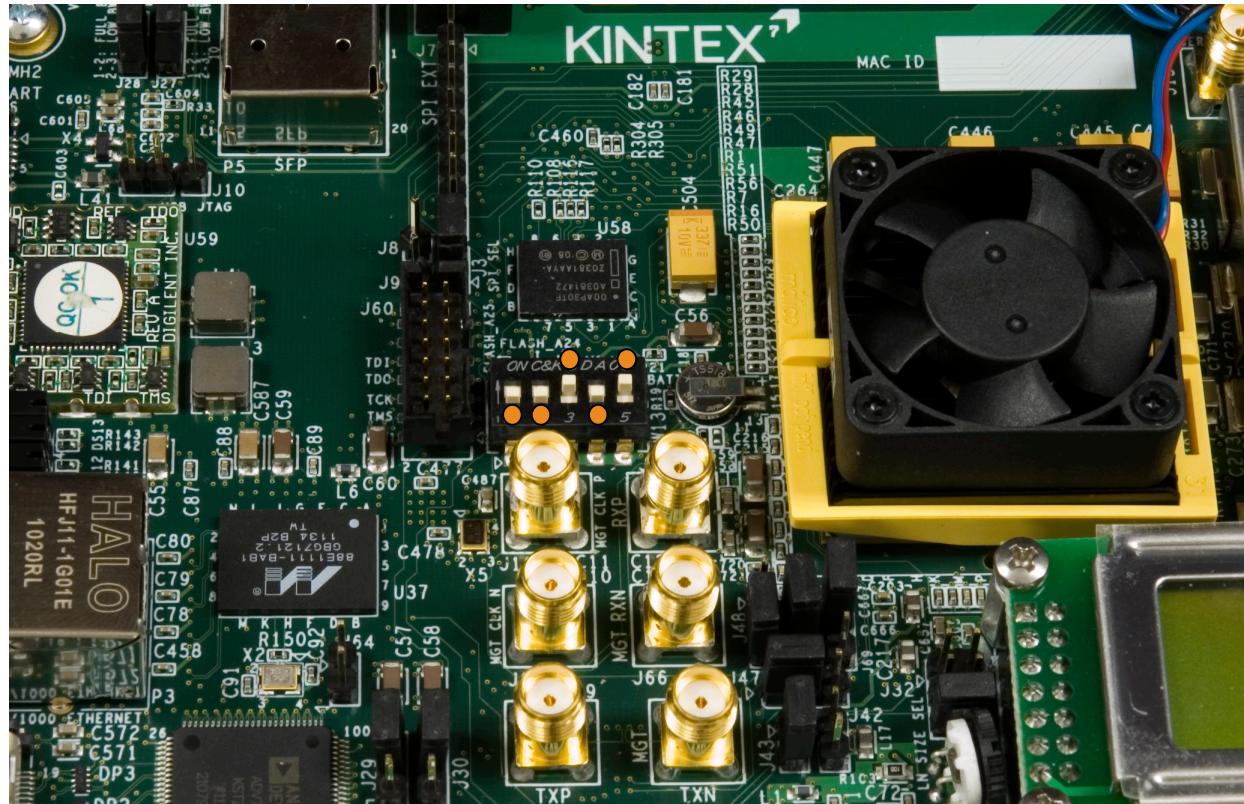
- kc705\_ibert\ready\_for\_download\\*
- Available through <http://www.xilinx.com/kc705>



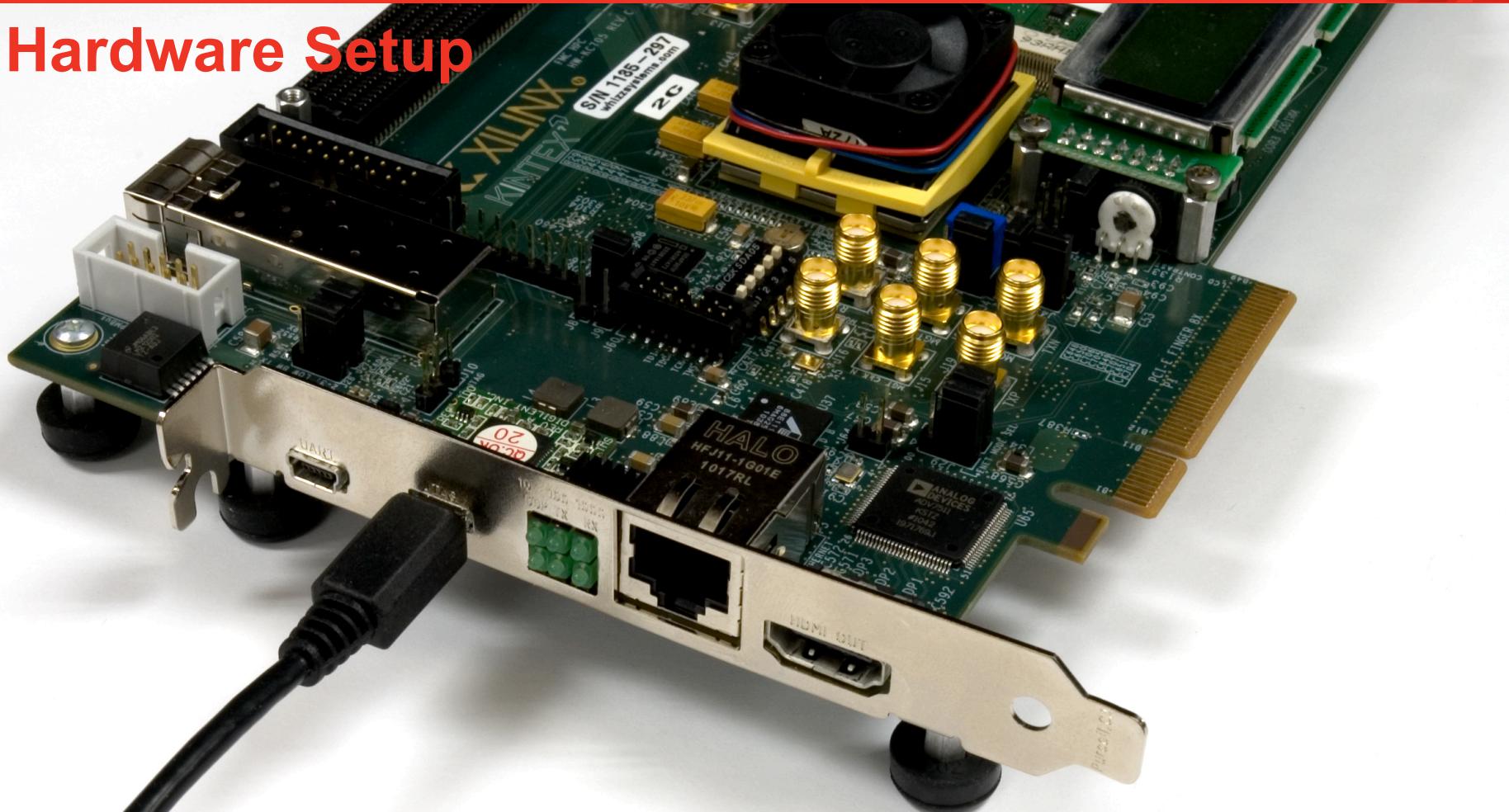
# Hardware Setup

## ► Set S13 to 00101 (1 = on, Position 1 → Position 5)

- This enables JTAG configuration



# Hardware Setup



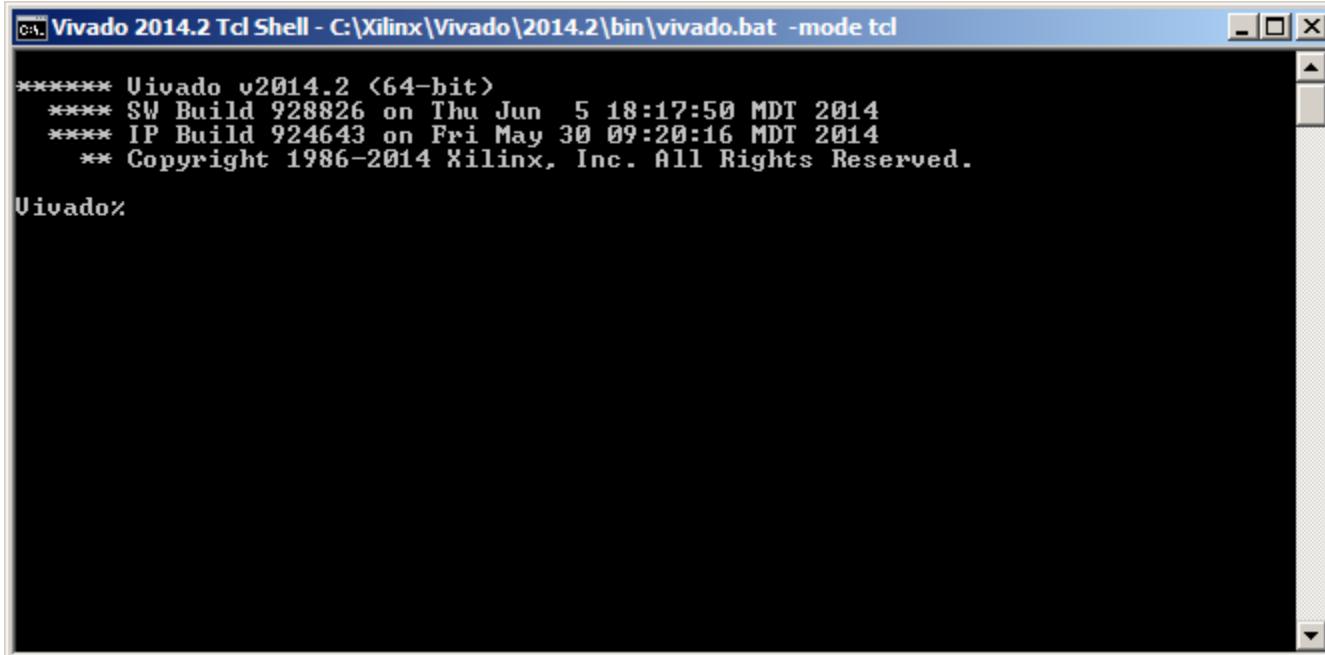
- **Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the KC705 board**
  - Connect this cable to your PC
  - Power on the KC705 board

# **Testing IBERT Banks 117 and 118**

# Testing IBERT Banks 117 and 118

## ► Open a Vivado Tcl Shell:

**Start → All Programs → Xilinx Design Tools → Vivado 2014.2 →  
Vivado 2014.2 Tcl Shell**



The screenshot shows a Windows command-line interface window titled "Vivado 2014.2 Tcl Shell - C:\Xilinx\Vivado\2014.2\bin\vivado.bat -mode tcl". The window displays the following startup information:

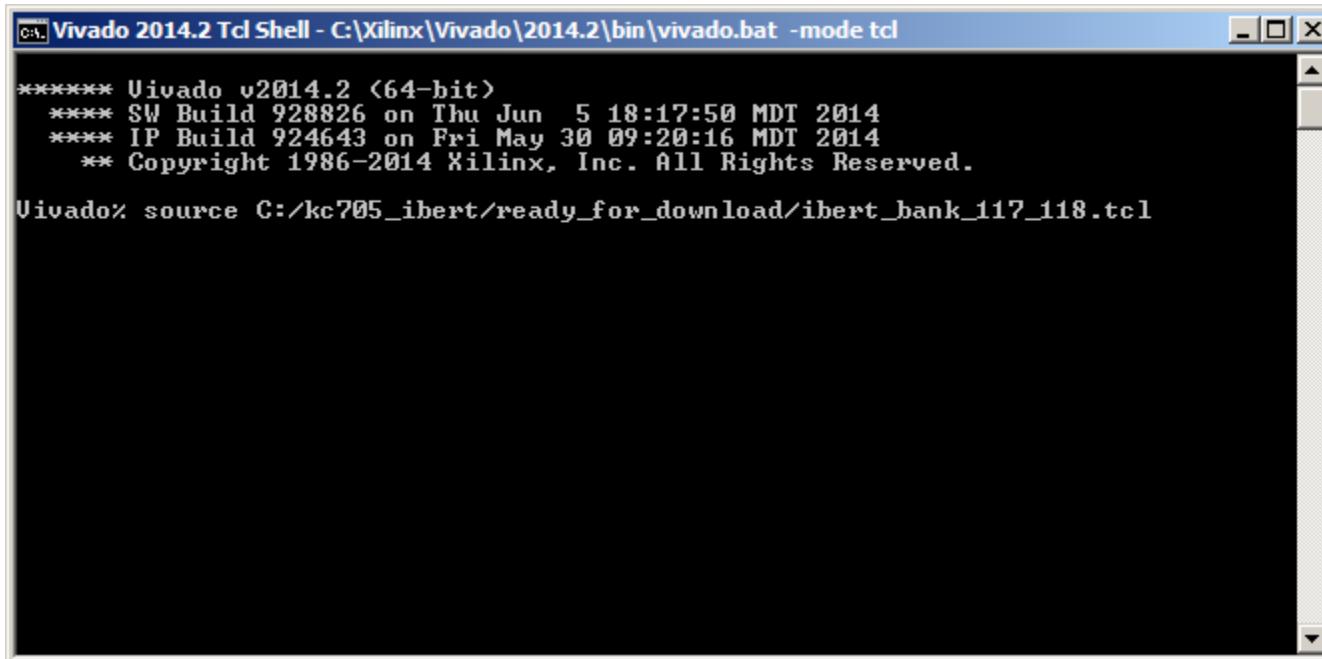
```
***** Vivado v2014.2 (64-bit)
***** SW Build 928826 on Thu Jun  5 18:17:50 MDT 2014
***** IP Build 924643 on Fri May 30 09:20:16 MDT 2014
** Copyright 1986-2014 Xilinx, Inc. All Rights Reserved.
```

The prompt "Vivado%" is visible at the bottom of the window.

# Testing IBERT Banks 117 and 118

- In the Vivado Tcl Shell type:

```
source C:/kc705_ibert/ready_for_download/ibert_bank_117_118.tcl
```



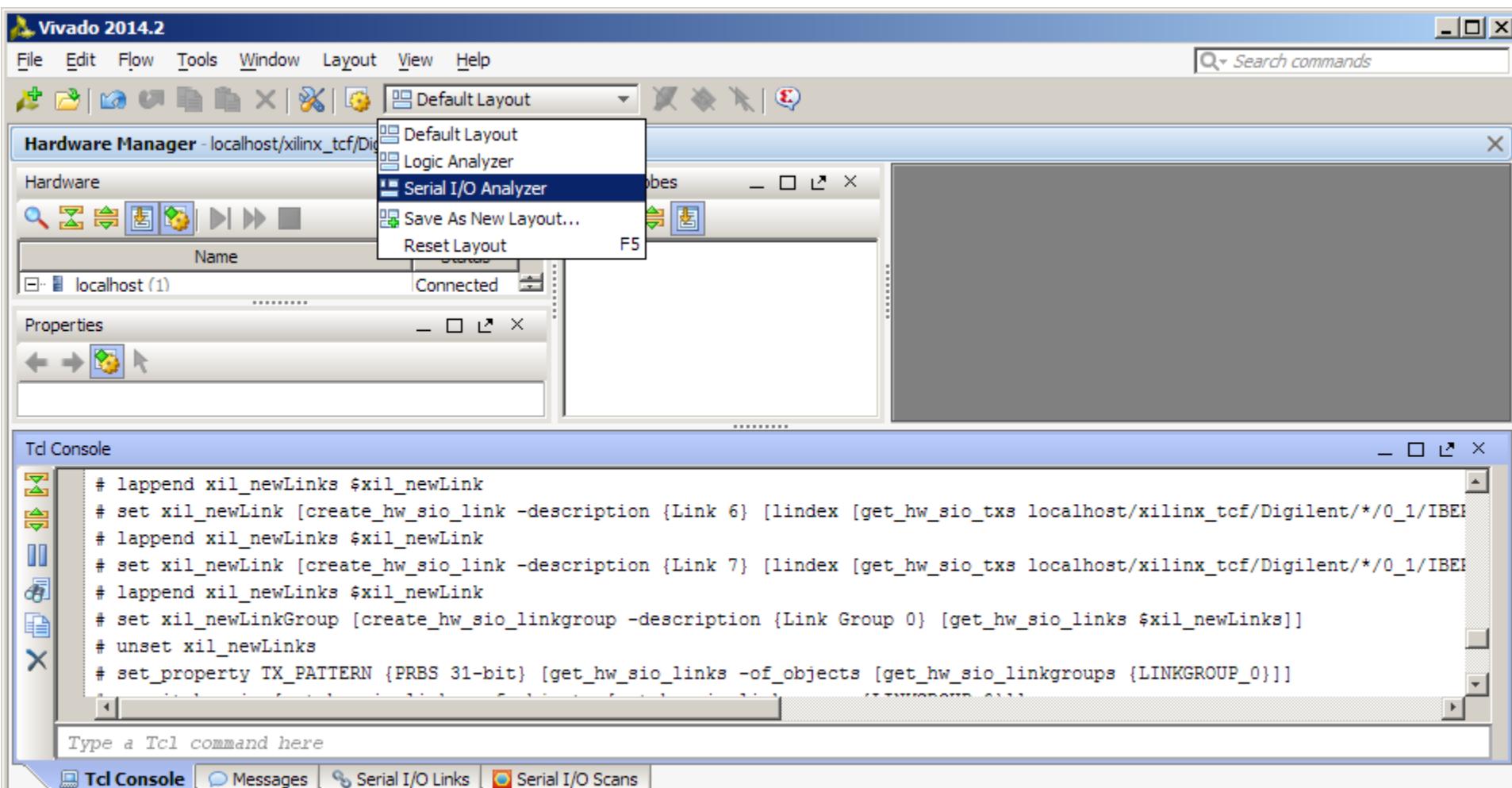
The screenshot shows a Windows command-line interface window titled "Vivado 2014.2 Tcl Shell - C:\Xilinx\Vivado\2014.2\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2014.2 (64-bit)
***** SW Build 928826 on Thu Jun  5 18:17:50 MDT 2014
***** IP Build 924643 on Fri May 30 09:20:16 MDT 2014
** Copyright 1986-2014 Xilinx, Inc. All Rights Reserved.

Vivado% source C:/kc705_ibert/ready_for_download/ibert_bank_117_118.tcl
```

# Testing IBERT Banks 117 and 118

- If needed, set Vivado GUI layout to Serial I/O Analyzer



# Testing IBERT Banks 117 and 118

- The Status column shows the line rate is 10.000 Gbps for all GTXs
- Scroll to the right to view the Loopback Mode

The screenshot shows the Vivado 2014.2 Hardware Manager interface. The main window displays the 'Serial I/O Links' table. The table has columns for Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, RX Pattern, TX Pre-Cursor, and TX Post-Code. The table lists 8 Link Groups, each containing 8 links. All links are operating at 10.000 Gbps. The BER values range from 9.78E-13 to 9.809E-13. The BERT Reset column shows 'Reset' for all entries. The TX and RX patterns are set to PRBS 31-bit. The TX Pre-Cursor and TX Post-Code values are mostly 1.67 dB (00111) or 0.68 dB (00000). The RX Pre-Cursor and RX Post-Code values are mostly 1.67 dB (00111) or 0.68 dB (00000).

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Code
Ungrouped Links (0)											
Link Group 0 (8)											
Link 0	MGT_X0Y8/TX	MGT_X0Y8/RX	10.000 Gbps	1.019E12	0E0	9.809E-13	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00000)
Link 1	MGT_X0Y9/TX	MGT_X0Y9/RX	10.000 Gbps	1.02E12	0E0	9.805E-13	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00000)
Link 2	MGT_X0Y10...	MGT_X0Y10...	10.000 Gbps	1.02E12	0E0	9.801E-13	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00000)
Link 3	MGT_X0Y11...	MGT_X0Y11...	10.000 Gbps	1.021E12	0E0	9.797E-13	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00000)
Link 4	MGT_X0Y12...	MGT_X0Y12...	10.000 Gbps	1.021E12	0E0	9.794E-13	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00000)
Link 5	MGT_X0Y13...	MGT_X0Y13...	10.000 Gbps	1.021E12	0E0	9.791E-13	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00000)
Link 6	MGT_X0Y14...	MGT_X0Y14...	10.000 Gbps	1.022E12	0E0	9.787E-13	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00000)
Link 7	MGT_X0Y15...	MGT_X0Y15...	10.000 Gbps	1.022E12	0E0	9.784E-13	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00000)

# Testing IBERT Banks 117 and 118

- Loopback Mode is set to Near-End PCS for all GTXs
- Close Vivado GUI after finished viewing

The screenshot shows the Vivado 2014.2 Hardware Manager interface with the title bar "Vivado 2014.2". The menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. A search bar "Search commands" is located in the top right. The main window is titled "Hardware Manager - localhost/xilinx\_tcf/Digilent/210203337270A". It displays a table titled "Serial I/O Links" with the following columns: RX Pattern, TX Pre-Cursor, TX Post-Cursor, TX Diff Swing, DFE Enabled, Inject Error, TX Reset, RX Reset, RX PLL Status, TX PLL Status, and Loopback Mode. There are 10 rows, each representing a PRBS 31-bit link. The "Loopback Mode" column for all rows is set to "Near-End PCS". The "Inject Error" column contains "Inject" for most rows and "Reset" for the last row. The "TX Reset" and "RX Reset" columns show various states like "Reset", "Locked", and "Locked". The "RX PLL Status" and "TX PLL Status" columns are mostly green, indicating good status.

	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode
1	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset			Near-End PCS
2	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS
3	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS
4	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS
5	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS
6	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS
7	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS
8	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS
9	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS
10	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS

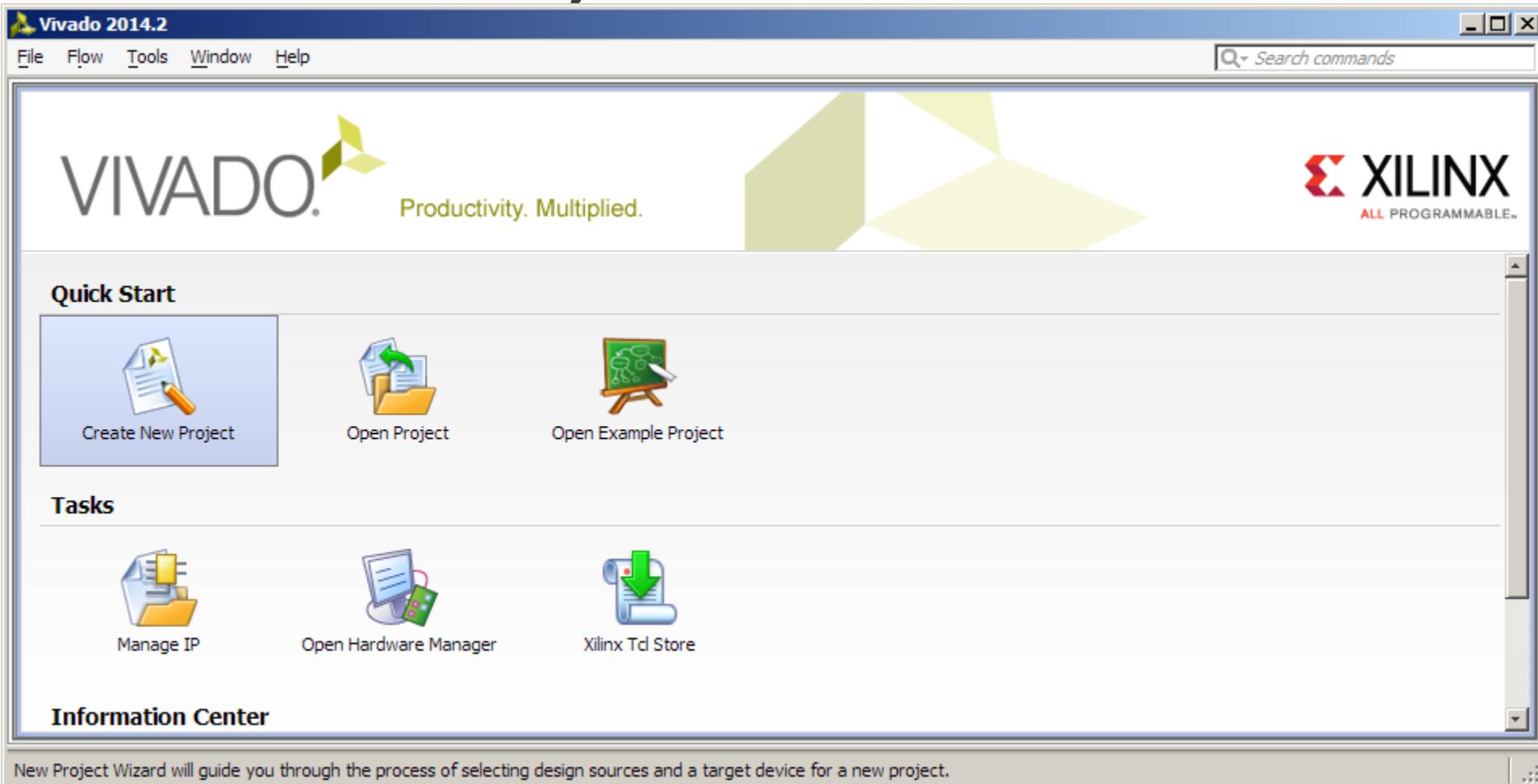
# Create IBERT Design for Banks 115, 116

# Create IBERT Design for Banks 115, 116

## ► Open Vivado

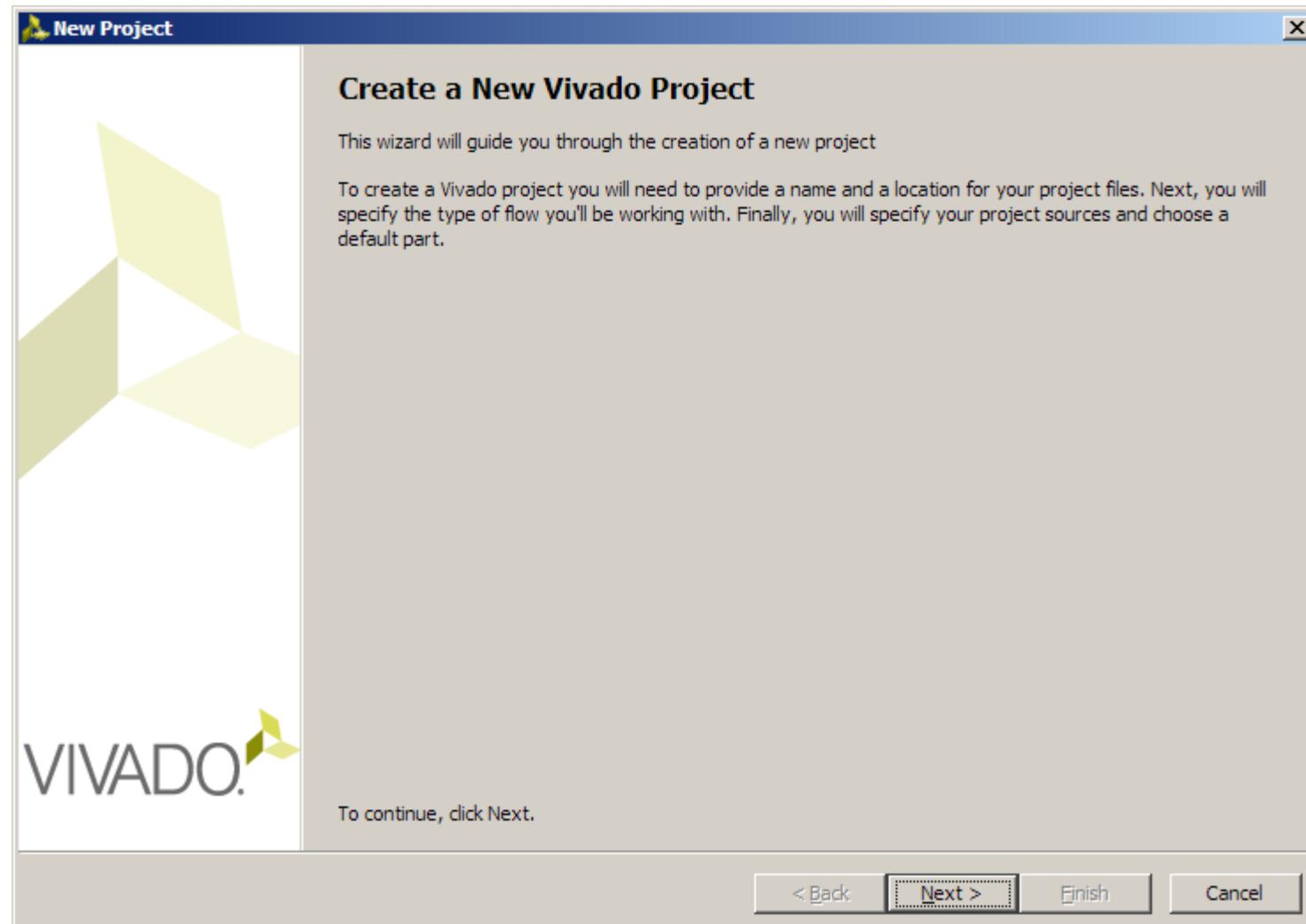
Start → All Programs → Xilinx Design Tools → Vivado 2014.2 → Vivado

## ► Select Create New Project



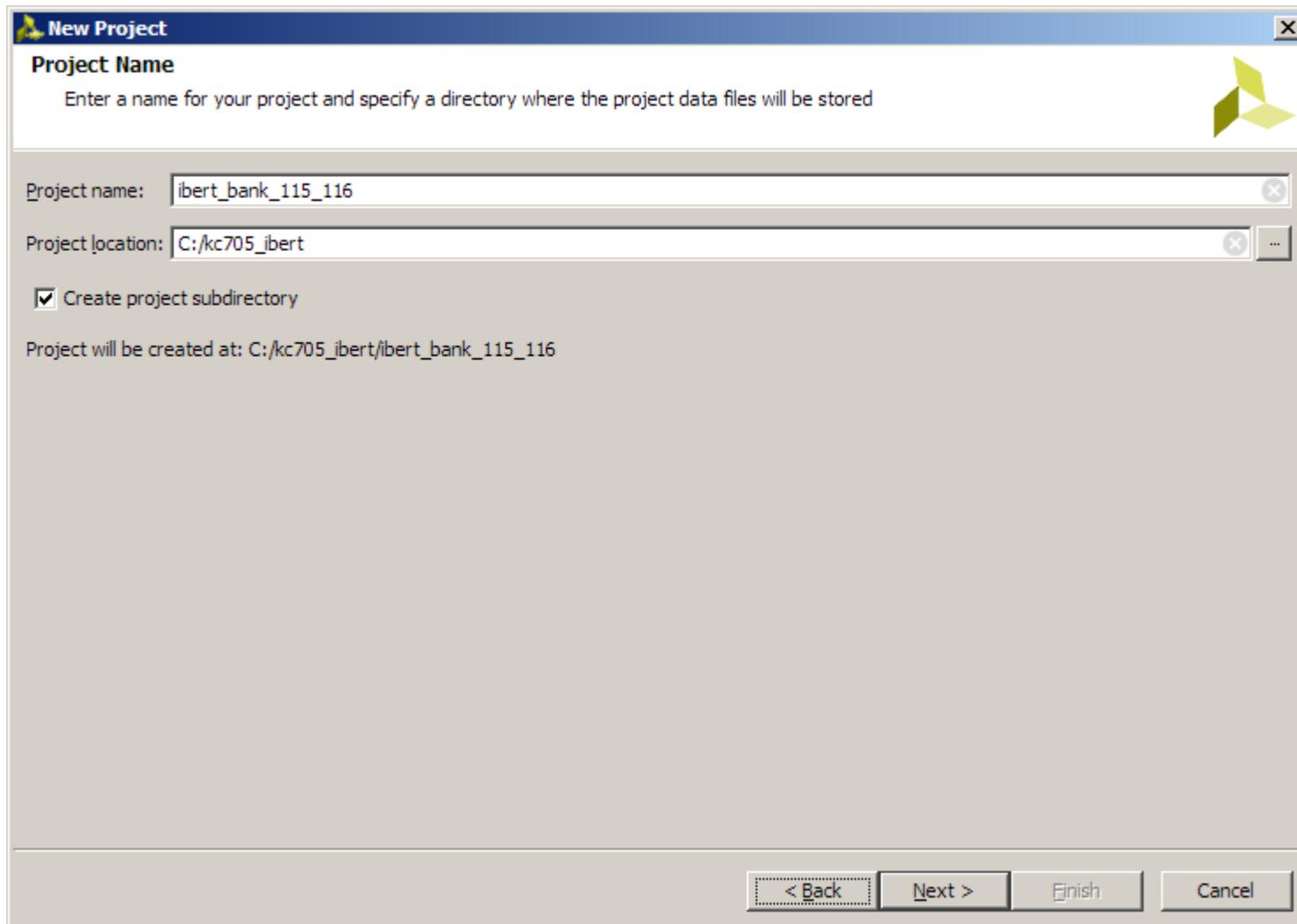
# Create IBERT Design for Banks 115, 116

► Click Next



# Create IBERT Design for Banks 115, 116

- Set the Project name and location to `ibert_bank_115_116` and `C:/kc705_ibert`; check Create project subdirectory



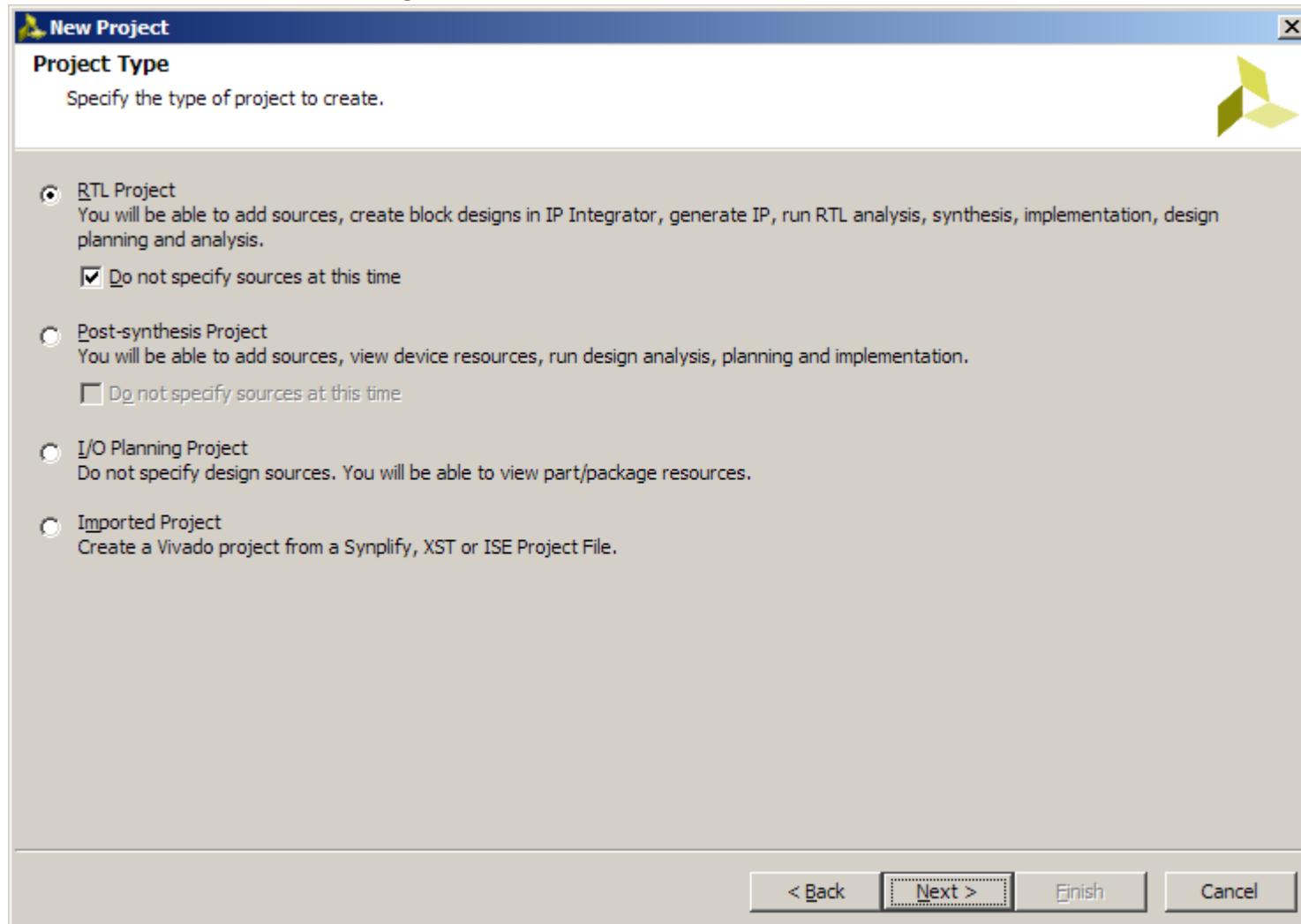
Note: Vivado generally requires forward slashes in paths

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# Create IBERT Design for Banks 115, 116

## ► Select RTL Project

- Select **Do not specify sources at this time**



# Create IBERT Design for Banks 115, 116

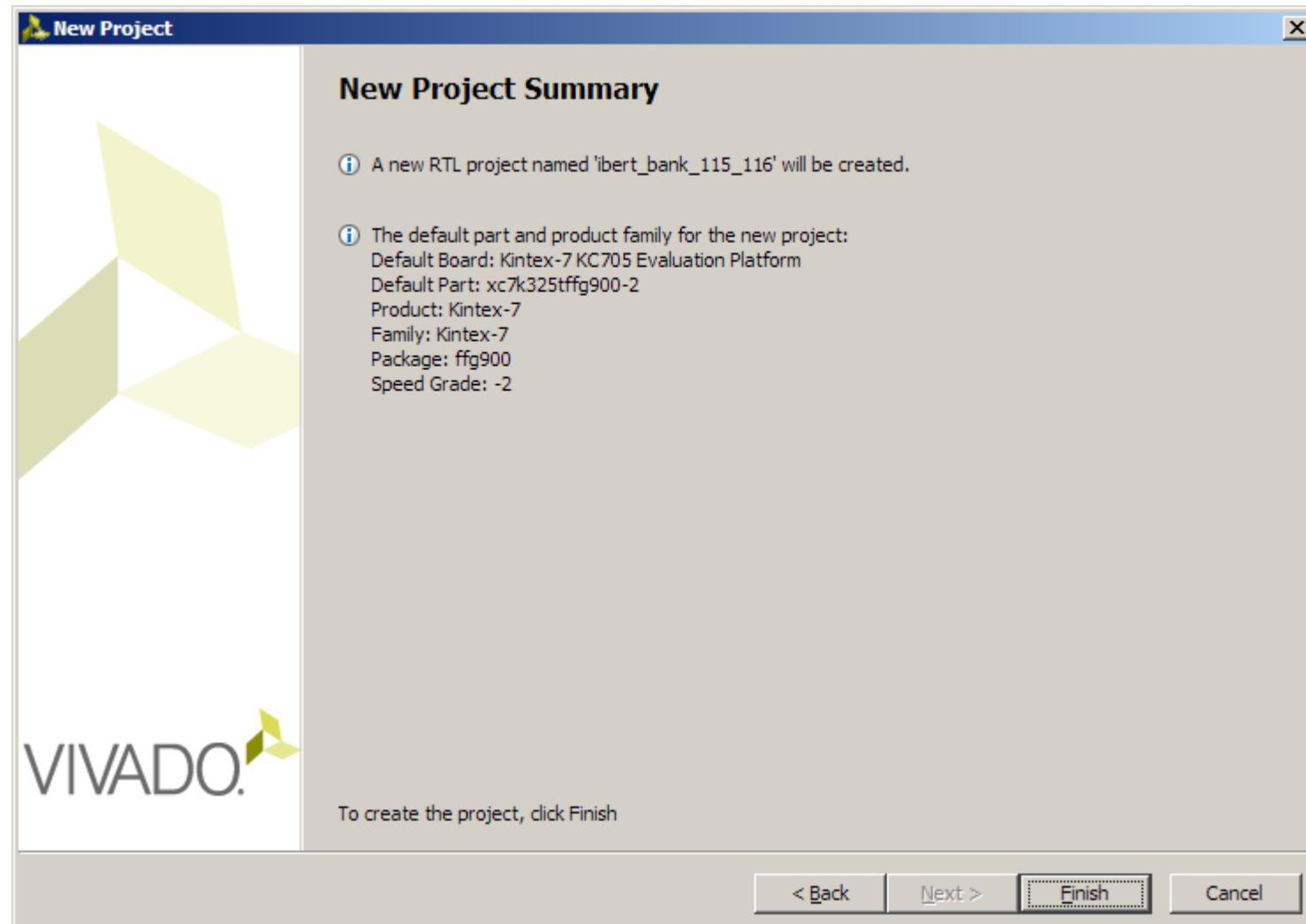
## ► Select the KC705 Board

The screenshot shows the 'New Project' dialog box with the title 'Default Part'. It includes a search bar, filter options for Vendor (All), Display Name (All), and Board Rev (Latest), and a 'Reset All Filters' button. A table lists various Xilinx evaluation boards, with the 'KC705 Evaluation Platform' selected. The table columns are: Display Name, Vendor, Board Rev, Part, I/O Pin Count, File Version, and Available IOBs.

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version	Available IOBs
MicroZed Board	em.avnet.com	e	xc7z010clg400-1	400	1.0	100
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1	484	1.0	200
Artix-7 AC701 Evaluation Platform	xilinx.com	1.0	xc7a200tfgb676-2	676	1.0	400
<b>Kintex-7 KC705 Evaluation Platform</b>	<b>xilinx.com</b>	<b>1.1</b>	<b>xc7k325tffg900-2</b>	<b>900</b>	<b>1.0</b>	<b>500</b>
Virtex-7 VC707 Evaluation Platform	xilinx.com	1.1	xc7vx485tffg1761-2	1,761	1.0	700
Virtex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2	1,761	1.0	850
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020clg484-1	484	1.0	200
ZYNQ-7 ZC706 Evaluation Board	xilinx.com	1.1	xc7z045ffg900-2	900	1.0	362

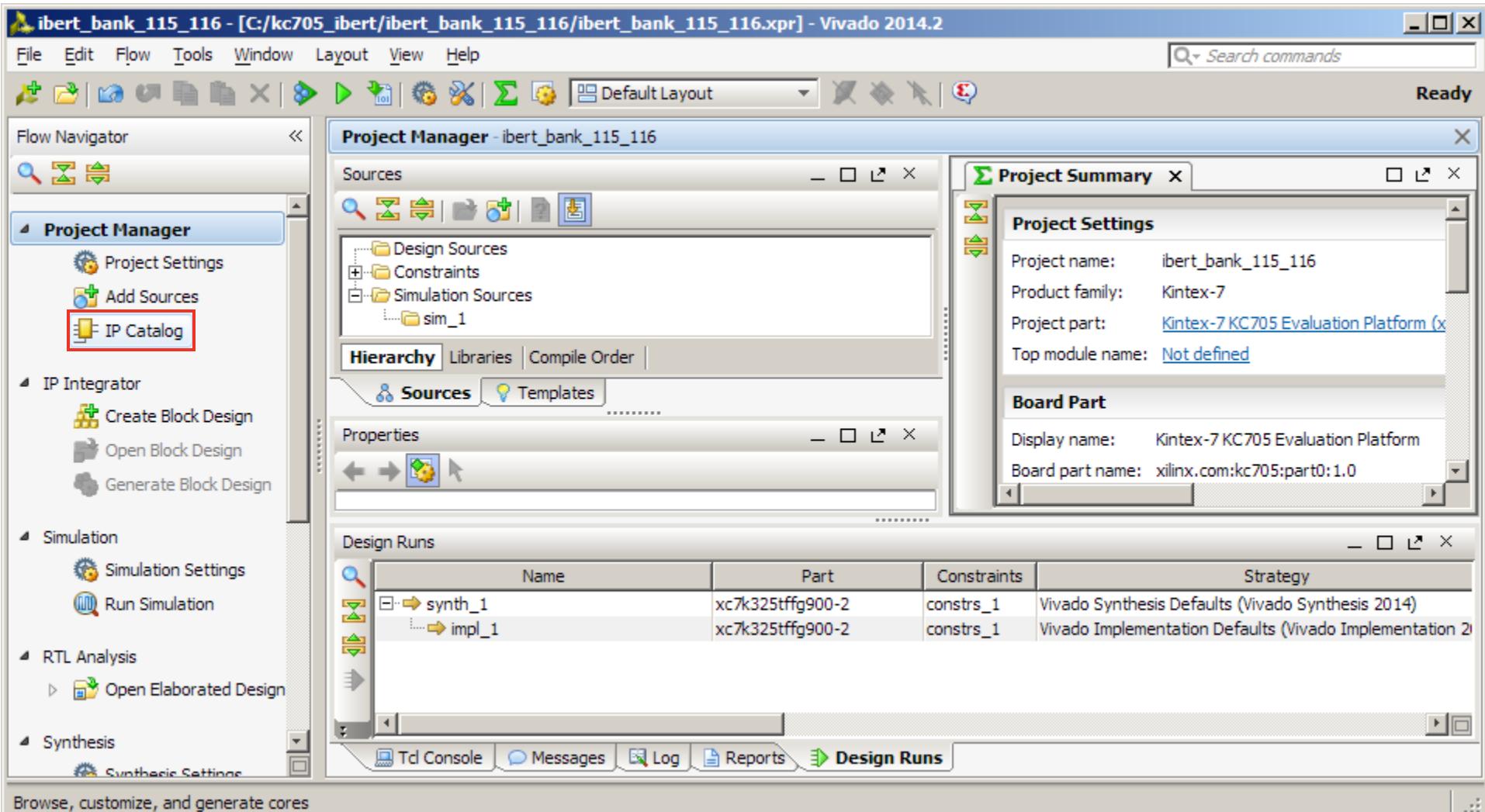
# Create IBERT Design for Banks 115, 116

► Click Finish



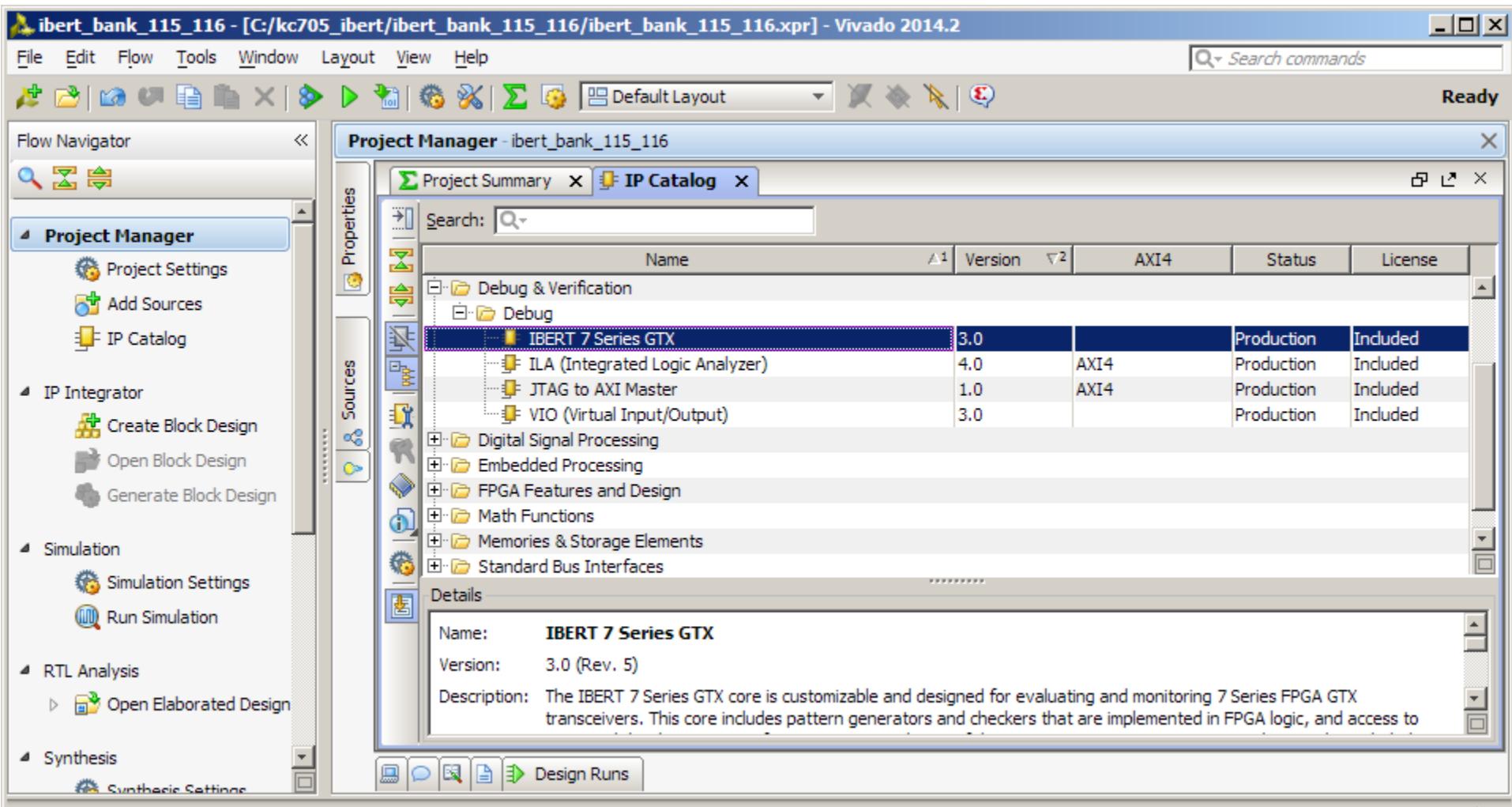
# Create IBERT Design for Banks 115, 116

► Click on IP Catalog



# Create IBERT Design for Banks 115, 116

► Select IBERT 7 Series GTX, v3.0 under Debug & Verification



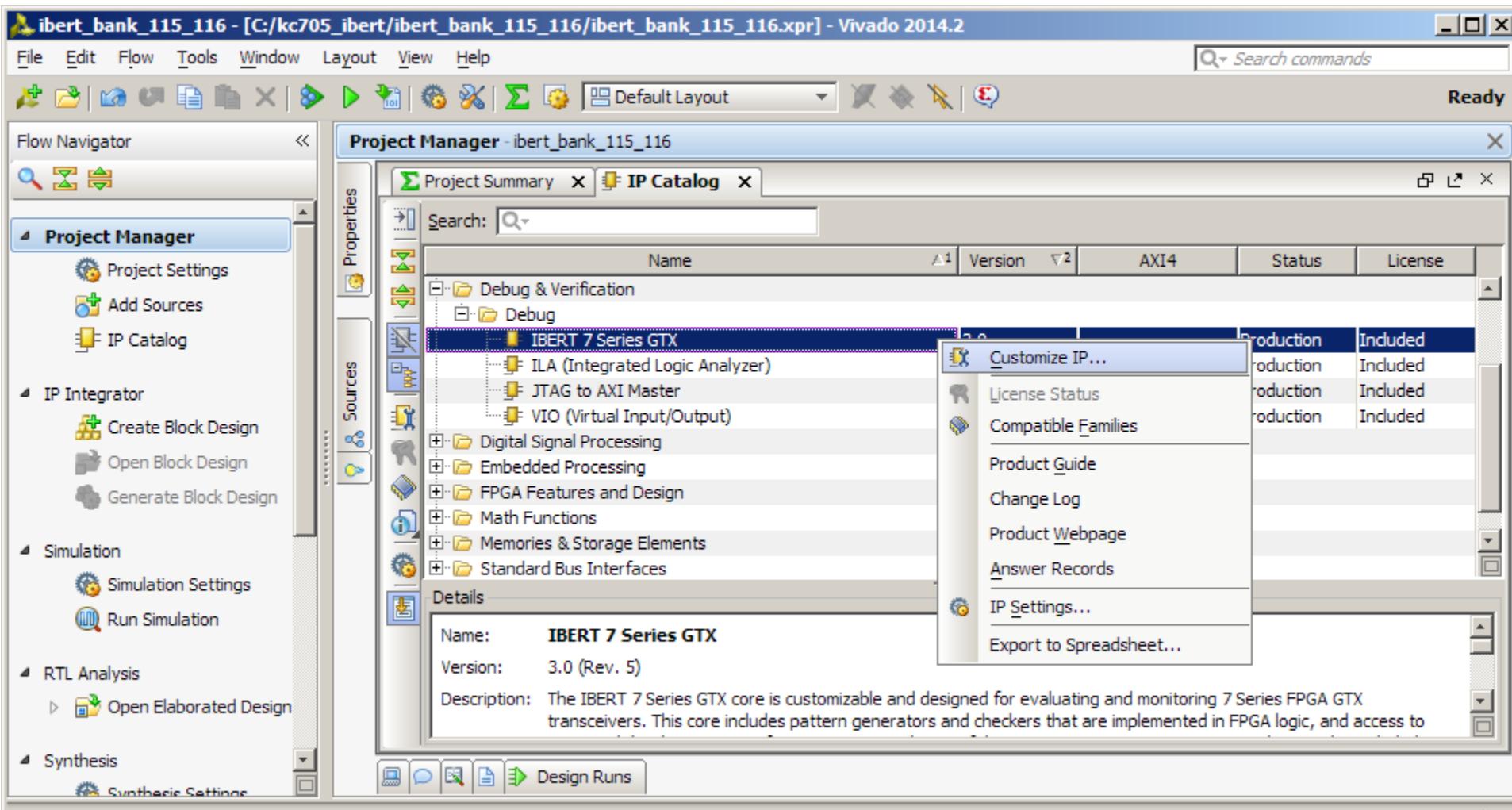
IP: IBERT 7 Series GTX

Note: Presentation applies to the KC705

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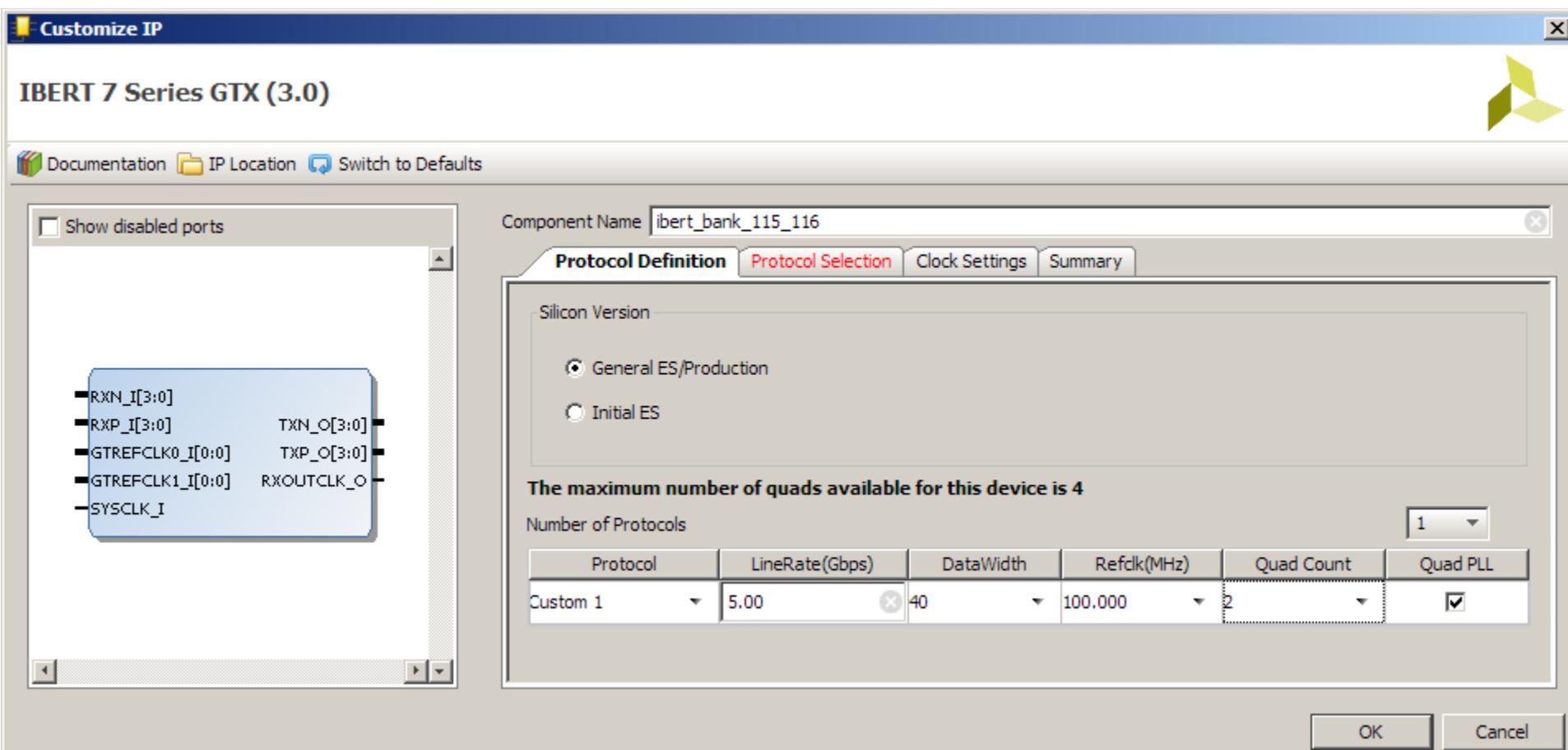
# Create IBERT Design for Banks 115, 116

► Right click on IBERT 7 Series GTX and select Customize IP...



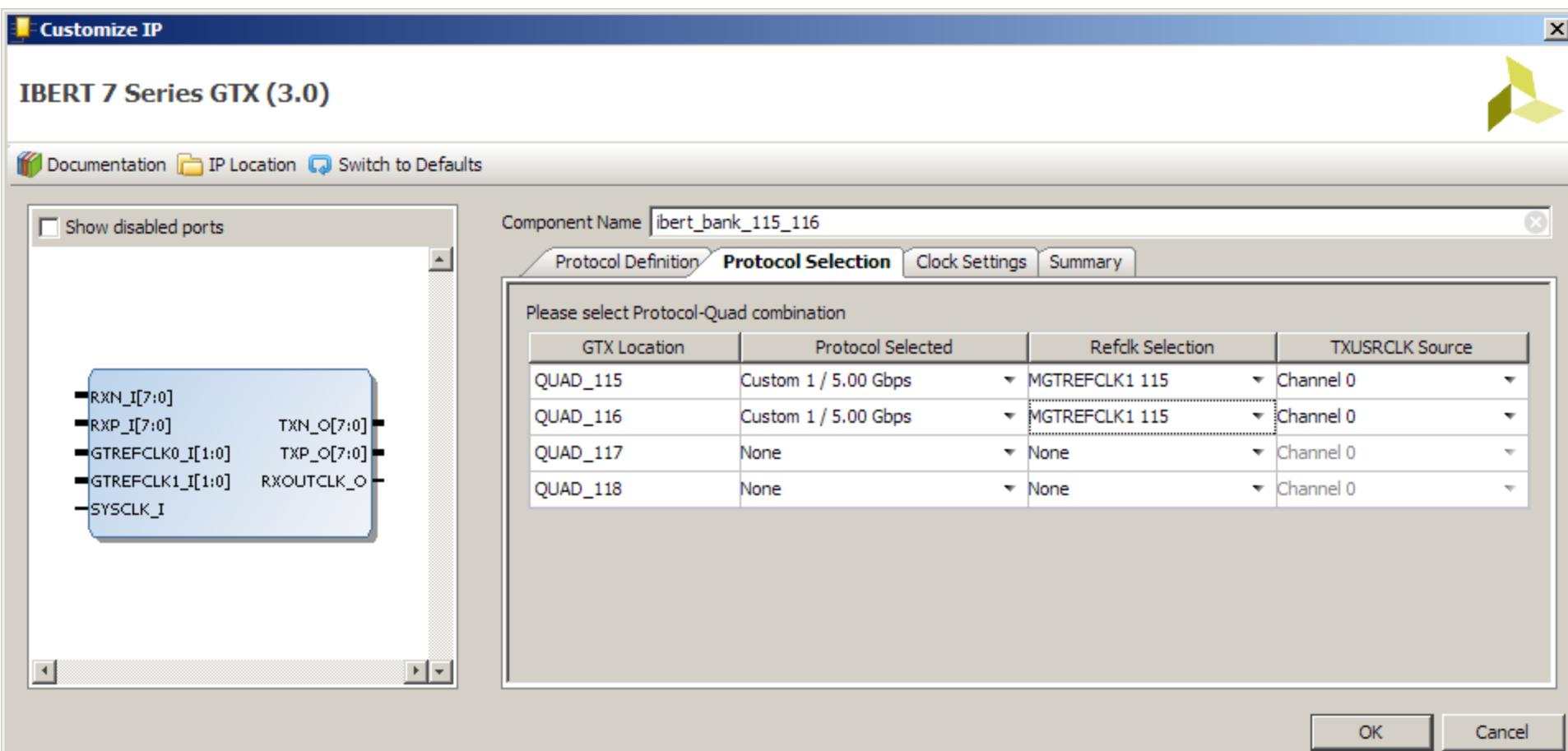
# Create IBERT Design for Banks 115, 116

- Set the Component name: **ibert\_bank\_115\_116**
- Under the Protocol Definition tab
  - Silicon Version: **General ES / Production**
  - Protocol: LineRate: **5.00**, DataWidth: **40** Refclk: **100.000** Quad Count: **2**



# Create IBERT Design for Banks 115, 116

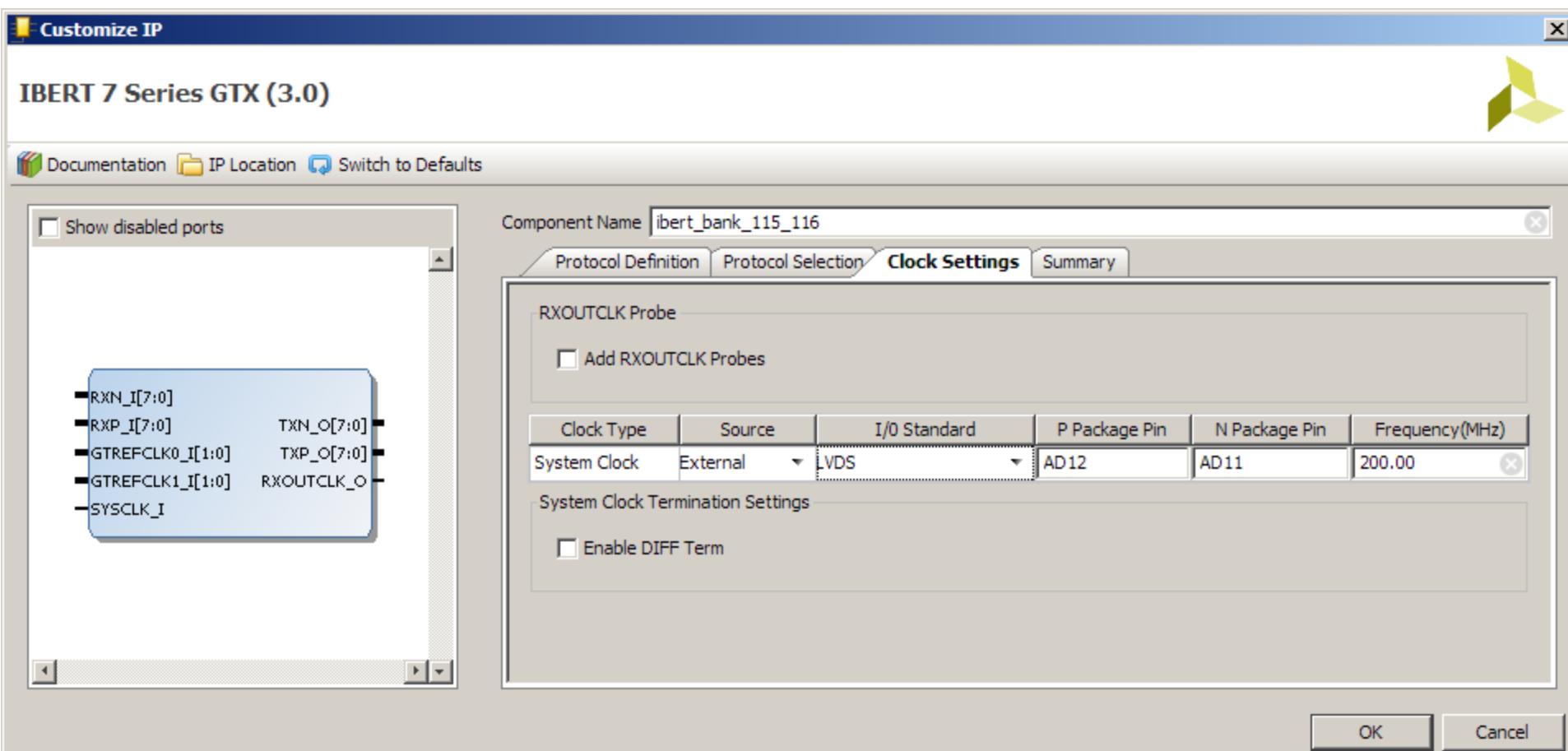
- Under the Protocol Selection tab
- Set QUAD\_115 and QUAD\_116 to
  - Custom 1 / 5.00 Gbps, and MGTREFCLK1 115



# Create IBERT Design for Banks 115, 116

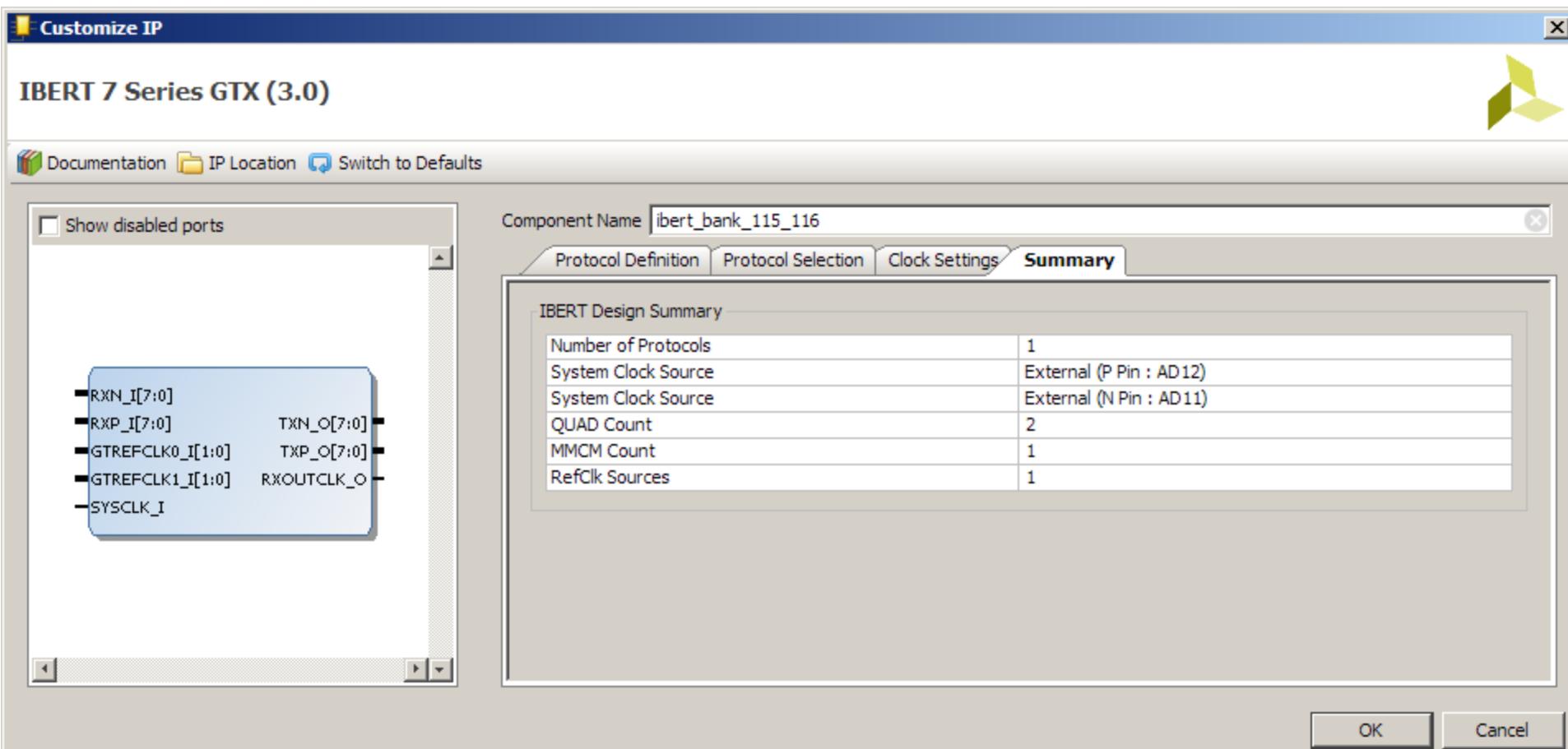
► Under the Clock Settings tab, set the System Clock:

- LVDS, P Pin Location: **AD12**, N Pin Location: **AD11**



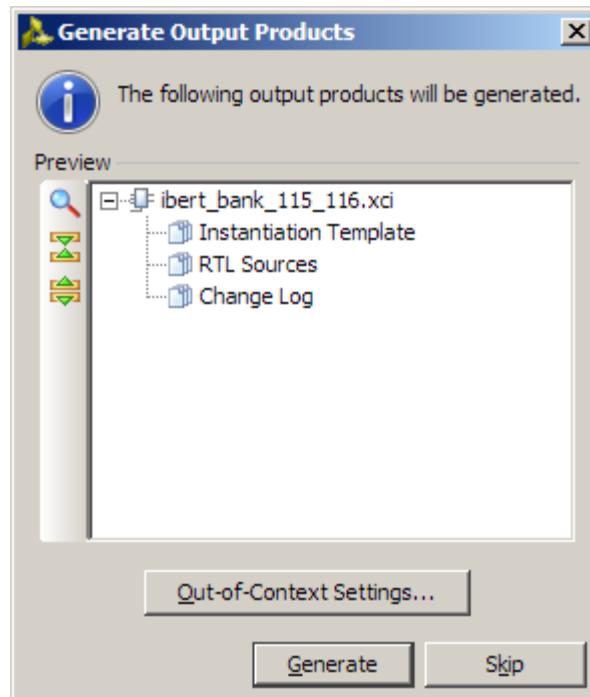
# Create IBERT Design for Banks 115, 116

► Review the summary and click OK



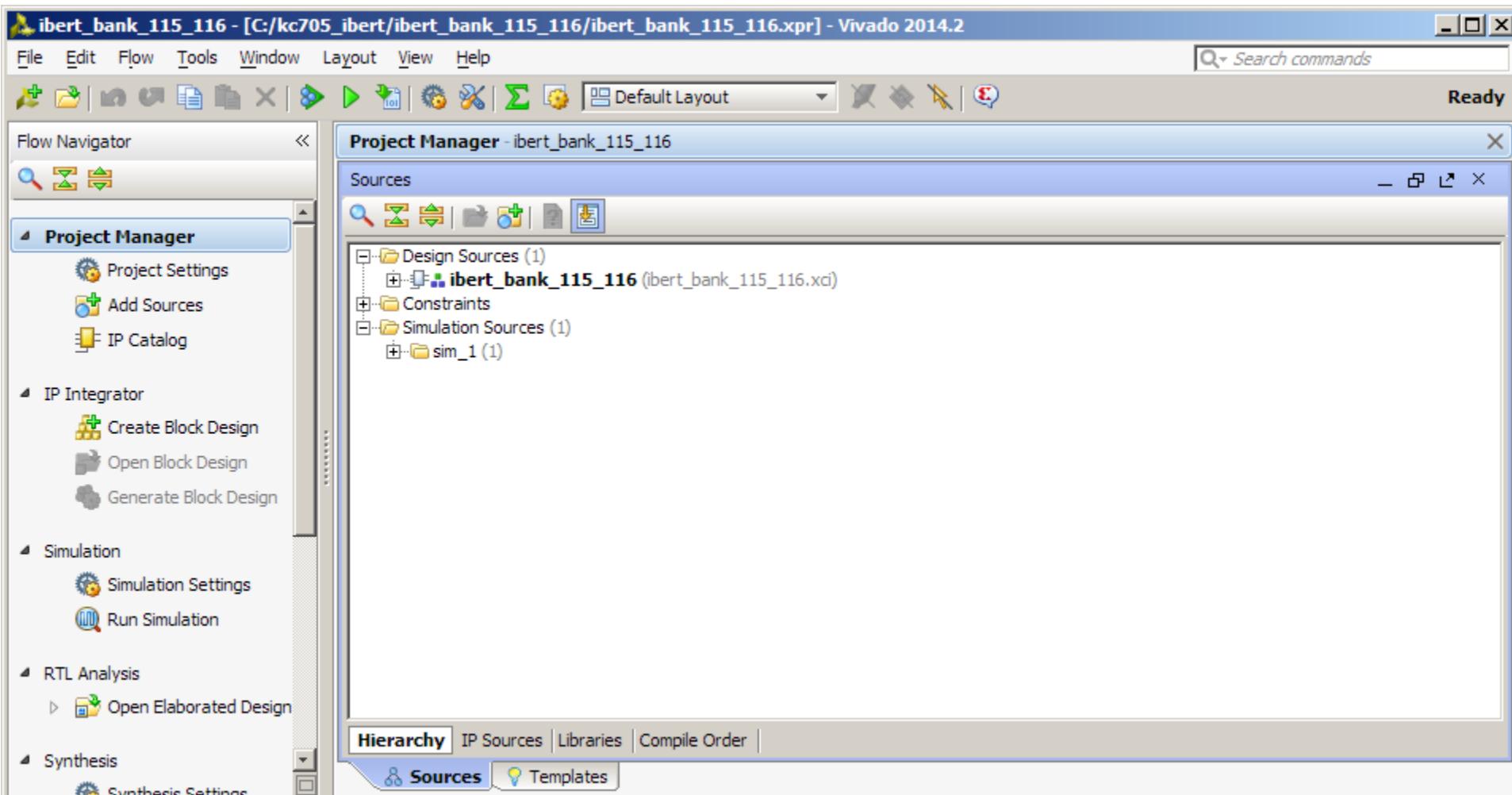
# Create IBERT Design for Banks 115, 116

► Click Generate



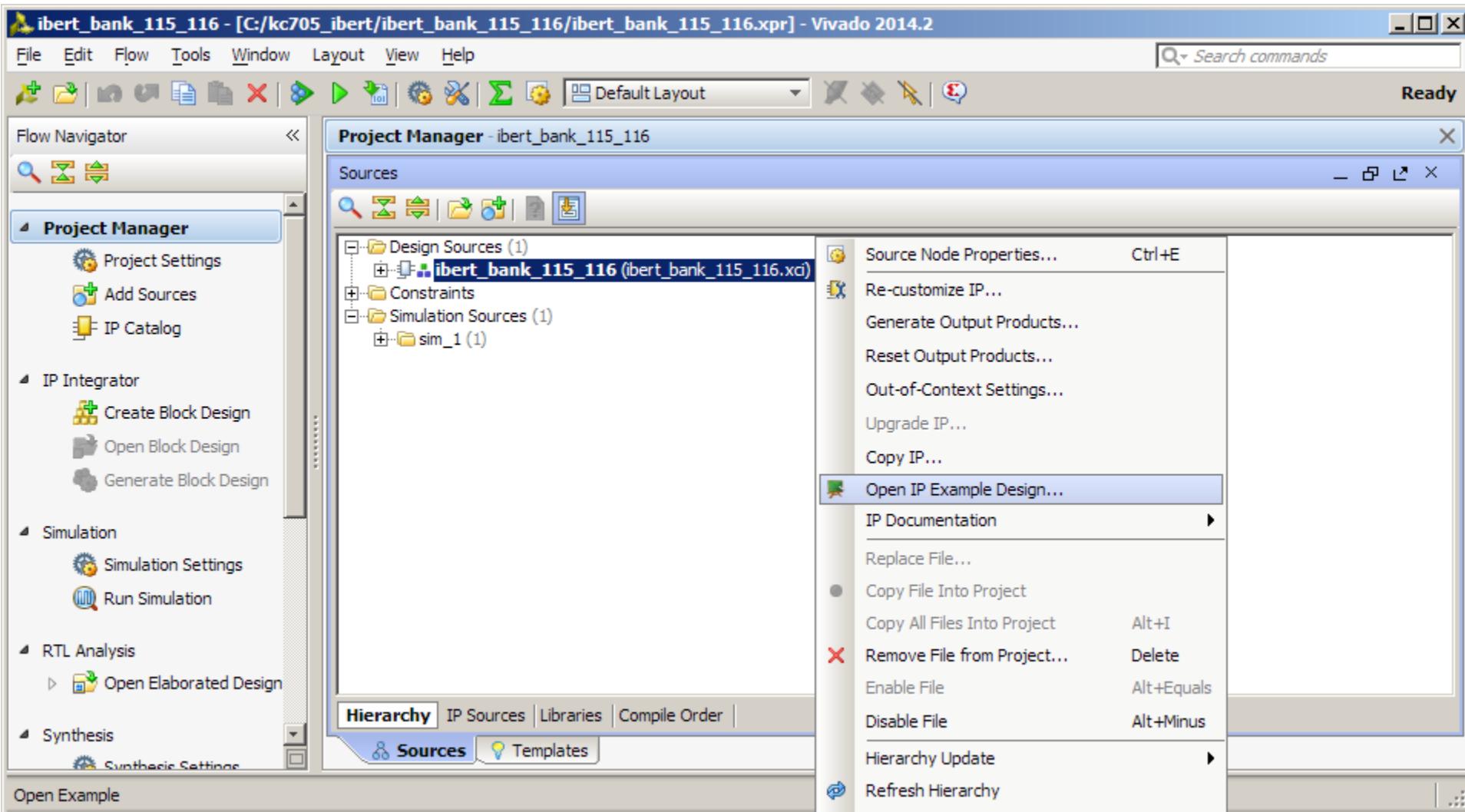
# Create IBERT Design for Banks 115, 116

► Bank 115 & 116 IBERT design appears in Design Sources



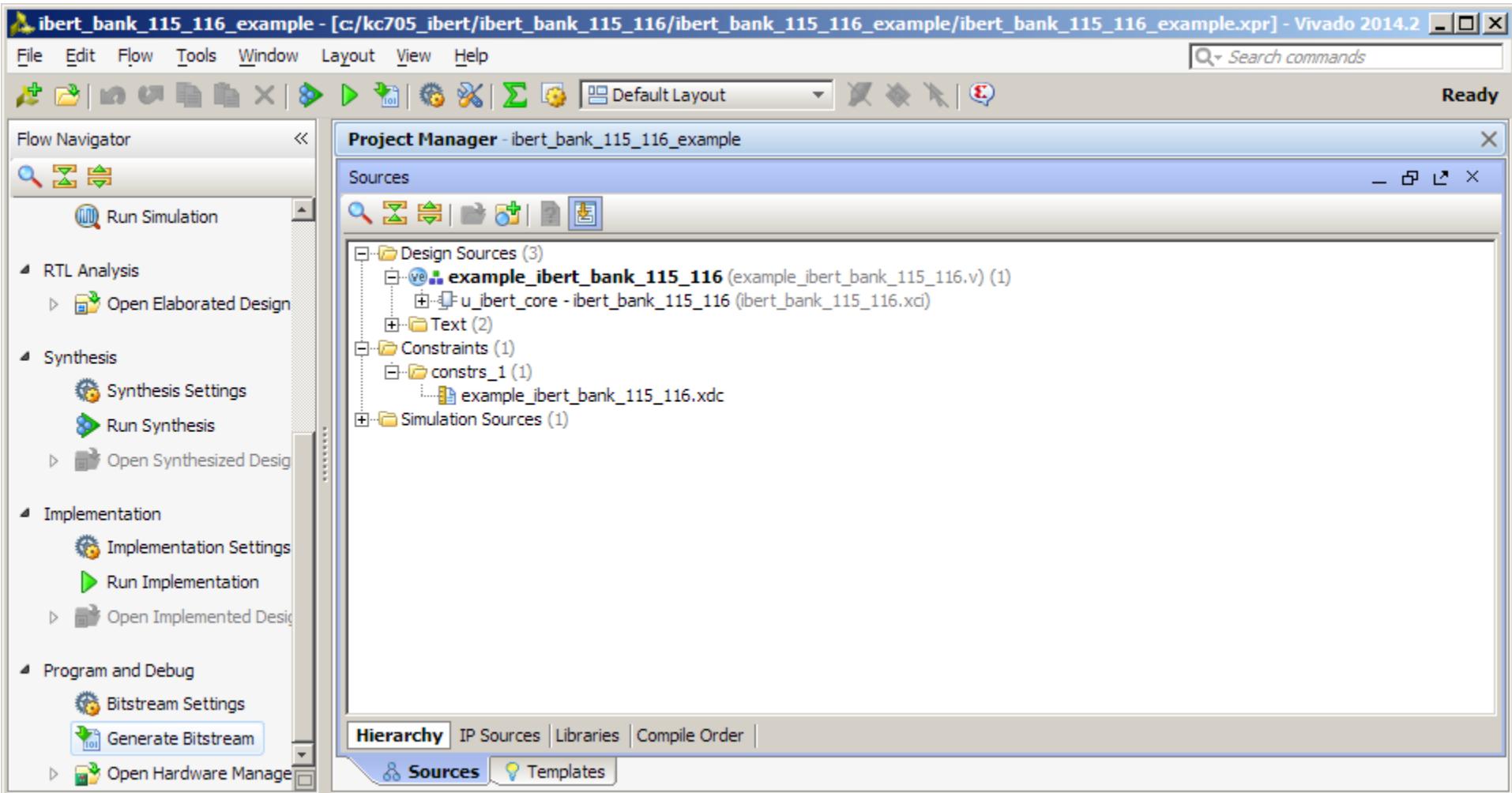
# Compile Example Design

- Right click on `ibert_bank_115_116` and select Open IP Example Design...



# Compile Example Design

- A new project is created under <design path>/
- Click Generate Bitstream



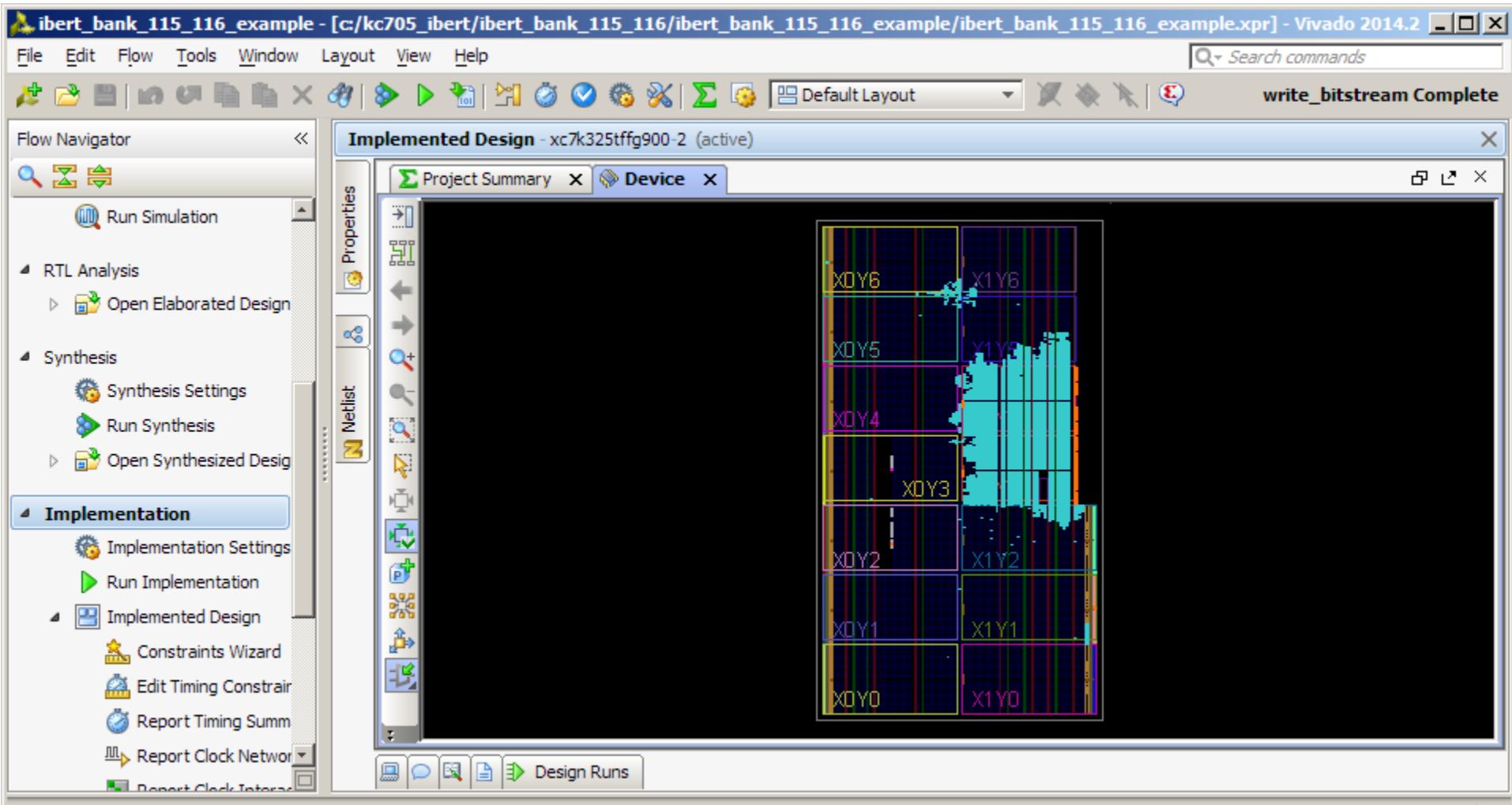
Generate a programming file after implementation

Note: The original project window can be closed

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# Compile Example Design

► Open and view the Implemented Design



## **Testing Banks 115 and 116 with Optional User Provided Hardware**

# Optional Testing with User Provided Hardware

## ► SMA Cables

- [www.rosenbergerna.com](http://www.rosenbergerna.com)
- Part number:  
72D-32S1-32S1-00610A



## ► SMA Quick connects

- RADIALL
- Part number: R125791501
- Available [here](#) or [here](#)

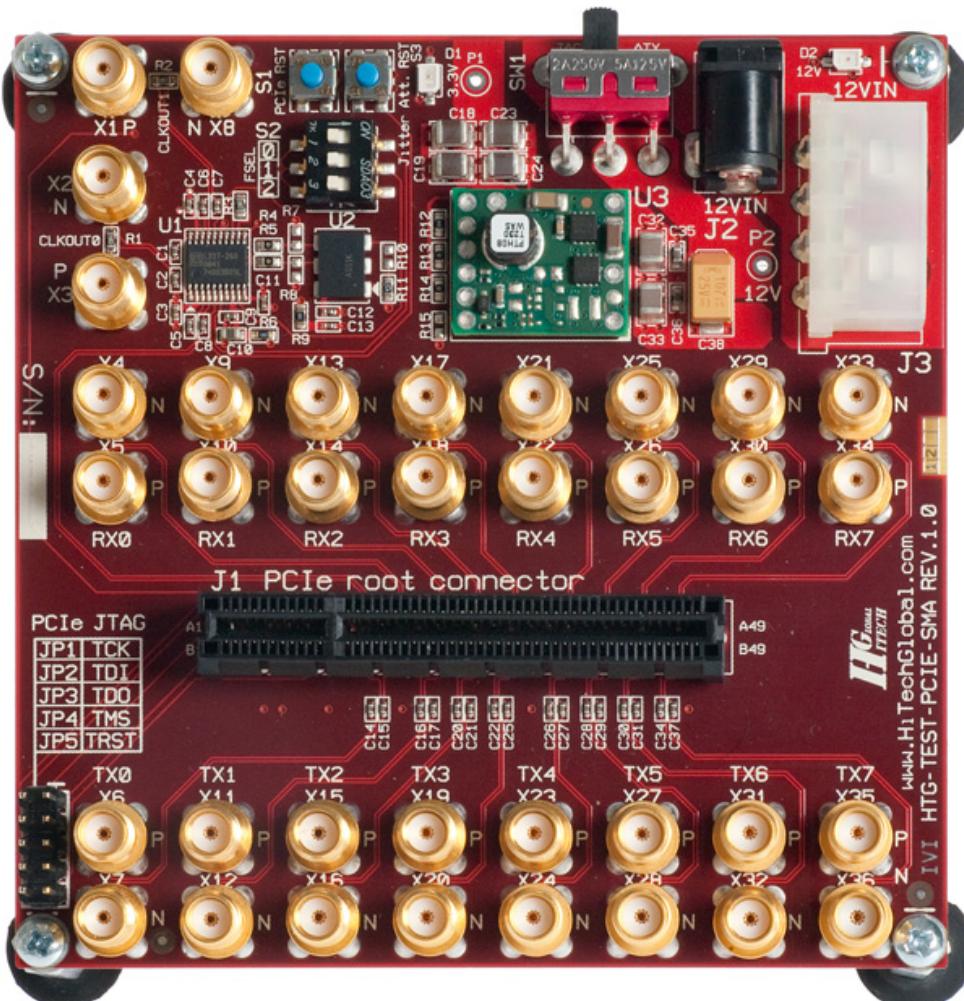


# Optional Testing with User Provided Hardware

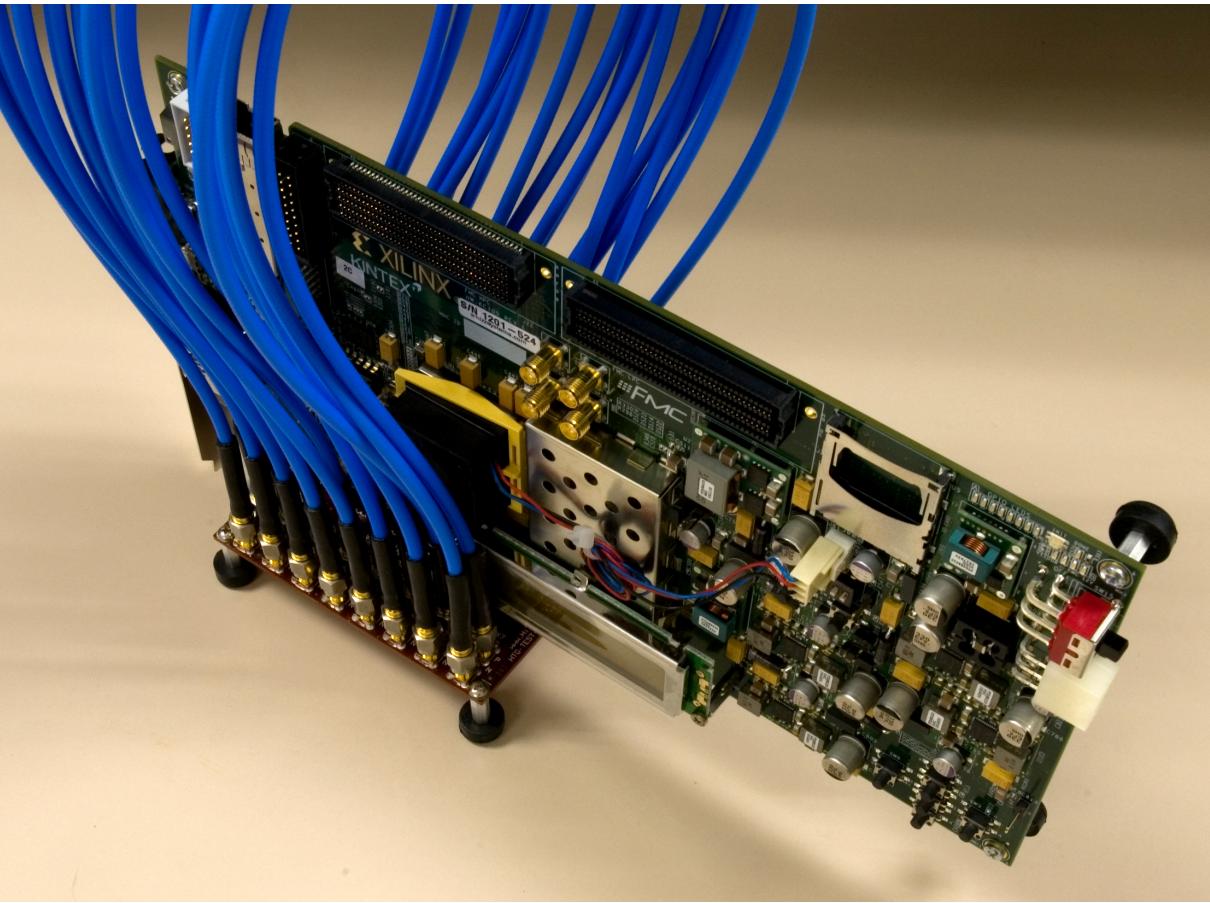
► For testing Banks 115 and 116:

► PCIe Testing Hardware:

- HiTechGlobal PCI Express Test & SerialIO Expansion Module
- [HTG-TEST-PCIE-SMA](#)
- 16 SMA cables required
- Requires power supply, either:
  - 4-pin Peripheral power connector from ATX power supply
- Or:
  - HiTechGlobal [PWR-12V-6A](#)



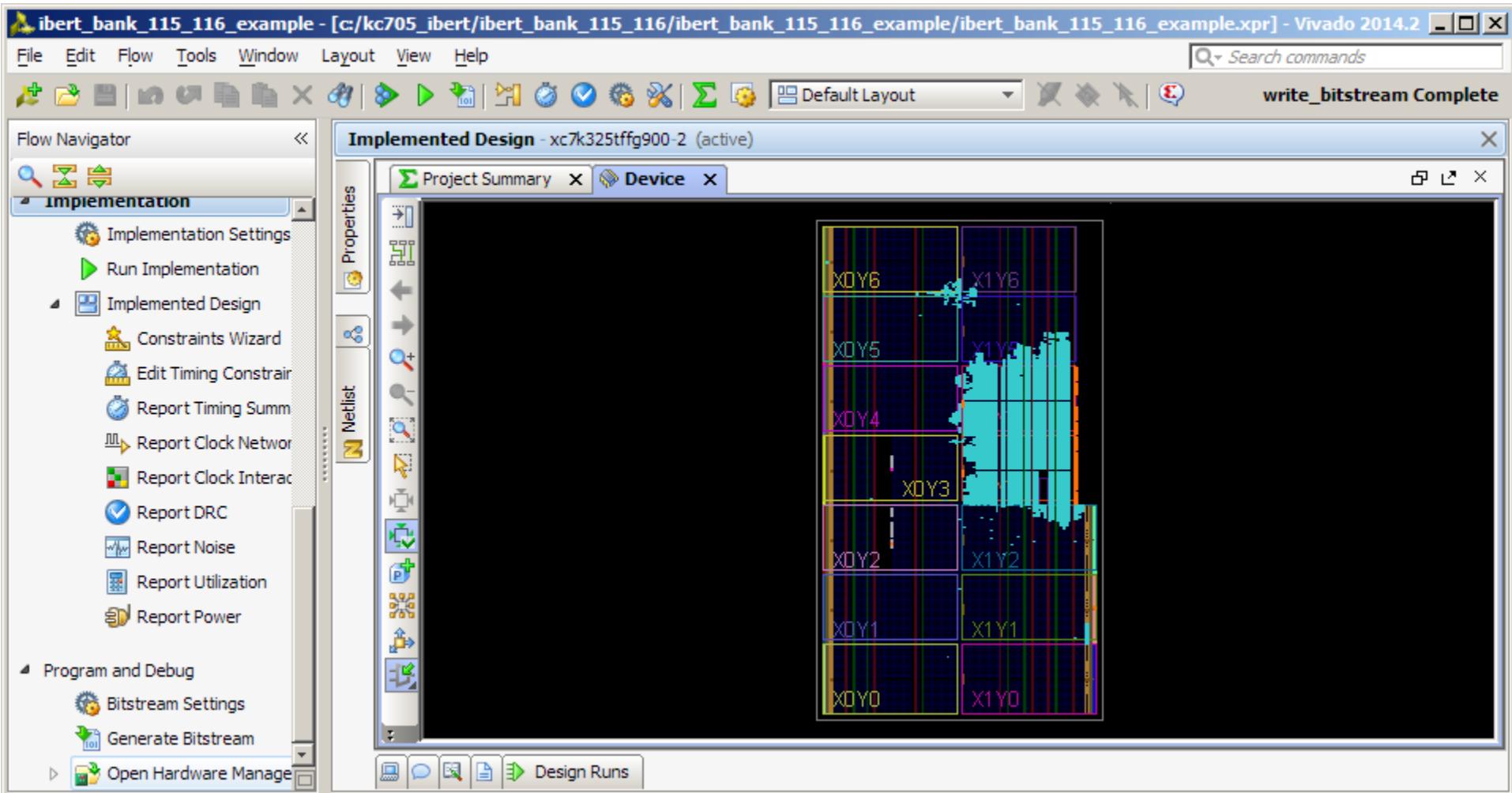
# Testing Banks 115 and 116 with Optional User Provided Hardware



- **Connect SMA Cables:**
  - TX0 P/N to RX0 P/N,
  - TX1 P/N to RX1 P/N,
  - etc.
- **Insert KC705 into PCIe slot**
- **Connect the KC705 and HiTechGlobal power supplies**
- **Power up the KC705 and HiTechGlobal boards**

# Run IBERT Example Design

► Click Open Hardware Manager



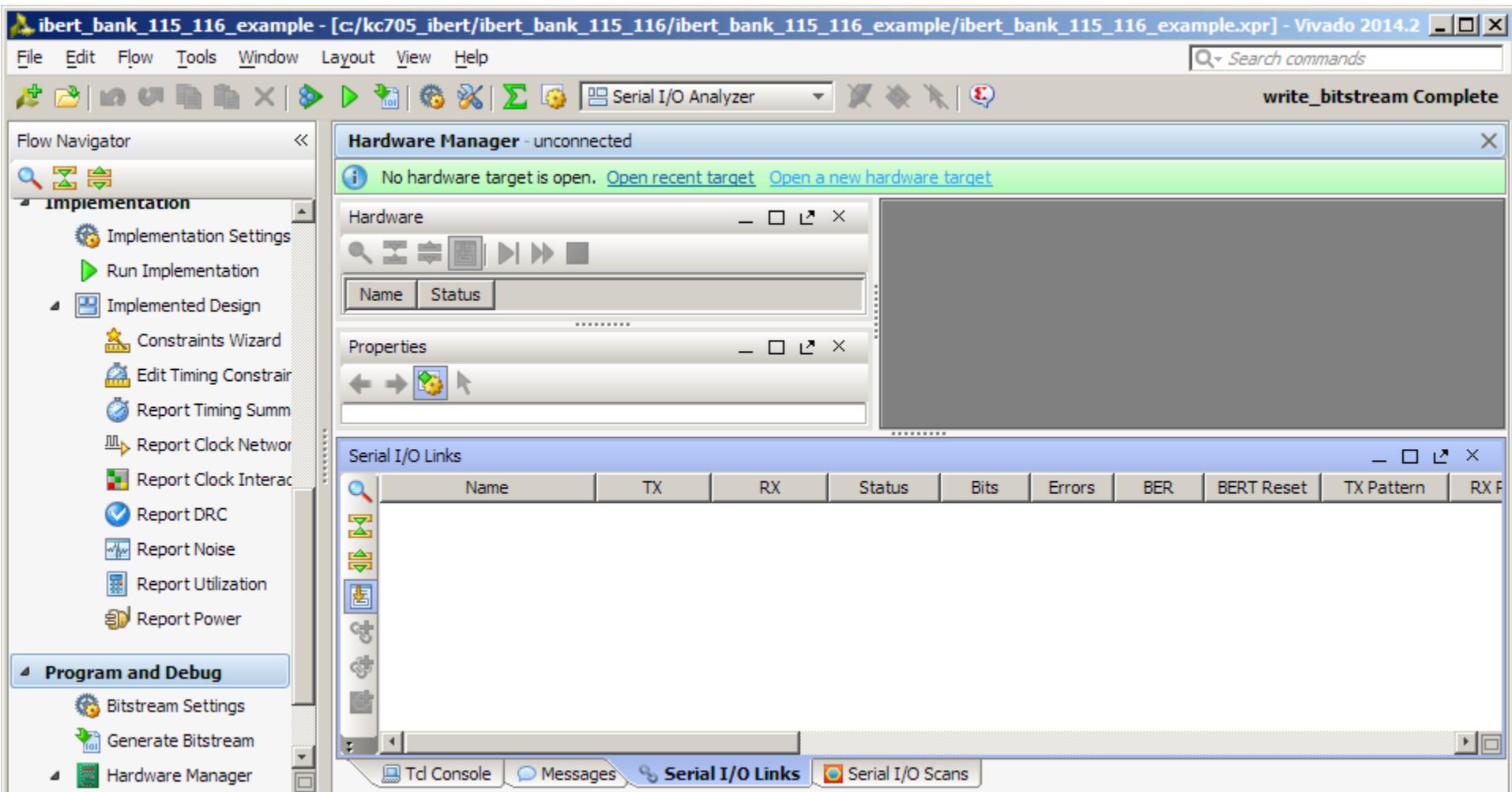
Open the hardware program and debug manager

Note: Presentation applies to the KC705

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# Run IBERT Example Design

► Click Open a new hardware target



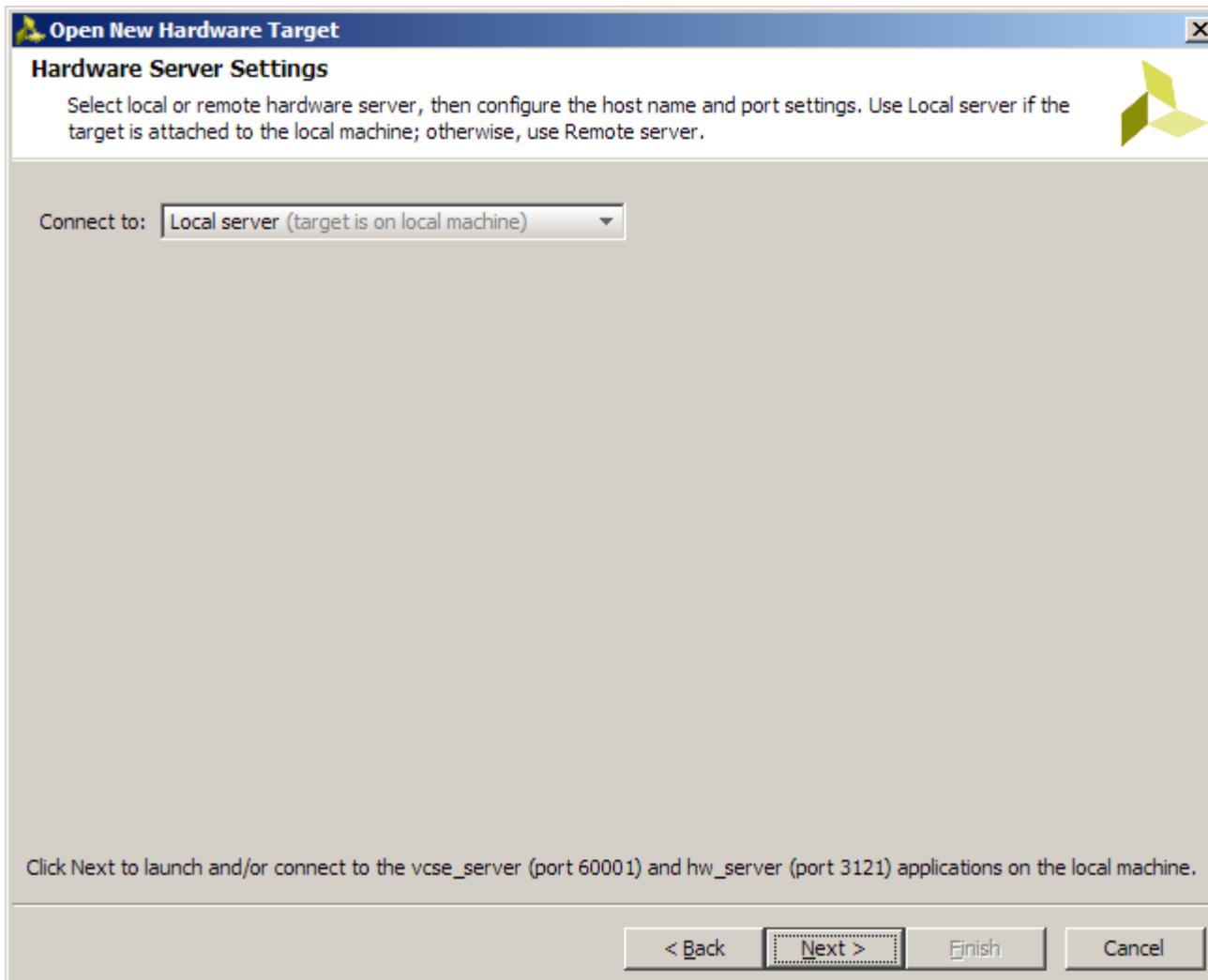
# Run IBERT Example Design

► Click Next



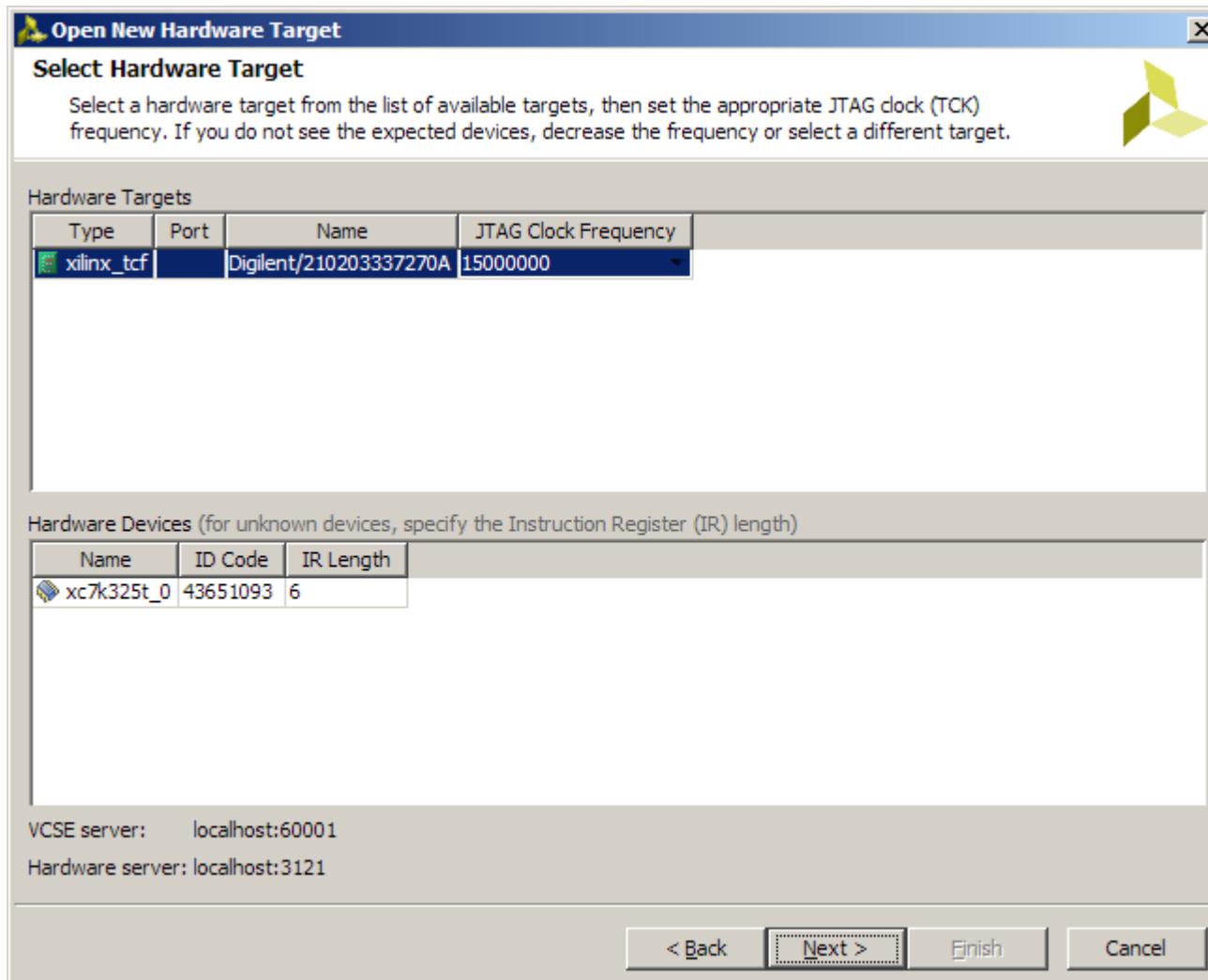
# Run IBERT Example Design

► Click Next



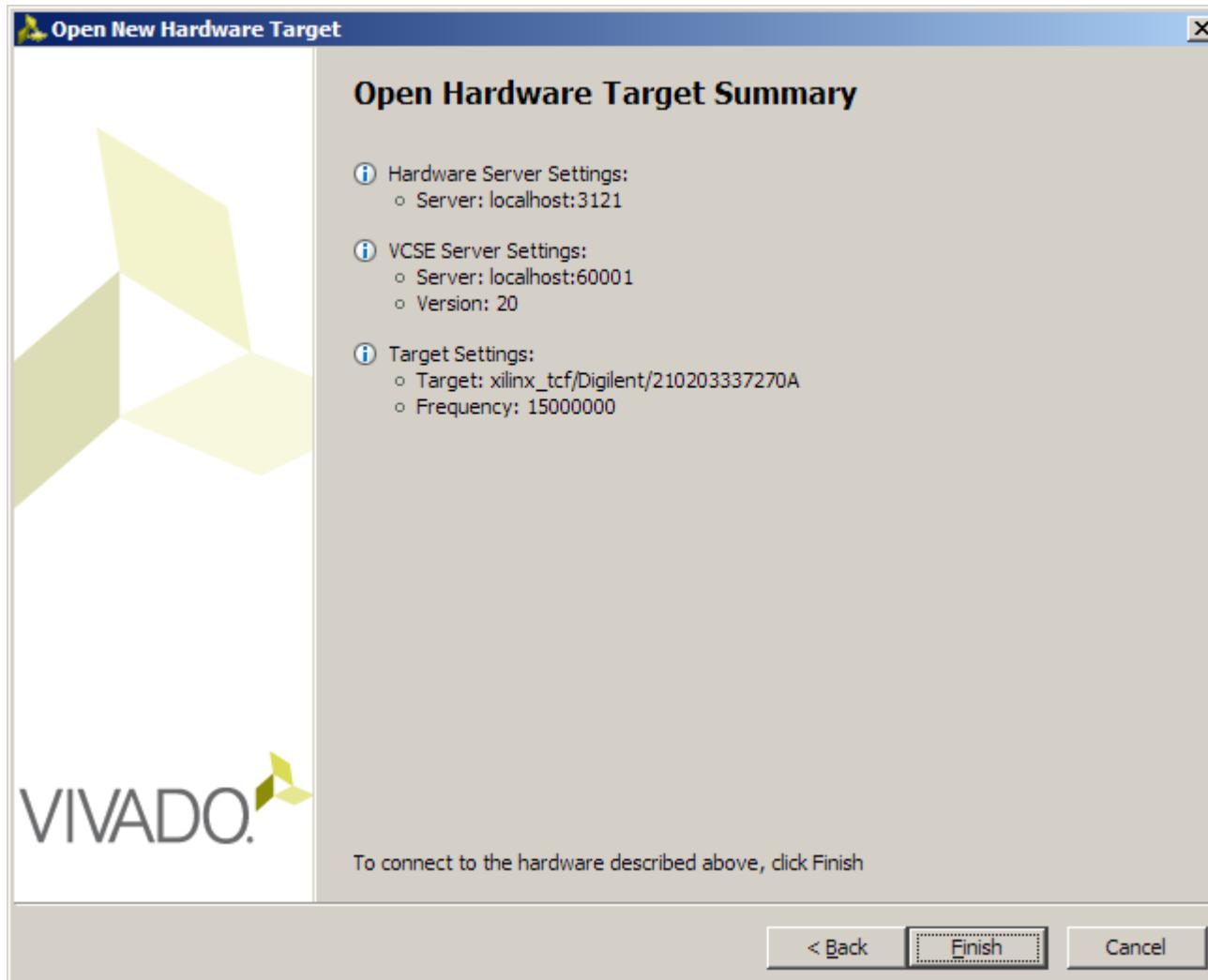
# Run IBERT Example Design

► Click Next



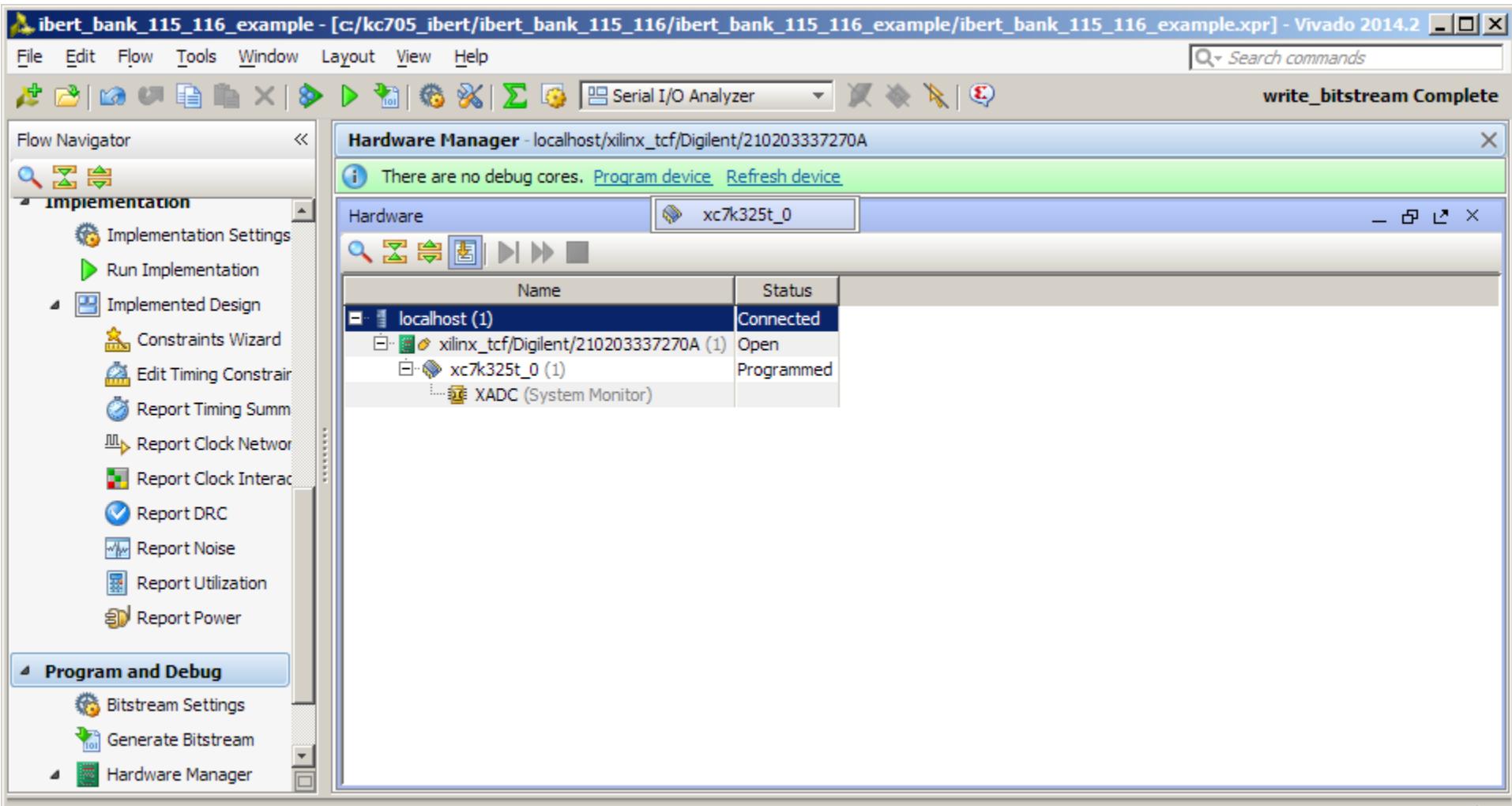
# Run IBERT Example Design

► Click Finish



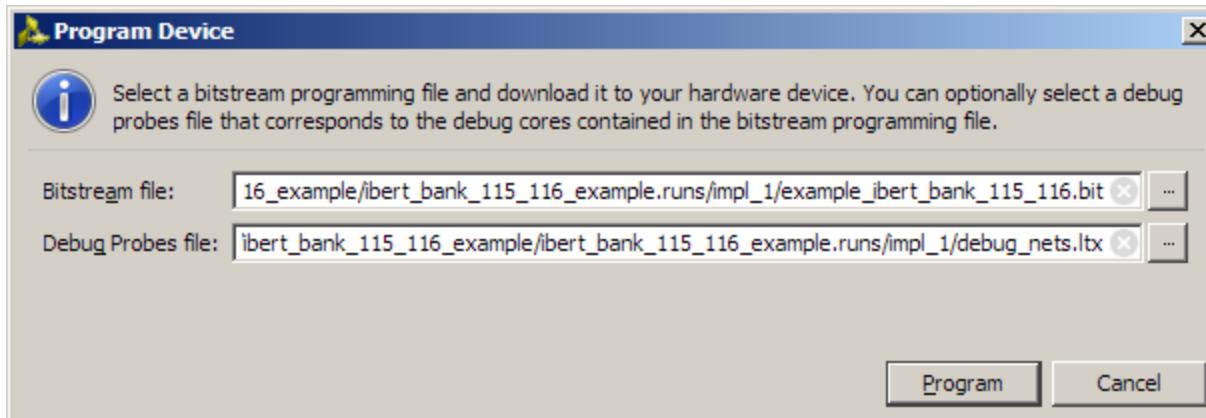
# Run IBERT Example Design

► Select Program device → xc7k325t\_0



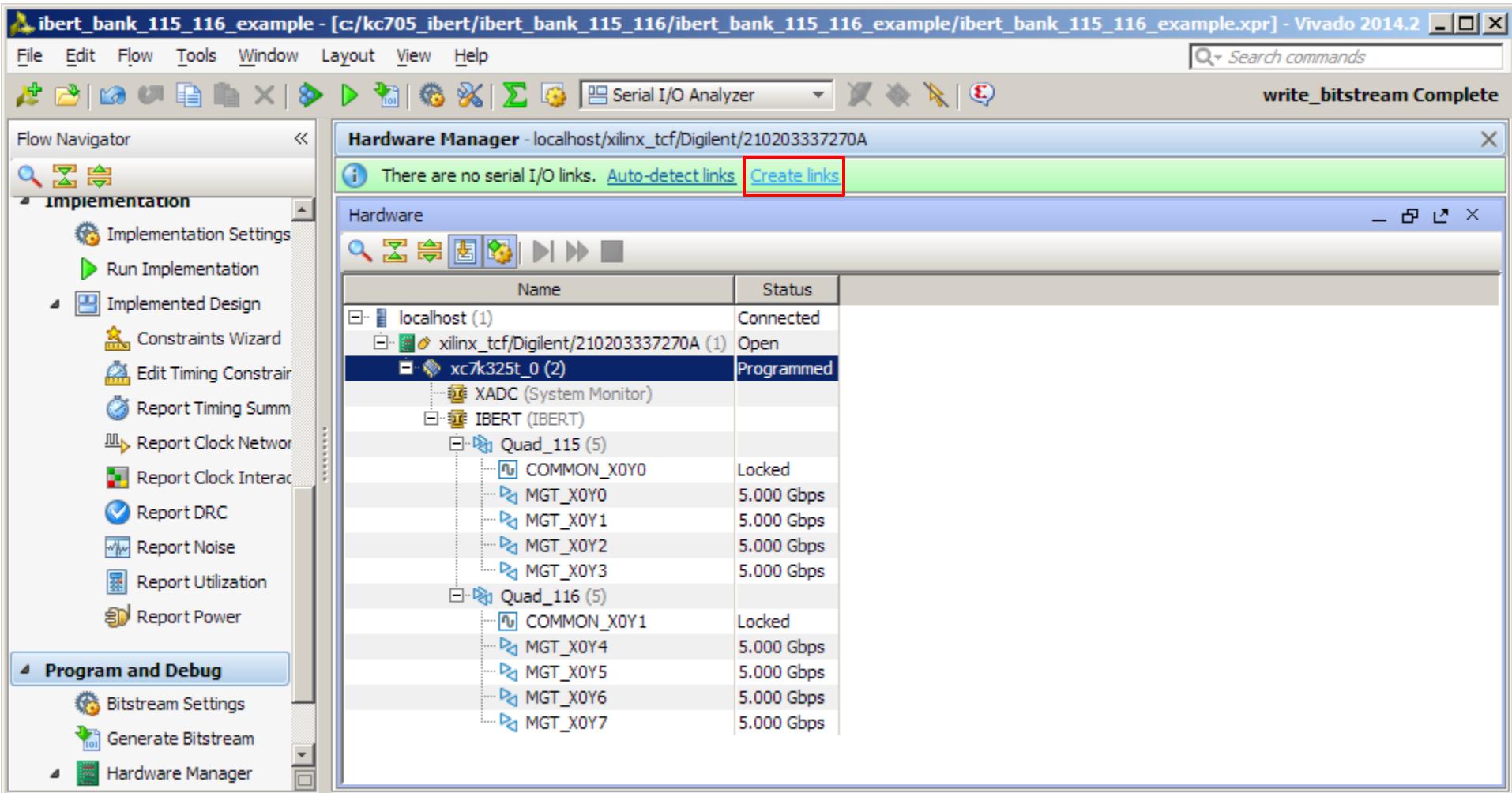
# Run IBERT Example Design

- The newly created bitstream is default
- Click Program



# Run IBERT Example Design

► Click Create links

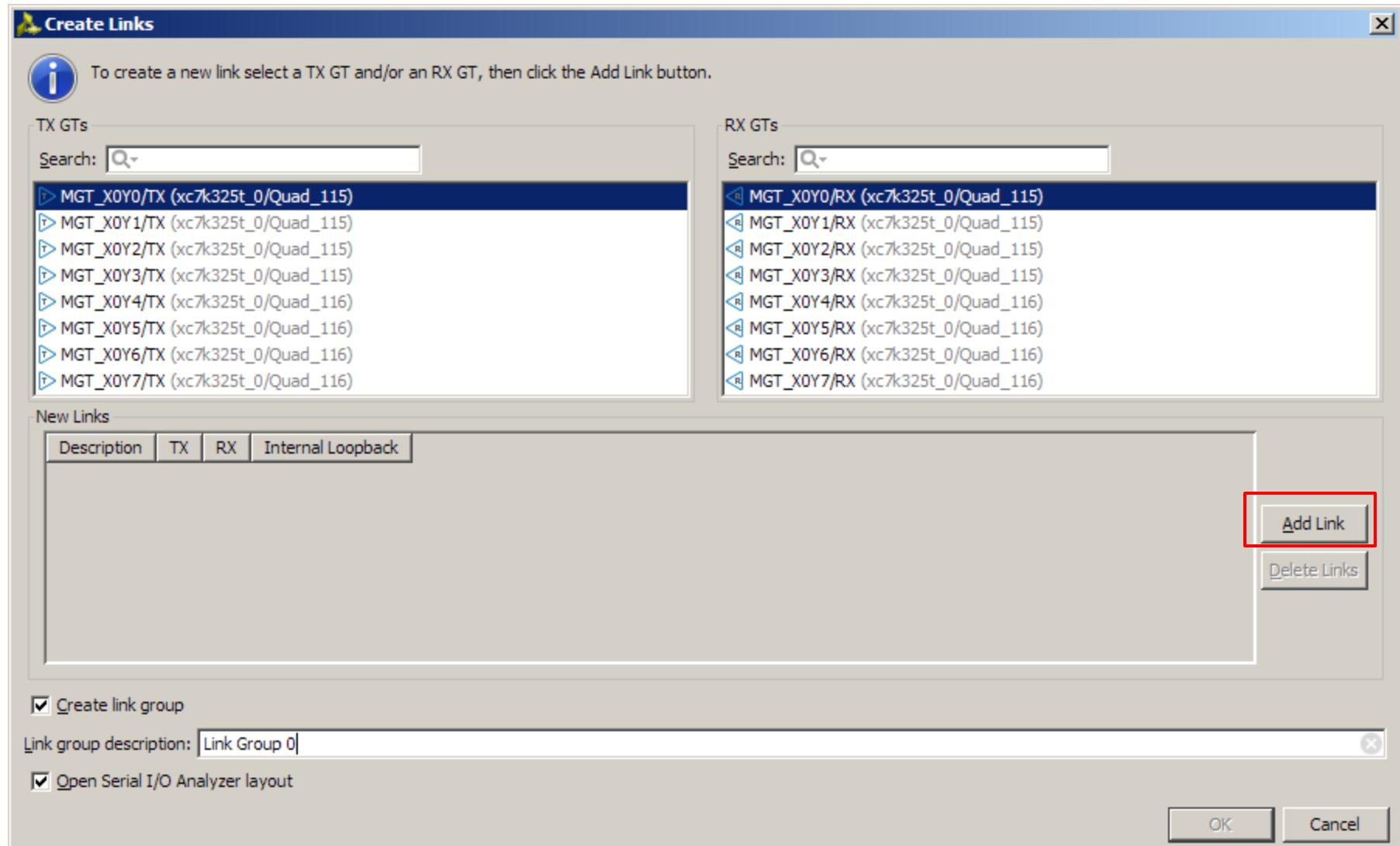


Note: Set to Serial I/O Analyzer layout

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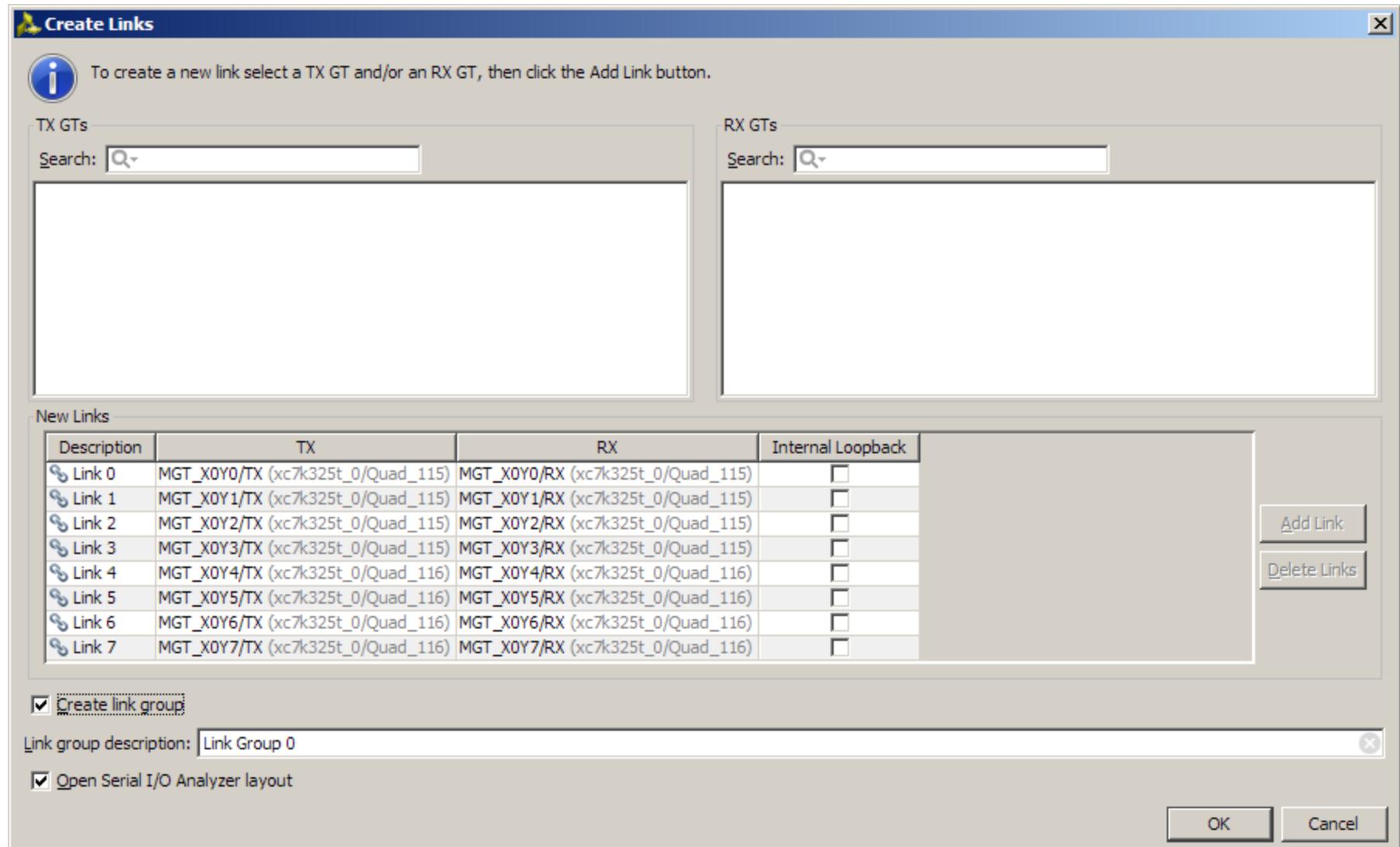
# Run IBERT Example Design

► Click on the Add Link button until all the MGT pairs are “linked”



# Run IBERT Example Design

► Click OK



# Run IBERT Example Design

► Select the Link Group 0 TX Pattern and set to PRBS 31-bit

The screenshot shows the Vivado 2014.2 Hardware Manager interface for the "ibert\_bank\_115\_116\_example" project. The main window displays the "Serial I/O Links" configuration table. The table has columns for Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, RX Pattern, TX Pre-Cursor, and TX Post-Cursor. The TX Pattern column for Link Group 0 is currently set to "PRBS 7-bit". The TX Pattern for Link 0 is highlighted in blue, indicating it is selected for modification. The TX Pattern dropdown menu for Link 0 shows "PRBS 31-bit" as an available option.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor
Ungrouped Links (0)											
Link Group 0 (8)							Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	5.000 Gbps	6.784E11	0E0	1.474E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	5.000 Gbps	6.786E11	0E0	1.474E-12	Reset	PRBS 15-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	5.000 Gbps	6.789E11	0E0	1.473E-12	Reset	PRBS 23-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	5.000 Gbps	6.791E11	0E0	1.473E-12	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	5.000 Gbps	6.793E11	0E0	1.472E-12	Reset	Fast Clk	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	5.000 Gbps	6.796E11	0E0	1.471E-12	Reset	Slow Clk	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	5.000 Gbps	6.798E11	0E0	1.471E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	5.000 Gbps	6.8E11	0E0	1.471E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB

# Run IBERT Example Design

- Now all eight links are set to a TX Pattern of PRBS 31-bit
- Repeat with the RX Pattern

The screenshot shows the Vivado 2014.2 Hardware Manager interface for the 'ibert\_bank\_115\_116\_example' project. The main window displays the 'Serial I/O Links' configuration table. The table has columns for Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, RX Pattern, TX Pre-Cursor, and TX Po. There are 8 rows representing Link Group 0, each corresponding to a MGT\_X0Yx pair. All links are currently set to 'No Link'. The TX and RX columns show the component names (e.g., MGT\_X0Y0/TX, MGT\_X0Y0/RX). The TX Pattern column is set to 'PRBS 31-bit' for all links. The RX Pattern column is set to 'PRBS 7-bit'. The BER values range from 4.143E-2 to 4.483E-2. The BERT Reset column contains 'Reset' buttons for each link. The TX Pre-Cursor and TX Po columns have dropdown menus. The bottom navigation bar shows tabs for Td Console, Messages, Serial I/O Links (which is selected), and Serial I/O Scans.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Po
Ungrouped Links (0)											
Link Group 0 (8)											
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	No Link	7.674E11	3.44E10	4.483E-2	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	No Link	7.676E11	3.45E10	4.494E-2	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	No Link	7.678E11	3.459E10	4.505E-2	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	No Link	7.681E11	3.471E10	4.52E-2	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	No Link	7.684E11	3.486E10	4.537E-2	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	No Link	7.618E11	3.156E10	4.143E-2	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	No Link	7.62E11	3.165E10	4.153E-2	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	No Link	7.622E11	3.174E10	4.164E-2	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB

# Run IBERT Example Design

- Now all eight links are set to a RX Pattern of PRBS 31-bit
- Click the BERT Reset button for Link Group 0 to reset all eight links

The screenshot shows the Vivado Hardware Manager interface for the 'ibert\_bank\_115\_116\_example' project. The main window displays a table of Serial I/O Links. The columns include Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, RX Pattern, TX Pre-Cursor, and TX Po. The 'BERT Reset' column for Link Group 0 is highlighted with a red box. The 'Reset' button in this row is also highlighted with a red box.

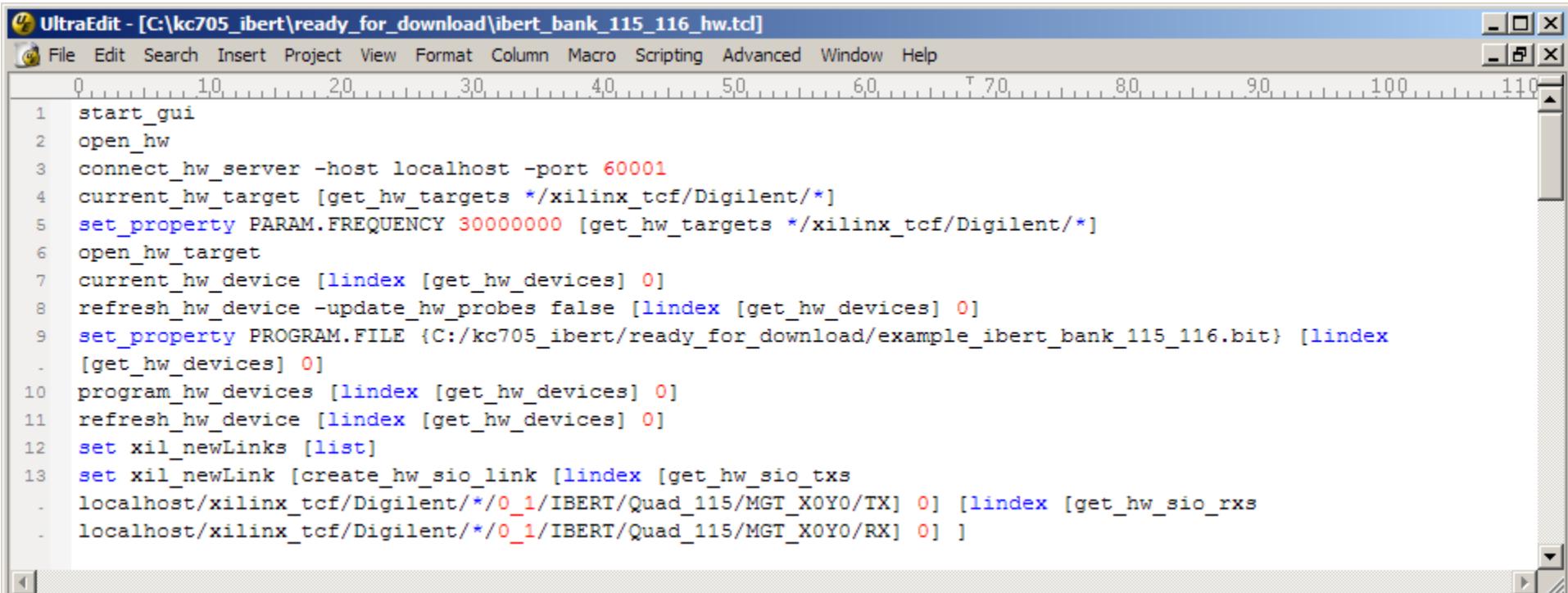
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Po
Ungrouped Links (0)											
Link Group 0 (8)							Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	5.000 Gbps	2.358E10	0E0	4.241E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	5.000 Gbps	2.379E10	0E0	4.204E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	5.000 Gbps	2.398E10	0E0	4.169E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	5.000 Gbps	2.418E10	0E0	4.136E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	5.000 Gbps	2.437E10	0E0	4.104E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	5.000 Gbps	2.455E10	0E0	4.073E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	5.000 Gbps	2.478E10	0E0	4.036E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	5.000 Gbps	2.496E10	0E0	4.007E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB

Note: Close the Vivado GUI when finished

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# Run IBERT Example Design

- The Hardware Manager actions are captured in the Vivado JOU file as Tcl commands; these can be used for scripting this test
- Review ready\_for\_download/ibert\_bank\_115\_116\_hw.tcl for an example of this



The screenshot shows a window titled "UltraEdit - [C:\kc705\_ibert\ready\_for\_download\ibert\_bank\_115\_116\_hw.tcl]" containing a Tcl script. The script performs several actions to prepare and program an FPGA target:

```
1 start_gui
2 open_hw
3 connect_hw_server -host localhost -port 60001
4 current_hw_target [get_hw_targets */xilinx_tcf/Digilent/*]
5 set_property PARAM.FREQUENCY 30000000 [get_hw_targets */xilinx_tcf/Digilent/*]
6 open_hw_target
7 current_hw_device [lindex [get_hw_devices] 0]
8 refresh_hw_device -update_hw_probes false [lindex [get_hw_devices] 0]
9 set_property PROGRAM.FILE {C:/kc705_ibert/ready_for_download/example_ibert_bank_115_116.bit} [lindex
. [get_hw_devices] 0]
10 program_hw_devices [lindex [get_hw_devices] 0]
11 refresh_hw_device [lindex [get_hw_devices] 0]
12 set xil_newLinks [list]
13 set xil_newLink [create_hw_sio_link [lindex [get_hw_sio_txs
. localhost/xilinx_tcf/Digilent/*/0_1/IBERT/Quad_115/MGT_XOYO/TX] 0] [lindex [get_hw_sio_rx
. localhost/xilinx_tcf/Digilent/*/0_1/IBERT/Quad_115/MGT_XOYO/RX] 0] ]
```



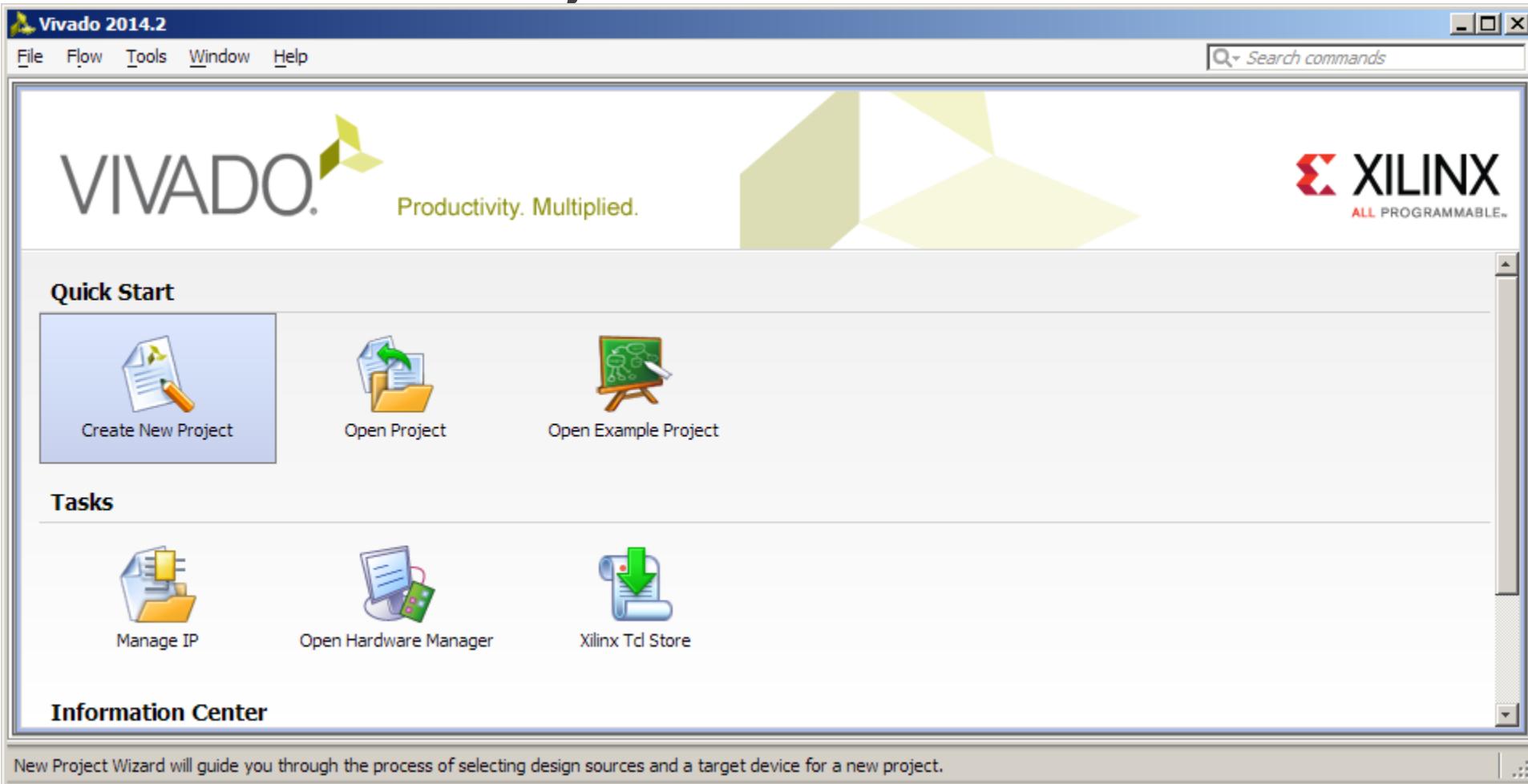
**Create IBERT Design for Banks 117, 118**

# Create IBERT Design for Banks 117, 118

## ► Open Vivado

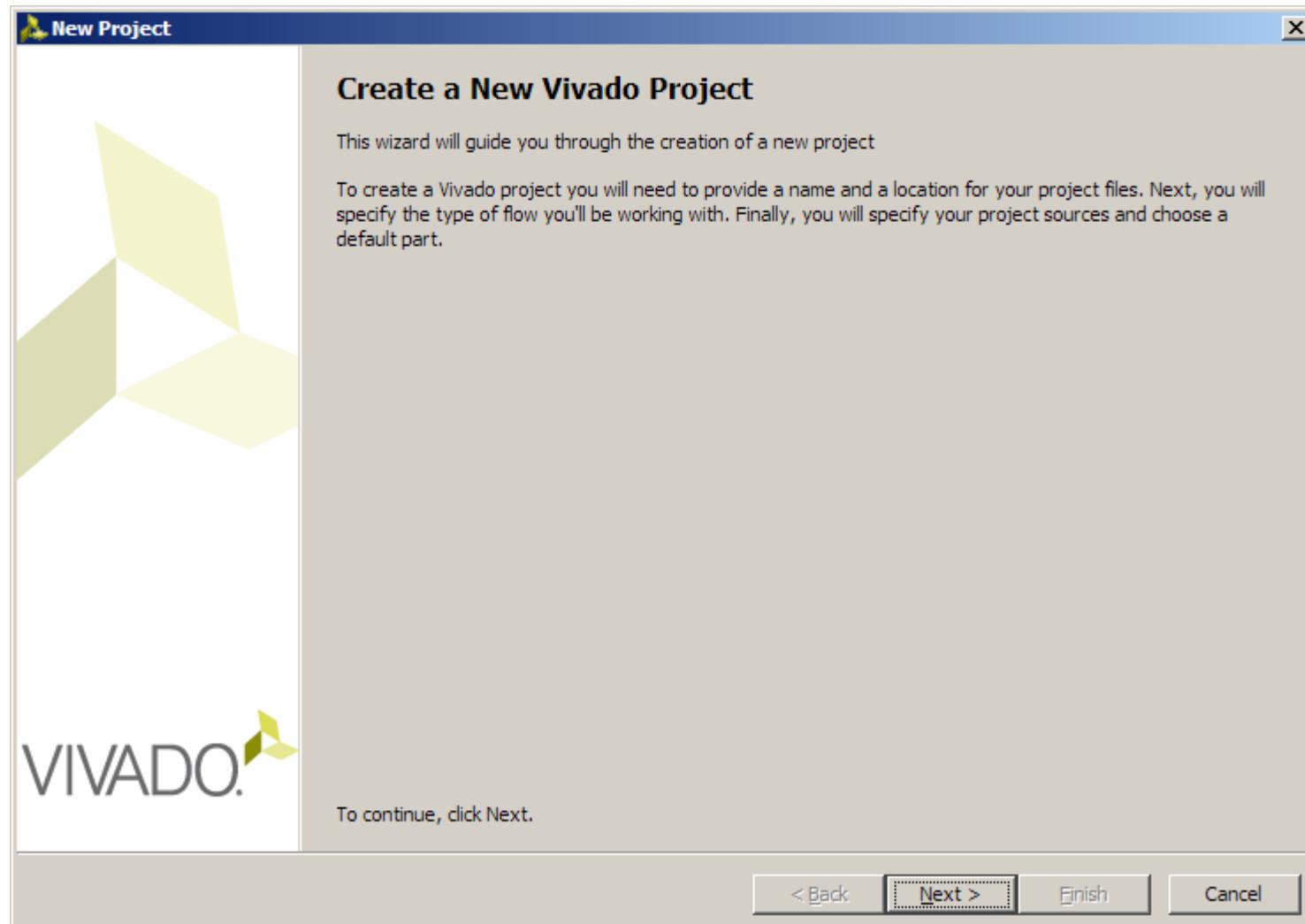
Start → All Programs → Xilinx Design Tools → Vivado 2014.2 → Vivado

## ► Select Create New Project



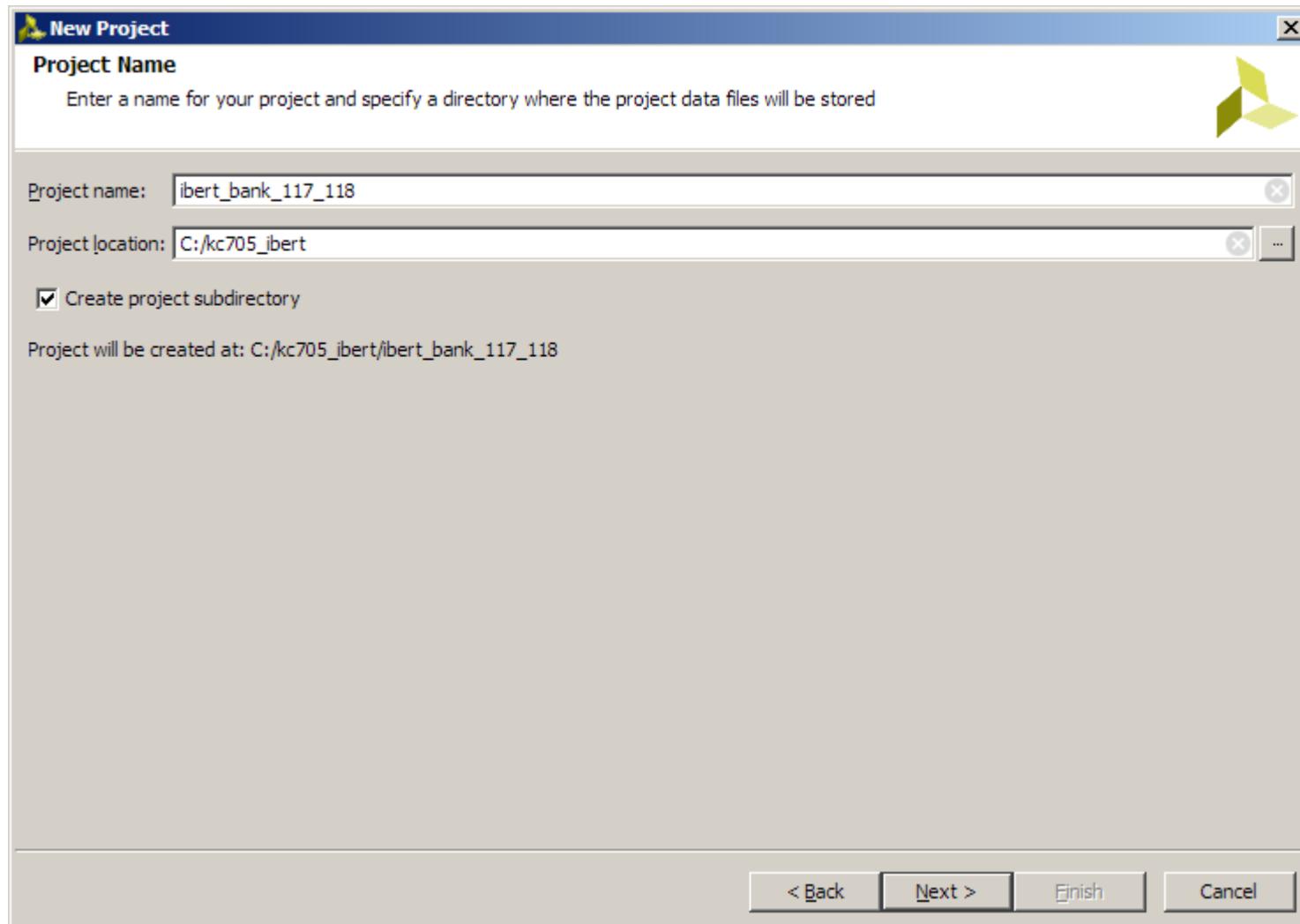
# Create IBERT Design for Banks 117, 118

► Click Next



# Create IBERT Design for Banks 117, 118

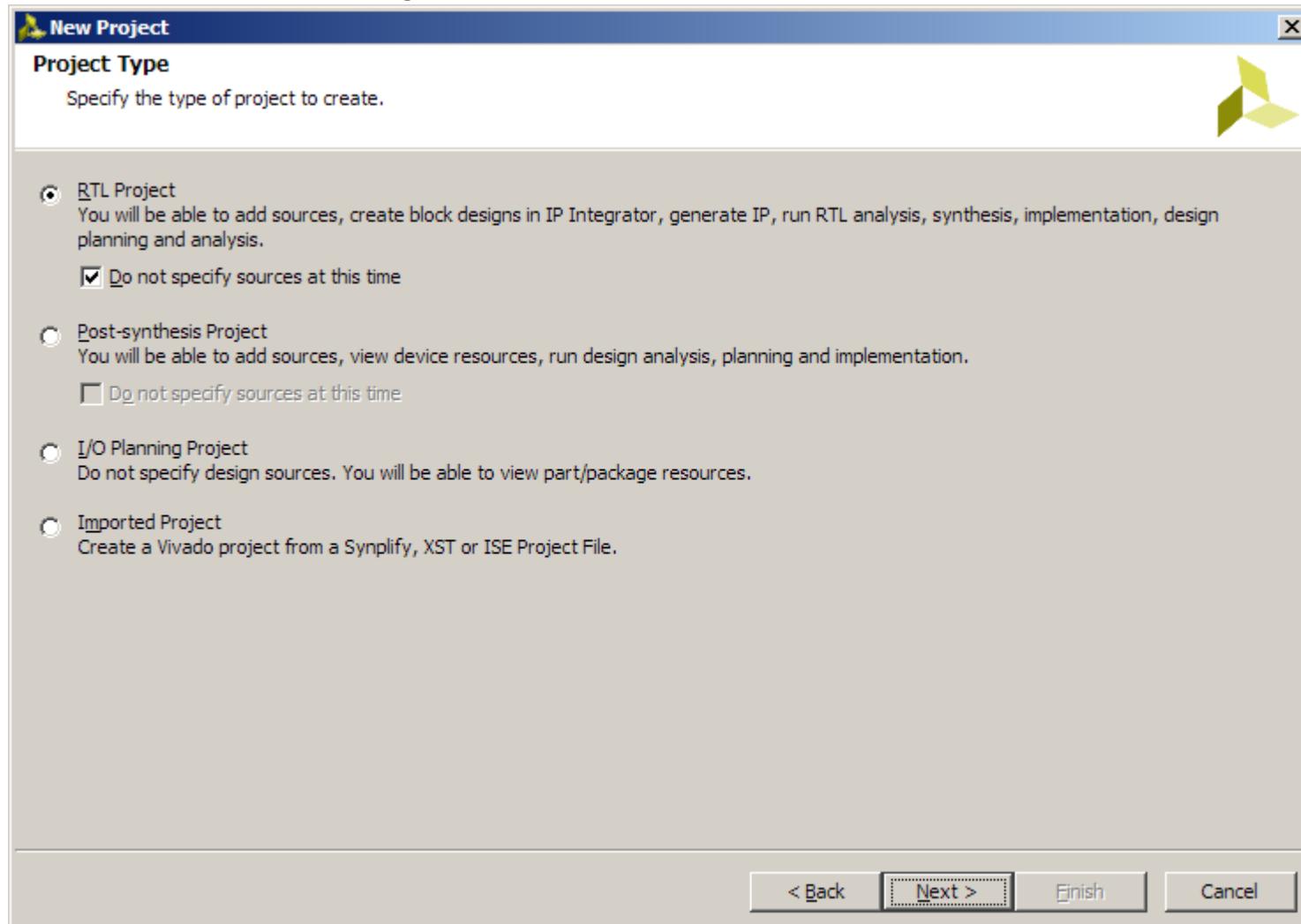
- Set the Project name and location to `ibert_bank_117_118` and `C:/kc705_ibert`; check Create project subdirectory



# Create IBERT Design for Banks 117, 118

## ► Select RTL Project

- Select **Do not specify sources at this time**



# Create IBERT Design for Banks 117, 118

## ► Select the KC705 Board

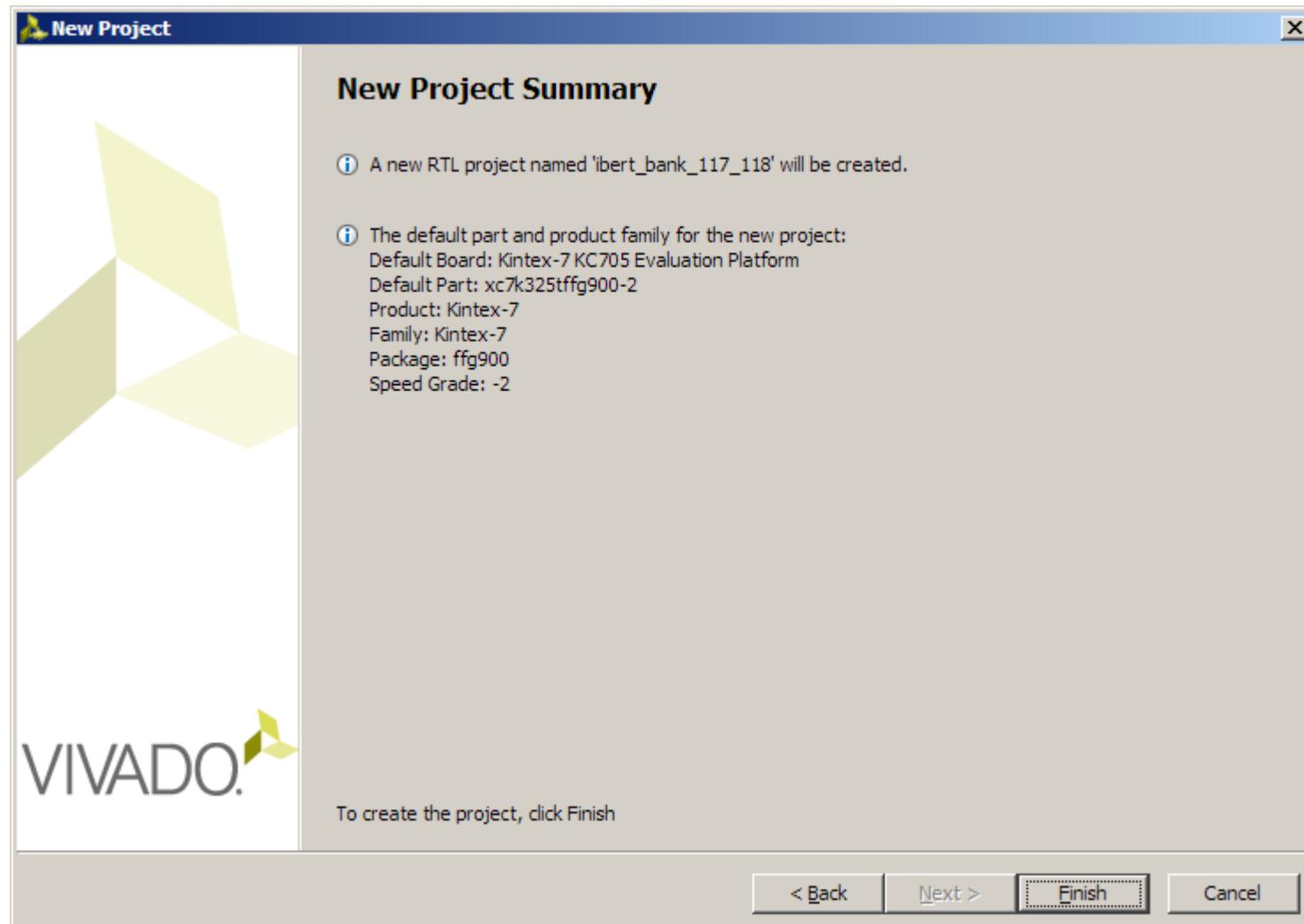
The screenshot shows the 'New Project' dialog box with the title 'Default Part'. It displays a search bar and filter options for 'Parts' and 'Boards'. The 'Boards' tab is selected. A search bar at the bottom left contains the text 'KC705'. The main area is a table listing various Xilinx boards:

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version	Avail IOBs
MicroZed Board	em.avnet.com	e	xc7z010clg400-1	400	1.0	100
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1	484	1.0	200
Artix-7 AC701 Evaluation Platform	xilinx.com	1.0	xc7a200tfgb676-2	676	1.0	400
Kintex-7 KC705 Evaluation Platform	xilinx.com	1.1	xc7k325tffg900-2	900	1.0	500
Virtual-Z VC707 Evaluation Platform	xilinx.com	1.1	xc7vx485tffg1761-2	1,761	1.0	700
Virtual-Z VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2	1,761	1.0	850
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020clg484-1	484	1.0	200
ZYNQ-7 ZC706 Evaluation Board	xilinx.com	1.1	xc7z045ffg900-2	900	1.0	362

At the bottom right of the dialog are buttons for '< Back', 'Next >', 'Finish', and 'Cancel'.

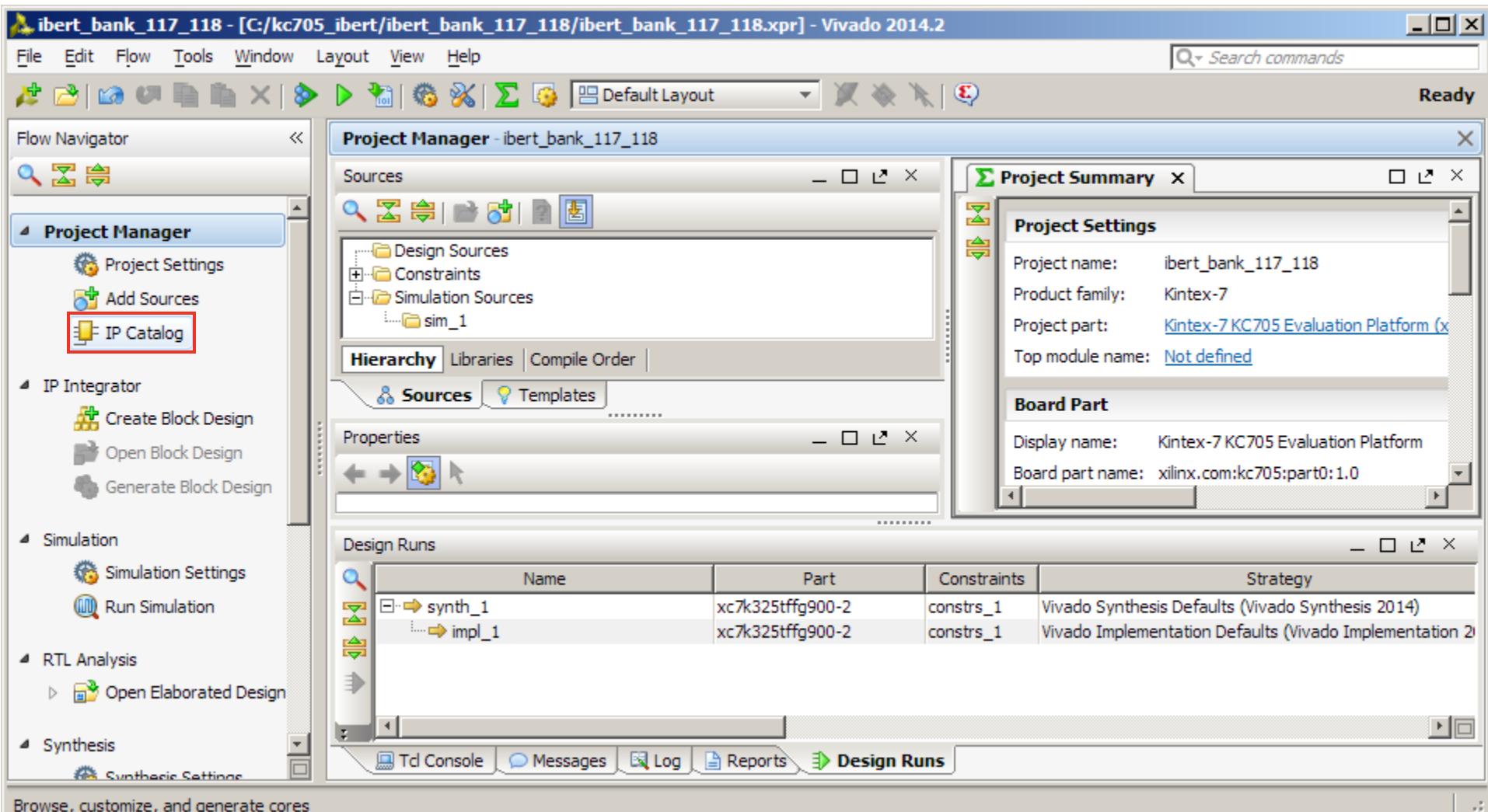
# Create IBERT Design for Banks 117, 118

► Click Finish



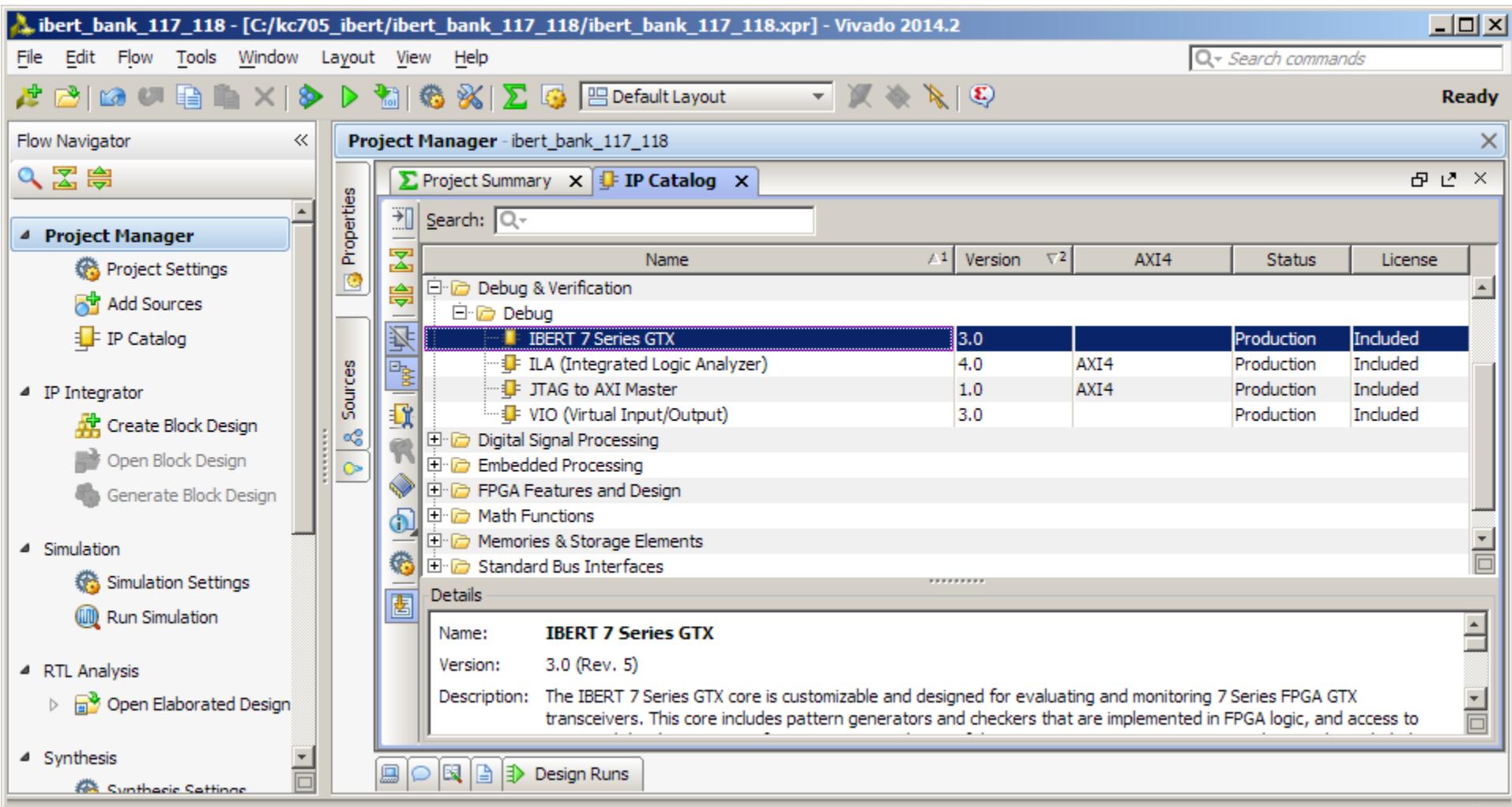
# Create IBERT Design for Banks 117, 118

► Click on IP Catalog



# Create IBERT Design for Banks 117, 118

► Select IBERT 7 Series GTX, v3.0 under Debug & Verification



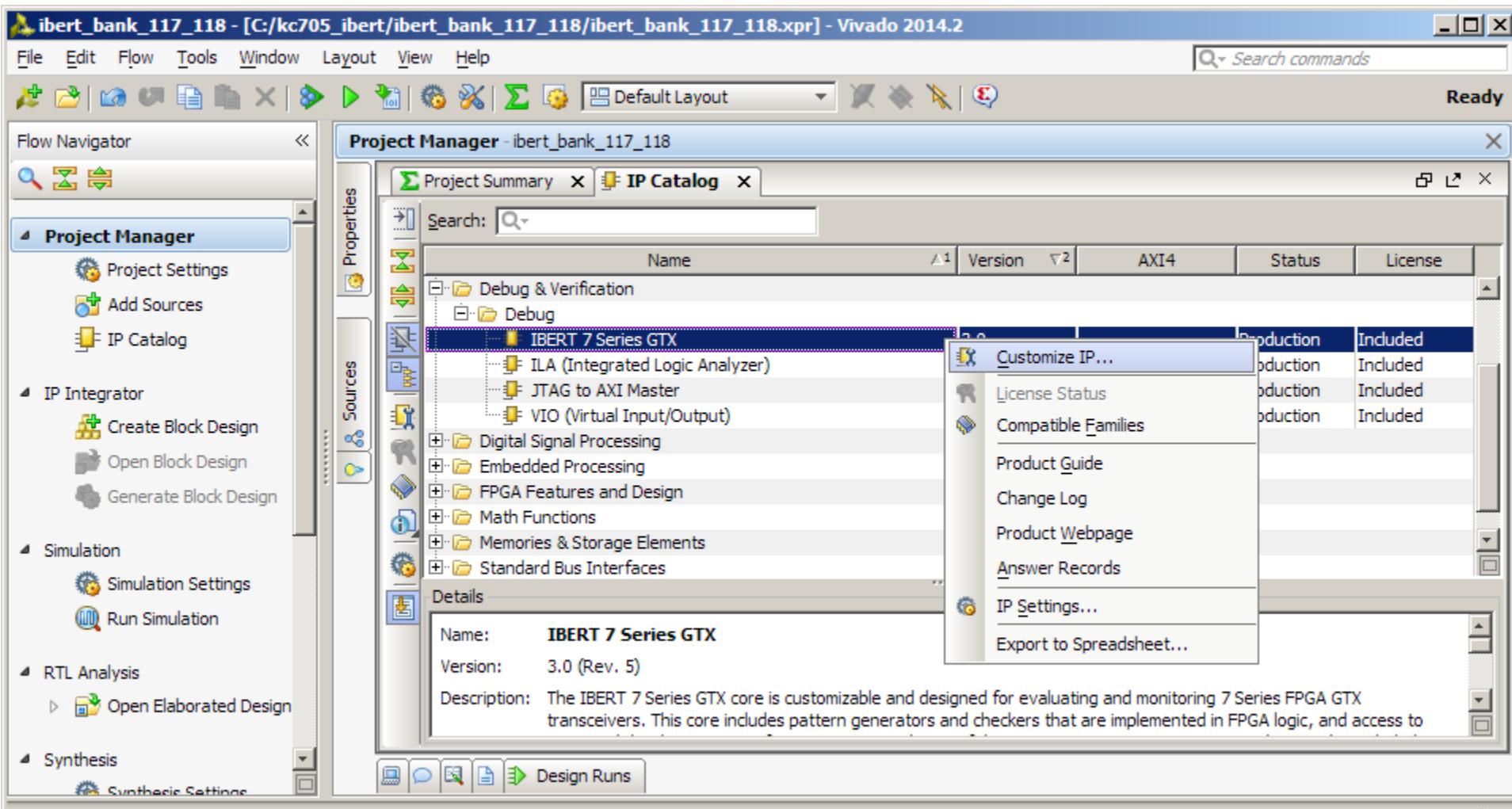
IP: IBERT 7 Series GTX

Note: Presentation applies to the KC705

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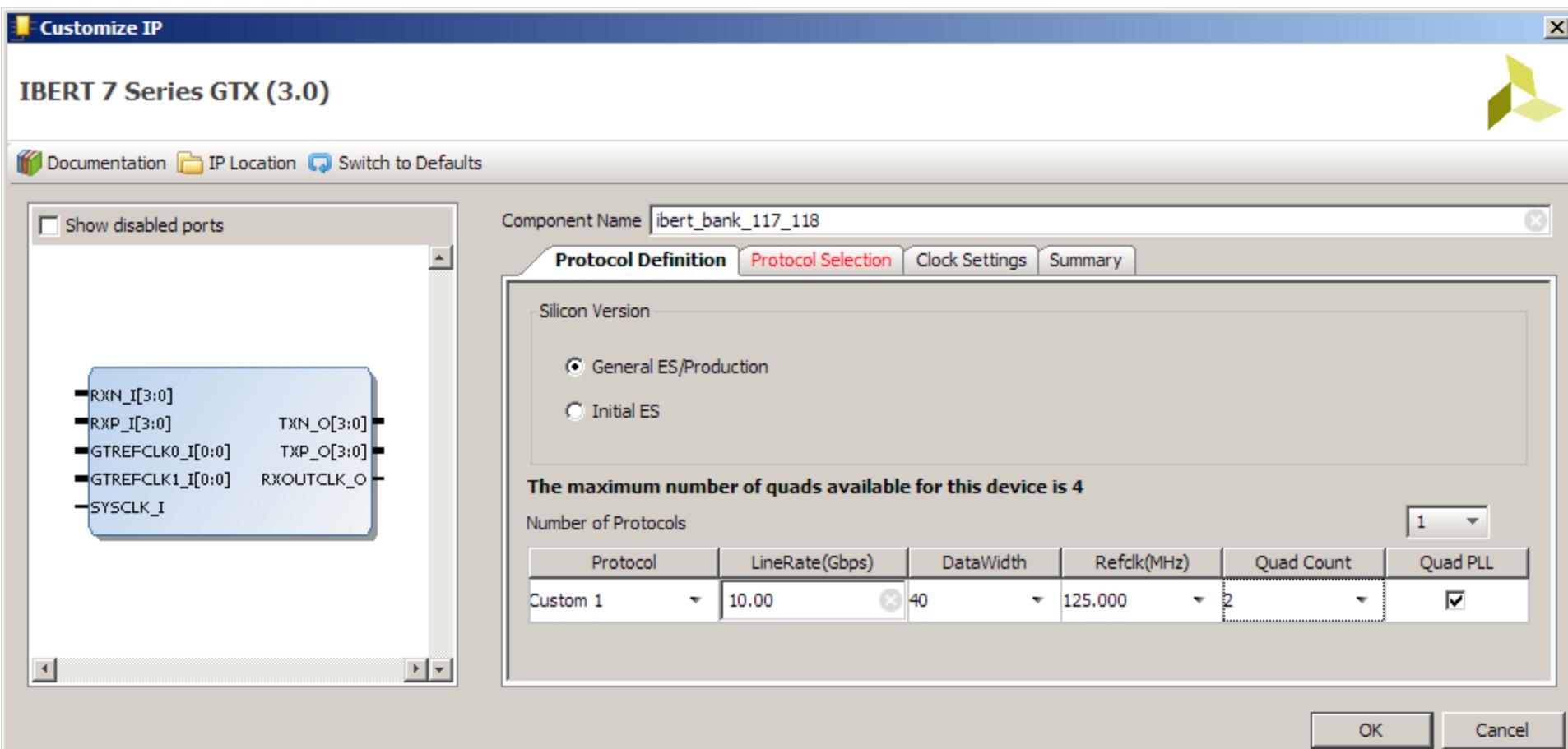
# Create IBERT Design for Banks 117, 118

► Right click on IBERT 7 Series GTX and select Customize IP...



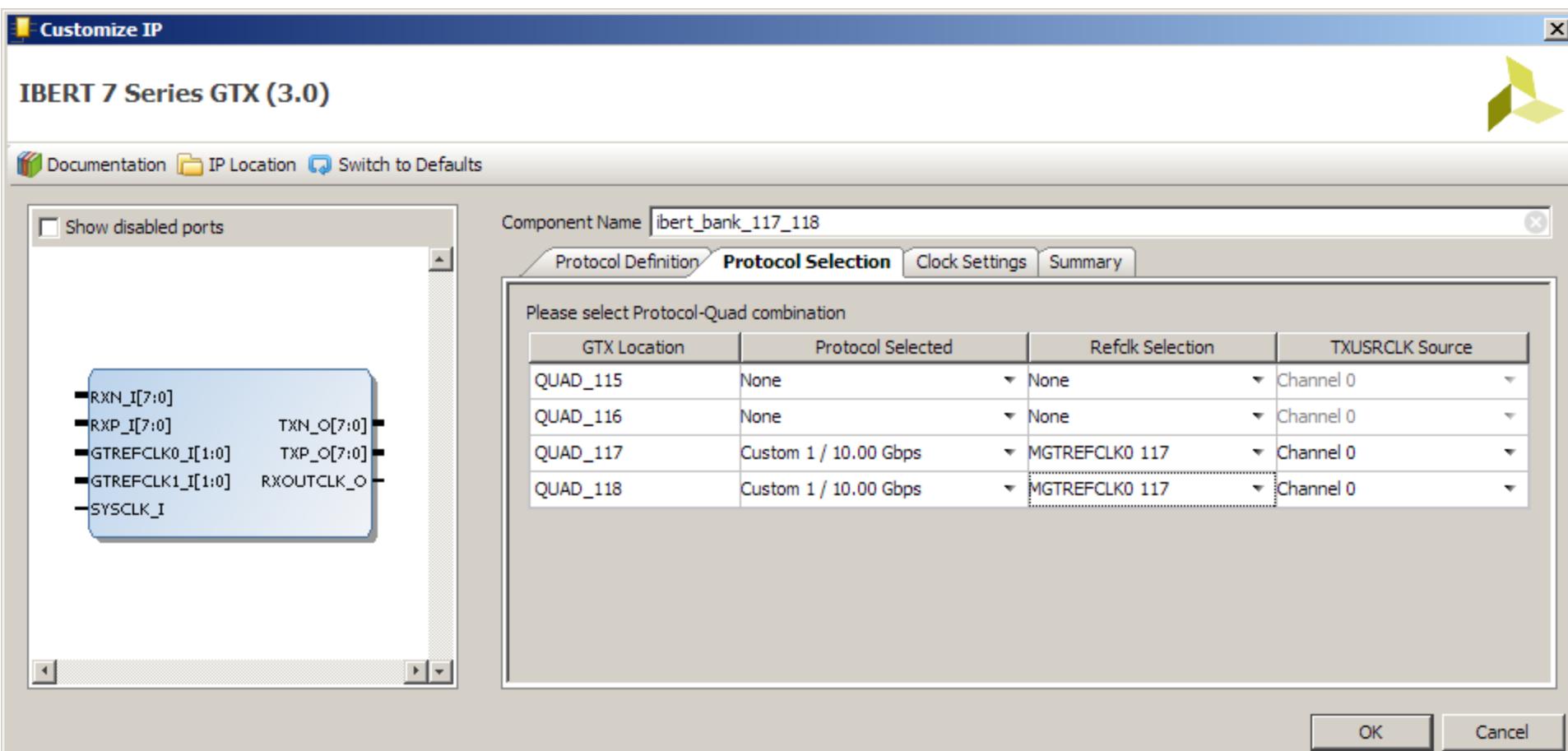
# Create IBERT Design for Banks 117, 118

- Set the Component name: **ibert\_bank\_117\_118**
- Under the Protocol Definition tab
  - Silicon Version: **General ES / Production**
  - Protocol: LineRate: **10.00**, DataWidth: **40** Refclk: **125.000** Quad Count: **2**



# Create IBERT Design for Banks 117, 118

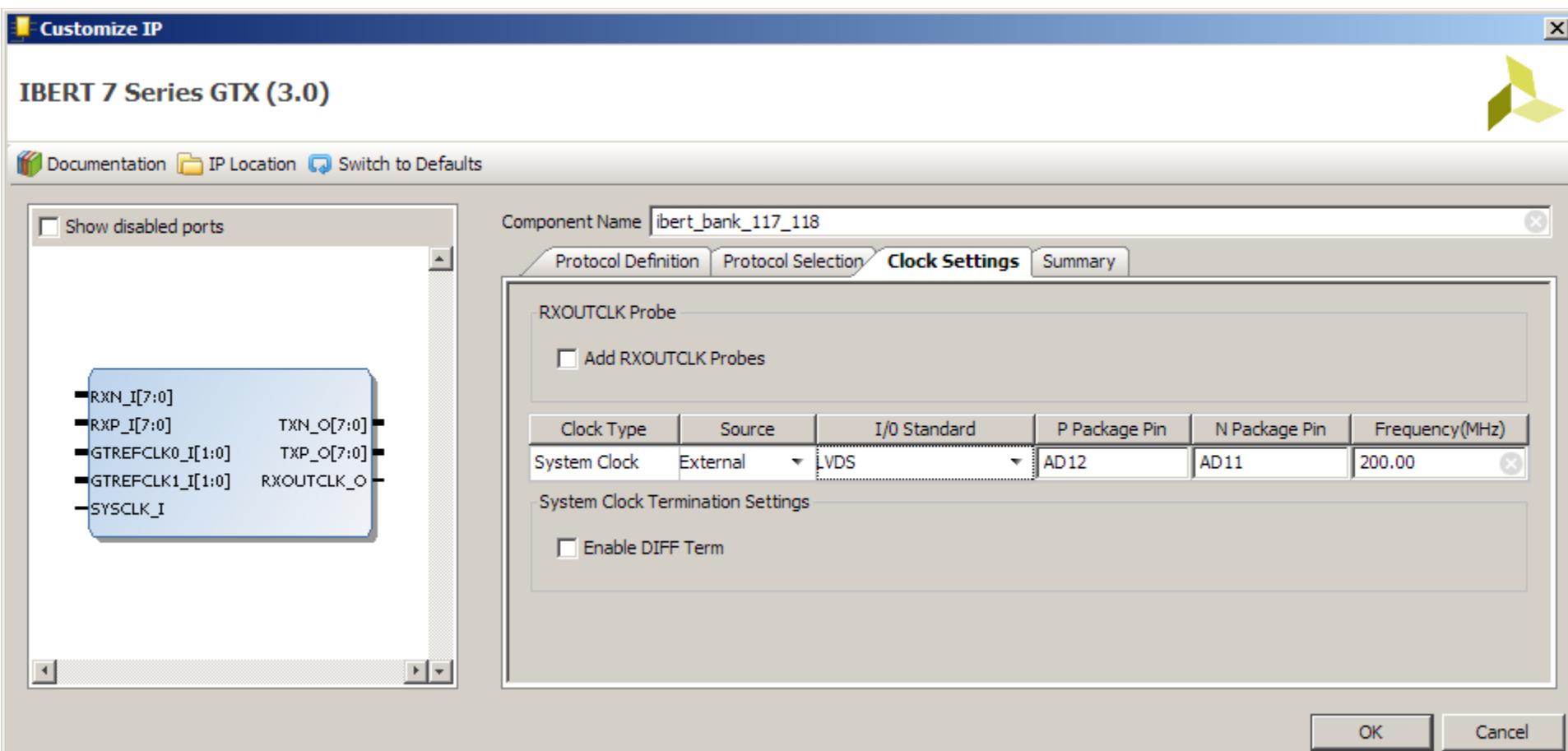
- Under the Protocol Selection tab
- Set QUAD\_117 and QUAD\_118 to
  - Custom 1 / 10.00 Gbps, and MGTREFCLK0 117



# Create IBERT Design for Banks 117, 118

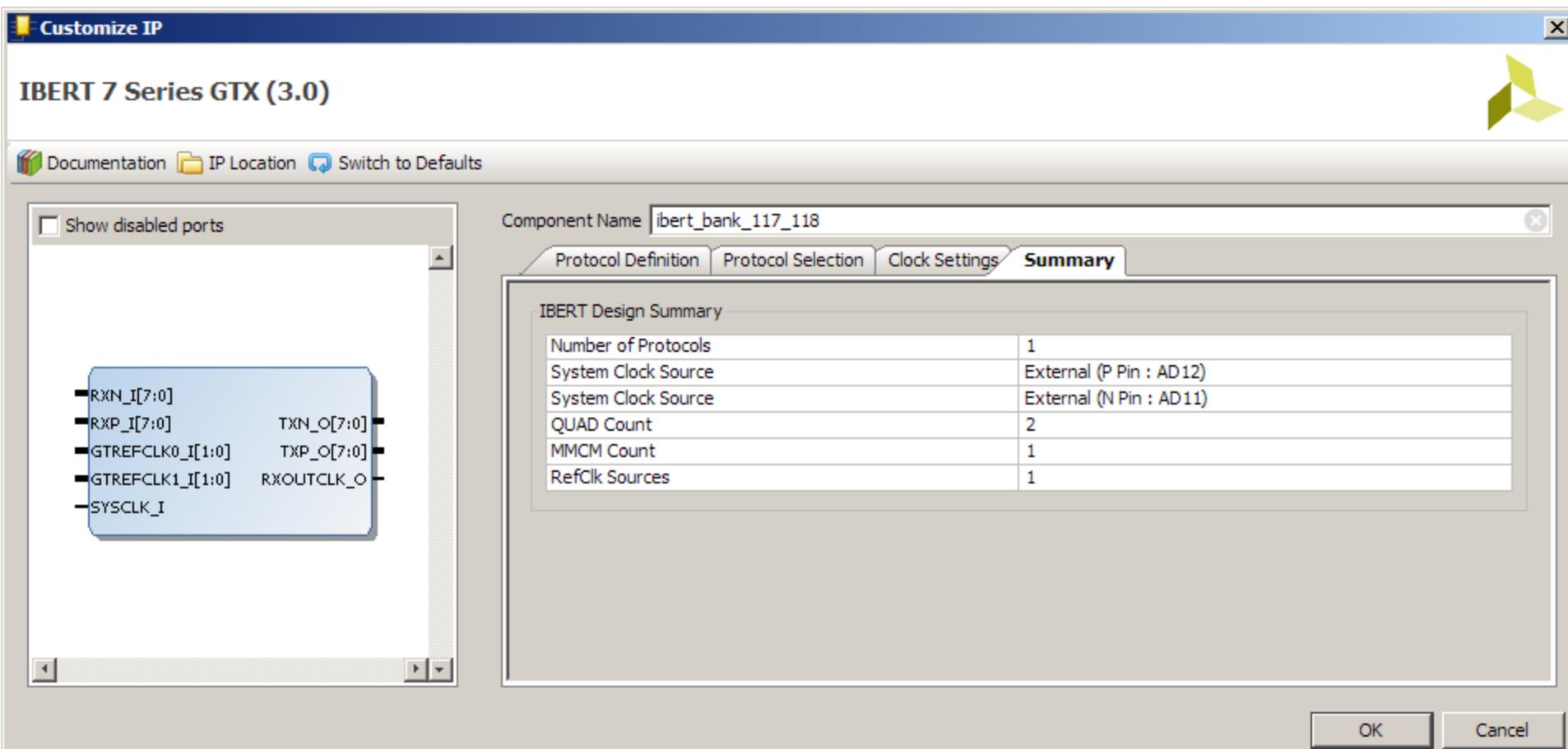
► Under the Clock Settings tab, set the System Clock:

- LVDS, P Pin Location: **AD12**, N Pin Location: **AD11**



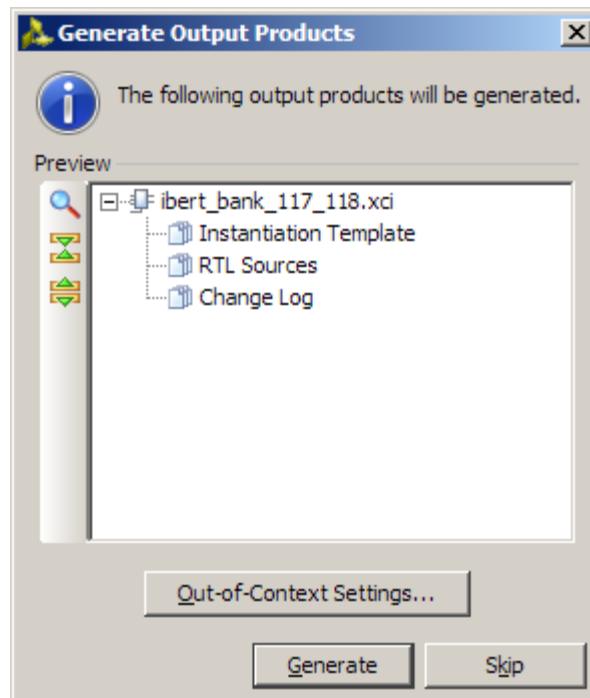
# Create IBERT Design for Banks 117, 118

► Review the summary and click OK



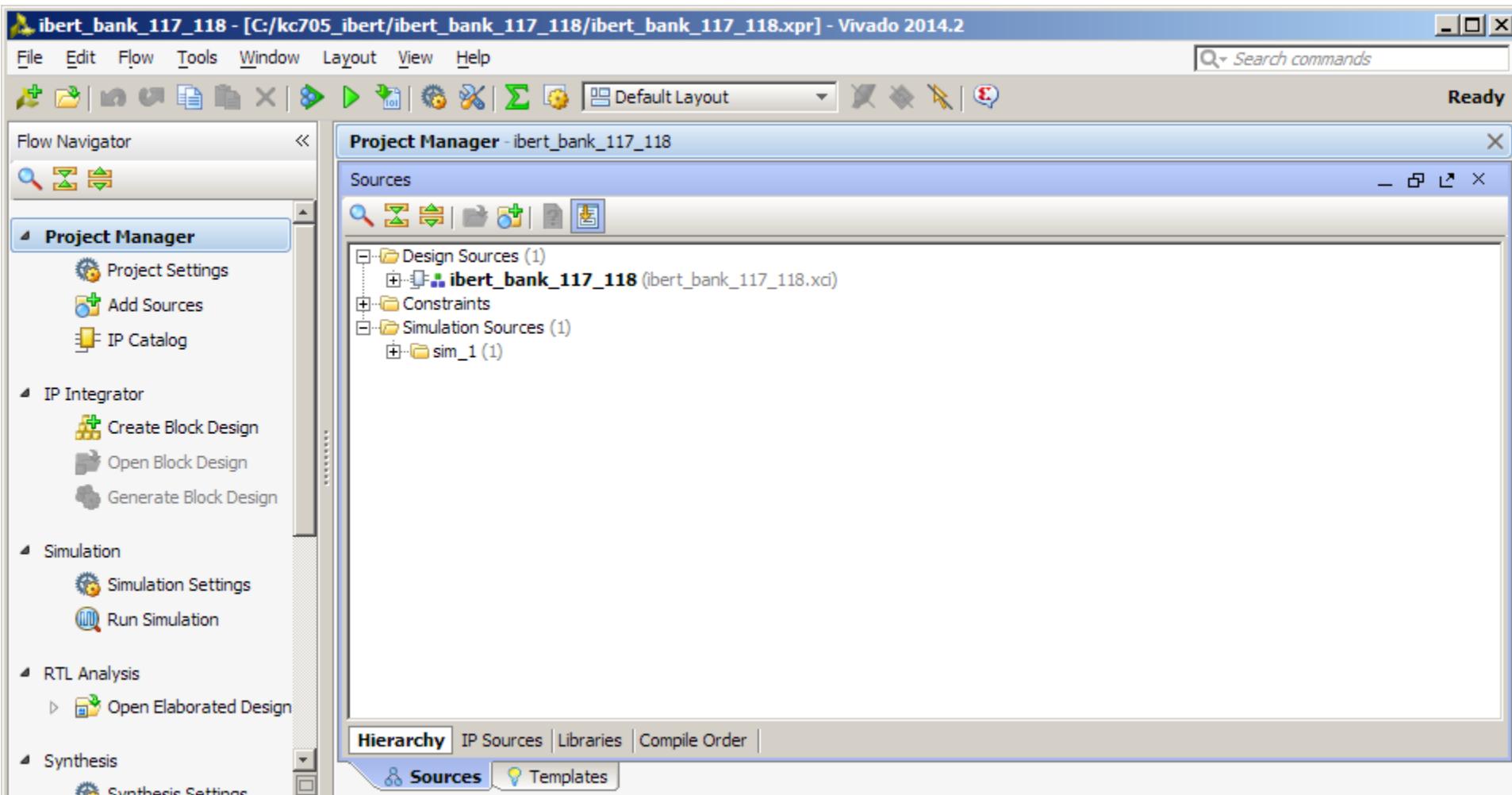
# Create IBERT Design for Banks 117, 118

► Click Generate



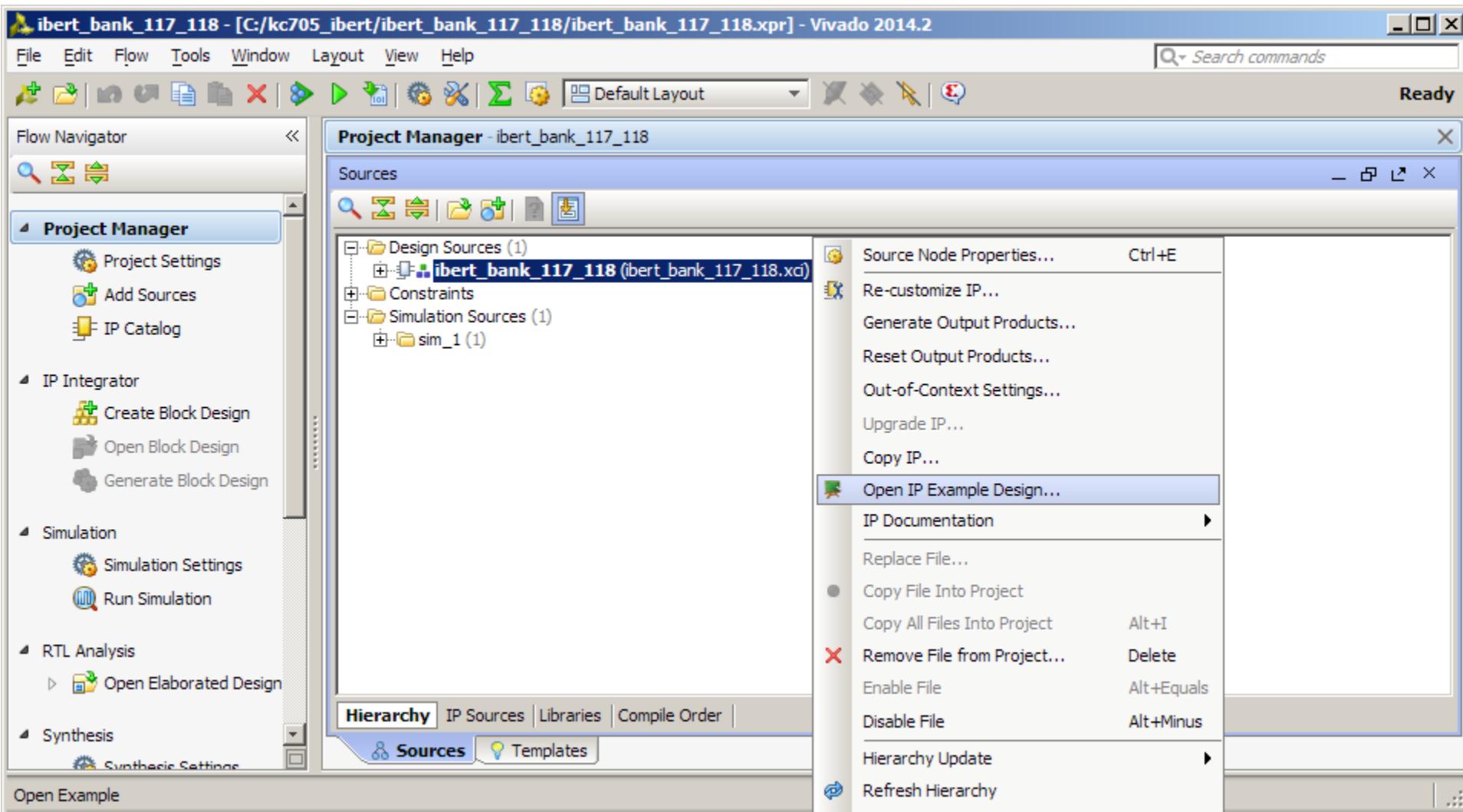
# Create IBERT Design for Banks 117, 118

► Bank 117 & 118 IBERT design appears in Design Sources



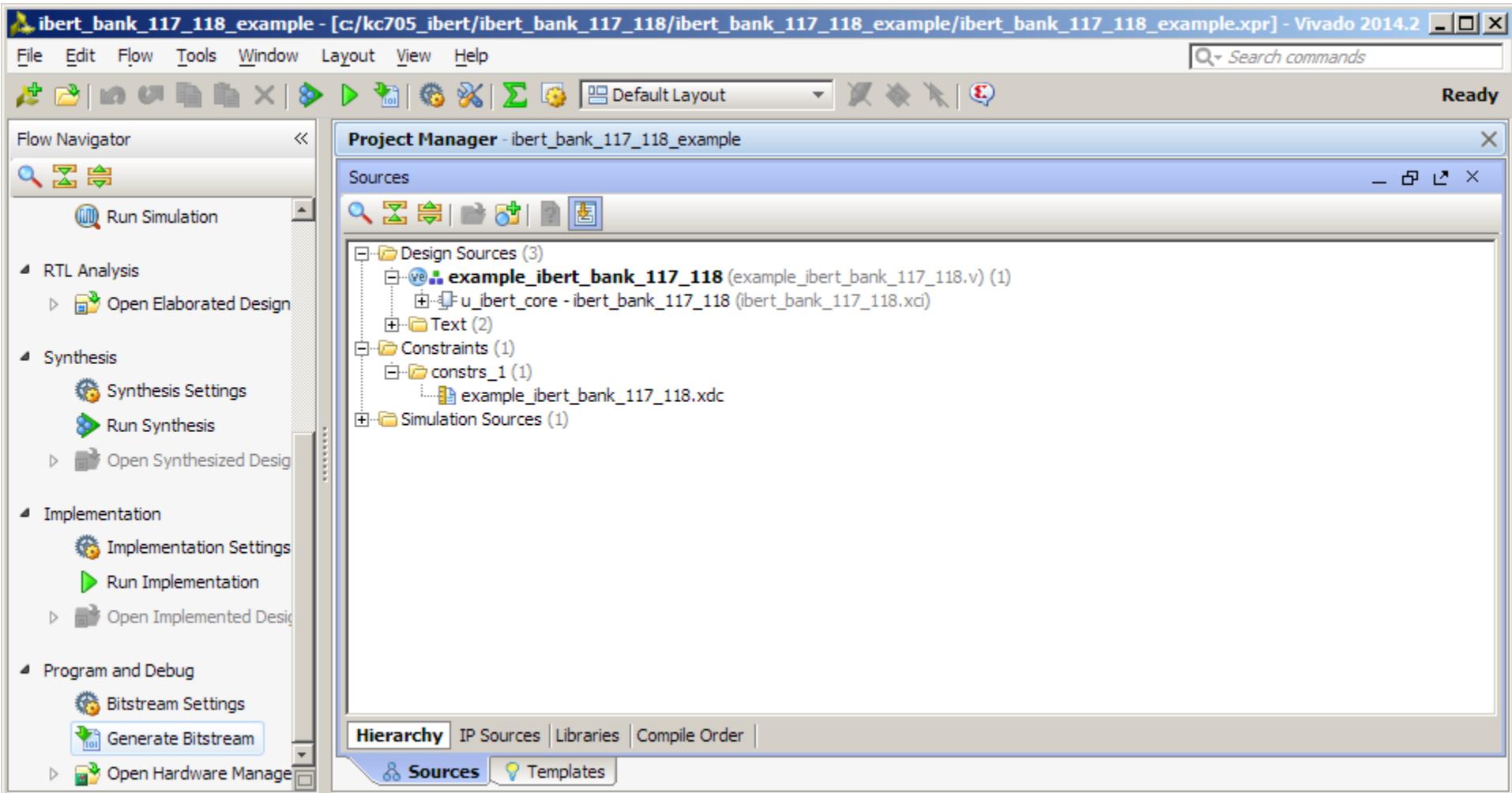
# Compile Example Design

- Right click on `ibert_bank_117_118` and select Open IP Example Design...



# Compile Example Design

- A new project is created under <design path>/
- Click Generate Bitstream



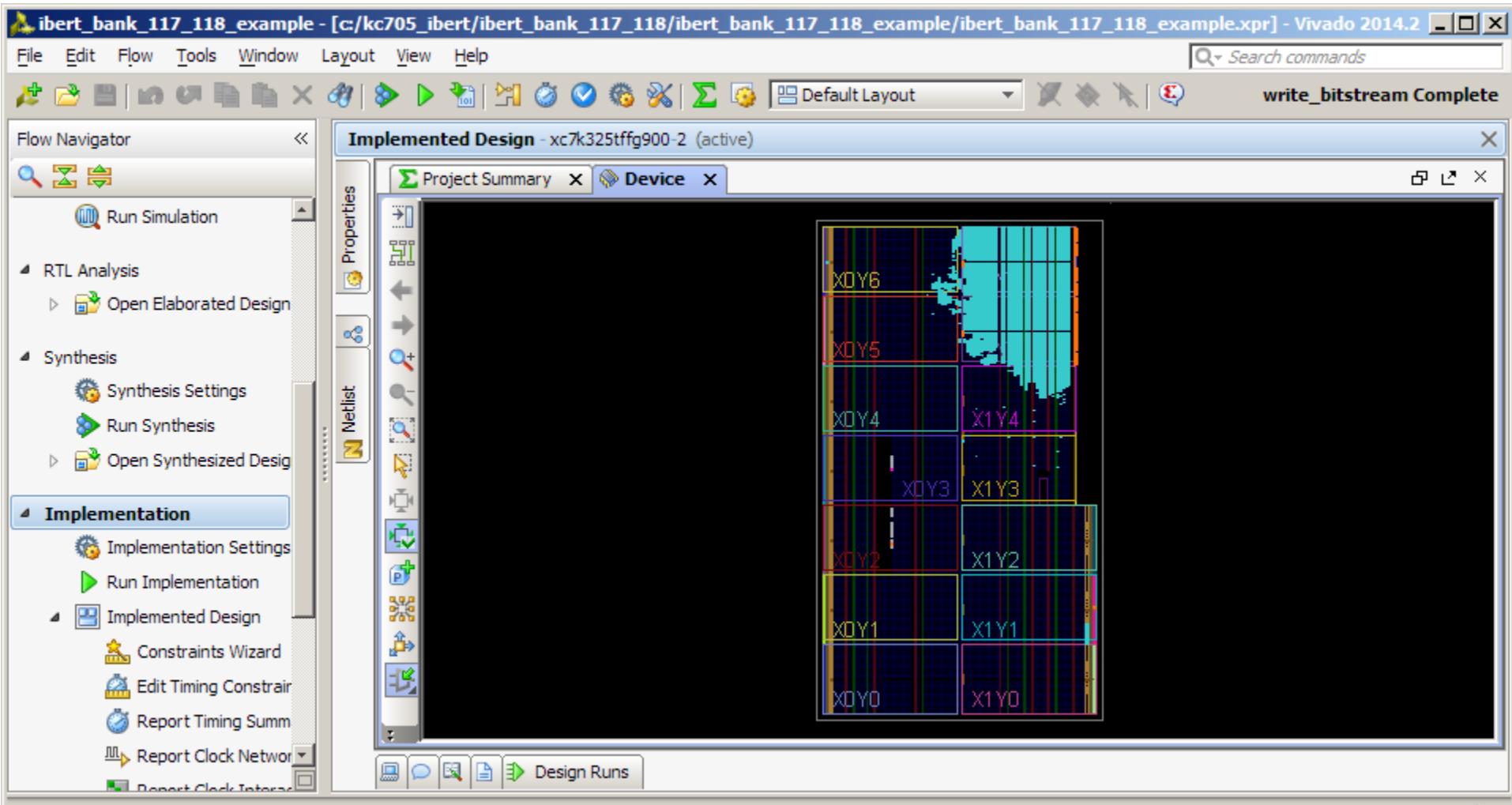
Generate a programming file after implementation

Note: The original project window can be closed

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# Compile Example Design

► Open and view the Implemented Design



## **Testing Bank 117 and 118 with Optional User Provided Hardware**

# Optional Testing with User Provided Hardware

## ► SMA Cables

- [www.rosenbergerna.com](http://www.rosenbergerna.com)
- Part number:  
72D-32S1-32S1-00610A



## ► SMA Quick connects

- RADIALL
- Part number: R125791501
- Available [here](#) or [here](#)



# Optional Testing with User Provided Hardware

## ► Connect Optical Loopback Adapter

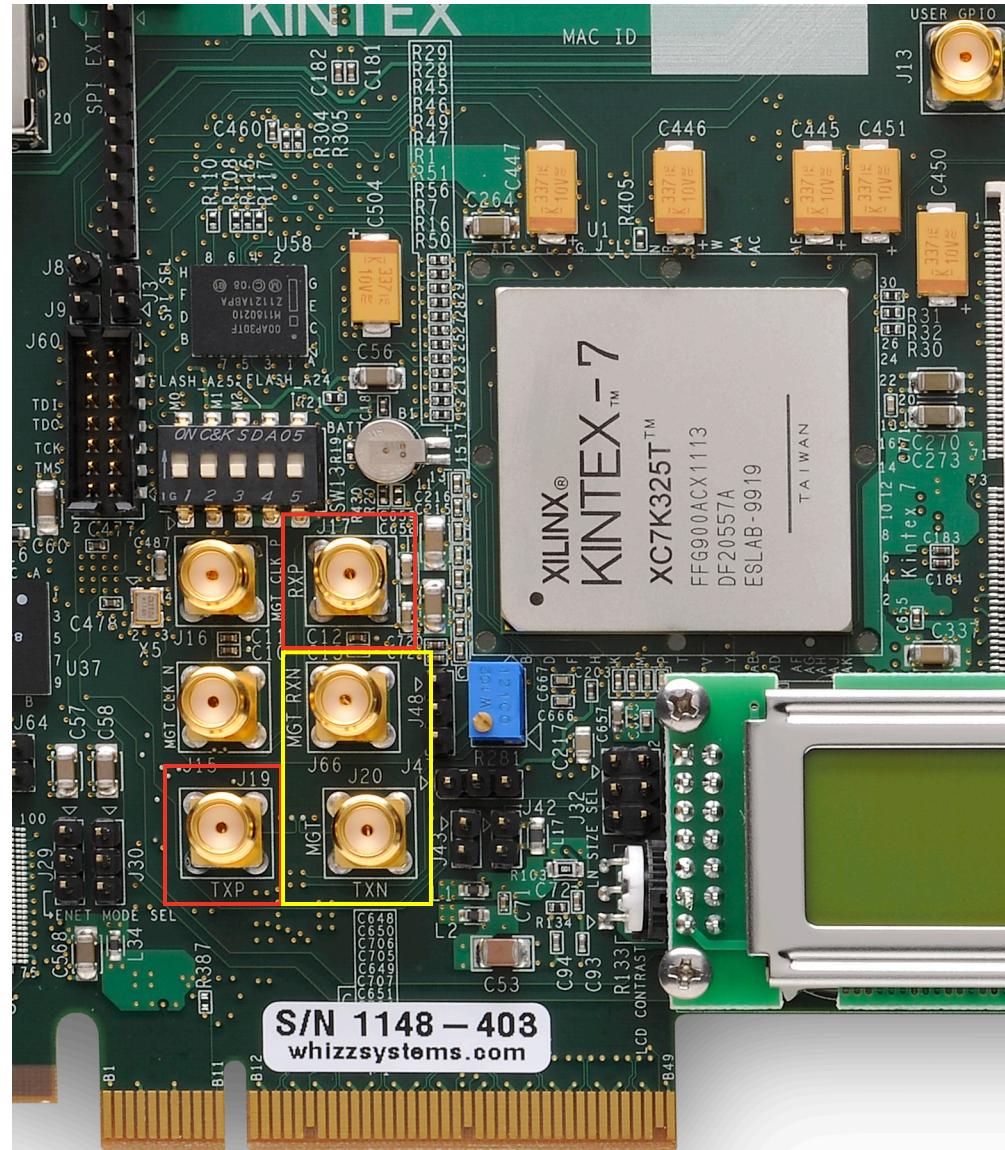
- [www.molex.com](http://www.molex.com)
- SFP Loopback Adapter,  
5.0 db Attenuation
- Part # [74765-0904](#)



# Testing Bank 117 and 118 with Optional User Provided Hardware

## ➤ Using the SMA cables:

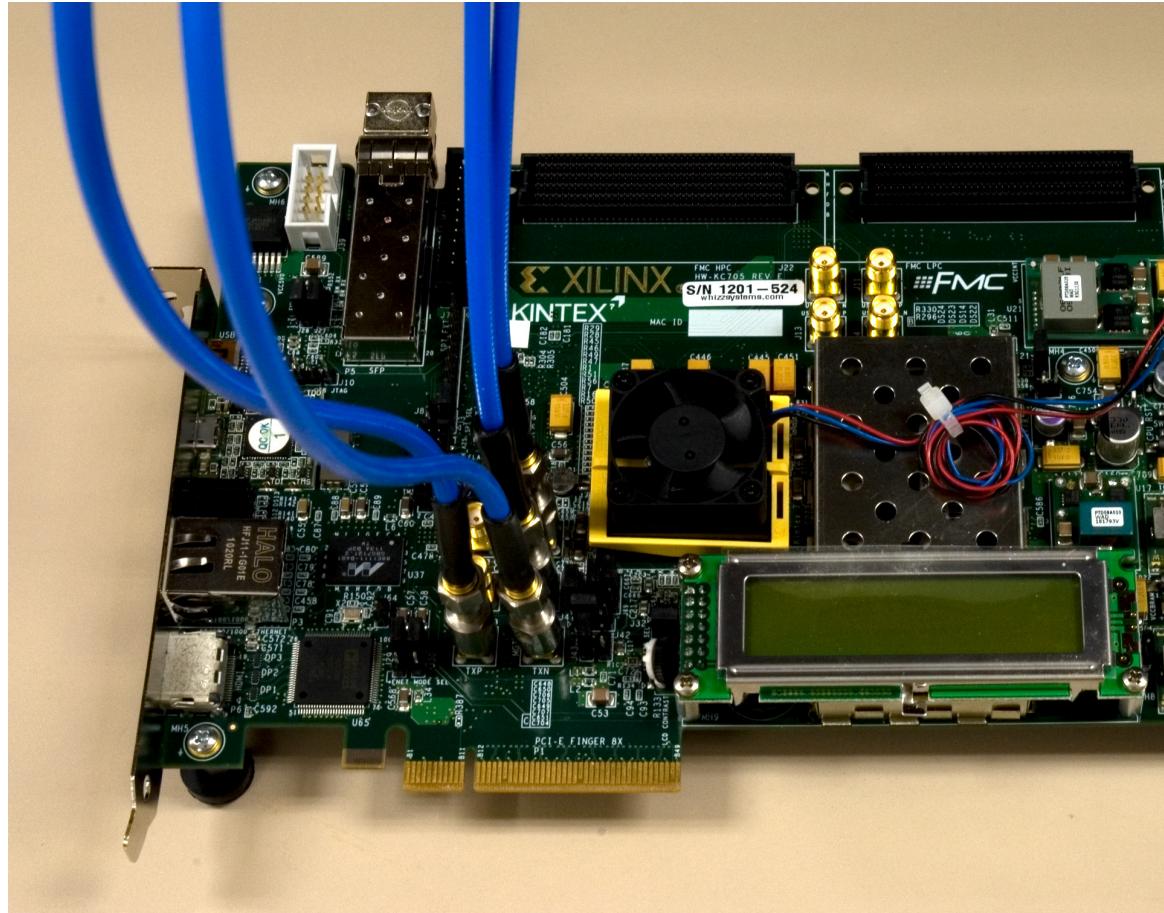
- Connect J19 to J17
- Connect J20 to J66



Note: Presentation applies to the KC705

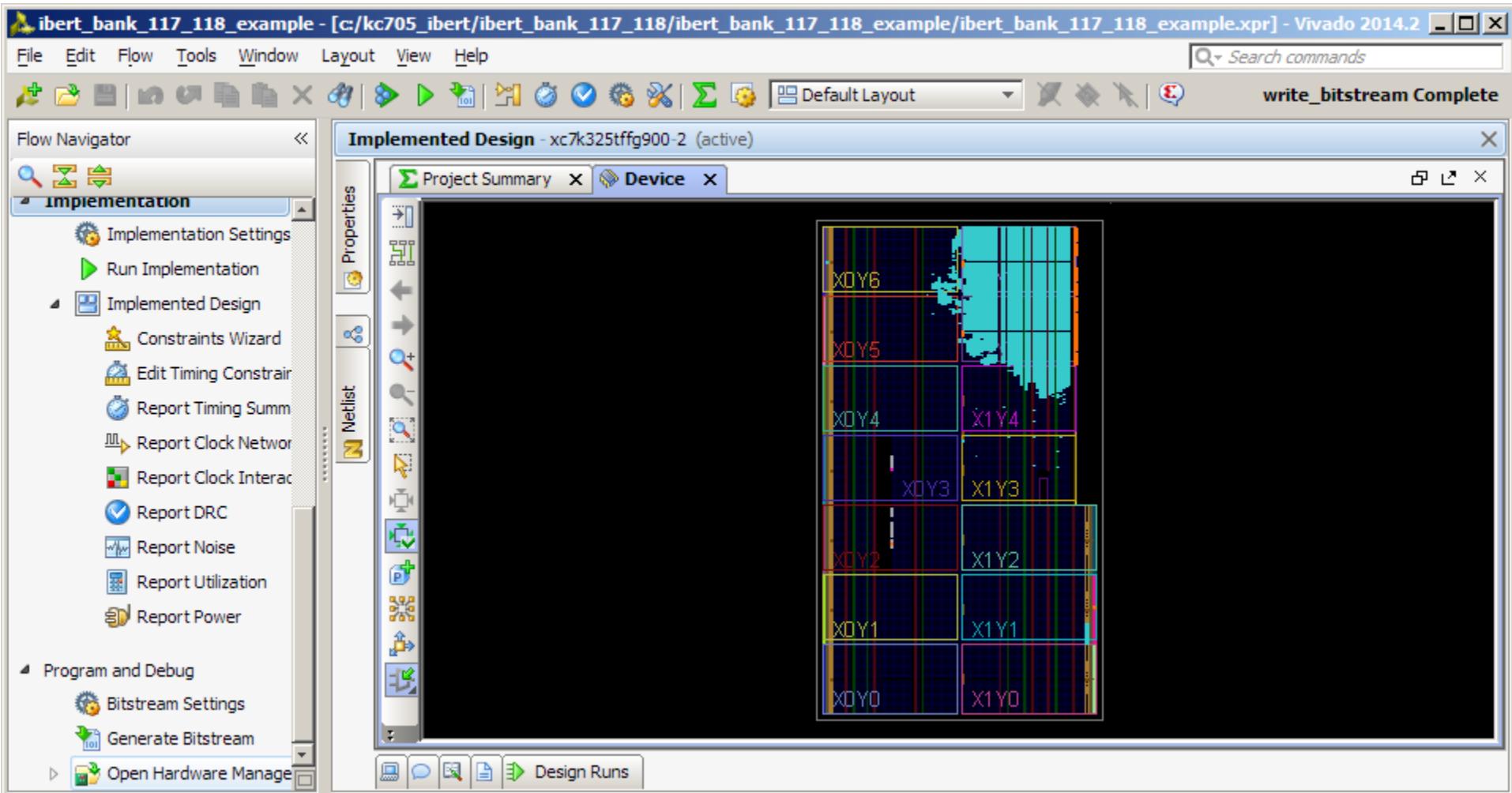
# Testing Bank 117 and 118 with Optional User Provided Hardware

- Insert the SFP Loopback Adapter
- Power on the KC705 board



# Run IBERT Example Design

► Click Open Hardware Manager



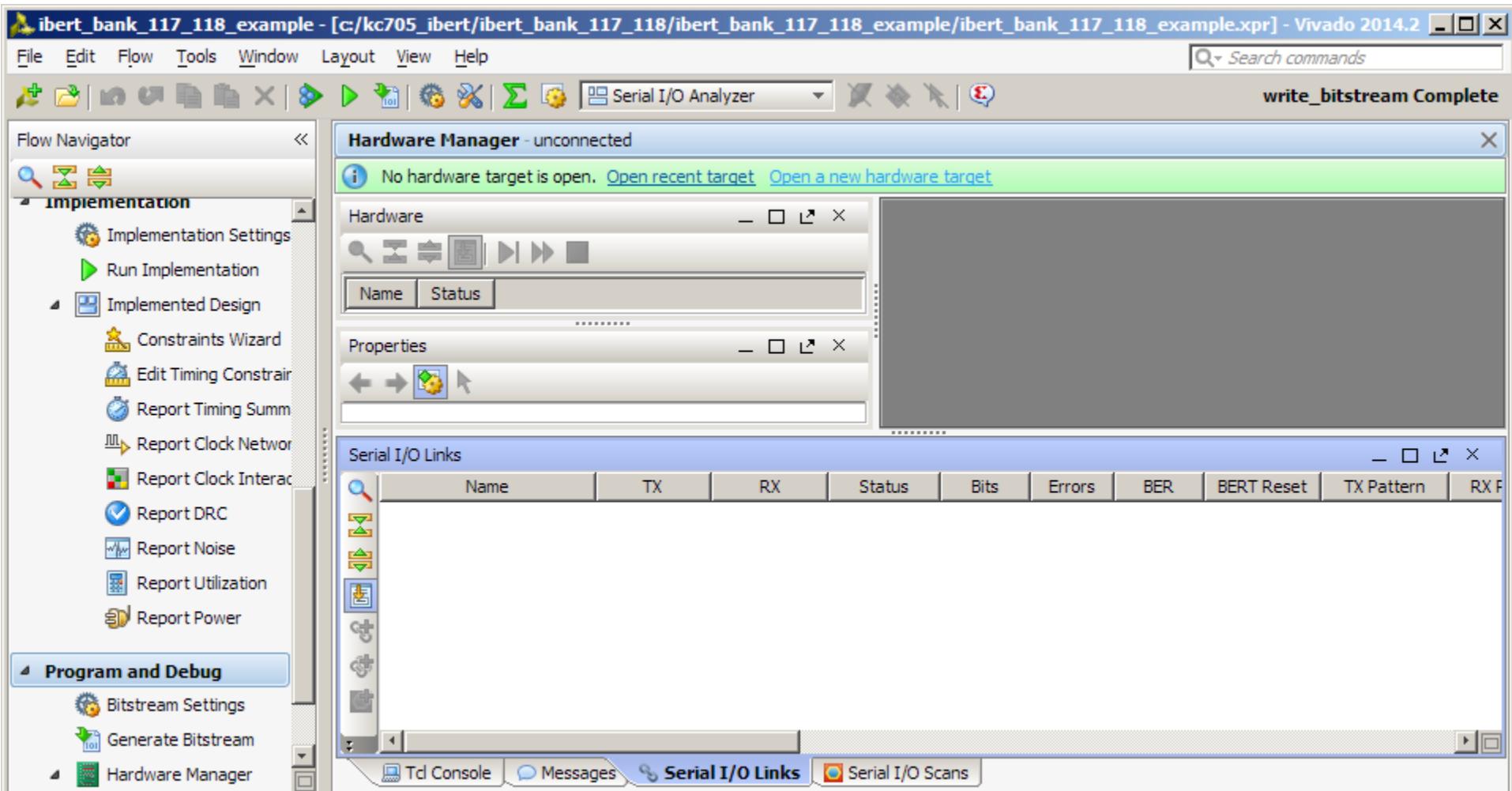
Open the hardware program and debug manager

Note: Presentation applies to the KC705

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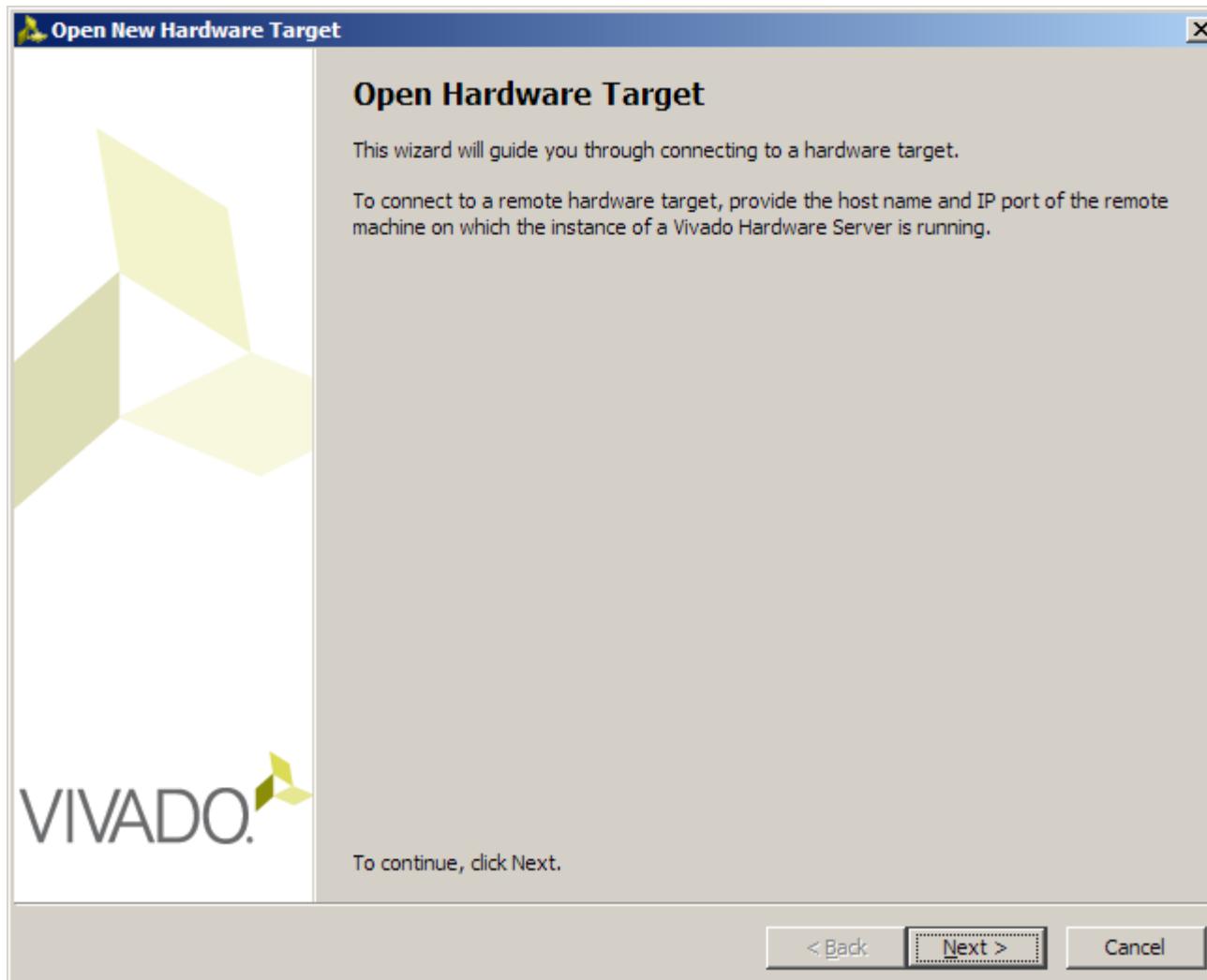
# Run IBERT Example Design

► Click Open a new hardware target



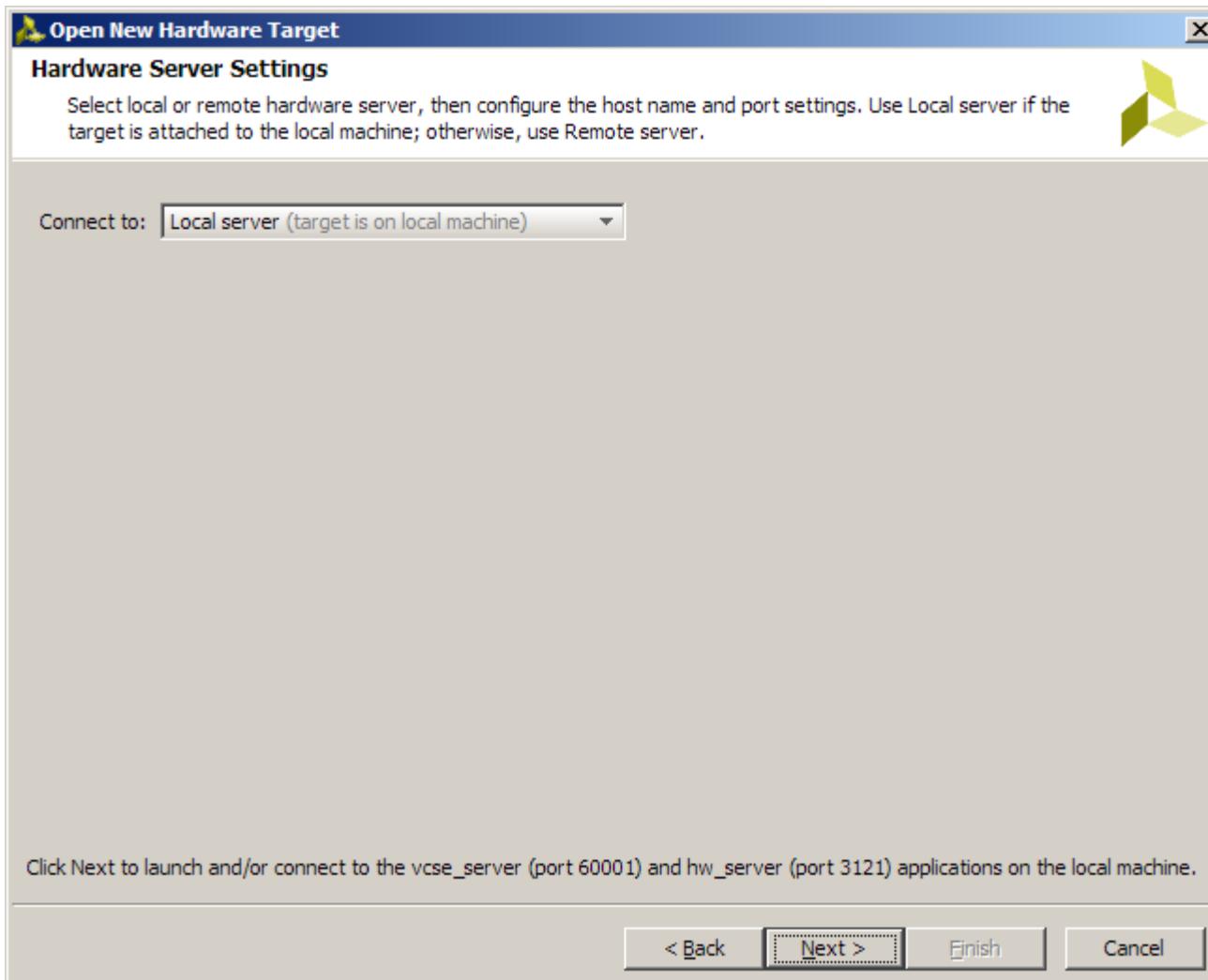
# Run IBERT Example Design

► Click Next



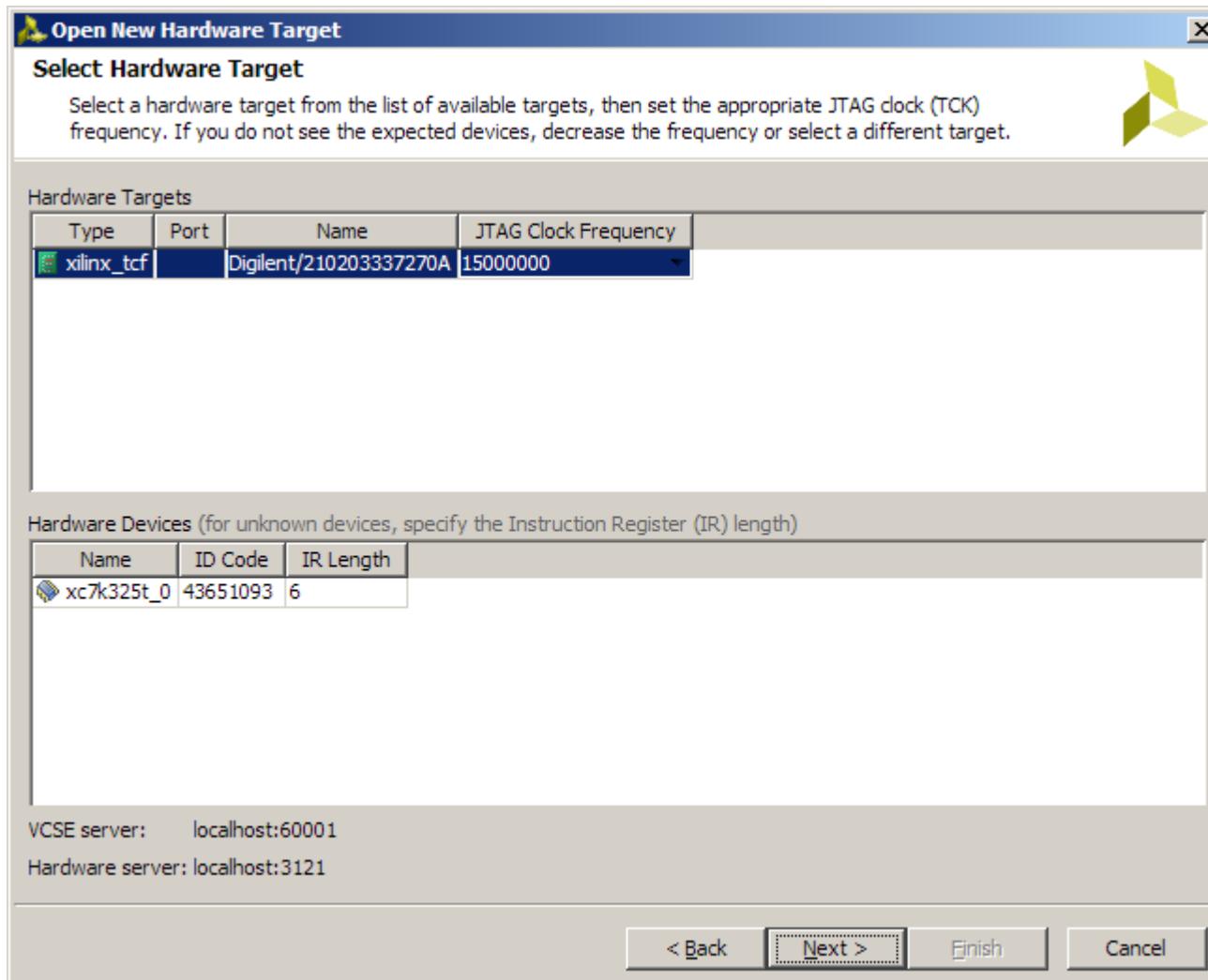
# Run IBERT Example Design

► Click Next



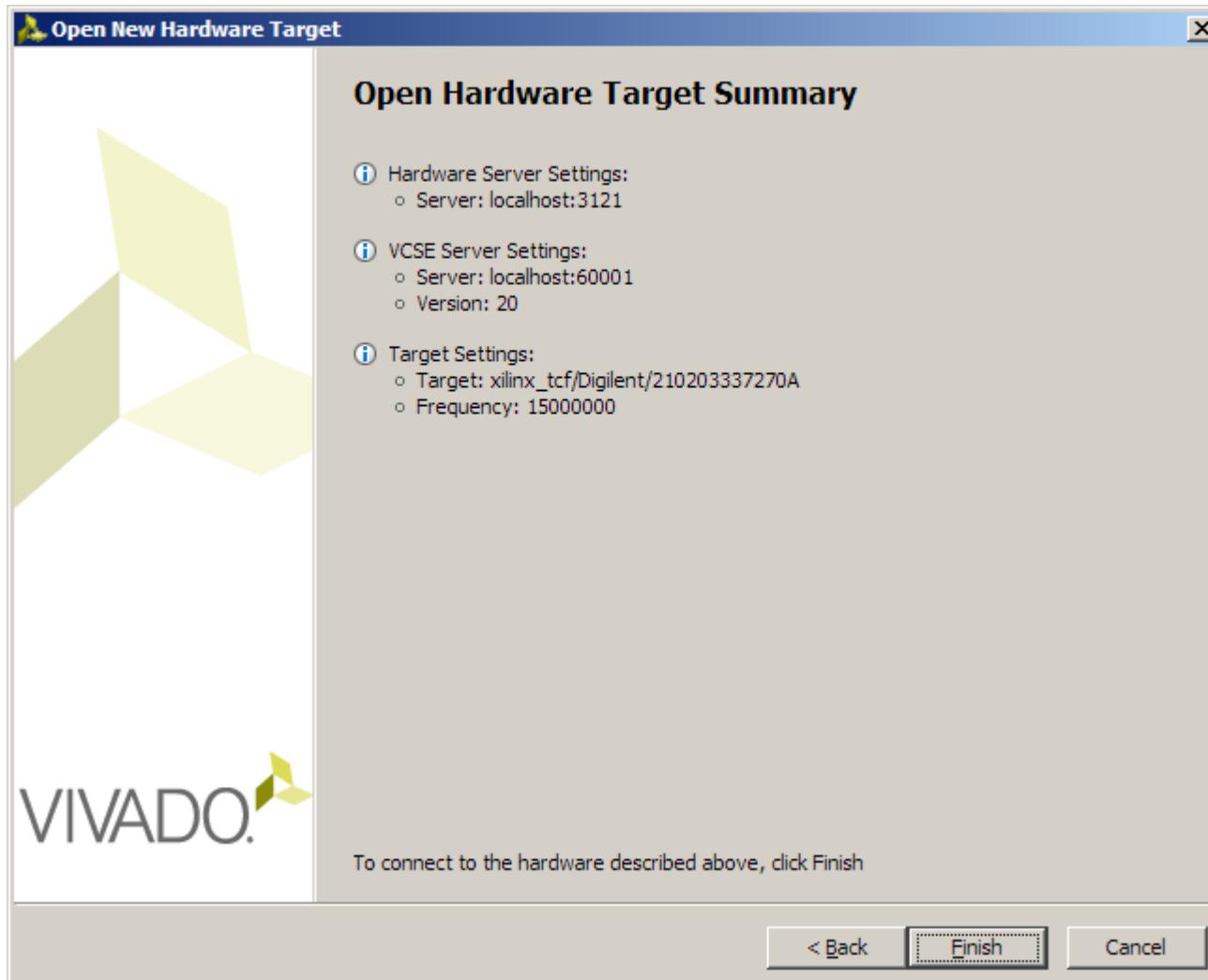
# Run IBERT Example Design

► Click Next



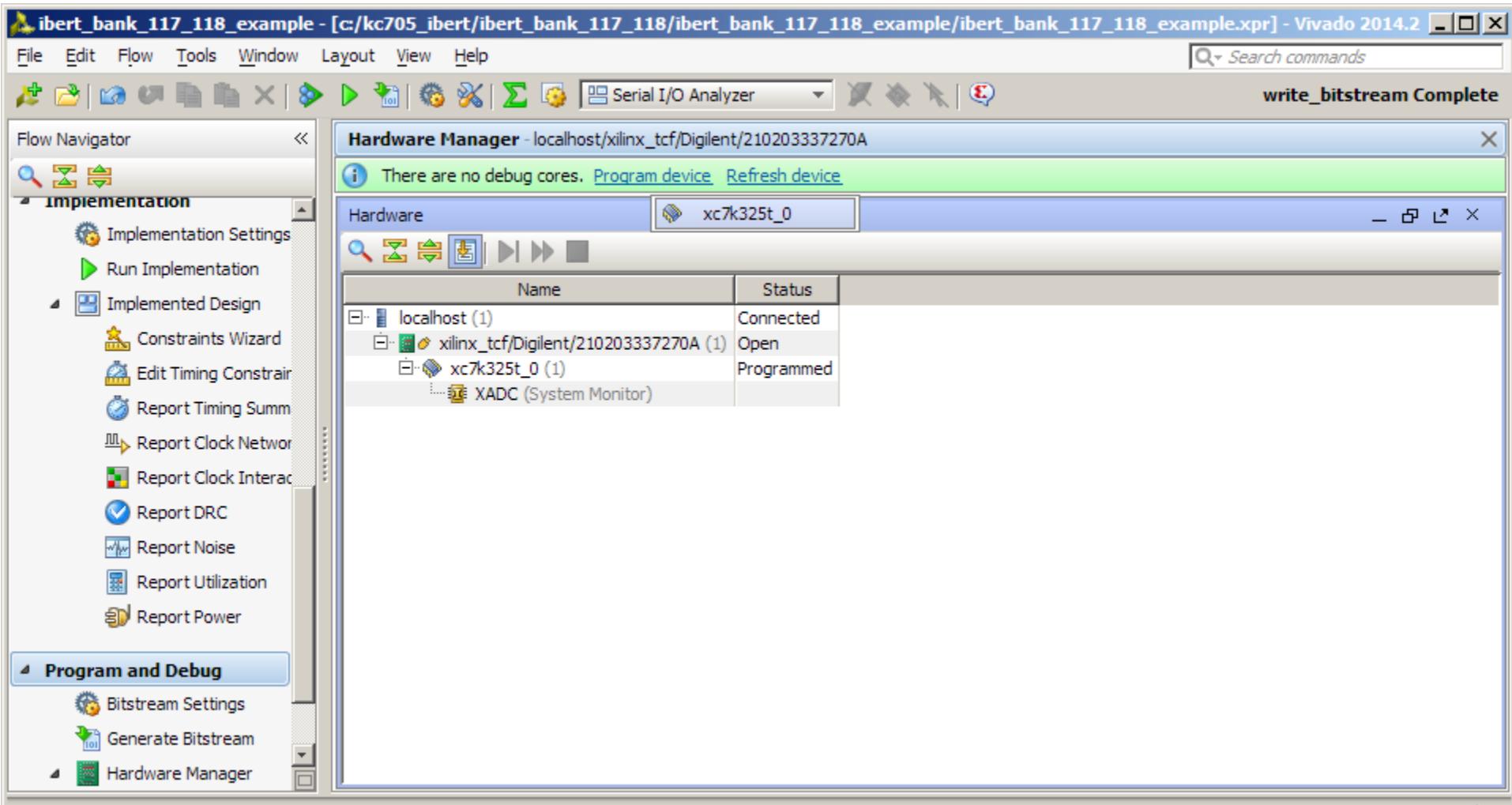
# Run IBERT Example Design

► Click Finish



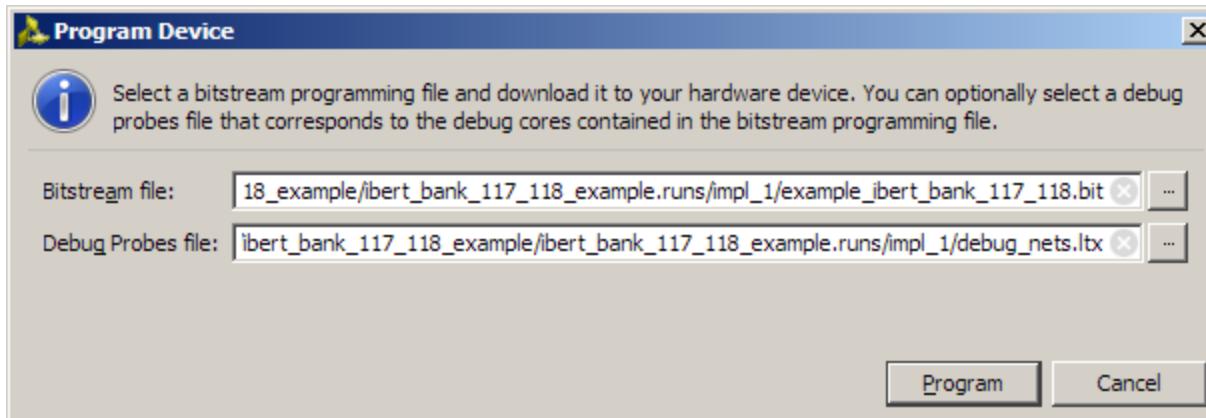
# Run IBERT Example Design

► Select Program device → XC7K325T\_0



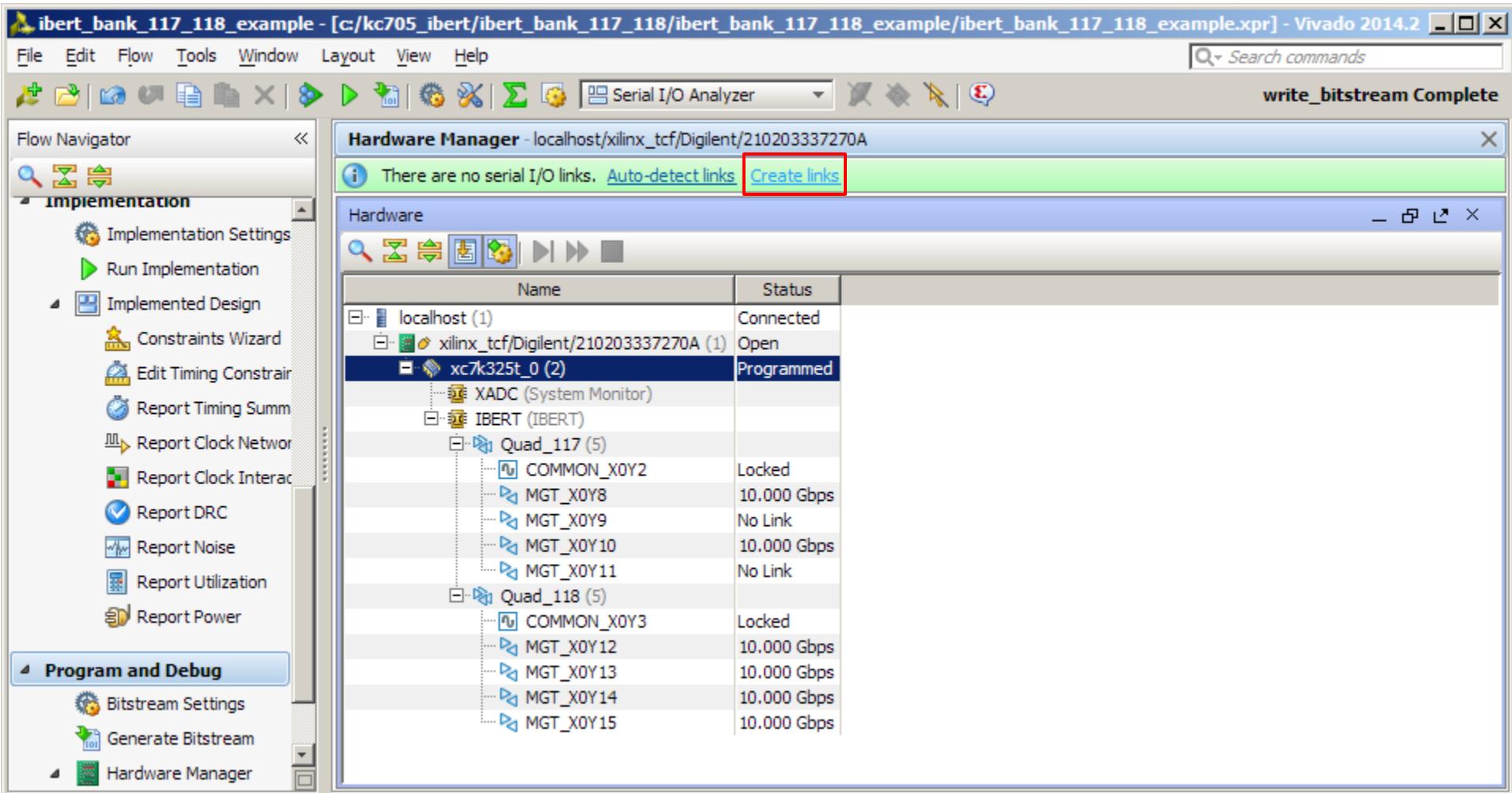
# Run IBERT Example Design

- The newly created bitstream is default
- Click Program



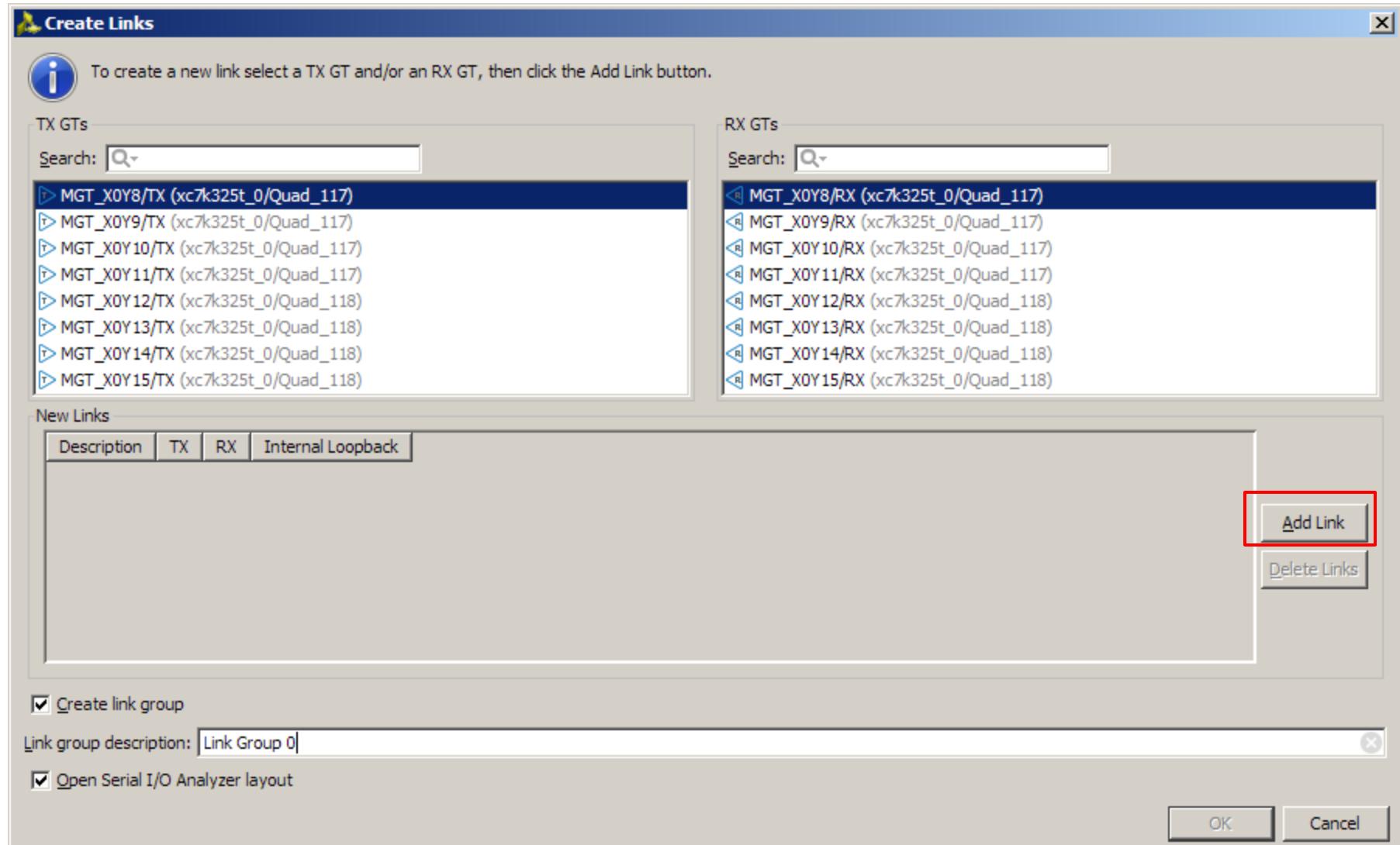
# Run IBERT Example Design

- Quad\_117 and Quad\_118 show Locked
- Click Create links



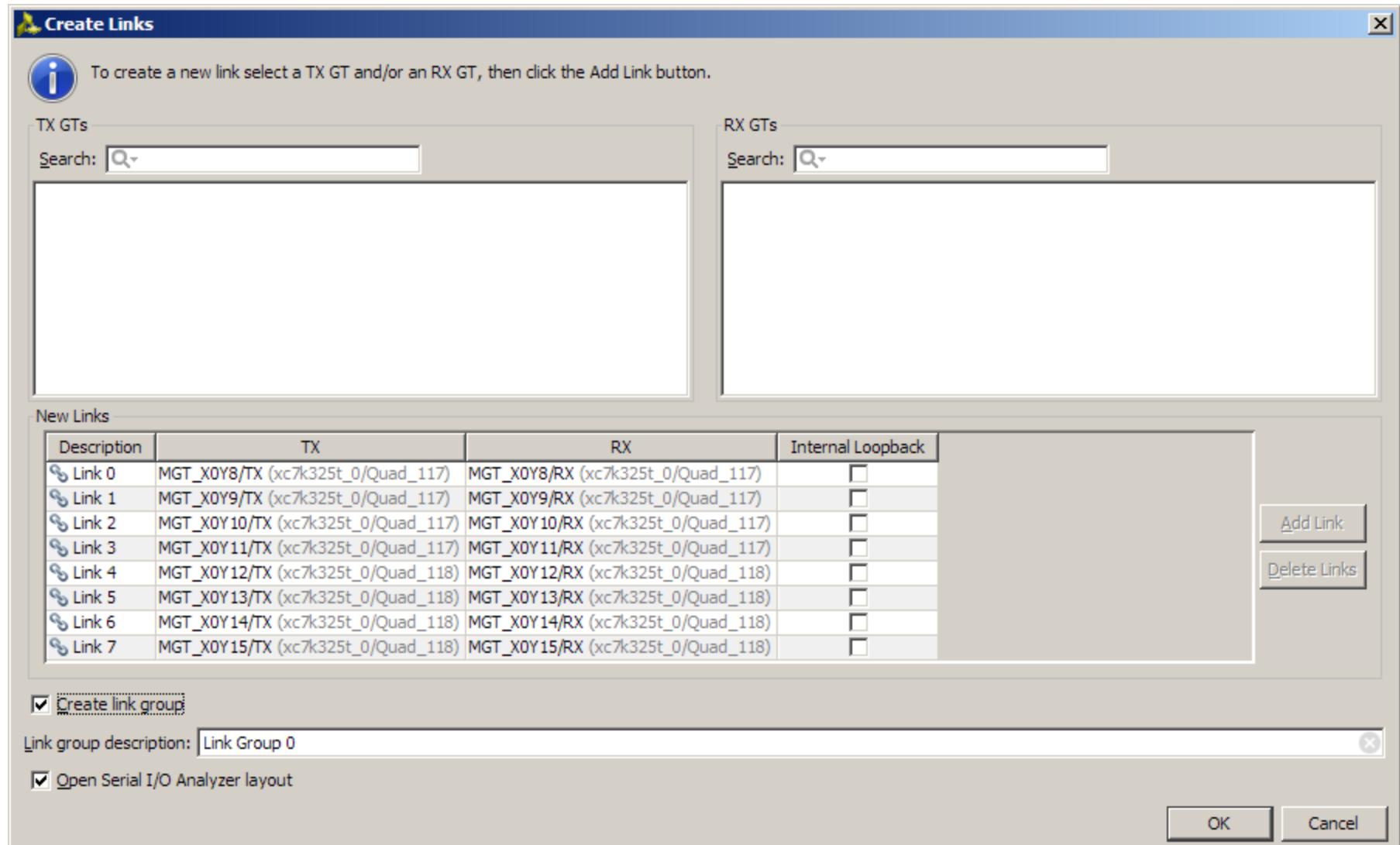
# Run IBERT Example Design

► Click on the Add Link button until all the MGT pairs are “linked”



# Run IBERT Example Design

► Click OK



# Run IBERT Example Design

► The IBERT data appears as seen below

The screenshot shows the Vivado 2014.2 Hardware Manager window titled "ibert\_bank\_117\_118\_example - [c:/kc705\_ibert/ibert\_bank\_117\_118/ibert\_bank\_117\_118\_example/ibert\_bank\_117\_118\_example.xpr] - Vivado 2014.2". The main area displays the "Serial I/O Links" table. The table has columns: Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, RX Pattern, TX Pre-Cursor, and TX Po. The table lists 8 Link Groups, each containing 8 links. Most links are connected (Status: "No Link") except for Link 0 which is connected ("MGT\_X0Y8/TX" to "MGT\_X0Y8/RX"). The table also includes a search bar at the top right labeled "Search commands" and tabs at the bottom: Td Console, Messages, Serial I/O Links (selected), and Serial I/O Scans.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Po
Ungrouped Links (0)											
Link Group 0 (8)											
Link 0	MGT_X0Y8/TX	MGT_X0Y8/RX	10.000 Gbps	3.336E11	0E0	2.998E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 1	MGT_X0Y9/TX	MGT_X0Y9/RX	No Link	3.34E11	1.74E11	5.209E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 2	MGT_X0Y10...	MGT_X0Y10...	10.000 Gbps	3.355E11	0E0	2.98E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 3	MGT_X0Y11...	MGT_X0Y11...	No Link	3.358E11	1.678E11	4.996E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 4	MGT_X0Y12...	MGT_X0Y12...	No Link	3.357E11	1.677E11	4.997E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 5	MGT_X0Y13...	MGT_X0Y13...	No Link	3.36E11	1.68E11	4.998E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 6	MGT_X0Y14...	MGT_X0Y14...	No Link	3.368E11	1.757E11	5.217E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 7	MGT_X0Y15...	MGT_X0Y15...	No Link	3.372E11	1.76E11	5.218E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB

# Run IBERT Example Design

► Select the Link Group 0 TX Pattern and set to PRBS 31-bit

The screenshot shows the Vivado 2013.4 Hardware Manager interface for the 'ibert\_bank\_117\_118\_example' project. The 'Links' tab is selected, displaying a table of 16 links (Link 0 to Link 7) grouped under 'Link Group 0 (8)'. The 'TX Pattern' column for Link 0 is currently set to 'PRBS 31-bit', which is highlighted in blue. Other TX patterns shown include PRBS 7-bit, PRBS 15-bit, PRBS 23-bit, Fast Clk, Slow Clk, and PRBS 7-bit. The RX Pattern for all links is set to 'PRBS 7-bit'. The TX Pre-Cursor and TX Post values are also listed for each link.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post
Link Group 0 (8)							Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (0)
Link 0	MGT_X0Y8/TX	MGT_X0Y8/RX	10.000 Gbps	5.301E11	0E0	1.886E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (0)
Link 1	MGT_X0Y9/TX	MGT_X0Y9/RX	No Link	5.303E11	3.049E11	5.75E-1	Reset	PRBS 15-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (0)
Link 2	MGT_X0Y10/TX	MGT_X0Y10/RX	10.000 Gbps	5.307E11	0E0	1.884E-12	Reset	PRBS 23-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (0)
Link 3	MGT_X0Y11/TX	MGT_X0Y11/RX	No Link	5.31E11	3.053E11	5.75E-1	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (0)
Link 4	MGT_X0Y12/TX	MGT_X0Y12/RX	No Link	5.303E11	2.622E11	4.945E-1	Reset	Fast Clk	PRBS 7-bit	1.67 dB (00111)	0.68 dB (0)
Link 5	MGT_X0Y13/TX	MGT_X0Y13/RX	No Link	5.306E11	2.797E11	5.272E-1	Reset	Slow Clk	PRBS 7-bit	1.67 dB (00111)	0.68 dB (0)
Link 6	MGT_X0Y14/TX	MGT_X0Y14/RX	No Link	5.31E11	2.668E11	5.025E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (0)
Link 7	MGT_X0Y15/TX	MGT_X0Y15/RX	No Link	5.323E11	3.194E11	6E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (0)

Link Group: Link Group 0

Note: Presentation applies to the KC705

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# Run IBERT Example Design

- Now all eight links are set to a TX Pattern of PRBS 31-bit
- Repeat with the RX Pattern

The screenshot shows the Vivado 2014.2 Hardware Manager interface for the 'ibert\_bank\_117\_118\_example' project. The main window displays the 'Serial I/O Links' configuration table. The table has columns for Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, RX Pattern, TX Pre-Cursor, and TX Po. There are 8 rows representing Link Group 0, each corresponding to a MGT\_X0Y link pair. All links are currently set to 'No Link'. The TX and RX patterns are all set to 'PRBS 31-bit'. The TX Pre-Cursor and TX Po values are all set to '1.67 dB (00111)' and '0.68 dB' respectively. The BERT Reset column contains 'Reset' buttons for each link.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Po
Ungrouped Links (0)											
Link Group 0 (8)											
Link 0	MGT_X0Y8/TX	MGT_X0Y8/RX	No Link	8.611E11	1.538E11	1.786E-1	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 1	MGT_X0Y9/TX	MGT_X0Y9/RX	No Link	8.615E11	4.905E11	5.693E-1	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 2	MGT_X0Y10...	MGT_X0Y10...	No Link	8.62E11	4.634E10	5.376E-2	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 3	MGT_X0Y11...	MGT_X0Y11...	No Link	8.623E11	4.705E11	5.456E-1	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 4	MGT_X0Y12...	MGT_X0Y12...	No Link	8.614E11	4.7E11	5.457E-1	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 5	MGT_X0Y13...	MGT_X0Y13...	No Link	8.617E11	4.702E11	5.457E-1	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 6	MGT_X0Y14...	MGT_X0Y14...	No Link	8.633E11	4.916E11	5.695E-1	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB
Link 7	MGT_X0Y15...	MGT_X0Y15...	No Link	8.636E11	4.918E11	5.695E-1	Reset	PRBS 31-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB

# Run IBERT Example Design

- Now all eight links are set to a RX Pattern of PRBS 31-bit
- Scroll to the right to set the loopback mode

The screenshot shows the Vivado 2014.2 Hardware Manager interface with the title bar "ibert\_bank\_117\_118\_example - [c:/kc705\_ibert/ibert\_bank\_117\_118/ibert\_bank\_117\_118\_example/ibert\_bank\_117\_118\_example.xpr] - Vivado 2014.2". The main window displays the "Hardware Manager - localhost/xilinx\_tcf/Digilent/210203337270A" tab. A message "write\_bitstream Complete" is visible in the top right. The "Serial I/O Links" table lists eight links under "Link Group 0": Link 0, Link 1, Link 2, Link 3, Link 4, Link 5, Link 6, and Link 7. All links are currently set to "No Link". The table includes columns for Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, RX Pattern, TX Pre-Cursor, and TX Po. The TX and RX columns show port assignments like MGT\_X0Y8/TX and MGT\_X0Y8/RX. The TX Pattern column for all links is set to "PRBS 31-bit". The RX Pattern column also shows "PRBS 31-bit". The TX Pre-Cursor and TX Po columns have dropdown menus. The bottom navigation bar includes tabs for Td Console, Messages, Serial I/O Links (which is selected), and Serial I/O Scans.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Po
Ungrouped Links (0)											
Link Group 0 (8)											
Link 0	MGT_X0Y8/TX	MGT_X0Y8/RX	10.000 Gbps	1.639E12	2.646E11	1.614E-1	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 1	MGT_X0Y9/TX	MGT_X0Y9/RX	No Link	1.639E12	8.876E11	5.414E-1	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 2	MGT_X0Y10...	MGT_X0Y10...	10.000 Gbps	1.624E12	1.566E11	9.643E-2	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 3	MGT_X0Y11...	MGT_X0Y11...	No Link	1.625E12	8.411E11	5.177E-1	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 4	MGT_X0Y12...	MGT_X0Y12...	No Link	1.623E12	1.111E12	6.846E-1	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 5	MGT_X0Y13...	MGT_X0Y13...	No Link	1.623E12	1.111E12	6.847E-1	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 6	MGT_X0Y14...	MGT_X0Y14...	No Link	1.626E12	8.812E11	5.42E-1	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 7	MGT_X0Y15...	MGT_X0Y15...	No Link	1.626E12	8.813E11	5.42E-1	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB

# Run IBERT Example Design

- Scroll to the right to find Loopback Mode
- Set all but the first and third GTXs to Near-End PCS

The screenshot shows the Vivado 2014.2 Hardware Manager interface with the title bar "ibert\_bank\_117\_118\_example - [c:/kc705\_ibert/ibert\_bank\_117\_118/ibert\_bank\_117\_118\_example/ibert\_bank\_117\_118\_example.xpr] - Vivado 2014.2". The main window displays the "Hardware Manager" for "localhost/xilinx\_tcf/Digilent/210203337270A". The "Serial I/O Links" table has the following columns: RX Pattern, TX Pre-Cursor, TX Post-Cursor, TX Diff Swing, DFE Enabled, Inject Error, TX Reset, RX Reset, RX PLL Status, TX PLL Status, and Loopback Mode. A red box highlights the "Loopback Mode" column for the second through tenth rows, which are all set to "Near-End PCS".

	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset				Multiple
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked		None
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked		Near-End PCS
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked		None
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked		Near-End PCS
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked		Near-End PCS
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked		Near-End PCS
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked		Near-End PCS
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked		Near-End PCS

# Run IBERT Example Design

► Click the BERT Reset button for Link Group 0 to reset all eight links

The screenshot shows the Vivado 2014.2 Hardware Manager interface for the 'ibert\_bank\_117\_118\_example' project. The main window displays the 'Serial I/O Links' table. The table has columns for Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, RX Pattern, TX Pre-Cursor, and TX Post-Cursor. A red box highlights the 'Reset' button for the first link in 'Link Group 0'. The table lists 8 links under 'Link Group 0' and 1 link under 'Ungrouped Links'. All links show 10.000 Gbps as their speed.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor
Ungrouped Links (0)											
Link Group 0 (8)											
Link 0	MGT_X0Y8/TX	MGT_X0Y8/RX	10.000 Gbps	6.83E10	0E0	1.464E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 1	MGT_X0Y9/TX	MGT_X0Y9/RX	10.000 Gbps	6.856E10	0E0	1.459E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 2	MGT_X0Y10...	MGT_X0Y10...	10.000 Gbps	6.877E10	0E0	1.454E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 3	MGT_X0Y11...	MGT_X0Y11...	10.000 Gbps	6.909E10	0E0	1.447E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 4	MGT_X0Y12...	MGT_X0Y12...	10.000 Gbps	6.929E10	0E0	1.443E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 5	MGT_X0Y13...	MGT_X0Y13...	10.000 Gbps	6.96E10	0E0	1.437E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 6	MGT_X0Y14...	MGT_X0Y14...	10.000 Gbps	6.983E10	0E0	1.432E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB
Link 7	MGT_X0Y15...	MGT_X0Y15...	10.000 Gbps	7.009E10	0E0	1.427E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB

# Run IBERT Example Design

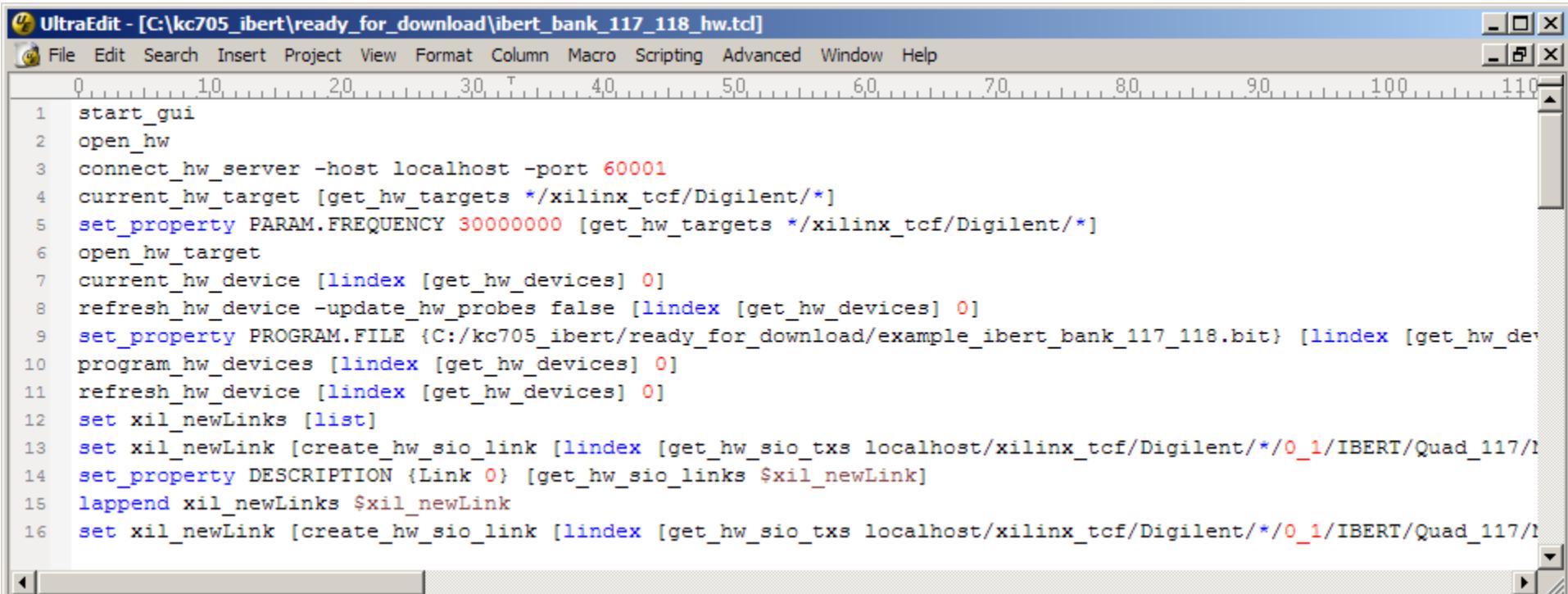
- If any channels are not resetting from the previous step, scroll to the right and click TX Reset and RX Reset

The screenshot shows the Vivado 2014.2 Hardware Manager interface with the title bar "ibert\_bank\_117\_118\_example - [c:/kc705\_ibert/ibert\_bank\_117\_118/ibert\_bank\_117\_118\_example/ibert\_bank\_117\_118\_example.xpr] - Vivado 2014.2". The main window displays the "Hardware Manager - localhost/xilinx\_tcf/Digilent/210203337270A" tab. The "Serial I/O Links" table has the following columns: RX Pattern, TX Pre-Cursor, TX Post-Cursor, TX Diff Swing, DFE Enabled, Inject Error, TX Reset, RX Reset, RX PLL Status, TX PLL Status, and Loopback Mode. There are ten rows, each representing a PRBS 31-bit link. The "TX Reset" and "RX Reset" columns contain "Inject" and "Reset" buttons. The "Reset" button for the first row is highlighted with a red box. The "RX PLL Status" and "TX PLL Status" columns show various states like Locked, Locked, and Near-End PCS.

RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset			Multiple
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	None
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	None
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS
PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV ...	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS

# Run IBERT Example Design

- The Hardware Manager actions are captured in the Vivado JOU file as Tcl commands; these can be used for scripting this test
- Review ready\_for\_download/ibert\_bank\_117\_118\_hw.tcl for an example of this



The screenshot shows a window titled "UltraEdit - [C:\kc705\_ibert\ready\_for\_download\ibert\_bank\_117\_118\_hw.tcl]" containing a Tcl script. The script performs several actions to prepare and program an Xilinx device:

```
1 start_gui
2 open_hw
3 connect_hw_server -host localhost -port 60001
4 current_hw_target [get_hw_targets */xilinx_tcf/Digilent/*]
5 set_property PARAM.FREQUENCY 30000000 [get_hw_targets */xilinx_tcf/Digilent/*]
6 open_hw_target
7 current_hw_device [lindex [get_hw_devices] 0]
8 refresh_hw_device -update_hw_probes false [lindex [get_hw_devices] 0]
9 set_property PROGRAM.FILE {C:/kc705_ibert/ready_for_download/example_ibert_bank_117_118.bit} [lindex [get_hw_devi
10 program_hw_devices [lindex [get_hw_devices] 0]
11 refresh_hw_device [lindex [get_hw_devices] 0]
12 set xil_newLinks [list]
13 set xil_newLink [create_hw_sio_link [lindex [get_hw_sio_txs localhost/xilinx_tcf/Digilent/*/0_1/IBERT/Quad_117/1
14 set_property DESCRIPTION {Link 0} [get_hw_sio_links $xil_newLink]
15 lappend xil_newLinks $xil_newLink
16 set xil_newLink [create_hw_sio_link [lindex [get_hw_sio_txs localhost/xilinx_tcf/Digilent/*/0_1/IBERT/Quad_117/1
```

## References

# References

## ➤ IBERT IP

- LogiCORE IP Integrated Bit Error Ratio Tester for 7 Series GTX
  - [http://www.xilinx.com/support/documentation/ip\\_documentation/ibert\\_7series\\_gtx/v3\\_0/pg132-ibert-7series-gtx.pdf](http://www.xilinx.com/support/documentation/ip_documentation/ibert_7series_gtx/v3_0/pg132-ibert-7series-gtx.pdf)

## ➤ Vivado Programming and Debugging

- Vivado Design Suite Programming and Debugging User Guide
  - [http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx2014\\_2/ug908-vivado-programming-debugging.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_2/ug908-vivado-programming-debugging.pdf)

# Documentation

# Documentation

## ► Kintex-7

- Kintex-7 FPGA Family
  - <http://www.xilinx.com/products/silicon-devices/fpga/kintex-7/index.htm>
- Design Advisory Master Answer Record for Kintex-7 FPGAs
  - <http://www.xilinx.com/support/answers/42946.htm>

## ► KC705 Documentation

- Kintex-7 FPGA KC705 Evaluation Kit
  - <http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm>
- KC705 Getting Started Guide
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/kc705/2013\\_2/ug883\\_K7\\_KC705\\_Eval\\_Kit.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/kc705/2013_2/ug883_K7_KC705_Eval_Kit.pdf)
- KC705 User Guide
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/kc705/ug810\\_KC705\\_Eval\\_Bd.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/kc705/ug810_KC705_Eval_Bd.pdf)