



KC705 PCIe Design Creation

June 2014

XTP197

Revision History

Date	Version	Description
06/09/14	9.0	Recompiled for 2014.2. AR44635 and AR54939 fixed.
04/16/14	8.0	Recompiled for 2014.1.
12/18/13	7.0	Recompiled for 2013.4.
10/23/13	6.0	Recompiled for 2013.3. Added AR54939.
06/19/13	5.0	Recompiled for 2013.2. AR55494 fixed.
04/03/13	4.0	Recompiled for 2013.1. Added AR55494.
12/18/12	3.0	Recompiled for 2012.4. Added AR53392.
10/23/12	2.0	Recompiled for 2012.3. Added AR52368.
08/20/12	1.0	Initial version. Added AR50886.

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Kintex-7 PCIe x8 Gen 2 Capability

► KC705 Supports PCIe Gen 1 and Gen 2 Capability

- x8, x4, x2, or x1 Gen 1 and Gen 2 lane width
- x8 Gen 2 not supported in -1 parts
- See [PG054](#) for details

► LogiCORE PIO Example Design

- RDF0187 - KC705 PCIe Design Files (2014.2 C) zip file
- Available through <http://www.xilinx.com/kc705>

► 7 Series Integrated Block for PCI Express

- See [PG054](#) for details

Kintex-7 PCIe x8 Gen 2 Capability

➤ Integrated Block for PCI Express

- PCI Express Base 2.0 Specification

➤ Configurable for Endpoint or Root Port Applications

- KC705 configured for Endpoint Applications

➤ GTX Transceivers implement a fully compliant PHY

➤ Large range of maximum payload size

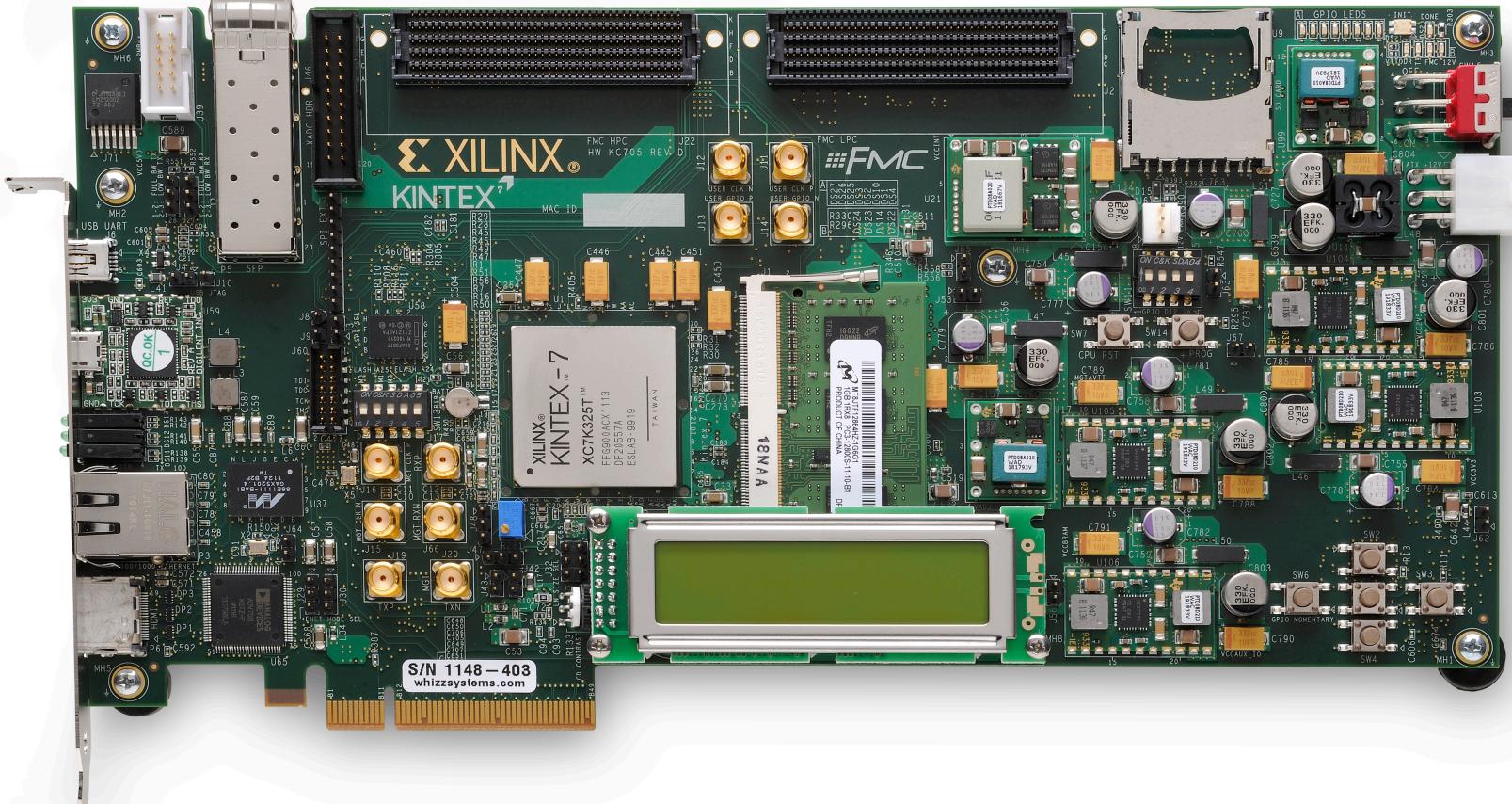
- 128 / 256 / 512 / 1024 bytes

➤ Configurable BAR spaces

- Up to 6 x 32 bit, 3 x 64 bit, or a combination
- Memory or IO
- BAR and ID filtering

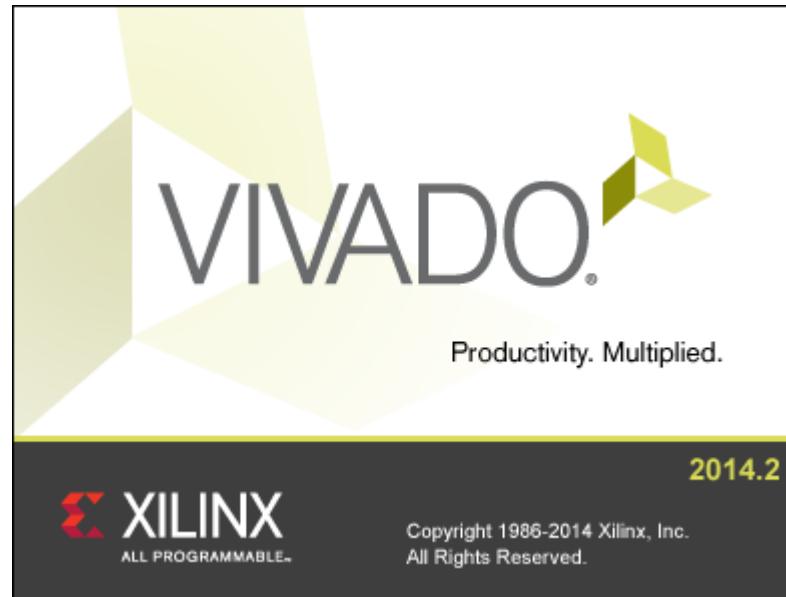
➤ Management and Statistics Interface

Xilinx KC705 Board



Vivado Software Requirements

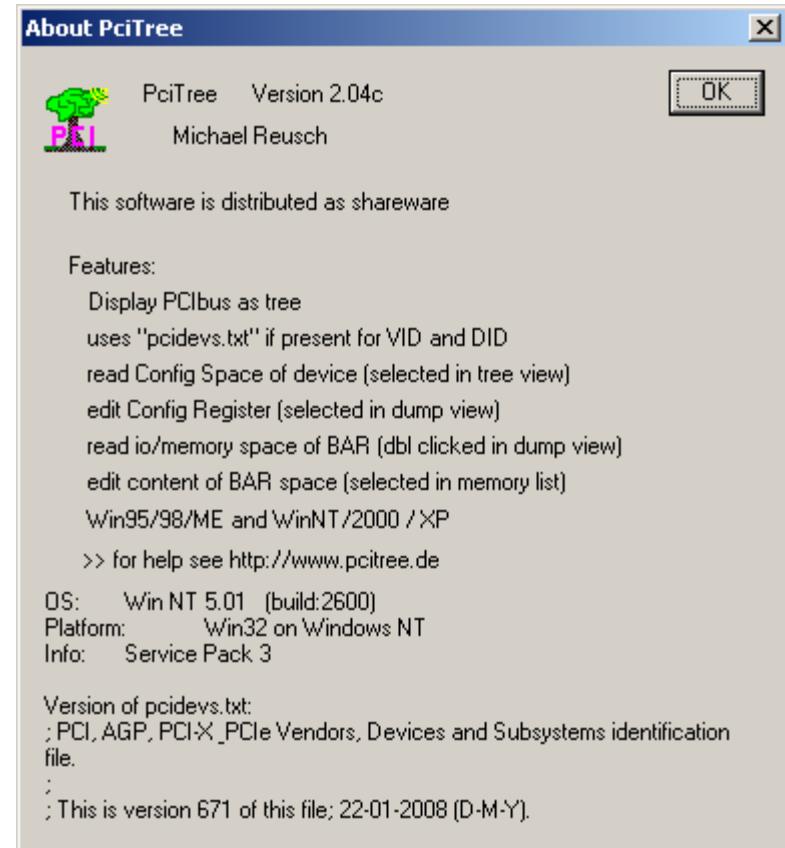
- Xilinx Vivado Design Suite 2014.2, Design Edition



PciTree Software Requirement

► PciTree Bus Viewer

- Free [download](#)
- HLP.SYS must be copied to
C:\WINDOWS\system32\drivers
directory



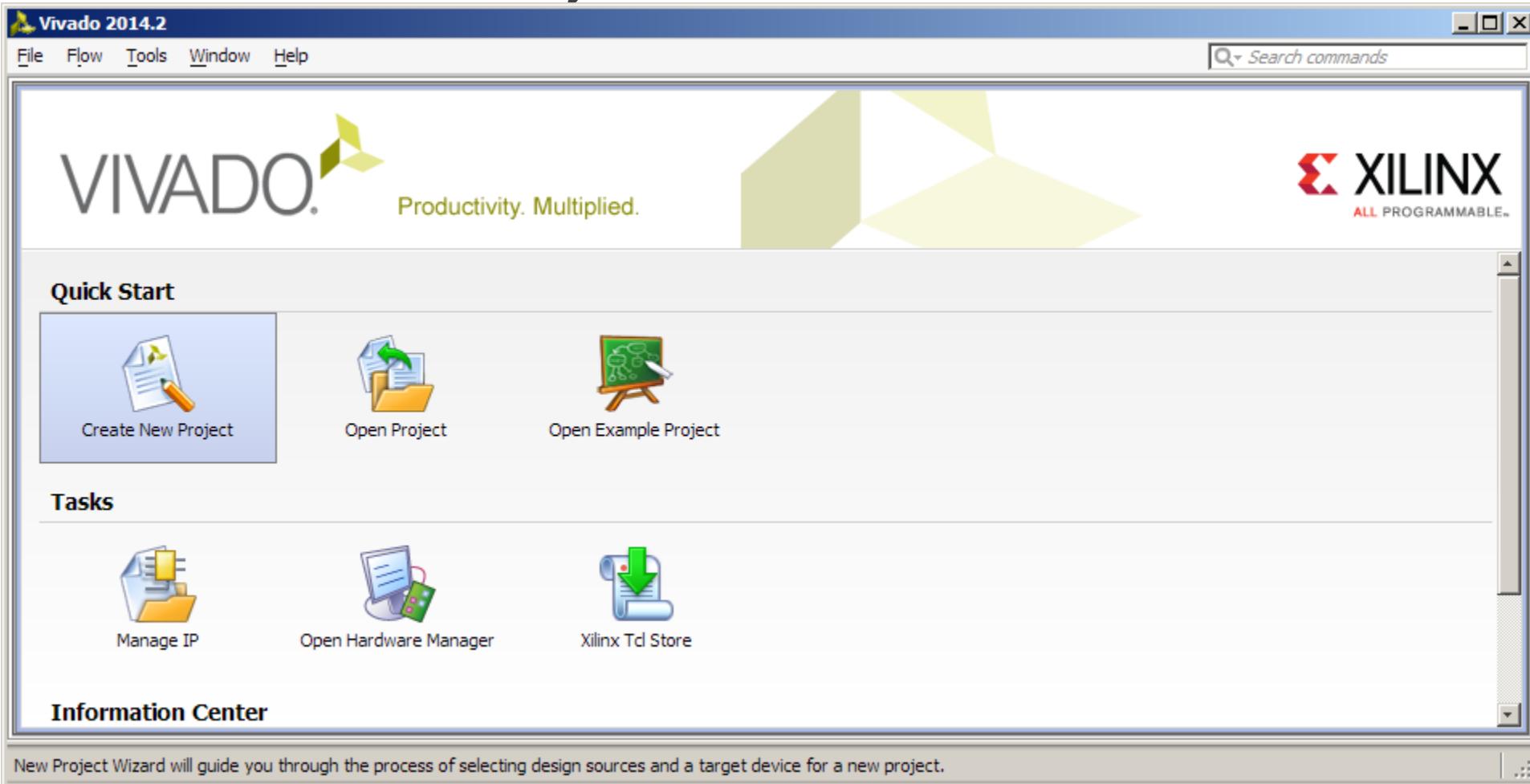
Generate x8 Gen 2 PCIe Core

Generate x8 Gen 2 PCIe Core

► Open Vivado

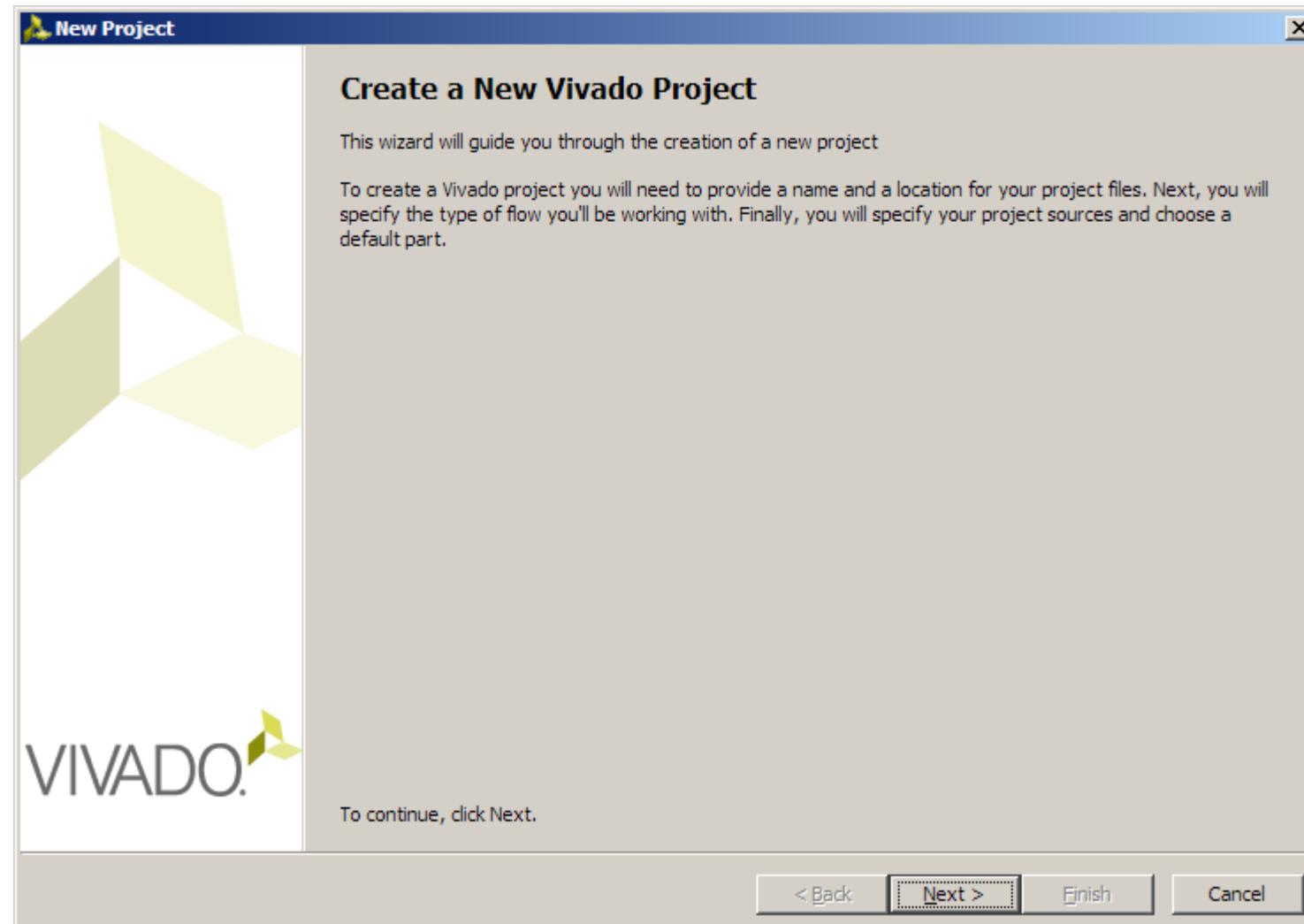
Start → All Programs → Xilinx Design Tools → Vivado 2014.2 → Vivado

► Select Create New Project



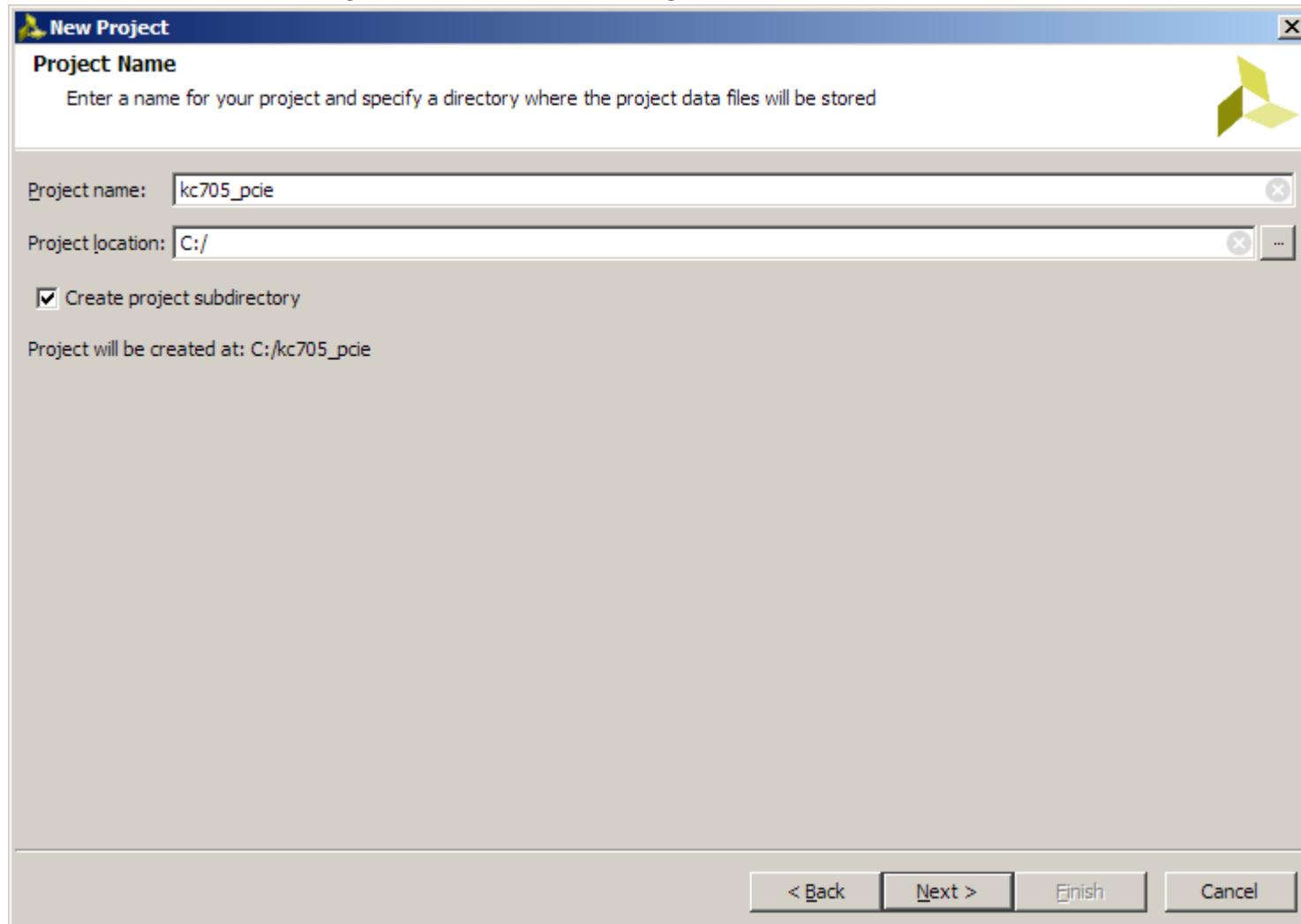
Generate x8 Gen 2 PCIe Core

► Click Next



Generate x8 Gen 2 PCIe Core

- Set the Project name and location to **kc705_pcnie** and **C:**
 - Check **Create project subdirectory**



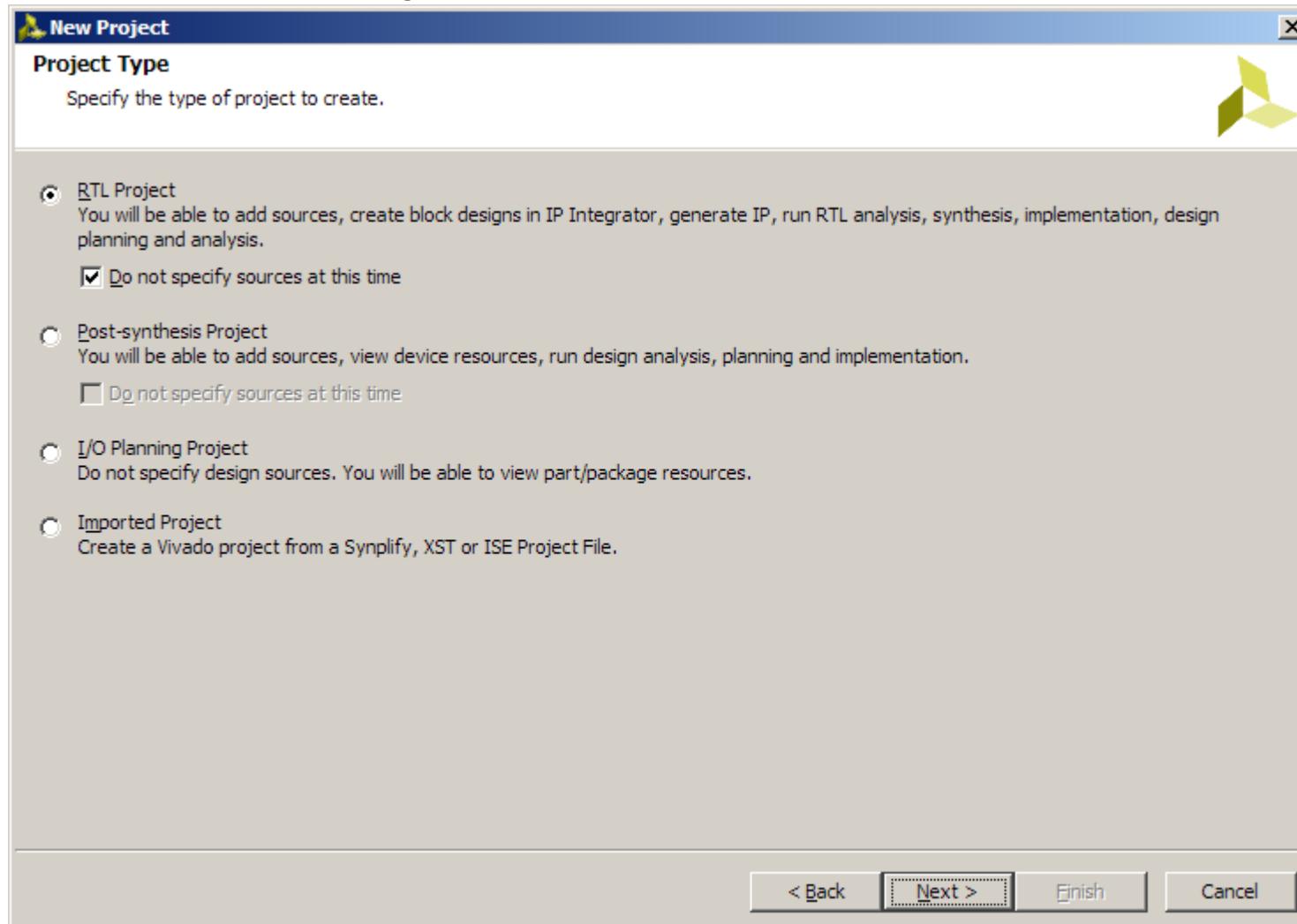
Note: Vivado generally requires forward slashes in paths

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Generate x8 Gen 2 PCIe Core

► Select RTL Project

- Select **Do not specify sources at this time**



Generate x8 Gen 2 PCIe Core

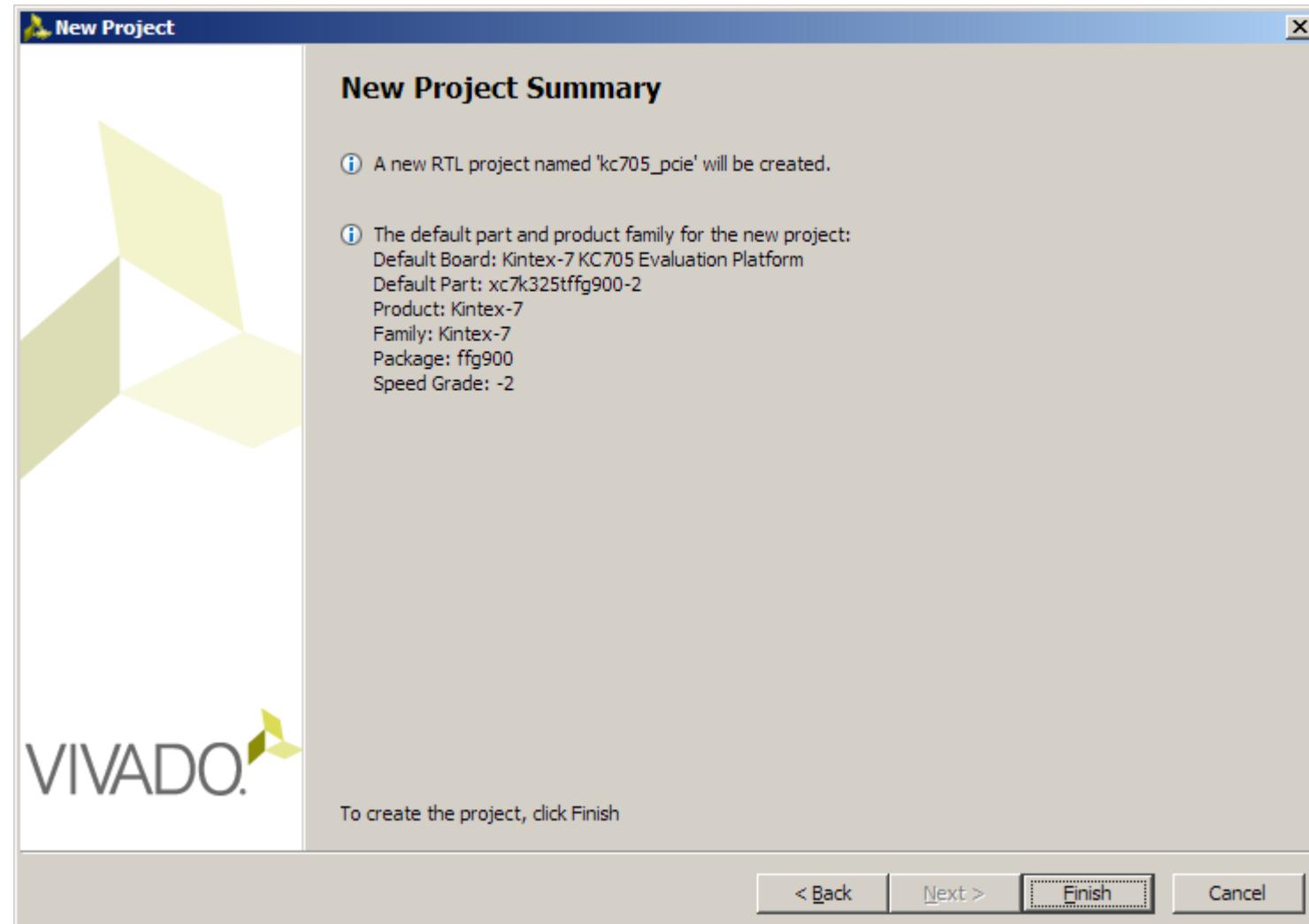
► Select the KC705 Board

The screenshot shows the 'New Project' dialog with the title 'Default Part'. It displays a search bar and filter options for selecting a Xilinx part or board. The 'Boards' tab is selected. A table lists various evaluation boards, with the 'Kintex-7 KC705 Evaluation Platform' highlighted. The table columns include Display Name, Vendor, Board Rev, Part, I/O Pin Count, File Version, and Available IOBs.

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version	Available IOBs
MicroZed Board	em.avnet.com	e	xc7z010clg400-1	400	1.0	100
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1	484	1.0	200
Artix-7 AC701 Evaluation Platform	xilinx.com	1.0	xc7a200tfgb676-2	676	1.0	400
Kintex-7 KC705 Evaluation Platform	xilinx.com	1.1	xc7k325tffg900-2	900	1.0	500
Virtex-7 VC707 Evaluation Platform	xilinx.com	1.1	xc7vx485tffg1761-2	1,761	1.0	700
Virtex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2	1,761	1.0	850
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020clg484-1	484	1.0	200
ZYNQ-7 ZC706 Evaluation Board	xilinx.com	1.1	xc7z045ffg900-2	900	1.0	362

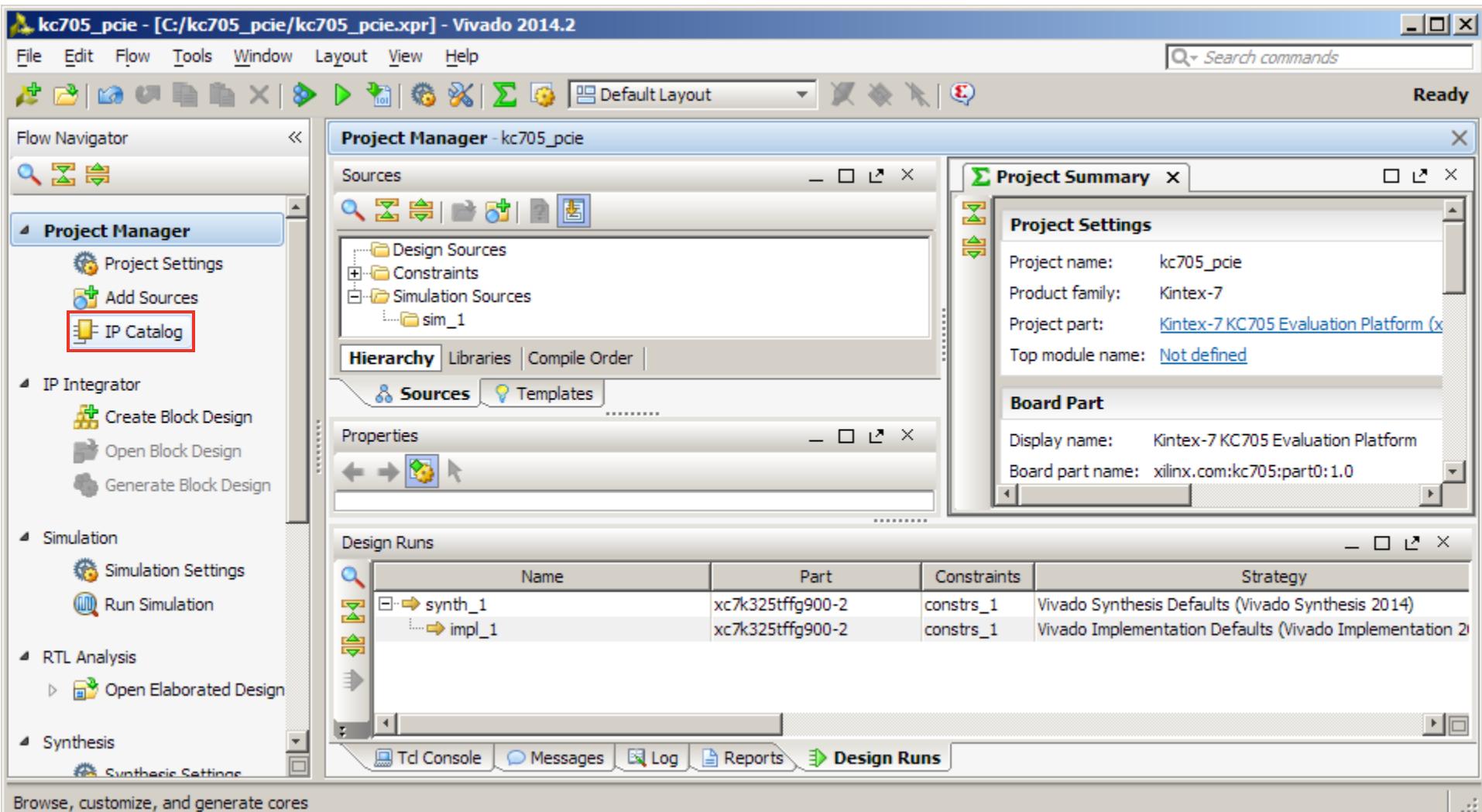
Generate x8 Gen 2 PCIe Core

► Click Finish



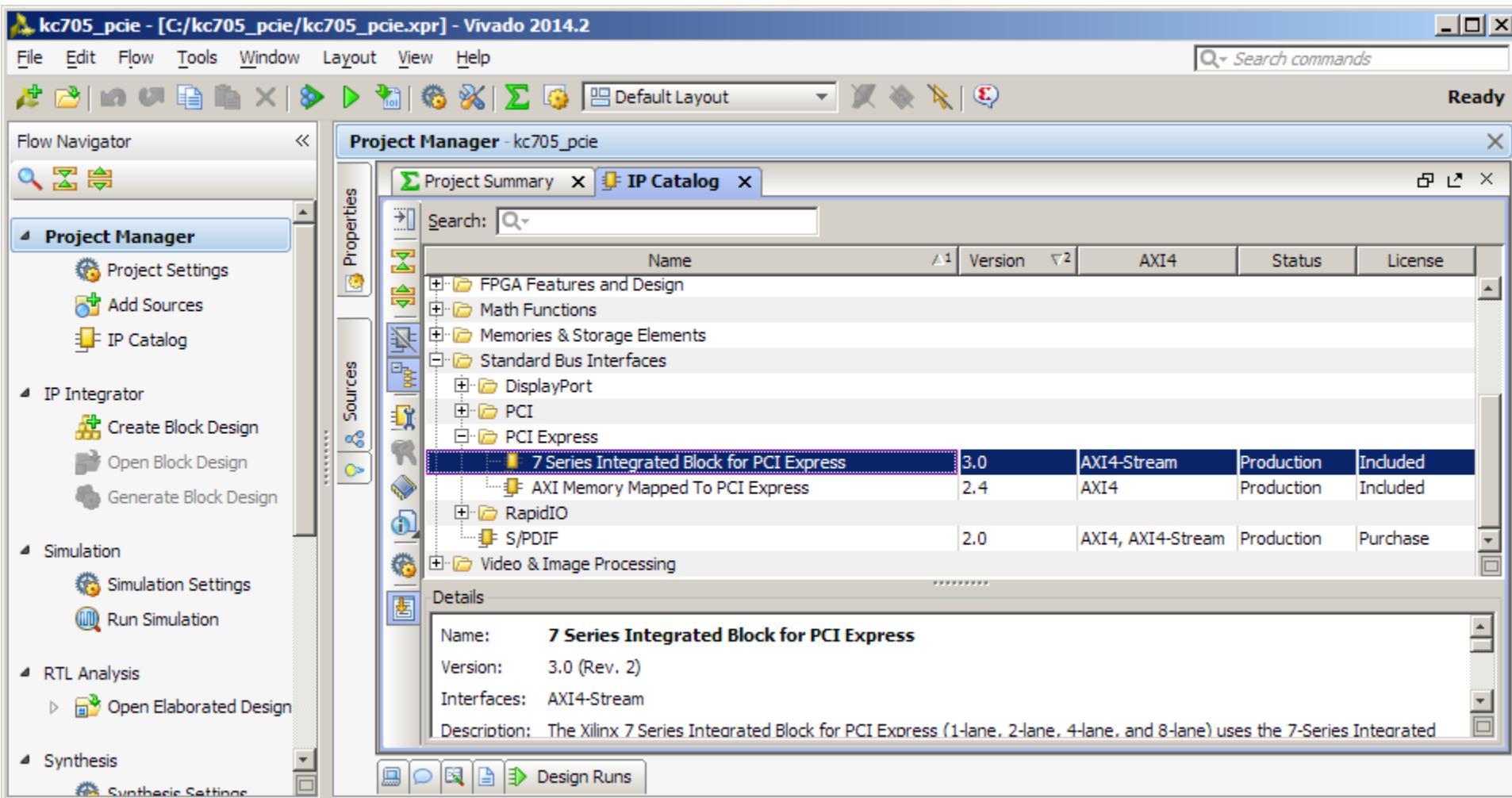
Generate x8 Gen 2 PCIe Core

► Click on IP Catalog



Generate x8 Gen 2 PCIe Core

- Select 7 Series Integrated Block for PCI Express, v3.0 under Standard Bus Interfaces



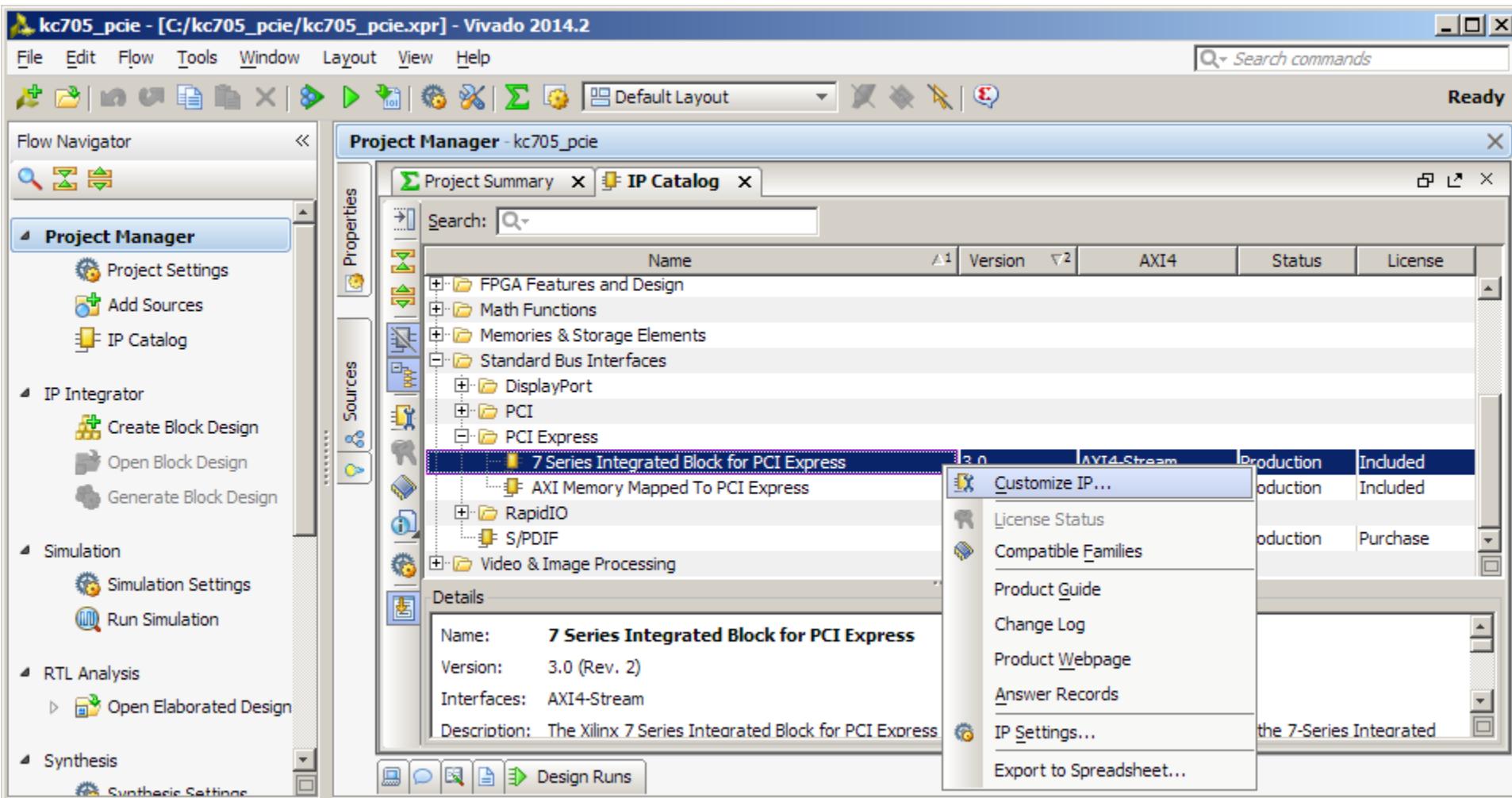
IP: 7 Series Integrated Block for PCI Express

Note: Presentation applies to the KC705

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Generate x8 Gen 2 PCIe Core

- ▶ Right click on 7 Series Integrated Block for PCI Express
 - Select Customize IP...

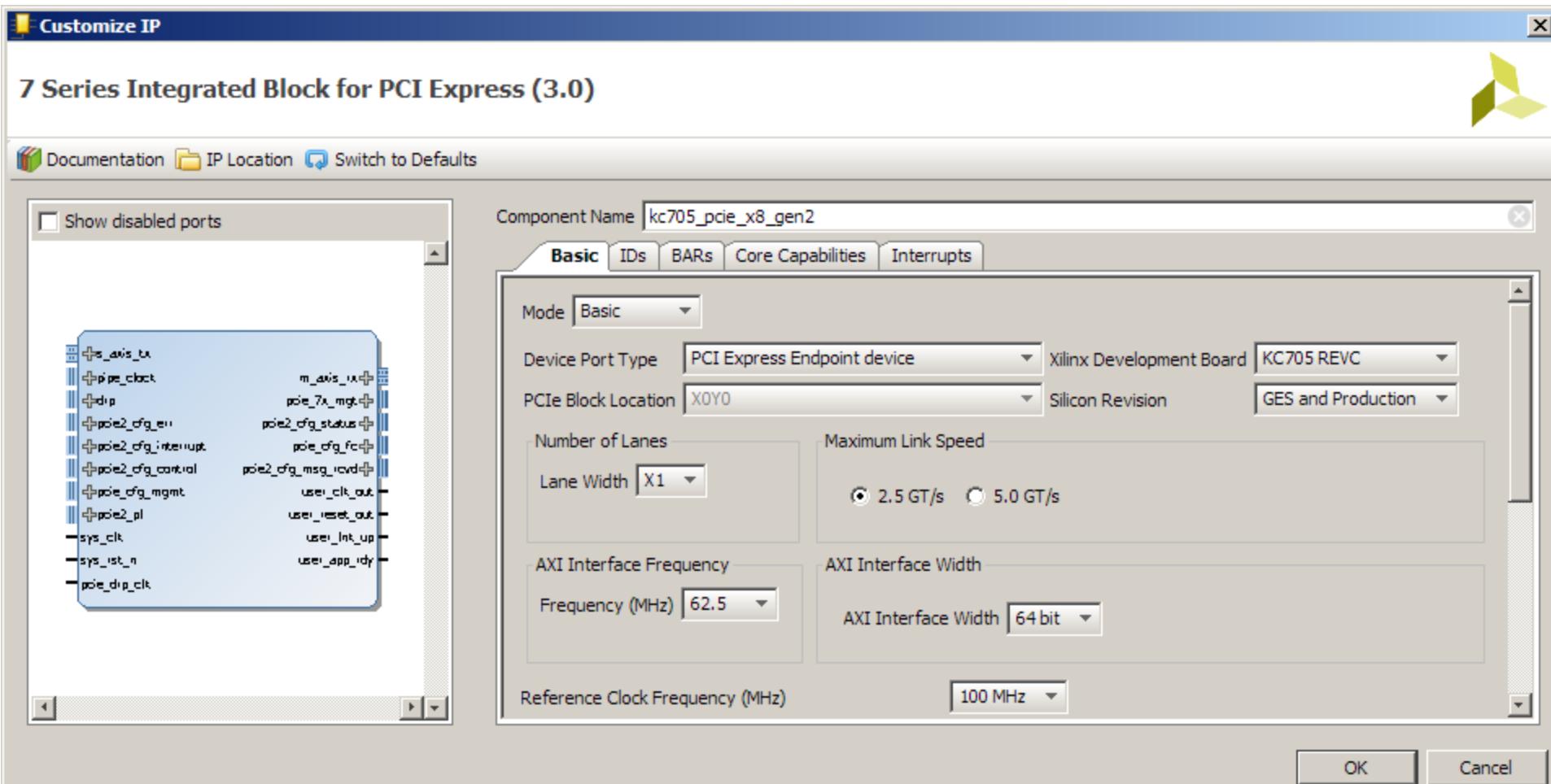


Customize the selected core

Generate x8 Gen 2 PCIe Core

► Under the Basic tab,

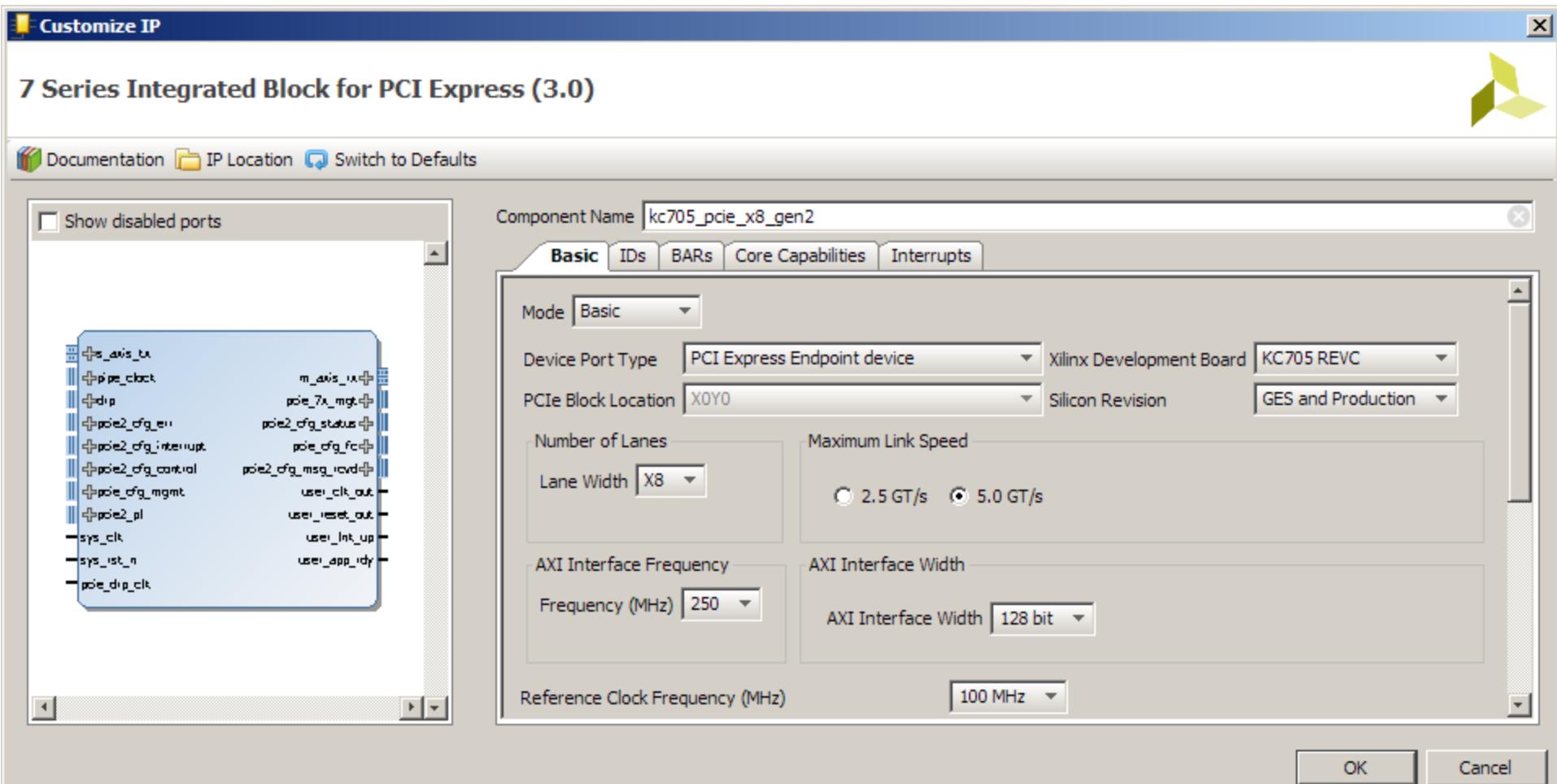
- Set Component name to **kc705_pcie_x8_gen2**
- Set Development Board to **KC705 REVC**
- Set Silicon to **GES and Production**



Generate x8 Gen 2 PCIe Core

► Under the Basic tab,

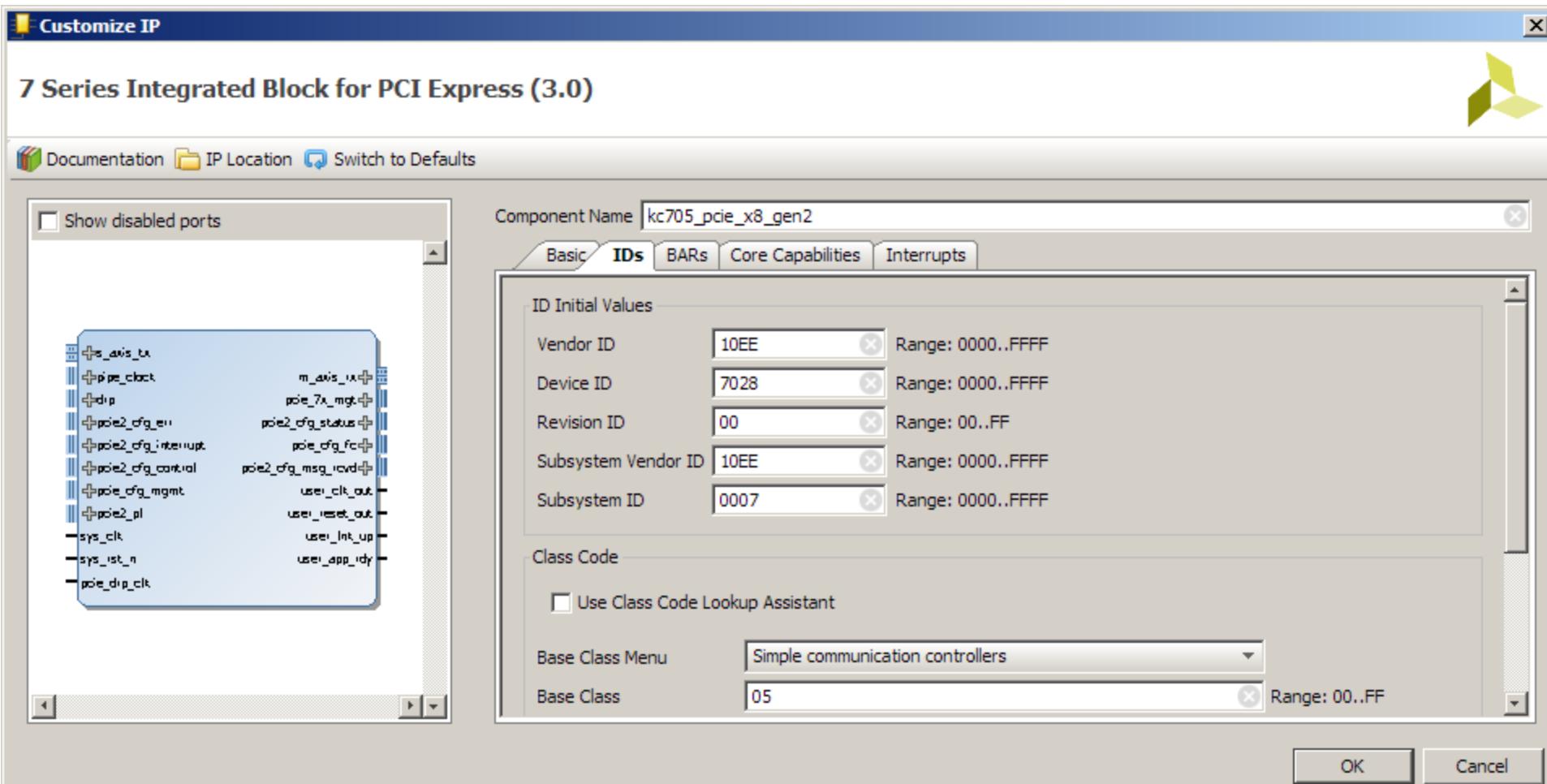
- Set the Lane Width to **X8**
- Set the Max Link Speed to **5 GT/s**
- Set the Ref Clock to **100 MHz**



Generate x8 Gen 2 PCIe Core

► Under the IDs tab, note the ID Initial Values

- Vendor ID = **10EE**; Device ID = **7028**; Revision ID = **00**
- Subsystem Vendor ID = **10EE**; Subsystem ID = **0007**

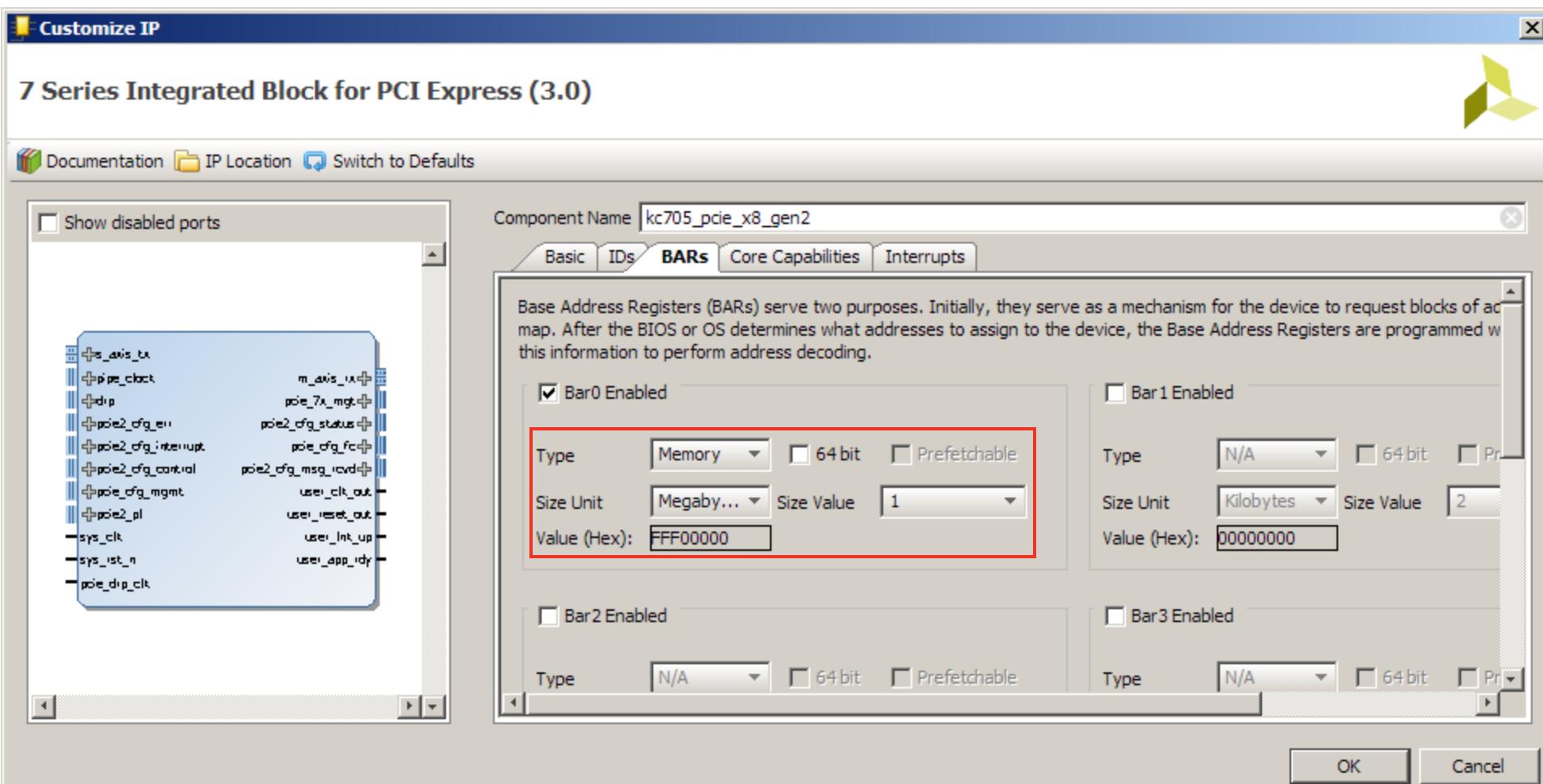


Generate x8 Gen 2 PCIe Core

► Under the BARs tab, set BAR 0

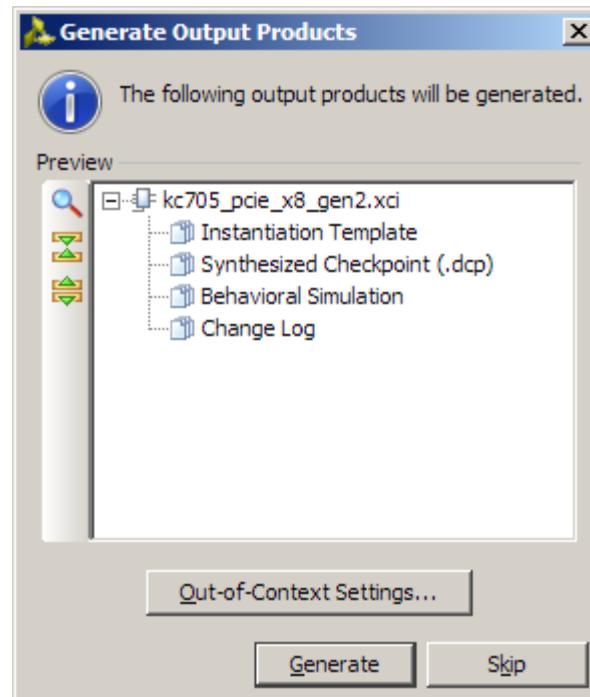
- Set to 1 Megabytes

► Click OK



Generate x8 Gen 2 PCIe Core

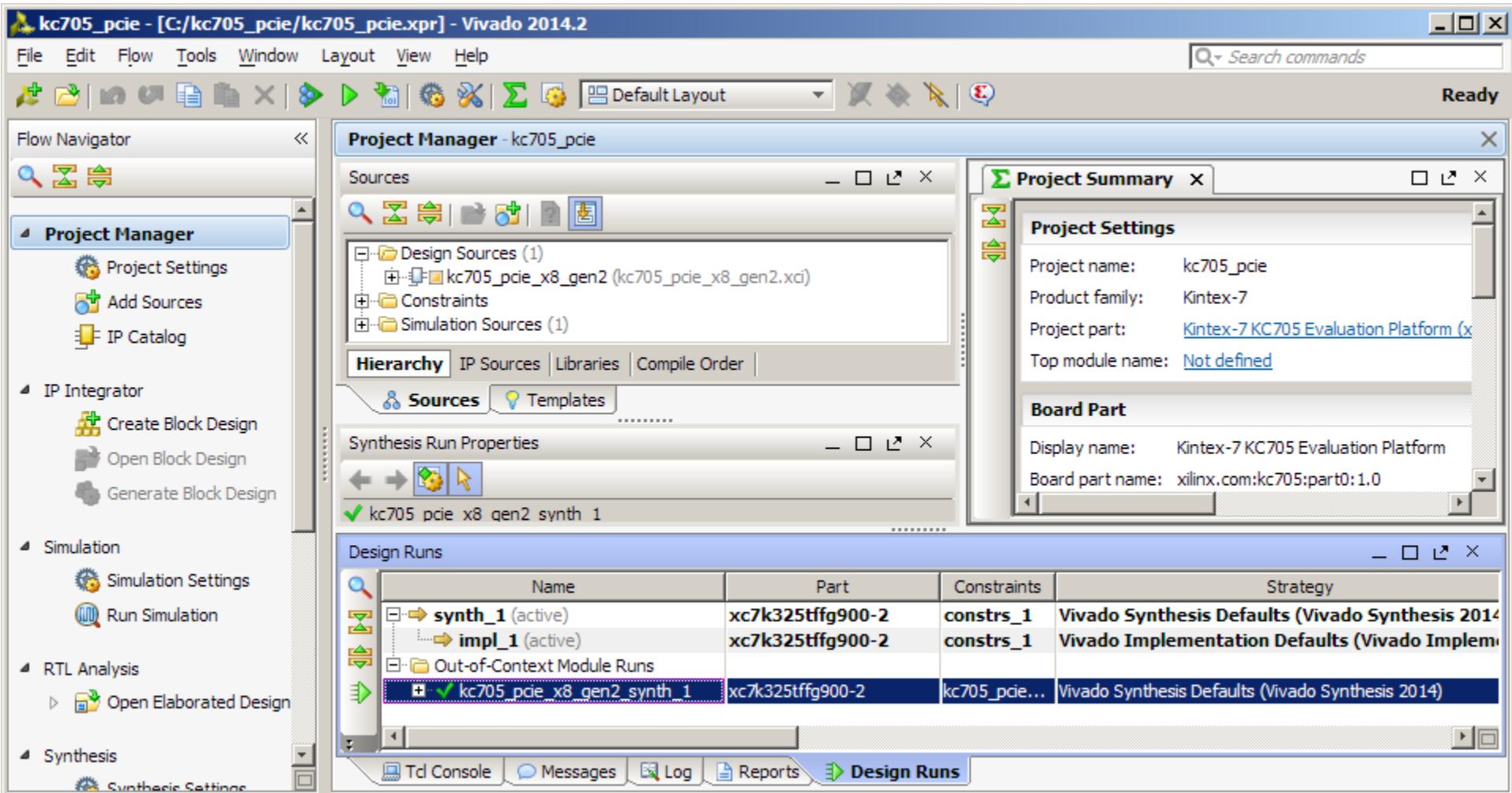
► Click Generate



Generate x8 Gen 2 PCIe Core

► PCIe design appears in Design Sources

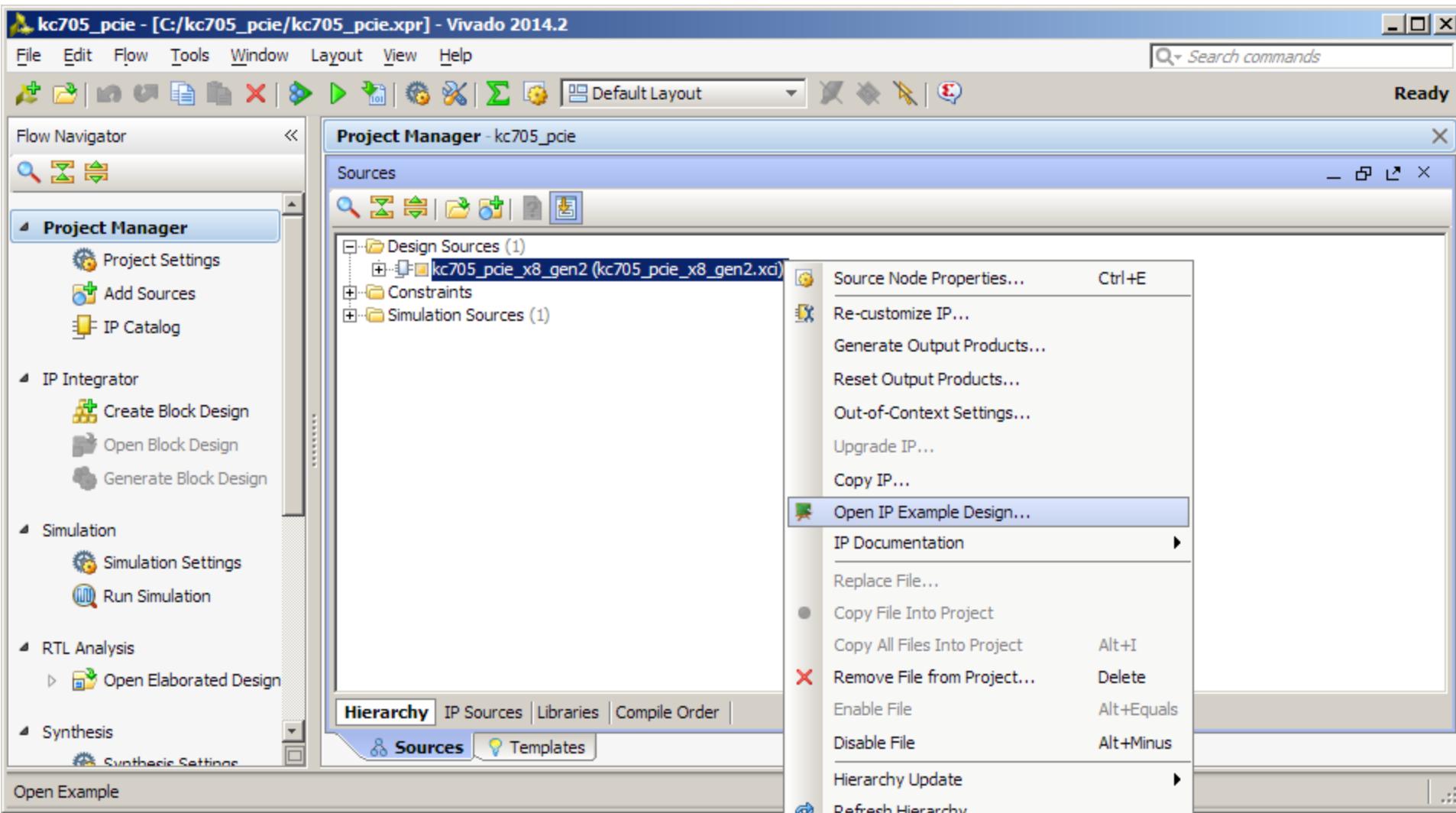
- Wait until checkmark appears on kc705_PCIE_x8_gen2_synth_1



Synthesis Run: kc705_PCIE_x8_gen2_synth_1

Generate x8 Gen 2 PCIe Core

- Right-click on `kc705_pcie_x8_gen2` and select Open IP Example Design...

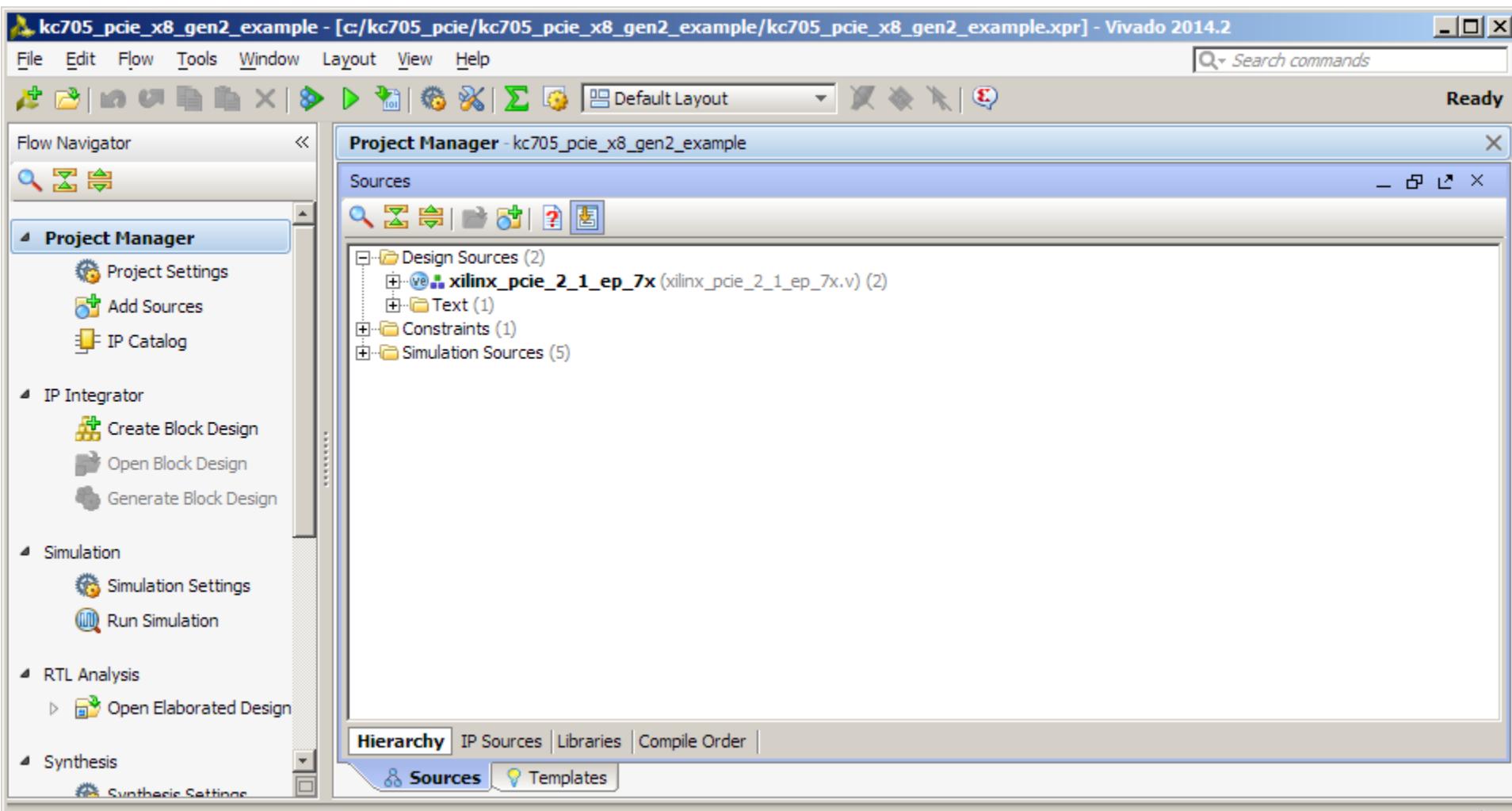


Note: Presentation applies to the KC705

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Generate x8 Gen 2 PCIe Core

- A new project is created under <design path>/
kc705_pcie_x8_gen2_example



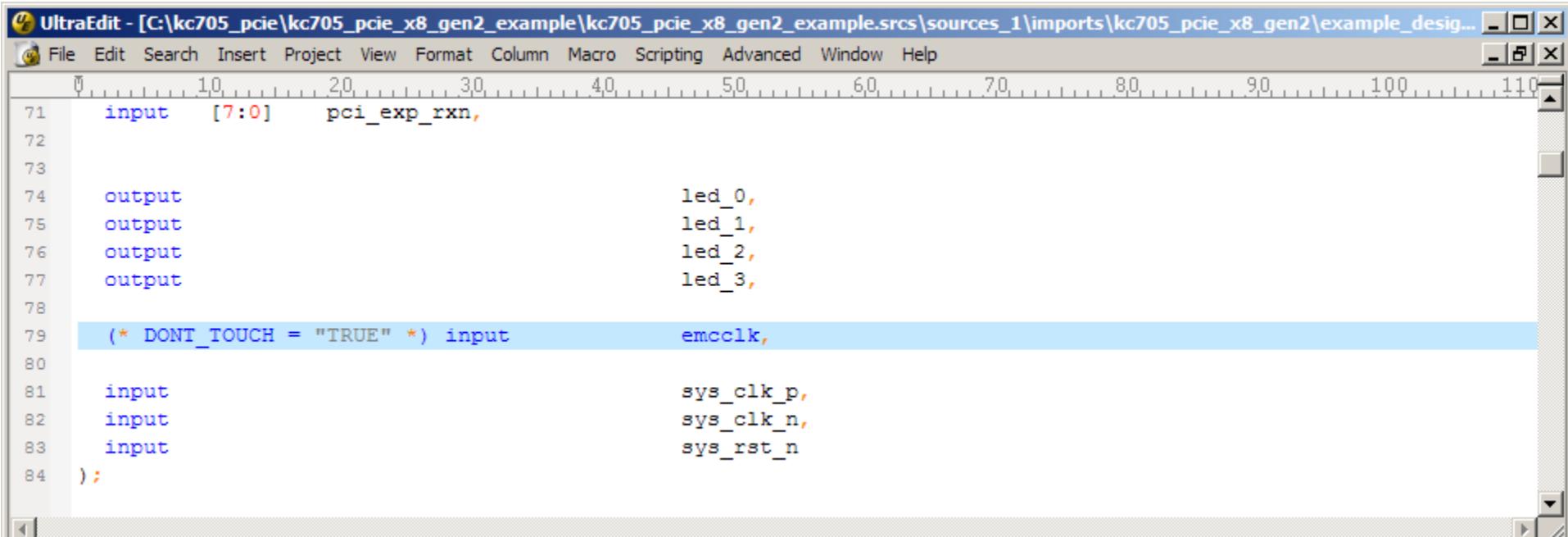
Note: The original project window can be closed

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Modify PCIe Core

► As per [AR44635](#), the design must be modified

- Open the file: <design path>\kc705_pcie_x8_gen2_example\kc705_pcie_x8_gen2_example.srcs\sources_1\imports\example_design\xilinx_pcie_2_1_ep_7x.v
- Add this line:
(* DONT_TOUCH = "TRUE" *) input emcclk,



The screenshot shows a code editor window titled "UltraEdit - [C:\kc705_pcie\kc705_pcie_x8_gen2_example\kc705_pcie_x8_gen2_example.srcs\sources_1\imports\kc705_pcie_x8_gen2\example_design\xilinx_pcie_2_1_ep_7x.v]". The file contains Verilog code. Line 79 has a blue background highlight, indicating the line where the new code was added.

```
71    input  [7:0]   pci_exp_rxn,
72
73
74    output          led_0,
75    output          led_1,
76    output          led_2,
77    output          led_3,
78
79    (* DONT_TOUCH = "TRUE" *) input      emcclk,
80
81    input           sys_clk_p,
82    input           sys_clk_n,
83    input           sys_rst_n
84  );
```

Note: Do this after creating the example design

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Modify PCIe Core

► As per [AR44635](#), the design must be modified

- Open the XDC file: <design path>\kc705_pcie_x8_gen2_example\kc705_pcie_x8_gen2_example.srcs\constrs_1\imports\example_design\xilinx_pcie_7x_ep_x8g2_KC705_REV.C.xdc
- Add these lines:
set_property IOSTANDARD LVCMOS25 [get_ports emcclk]
set_property LOC R24 [get_ports emcclk]



The screenshot shows the UltraEdit text editor displaying an XDC (Hardware Constraints Description) file. The file contains various set_property commands for pins like led_0 through led_3, along with comments for a user clock and physical constraints. The specific lines being added or modified are highlighted in blue.

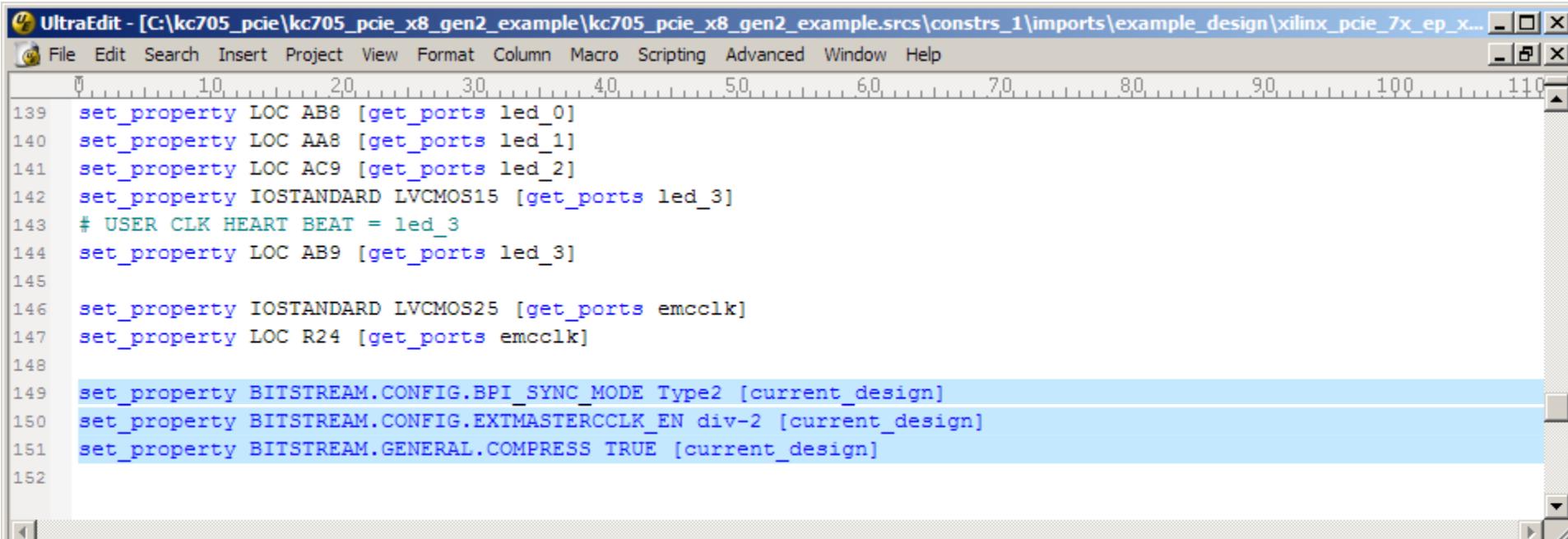
```
UltraEdit - [C:\kc705_pcie\kc705_pcie_x8_gen2_example\kc705_pcie_x8_gen2_example.srcs\constrs_1\imports\example_design\xilinx_pcie_7x_ep_x8g2_KC705_REV.C.xdc]
File Edit Search Insert Project View Format Column Macro Scripting Advanced Window Help
139 set_property LOC AB8 [get_ports led_0]
140 set_property LOC AA8 [get_ports led_1]
141 set_property LOC AC9 [get_ports led_2]
142 set_property IOSTANDARD LVCMOS15 [get_ports led_3]
143 # USER CLK HEART BEAT = led_3
144 set_property LOC AB9 [get_ports led_3]
145
146 set_property IOSTANDARD LVCMOS25 [get_ports emcclk]
147 set_property LOC R24 [get_ports emcclk]
148
149 #####
150 # Physical Constraints
151 #####
152 #
```

Modify PCIe Core

► As per [UG470](#), [UG908](#), and [P30 Flash](#) specifications

- In the XDC file, `xilinx_pcie_7x_ep_x8g2_KC705_REV.C.xdc`, add these lines:

```
set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type2 [current_design]
set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-2 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
```



The screenshot shows a Windows-based text editor window titled "UltraEdit - [C:\kc705_PCIE\kc705_PCIE_X8_GEN2_EXAMPLE\kc705_PCIE_X8_GEN2_EXAMPLE.srcts\constrs_1\imports\example_design\xilinx_pcie_7x_ep_x...]" with a status bar indicating line numbers from 139 to 152. The menu bar includes File, Edit, Search, Insert, Project, View, Format, Column, Macro, Scripting, Advanced, Window, and Help. The main text area contains XDC configuration code. Lines 149 through 151 are highlighted in blue, indicating the new properties added to the file.

```
139 set_property LOC AB8 [get_ports led_0]
140 set_property LOC AA8 [get_ports led_1]
141 set_property LOC AC9 [get_ports led_2]
142 set_property IOSTANDARD LVCMOS15 [get_ports led_3]
143 # USER CLK HEART BEAT = led_3
144 set_property LOC AB9 [get_ports led_3]
145
146 set_property IOSTANDARD LVCMOS25 [get_ports emccclk]
147 set_property LOC R24 [get_ports emccclk]
148
149 set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type2 [current_design]
150 set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-2 [current_design]
151 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
152
```

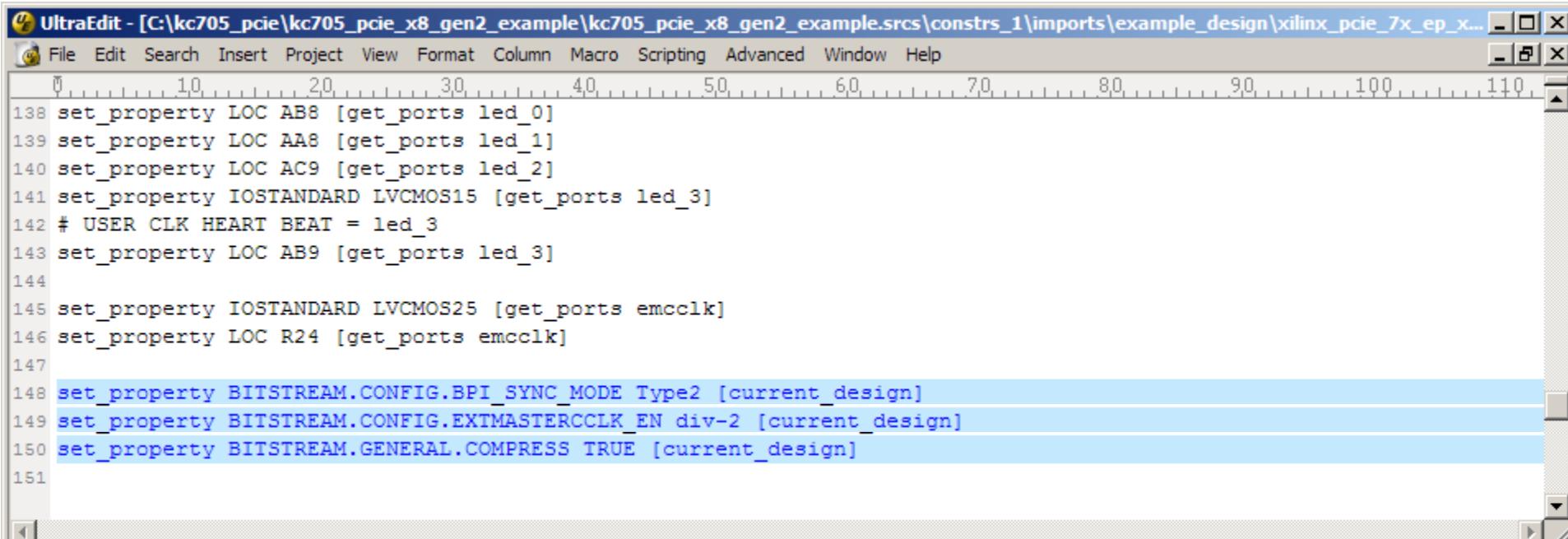
Note: Do this after creating the example design

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Modify PCIe Core

► Details on the XDC constraints :

- P30T Maximum Frequency: 52 MHz; KC705 EMCCLK Frequency: 66 MHz
- **BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-2**: Sets the EMCCLK in the FPGA to divide by 2, which meets the P30T Maximum Frequency specification
- **BITSTREAM.CONFIG.BPI_SYNC_MODE Type2**: For Numonyx P30 Family
- **BITSTREAM.GENERAL.COMPRESS TRUE**: Shrinks the bitstream

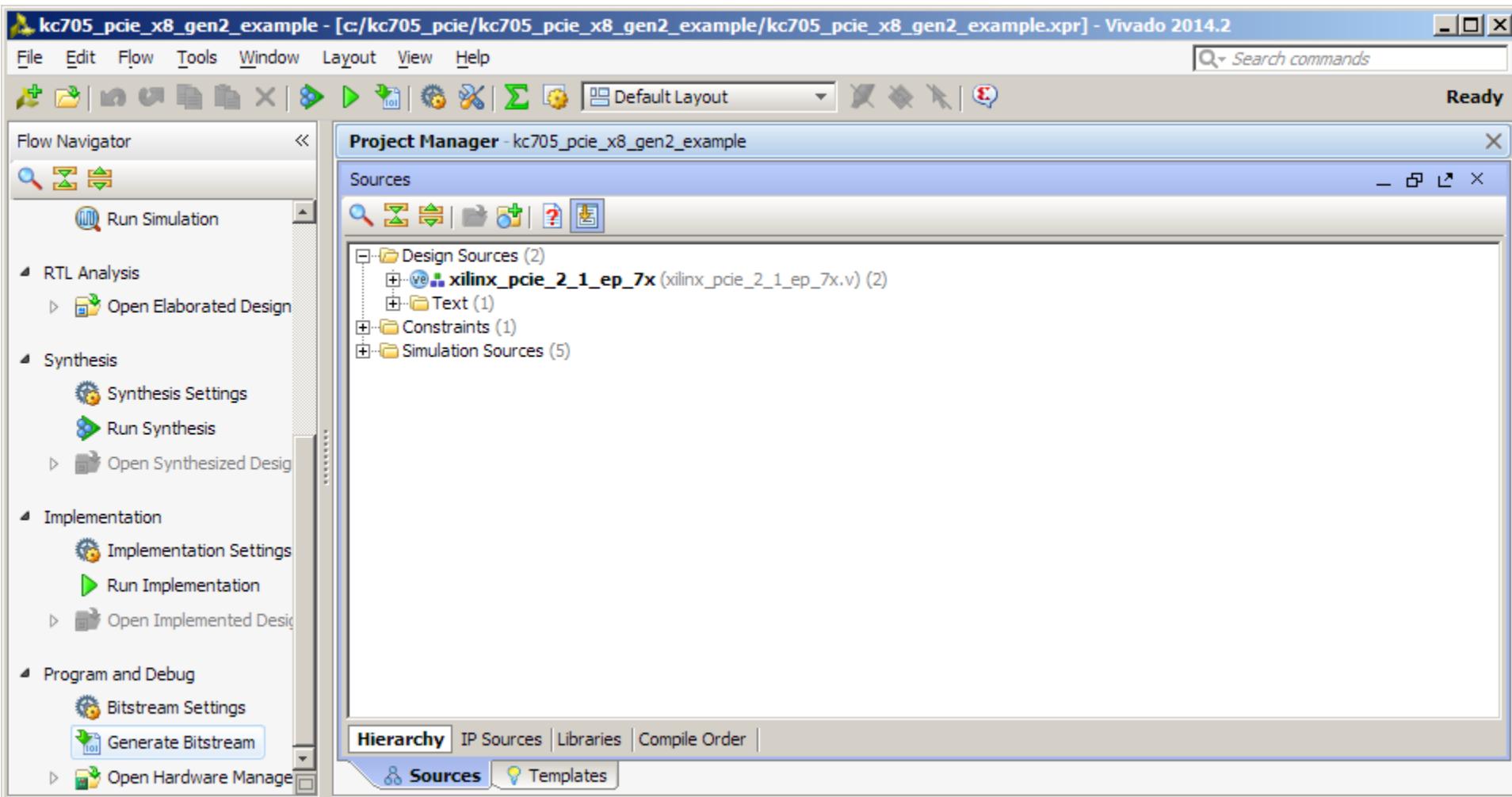


The screenshot shows a Windows application window titled "UltraEdit - [C:\kc705_PCIE\kc705_PCIE_x8_gen2_example\kc705_PCIE_x8_gen2_example.srcts\constrs_1\imports\example_design\xilinx_PCIE_7x_EP_X...]" with a status bar indicating "Line 151". The menu bar includes File, Edit, Search, Insert, Project, View, Format, Column, Macro, Scripting, Advanced, Window, and Help. The main window displays a text file with the following content:

```
138 set_property LOC AB8 [get_ports led_0]
139 set_property LOC AA8 [get_ports led_1]
140 set_property LOC AC9 [get_ports led_2]
141 set_property IOSTANDARD LVCMOS15 [get_ports led_3]
142 # USER CLK HEART BEAT = led_3
143 set_property LOC AB9 [get_ports led_3]
144
145 set_property IOSTANDARD LVCMOS25 [get_ports emcclk]
146 set_property LOC R24 [get_ports emcclk]
147
148 set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type2 [current_design]
149 set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-2 [current_design]
150 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
151
```

Compile Example Design

► Click on Generate Bitstream



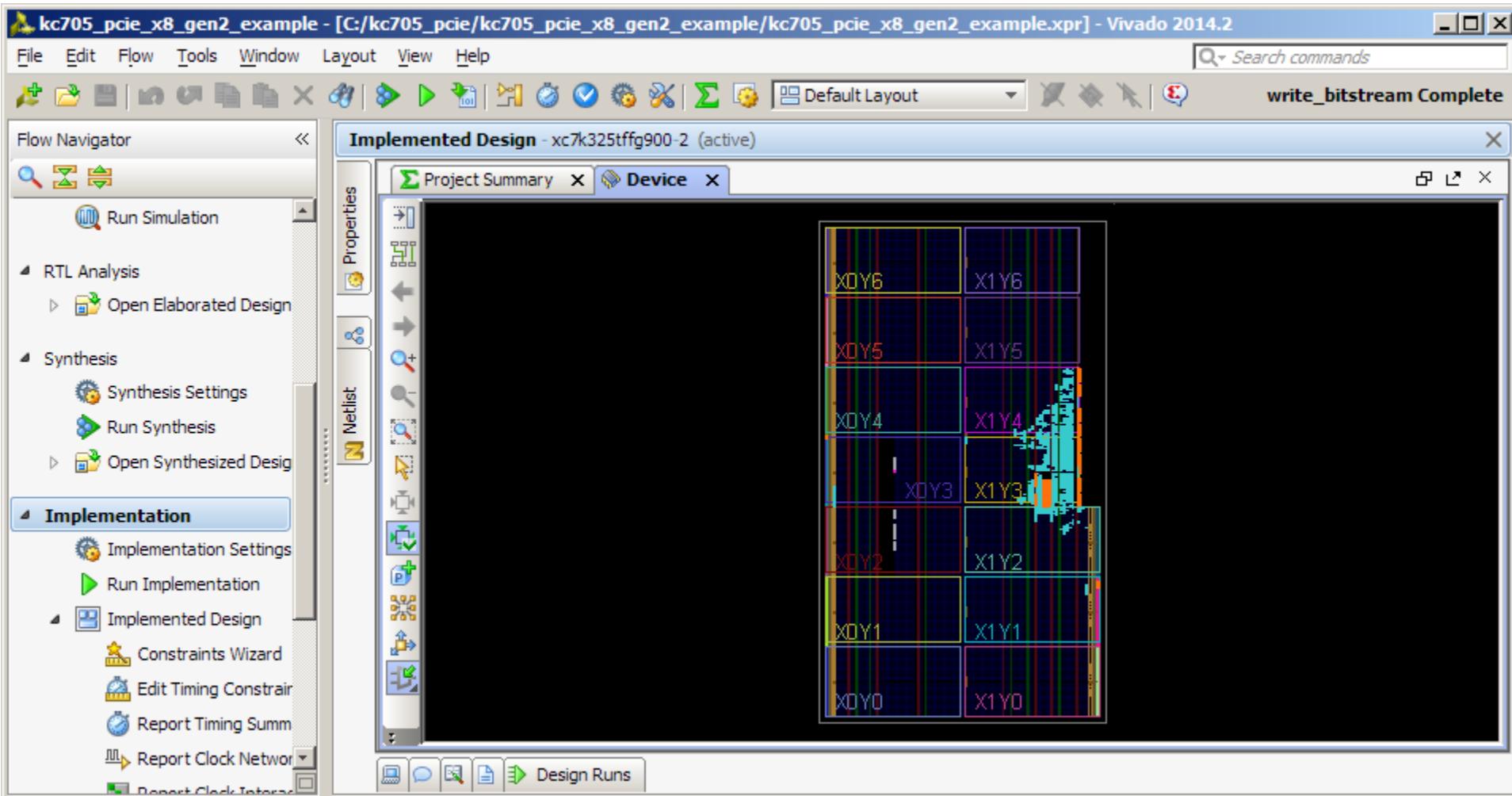
Generate a programming file after implementation

Note: Presentation applies to the KC705

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Compile Example Design

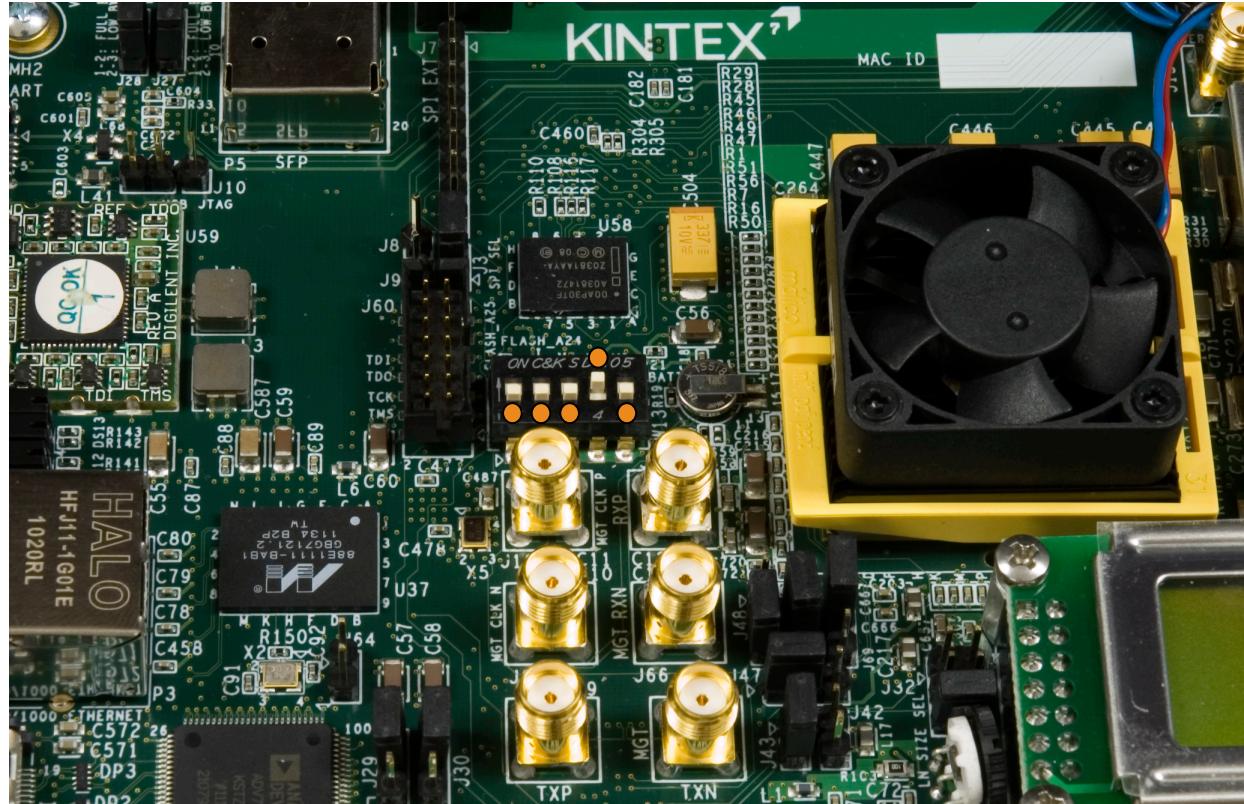
► Open and view the Implemented Design



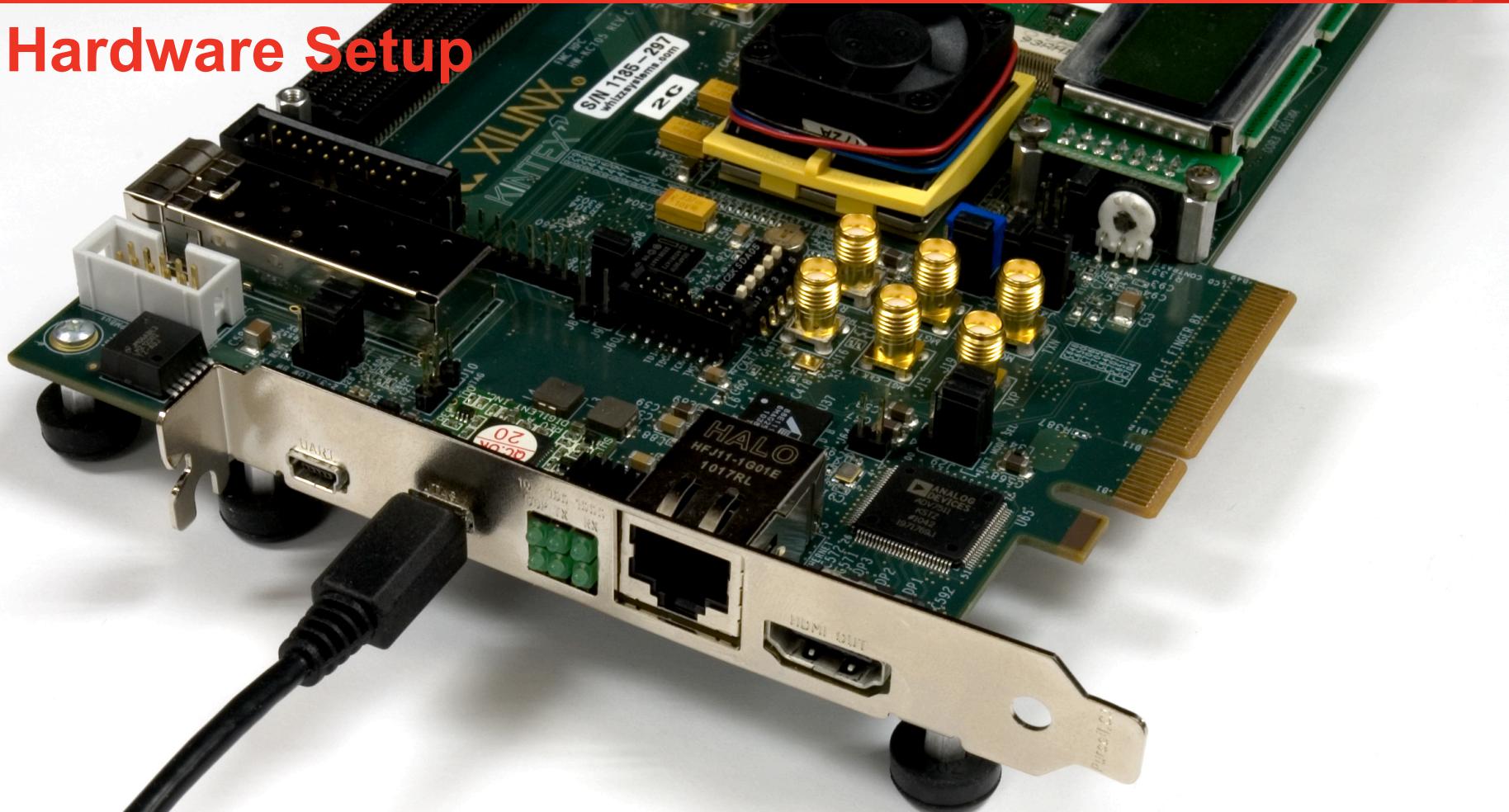
Hardware Setup

► Set S13 to 00010 (1 = on, Position 1 → Position 5)

- This enables Master BPI configuration from Slot #1
- Flash A25, A24 = 00
- FPGA mode pins M[2:0] = 010



Hardware Setup

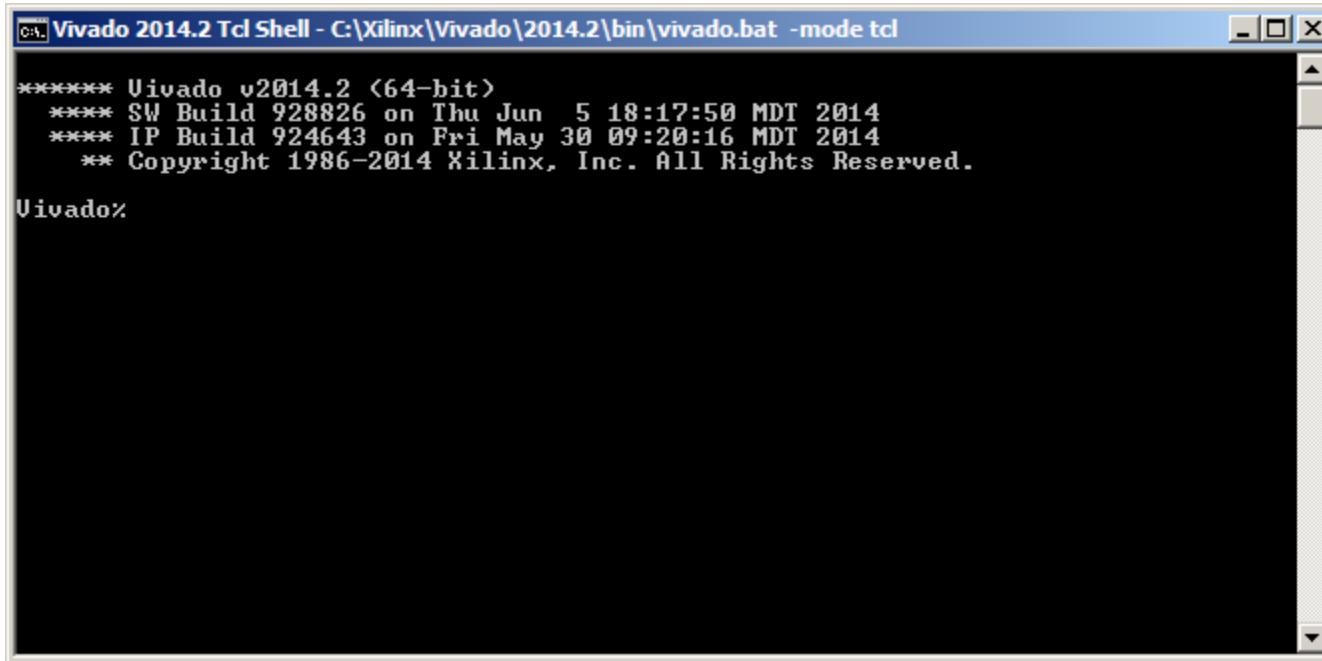


- **Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the KC705 board**
 - Connect this cable to your PC
 - Power on the KC705 board

Generate PCIe MCS File

► Open a Vivado Tcl Shell:

**Start → All Programs → Xilinx Design Tools → Vivado 2014.2 →
Vivado 2014.2 Tcl Shell**



The screenshot shows a Windows command-line interface window titled "Vivado 2014.2 Tcl Shell - C:\Xilinx\Vivado\2014.2\bin\vivado.bat -mode tcl". The window displays the following startup information:

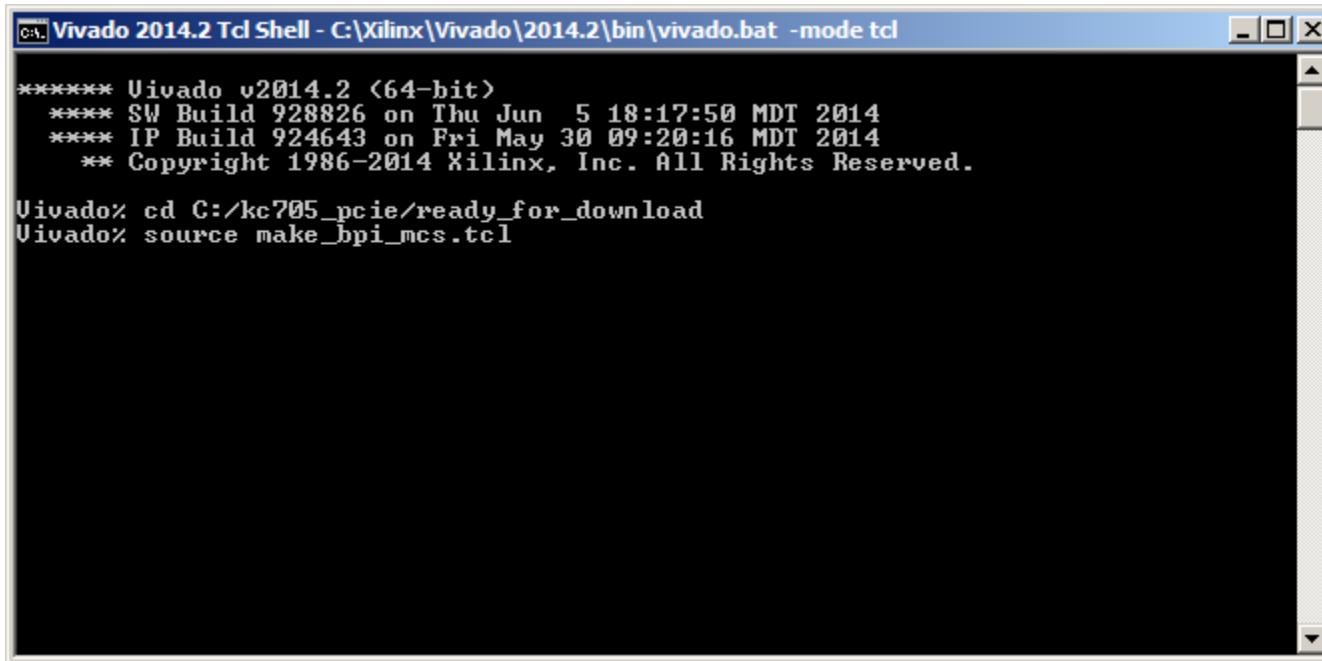
```
***** Vivado v2014.2 (64-bit)
***** SW Build 928826 on Thu Jun  5 18:17:50 MDT 2014
***** IP Build 924643 on Fri May 30 09:20:16 MDT 2014
** Copyright 1986-2014 Xilinx, Inc. All Rights Reserved.
```

The prompt "Vivado%" is visible at the bottom of the window.

Generate PCIe MCS File

- In the Vivado Tcl Shell type:

```
cd C:/kc705_pcie/ready_for_download  
source make_bpi_mcs.tcl
```



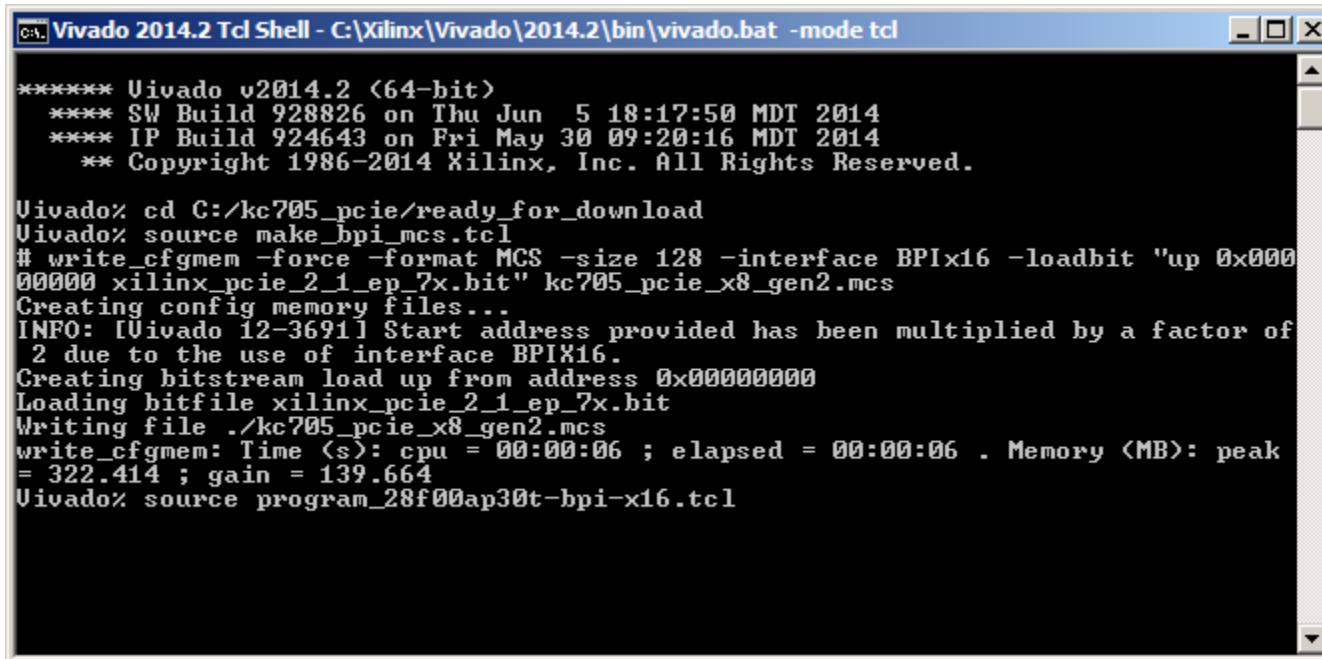
The screenshot shows a Windows command-line interface window titled "Vivado 2014.2 Tcl Shell - C:\Xilinx\Vivado\2014.2\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2014.2 (64-bit)  
***** SW Build 928826 on Thu Jun  5 18:17:50 MDT 2014  
***** IP Build 924643 on Fri May 30 09:20:16 MDT 2014  
** Copyright 1986-2014 Xilinx, Inc. All Rights Reserved.  
  
Vivado% cd C:/kc705_pcie/ready_for_download  
Vivado% source make_bpi_mcs.tcl
```

Program BPI Flash with PCIe Design

- In the Vivado Tcl Shell type:

```
source program_28f00ap30t-bpi-x16.tcl
```



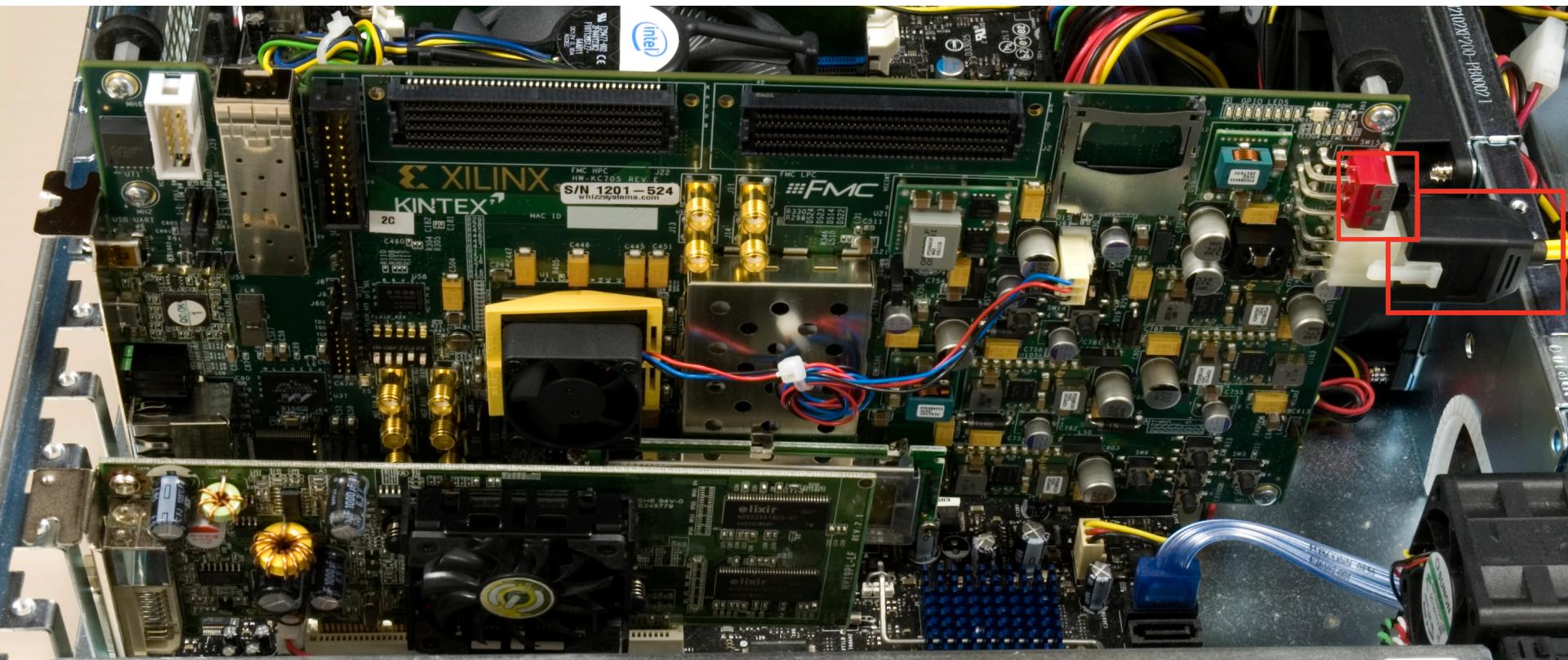
```
Vivado 2014.2 (64-bit)
 **** SW Build 928826 on Thu Jun  5 18:17:50 MDT 2014
 **** IP Build 924643 on Fri May 30 09:20:16 MDT 2014
 ** Copyright 1986-2014 Xilinx, Inc. All Rights Reserved.

Vivado% cd C:/kc705_pcie/ready_for_download
Vivado% source make_bpi_mcs.tcl
# write_cfmem -force -format MCS -size 128 -interface BPIx16 -loadbit "up 0x000
00000 xilinx_pcie_2_1_ep_7x.bit" kc705_pcie_x8_gen2.mcs
Creating config memory files...
INFO: [Vivado 12-3691] Start address provided has been multiplied by a factor of
2 due to the use of interface BPIX16.
Creating bitstream load up from address 0x00000000
Loading bitfile xilinx_pcie_2_1_ep_7x.bit
Writing file ./kc705_pcie_x8_gen2.mcs
write_cfmem: Time <s>: cpu = 00:00:06 ; elapsed = 00:00:06 . Memory <MB>: peak
= 322.414 ; gain = 139.664
Vivado% source program_28f00ap30t-bpi-x16.tcl
```

Hardware Setup

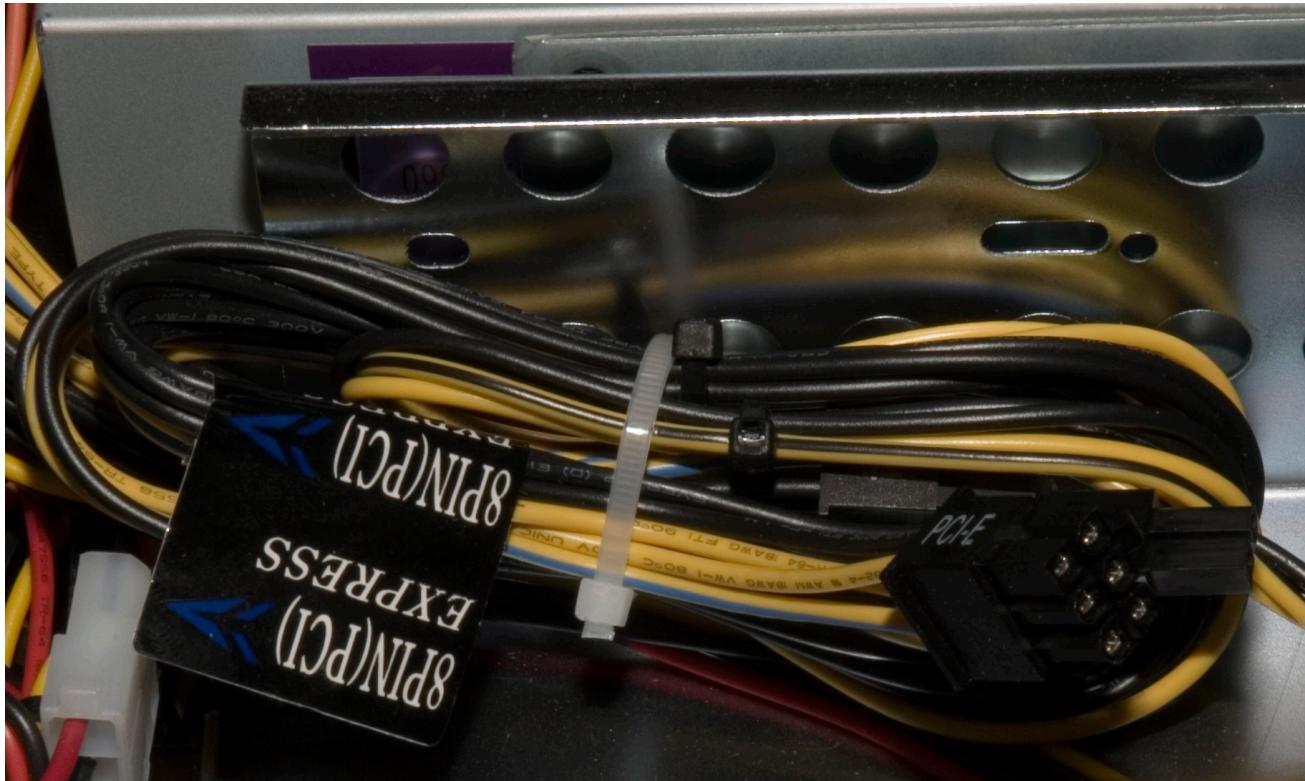
► Insert the KC705 Board into a PCIe slot

- Use the included PC Power adapter; turn on Power Switch



Hardware Setup

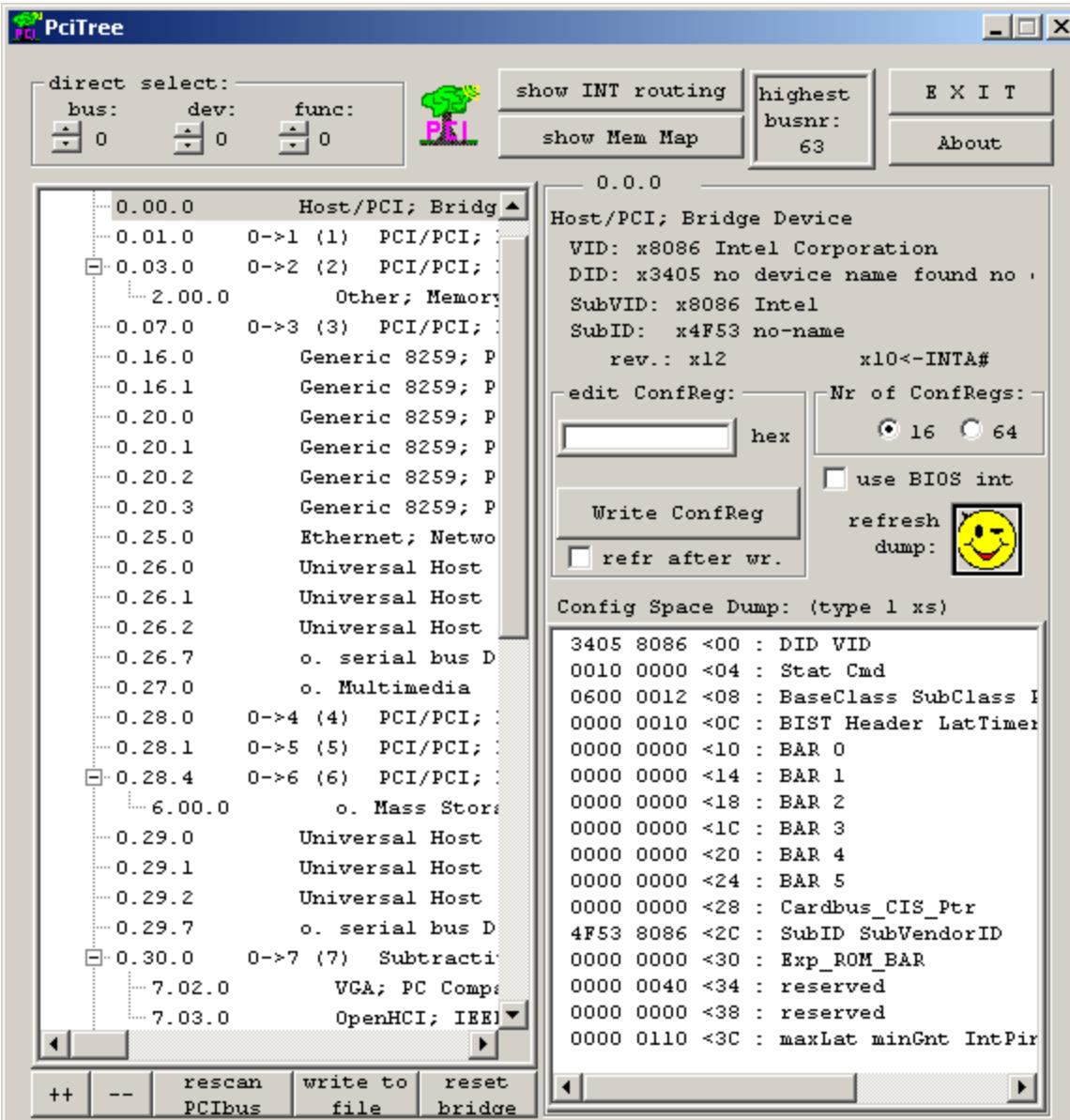
- Do not use the PCIe connector from the PC power supply



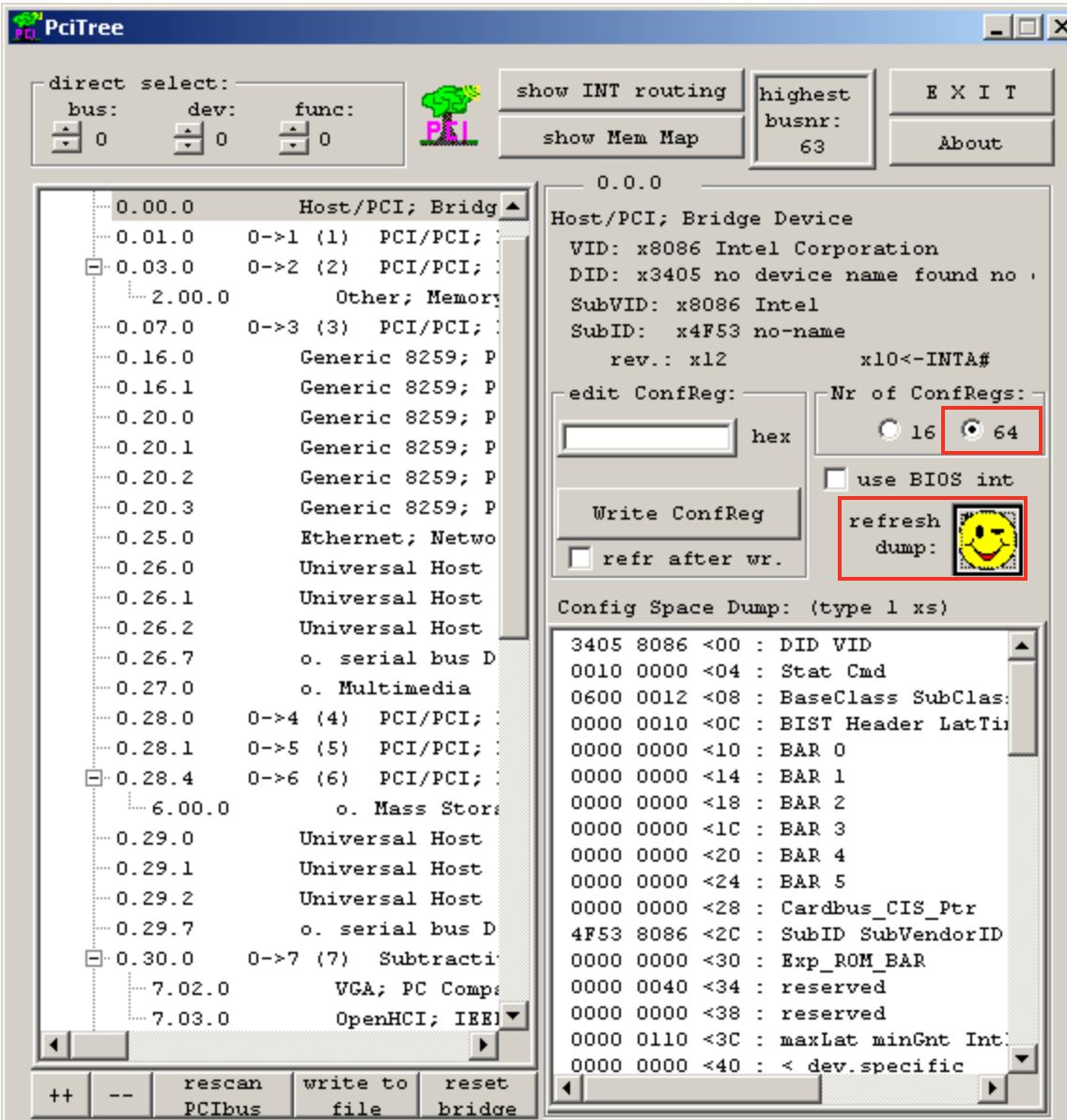
Running the PCIe x8 Gen 2 Design

➤ Power on the PC

➤ Start PciTree



Running the PCIe x8 Gen 2 Design



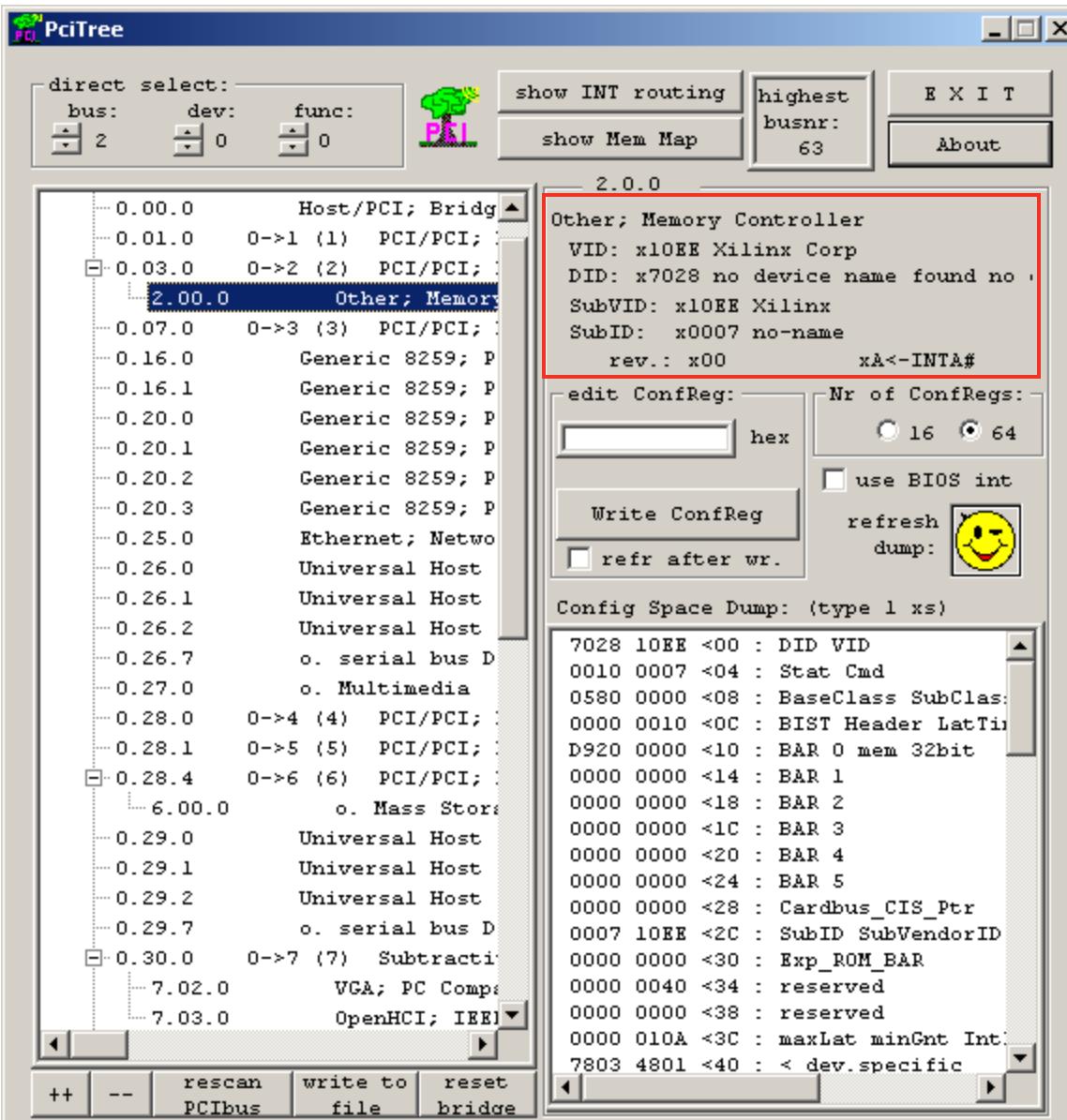
➤ Set Number of Configuration Registers to 64

➤ Click on Refresh dump

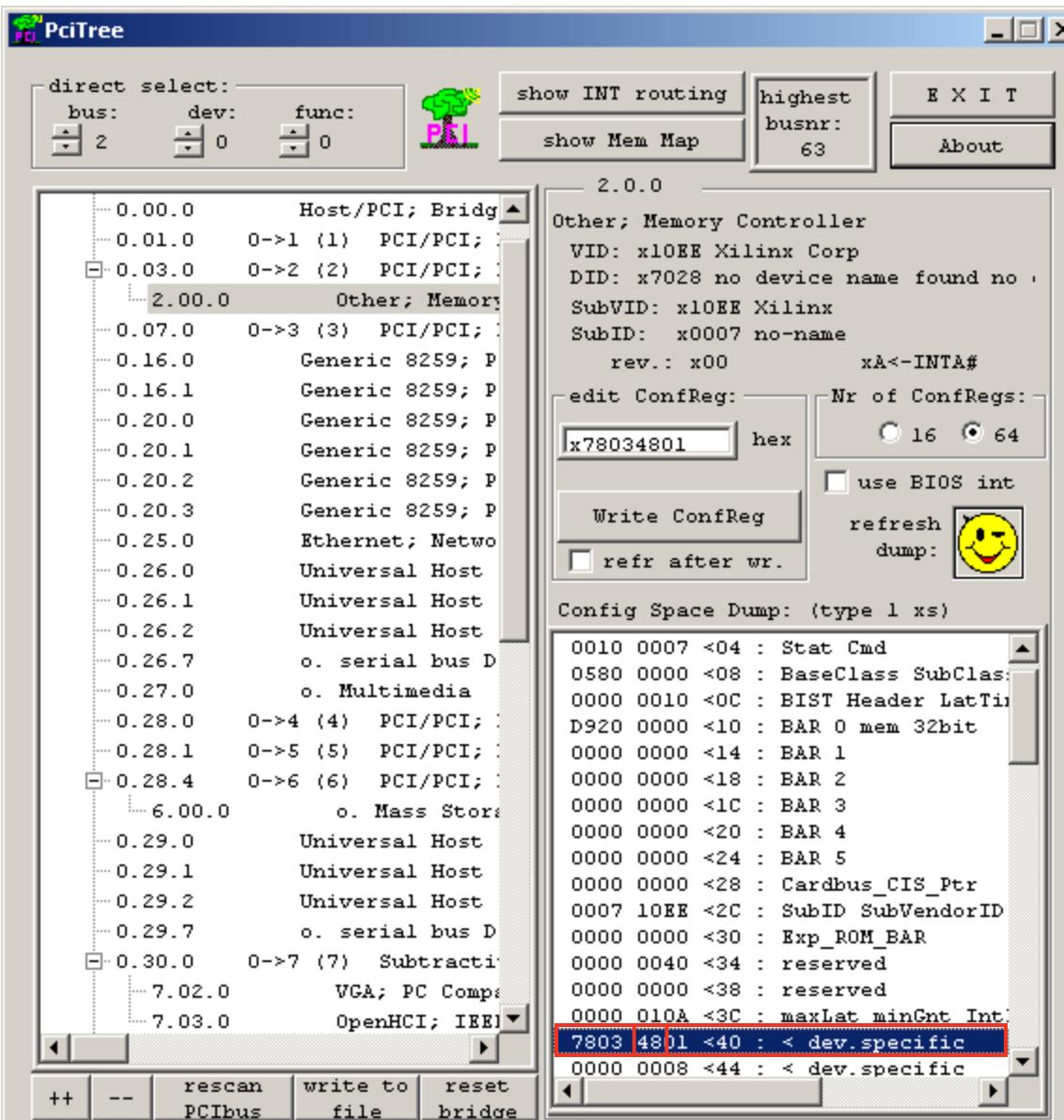
Running the PCIe x8 Gen 2 Design

► Locate the Xilinx Device

- Vendor ID is 0x10EE
- The x8 Gen 2 configuration will have a Device ID of 0x7028



Running the PCIe x8 Gen 2 Design



➤ Navigate the linked list in configuration space to locate the PCIe Capabilities Structure

- See [PG054](#) for details

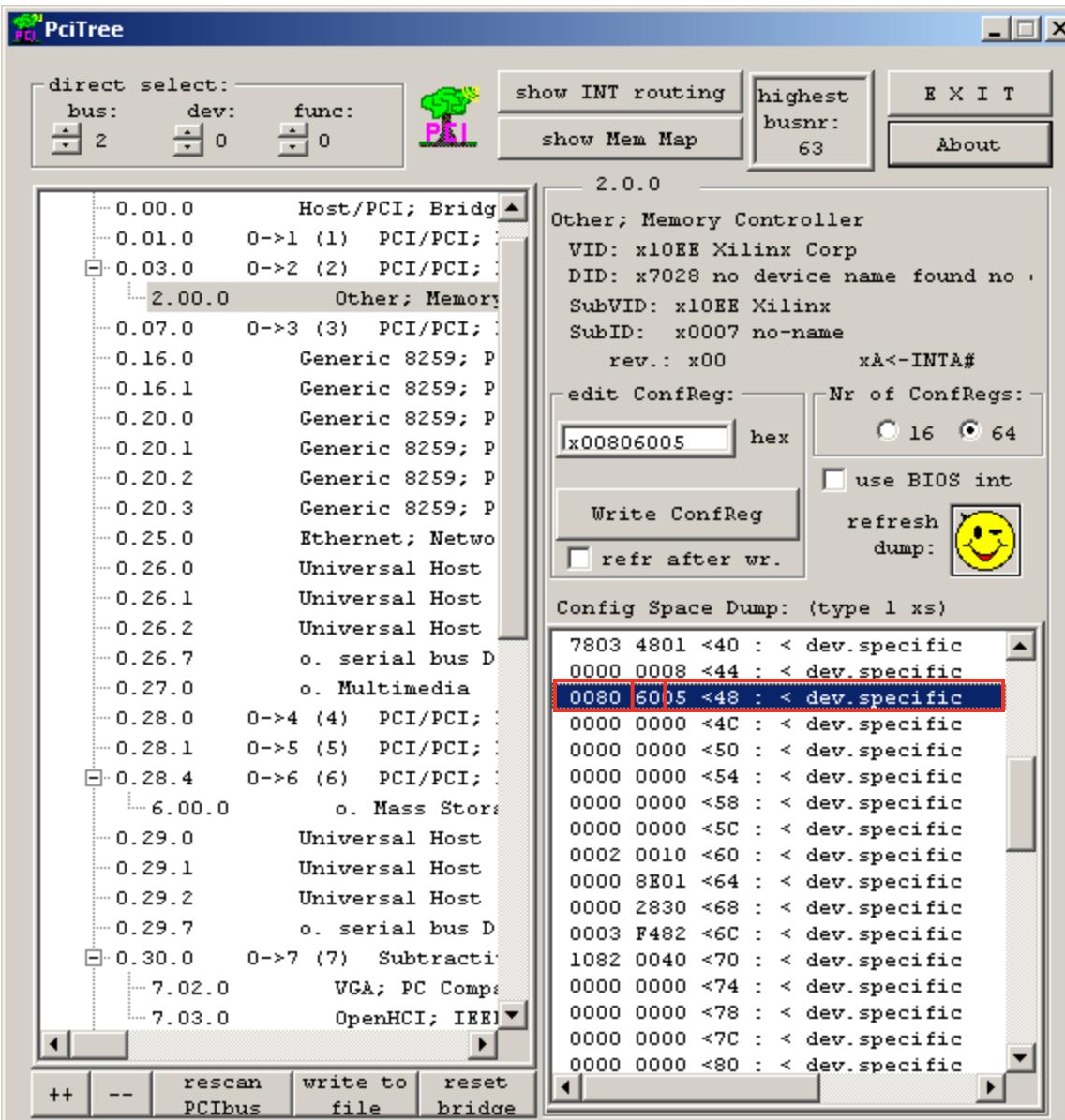
➤ With the Xilinx device selected, select Register 0x40

- Register 0x40 points to the next structure
- 0x48 is the address of the next structure

Running the PCIe x8 Gen 2 Design

► Select Register 0x48

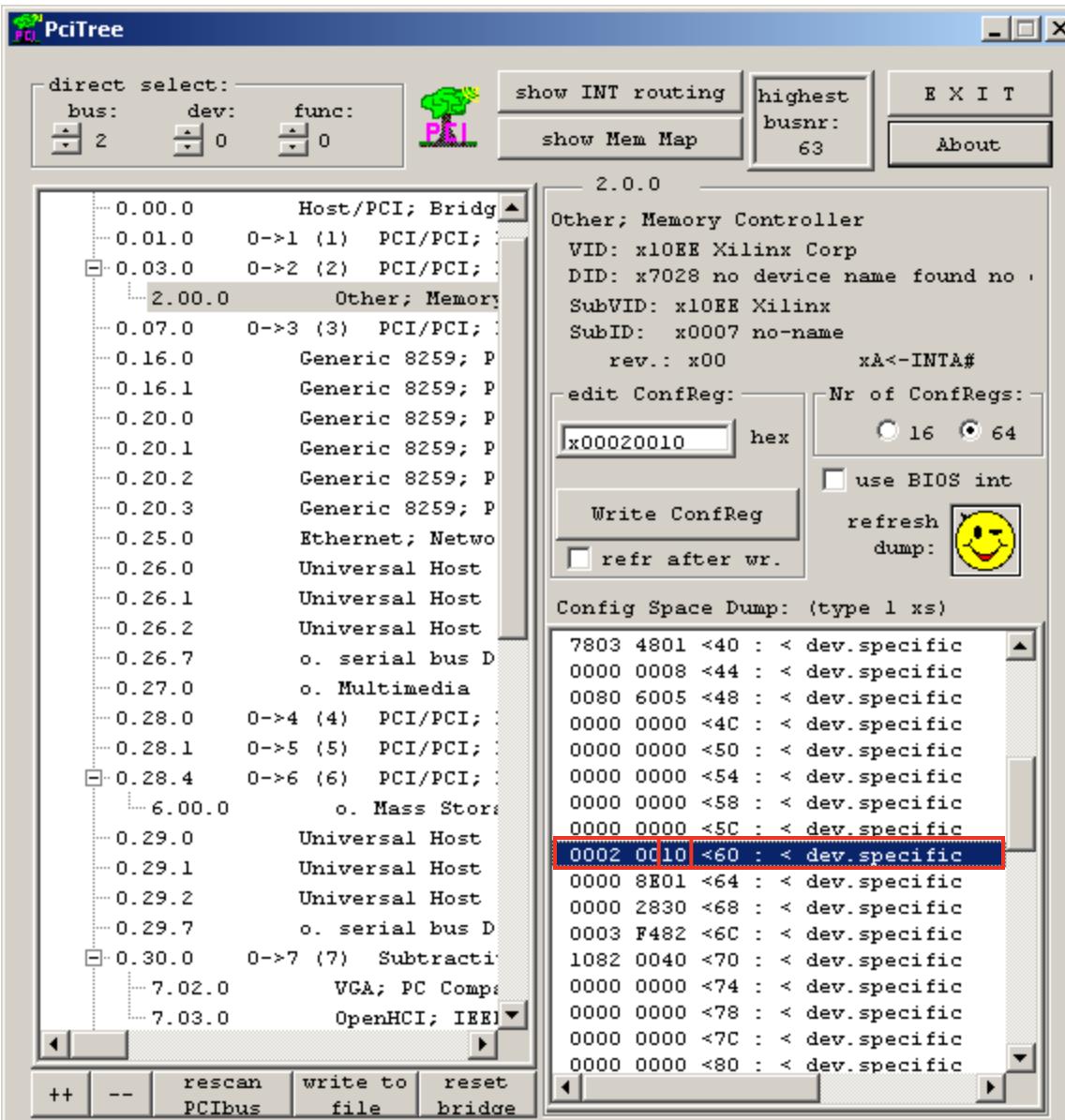
- Register 0x48 points to the next structure
- 0x60 is the address of the next structure



Running the PCIe x8 Gen 2 Design

► Register 0x60

- 0x60 is a type 0x10, indicating PCIe Capabilities Structure
- Last Structure



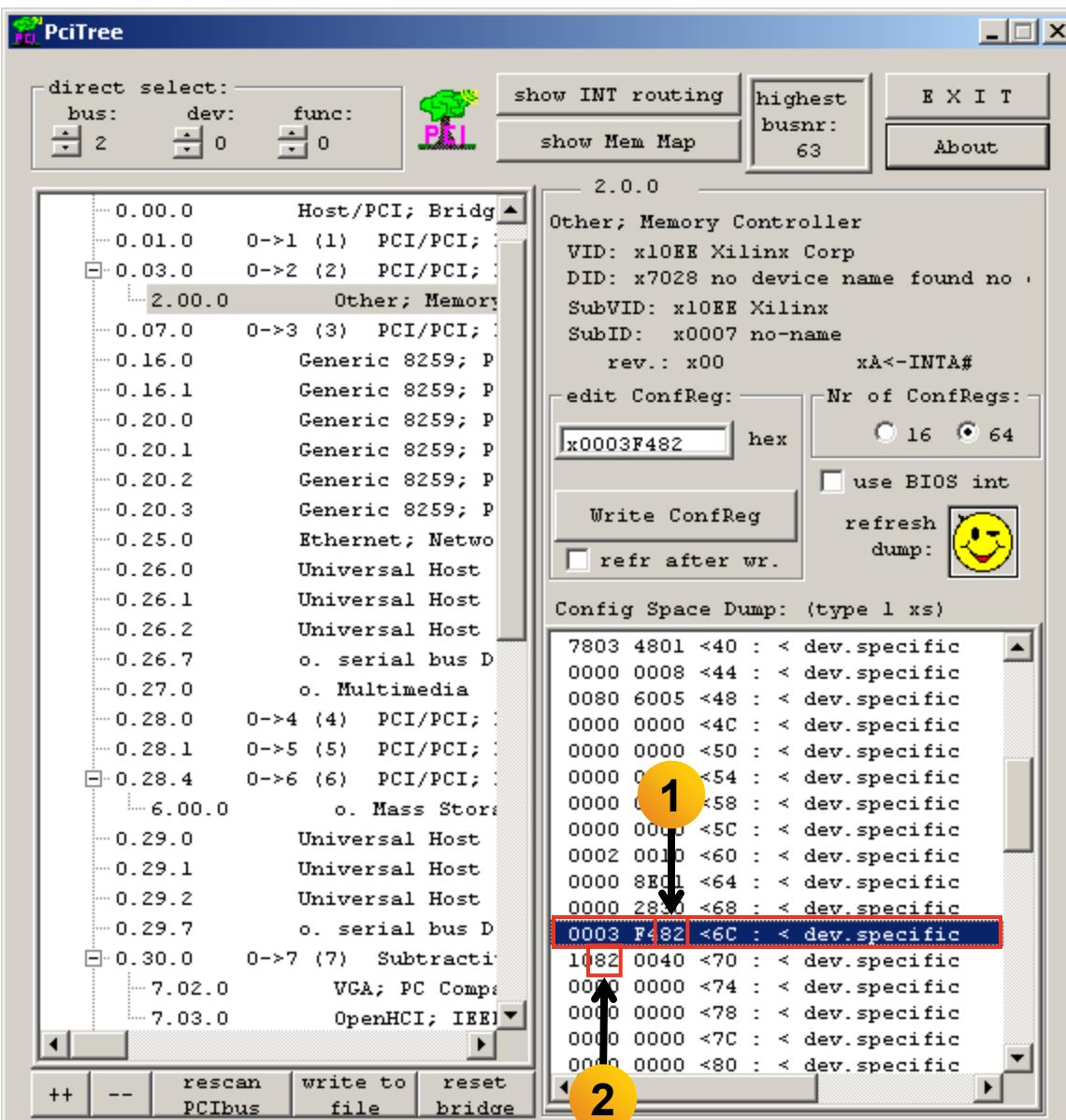
Running the PCIe x8 Gen 2 Design

► Register 0x6C

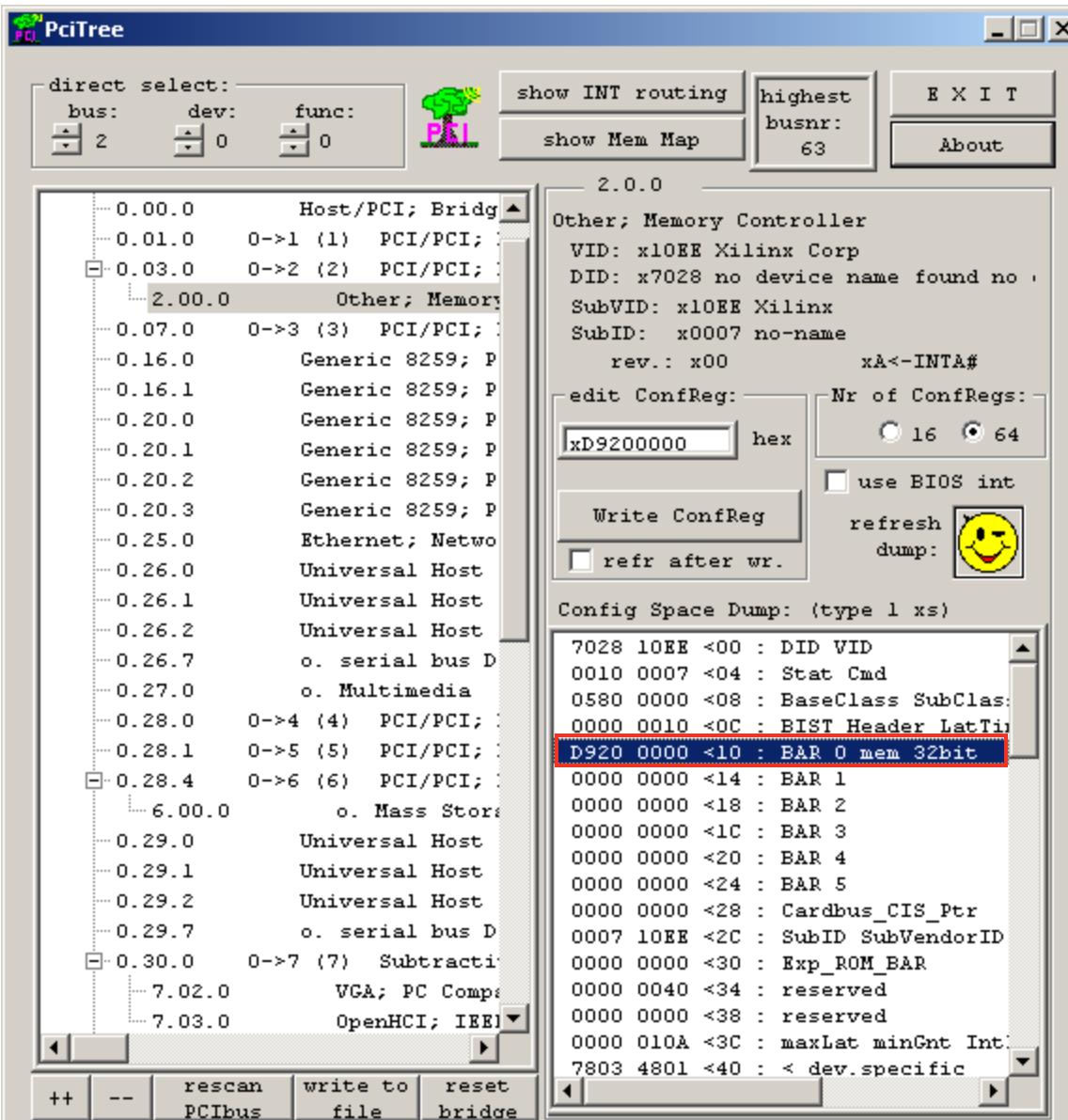
- Link Capabilities Register
- Indicates the maximum number of lanes and speed (Gen 1, Gen 2) for device
- The value 0x82 shows this is an x8 Gen 2 device (1)

► Link Status Register

- 0x70
- Shows the current link status
- This design, in a Gen 2 chassis, trained to x8 Gen 2 (2)



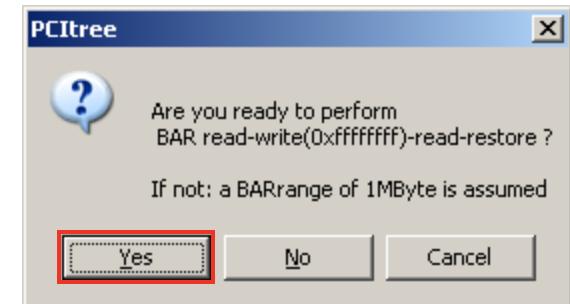
Running the PCIe x8 Gen 2 Design



► Double-click on BAR 0

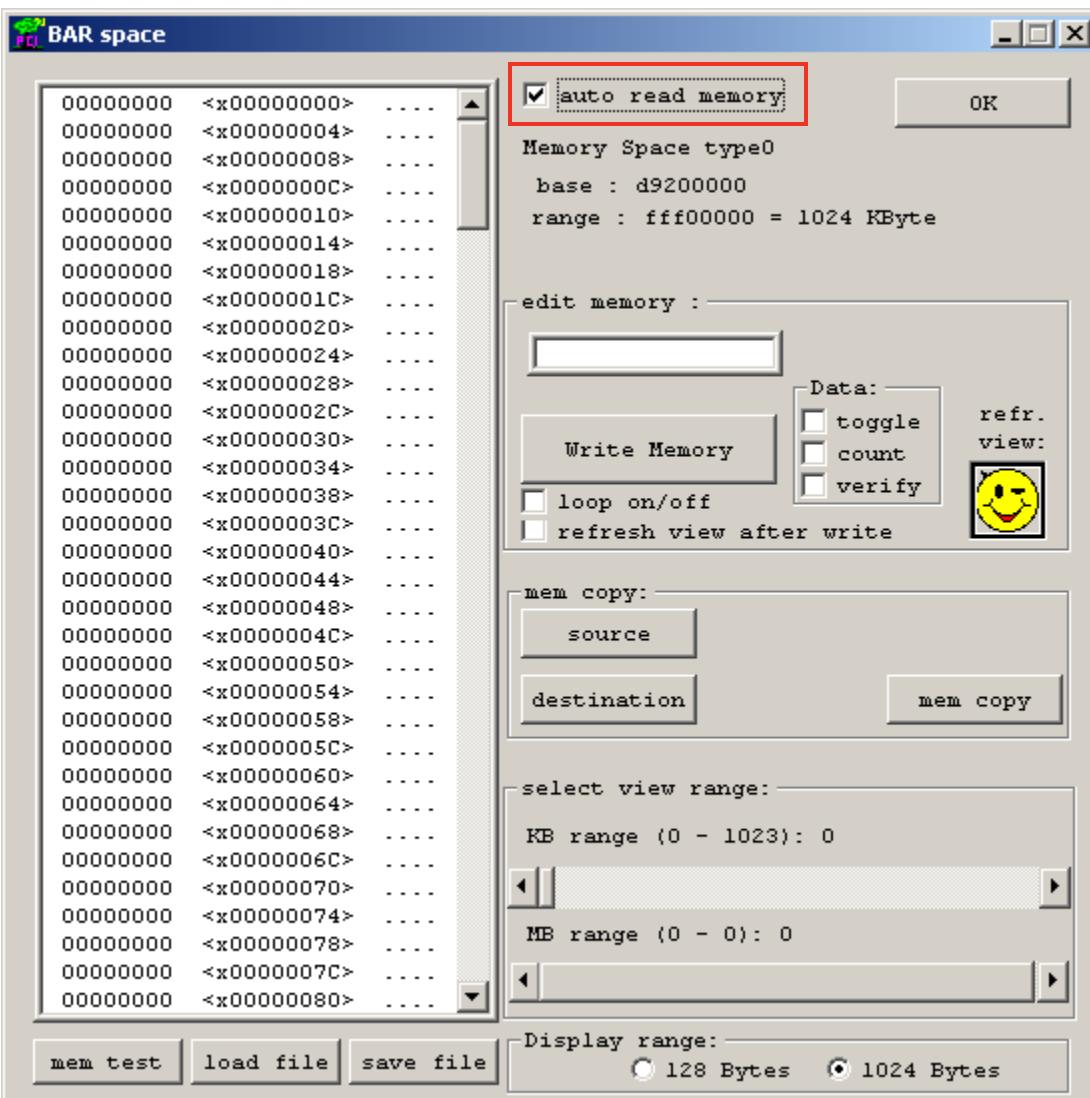
- BAR 0 Address is machine dependent

► Click Yes on the Dialog box seen below



Running the PCIe x8 Gen 2 Design

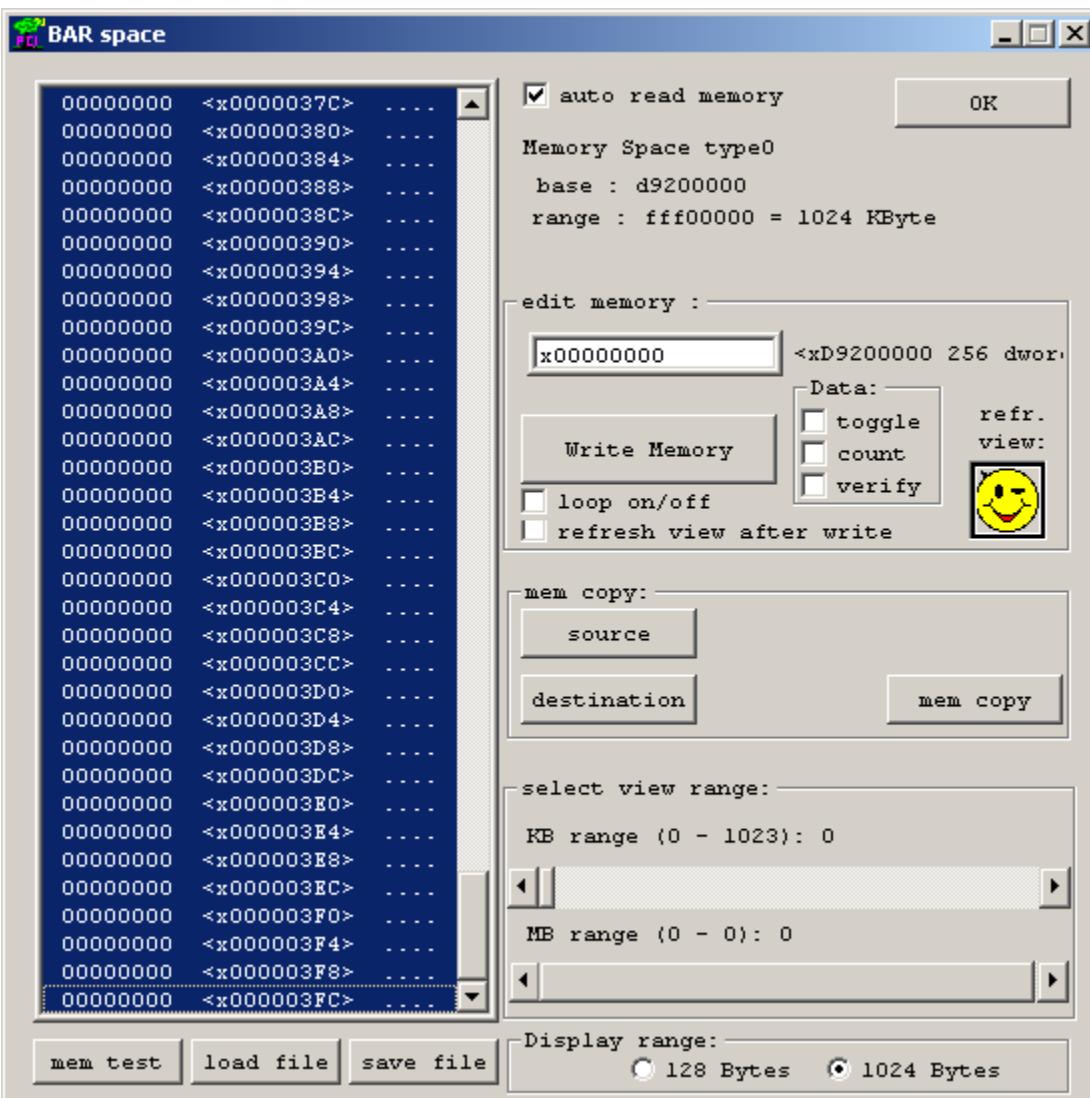
► Select auto read memory



Running the PCIe x8 Gen 2 Design

► Click on the first memory location

- Type <Shift-End> to select 1024 Bytes

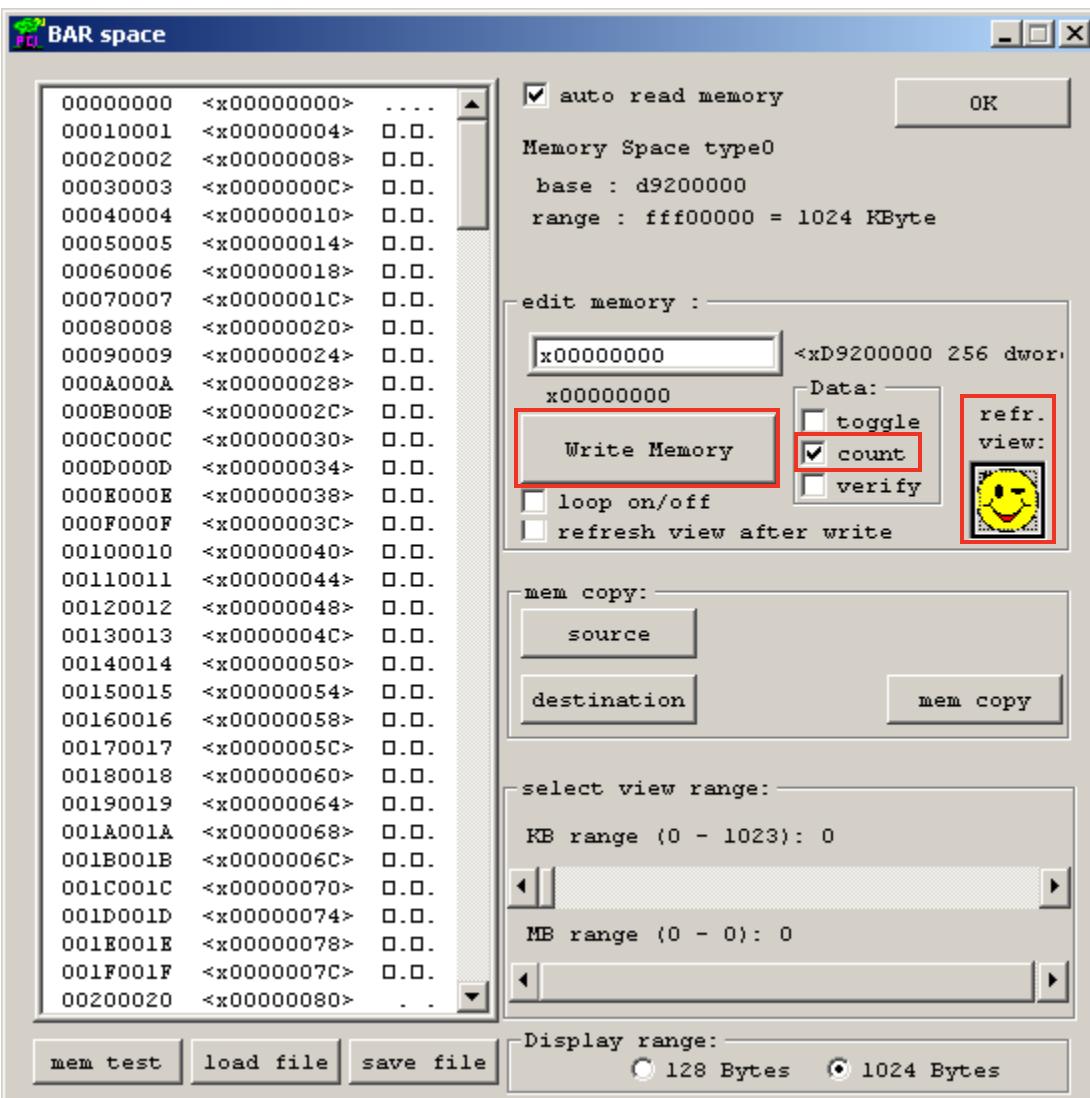


Running the PCIe x8 Gen 2 Design

➤ Write Memory

- Select count
- Click Write Memory
- Click refr view

➤ View results – counting up to FF



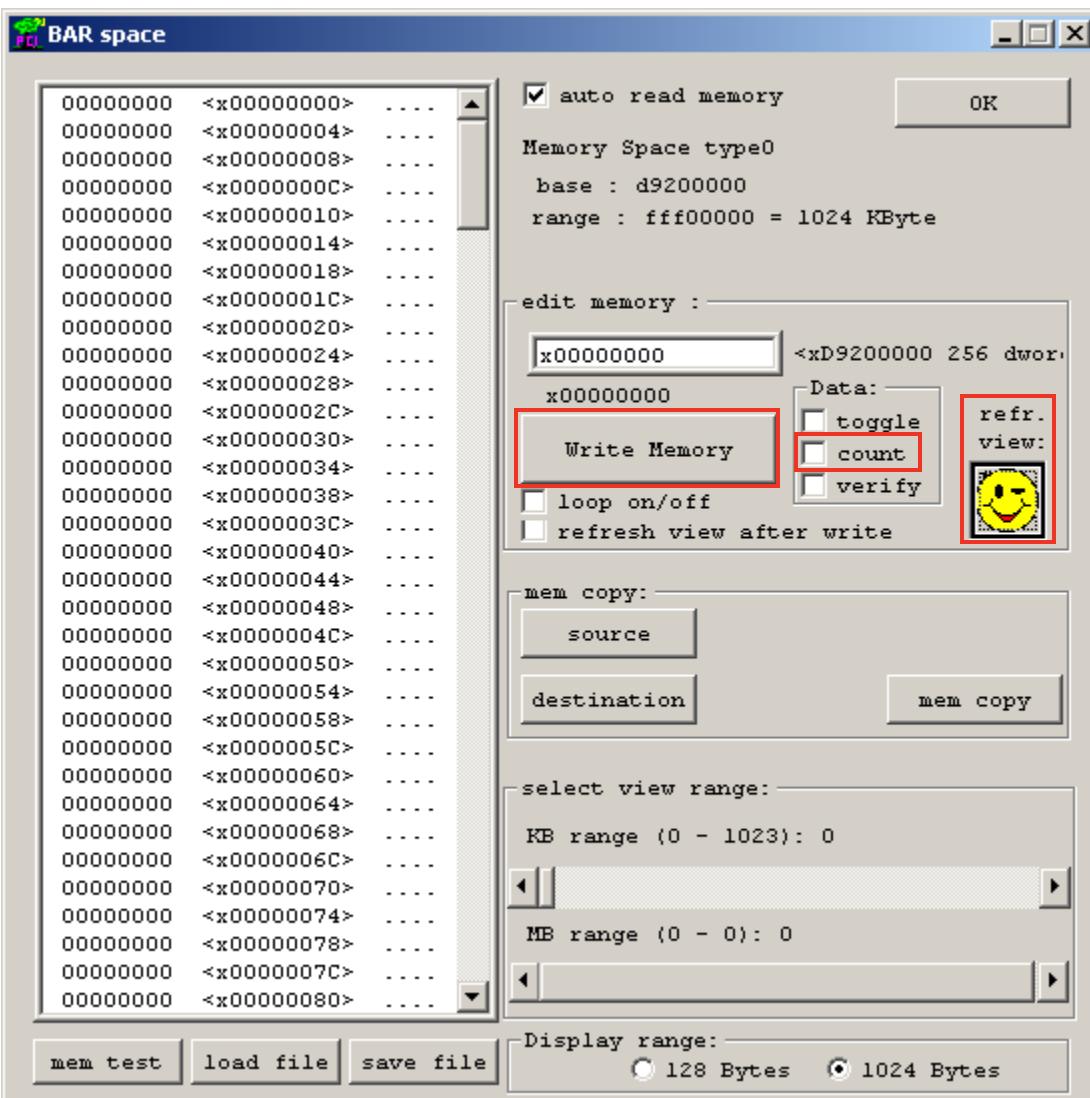
Running the PCIe x8 Gen 2 Design

➤ Restore Memory

- Deselect count
- Click Write Memory
- Click refr view

➤ Memory is reset to zeros

➤ Turn off PCIe chassis and remove KC705 board



References

References

► PCIe Base Specification

- PCI SIG Web Site
 - <http://www.pcisig.com/home>

► Xilinx PCI Express

- Xilinx PCI Express Overview
 - <http://www.xilinx.com/technology/protocols/pciexpress.htm>
- 7 Series Integrated Block for PCI Express Product Page
 - http://www.xilinx.com/products/intellectual-property/7_SERIES_PCI_Express_Block.htm
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 - <http://www.xilinx.com/support/answers/40469.htm>

References

► Micron NOR Flash

- Micron P30 Flash
 - <http://www.micron.com/partsnor-flash/parallel-nor-flash/pc28f00ap30tfa>
- Datasheet
 - http://www.micron.com/~media/Documents/Products/Data%20Sheet/NOR%20Flash/Parallel/P30/p30-65nm_mlc_512mb_1gb_2gb.pdf

► Xilinx Generation 7 Configuration with BPI Flash

- 7 Series FPGAs Configuration User Guide – UG470
 - http://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf
- Vivado Design Suite Programming and Debugging User Guide
 - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_2/ug908-vivado-programming-debugging.pdf
- BPI Fast Configuration with 7 Series FPGAs – XAPP587
 - http://www.xilinx.com/support/documentation/application_notes/xapp587-bpi-fast-configuration.pdf

Documentation

Documentation

► Kintex-7

- Kintex-7 FPGA Family
 - <http://www.xilinx.com/products/silicon-devices/fpga/kintex-7/index.htm>
- Design Advisory Master Answer Record for Kintex-7 FPGAs
 - <http://www.xilinx.com/support/answers/42946.htm>

► KC705 Documentation

- Kintex-7 FPGA KC705 Evaluation Kit
 - <http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm>
- KC705 Getting Started Guide
 - http://www.xilinx.com/support/documentation/boards_and_kits/kc705/2013_2/ug883_K7_KC705_Eval_Kit.pdf
- KC705 User Guide
 - http://www.xilinx.com/support/documentation/boards_and_kits/kc705/ug810_KC705_Eval_Bd.pdf