



KC705 Built-In Self Test Flash Application

June 2014

XTP195

Revision History

Date	Version	Description
06/09/14	9.0	Recompiled for 2014.2.
04/16/14	8.0	Recompiled for 2014.1.
12/18/13	7.0	Recompiled for 2013.4.
10/23/13	6.0	Recompiled for 2013.3. Converted to IPI.
06/19/13	5.0	Recompiled for 2013.2. AR55738, AR55939 and AR55531 fixed.
05/10/13	4.1	Added AR55939.
04/03/13	4.0	Recompiled for 2013.1. Added AR55738, AR55531, and AR55431.
02/22/13	3.1	Added AR53420.
12/18/12	3.0	Recompiled for 2012.4. Added AR53392.
10/23/12	2.0	Recompiled for 2012.3. AR51180 fixed. Added AR52368.
09/20/12	1.0	Initial version for 2012.2. Added AR50886. Added AR51180. Added AR51758.

© Copyright 2014 Xilinx, Inc. All Rights Reserved.

XILINX, the Xilinx logo, the Brand Window and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

NOTICE OF DISCLAIMER: The information disclosed to you hereunder (the "Information") is provided "AS-IS" with no warranty of any kind, express or implied. Xilinx does not assume any liability arising from your use of the Information. You are responsible for obtaining any rights you may require for your use of this Information. Xilinx reserves the right to make changes, at any time, to the Information without notice and at its sole discretion. Xilinx assumes no obligation to correct any errors contained in the Information or to advise you of any corrections or updates. Xilinx expressly disclaims any liability in connection with technical support or assistance that may be provided to you in connection with the Information. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE INFORMATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NONINFRINGEMENT OF THIRD-PARTY RIGHTS.

Overview

- Xilinx KC705 Board
- Software Requirements
- KC705 Setup
- KC705 BIST (Built-In Self Test)
- Compile KC705 BIST Design
- Program KC705 with BIST Design
- Run the LwIP Ethernet Design
- References

KC705 BIST Design Description

► Description

- The Built-In System Test (BIST) application uses an IPI MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.

► Block Design Source

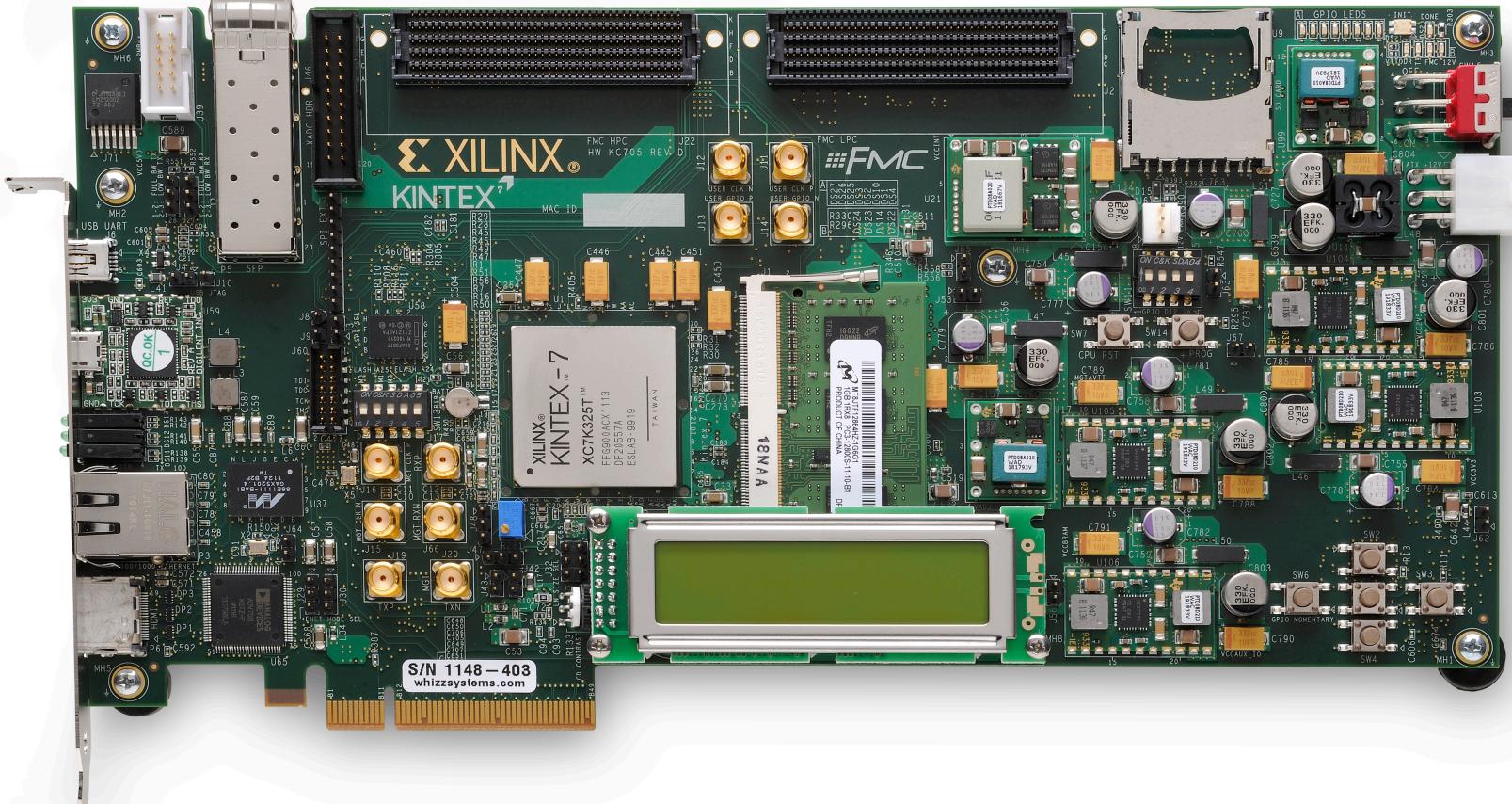
- RDF0185 - KC705 BIST Design Files (2014.2 C) zip file
- Available through <http://www.xilinx.com/kc705>

KC705 BIST Design Description

► Block Design IP

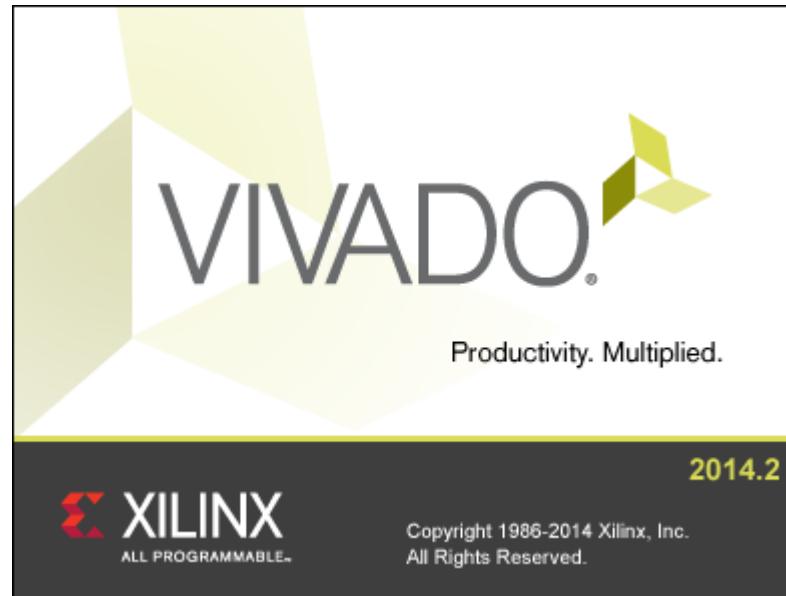
- Processor and Subsystems: MicroBlaze, MicroBlaze Debug Module (MDM), Local Memory Bus, LMB BRAM Controller, Block Memory Generator, Proc Sys Reset, AXI Interrupt Controller
- AXI Bus: AXI Interconnect, AXI Timer
- Memory: AXI BRAM Controller, MIG 7 Series, AXI DMA
- Peripherals: AXI Ethernet, AXI EMC, AXI IIC, AXI GPIO, AXI UART 16550, XADC Wizard
- Other IP: Clocking Wizard, Constant, Concat, Slice, gte2_top
 - [Vivado Design Suite Tcl Command Reference Guide](#) (UG835)
 - [Designing IP Subsystems Using IP Integrator](#) (UG994)

Xilinx KC705 Board

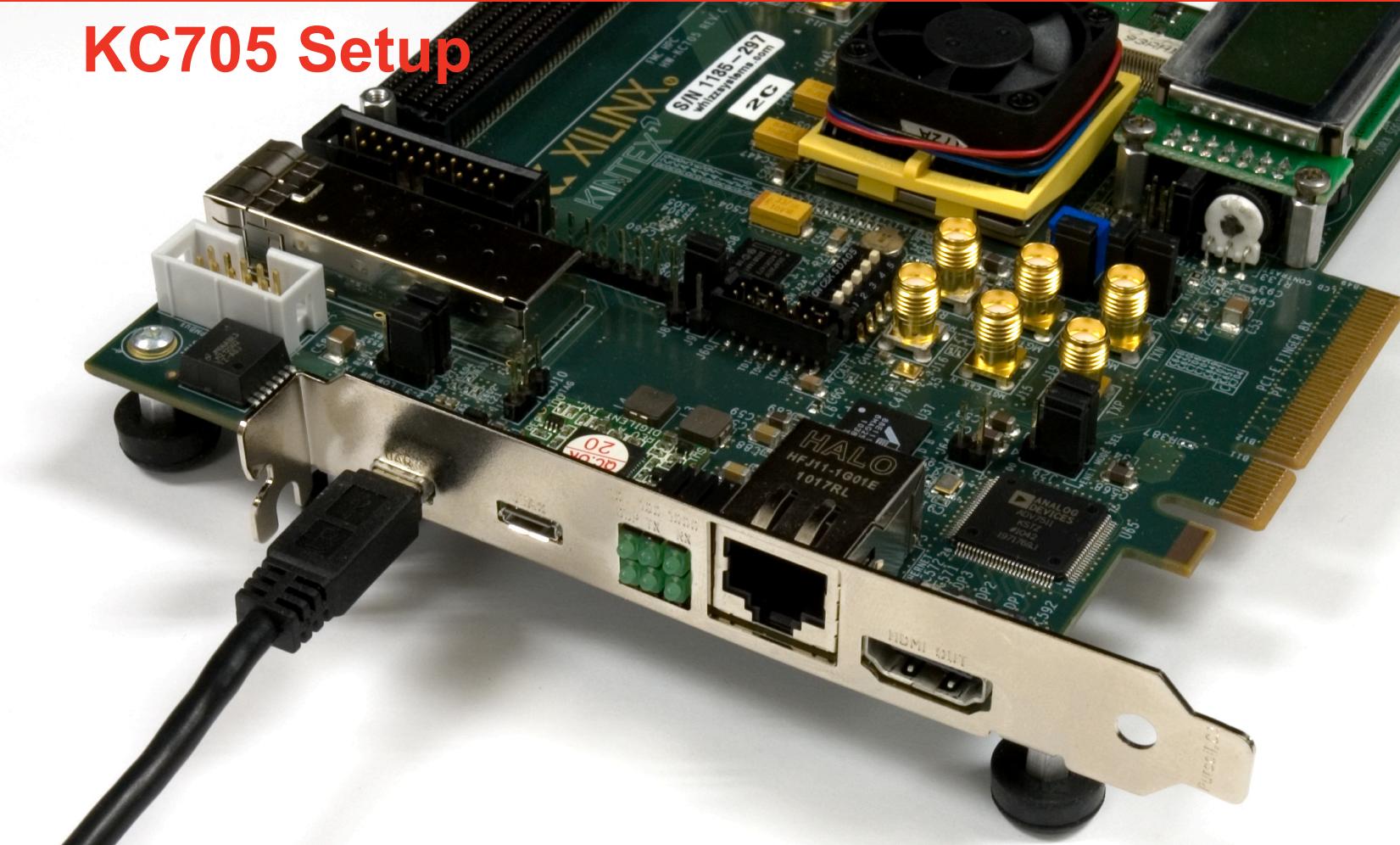


Vivado Software Requirements

- Xilinx Vivado Design Suite 2014.2, Design Edition + SDK
 - Combined installer

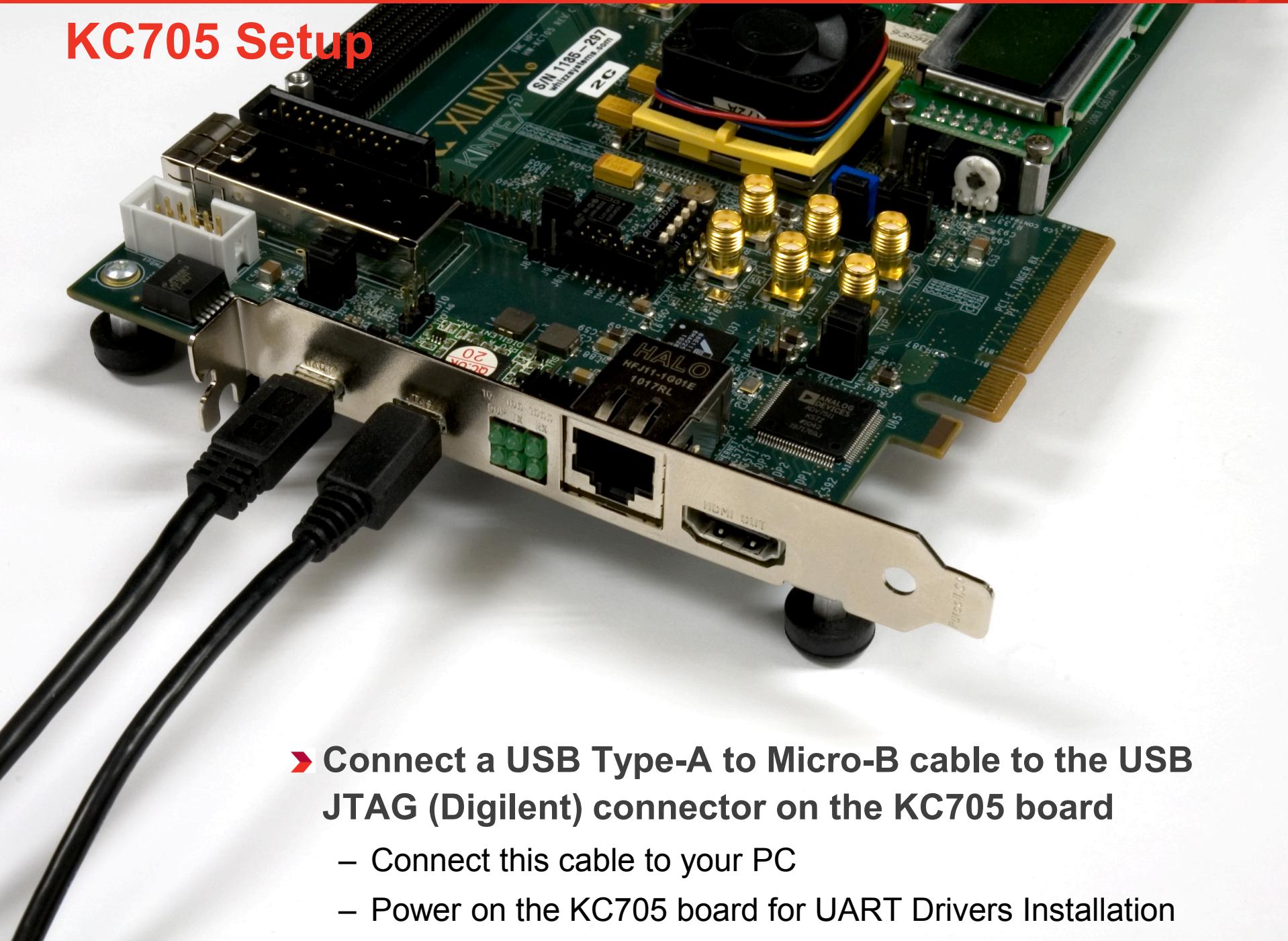


KC705 Setup



- Connect a USB Type-A to Mini-B cable to the USB UART connector on the KC705 board
 - Connect this cable to your PC

KC705 Setup

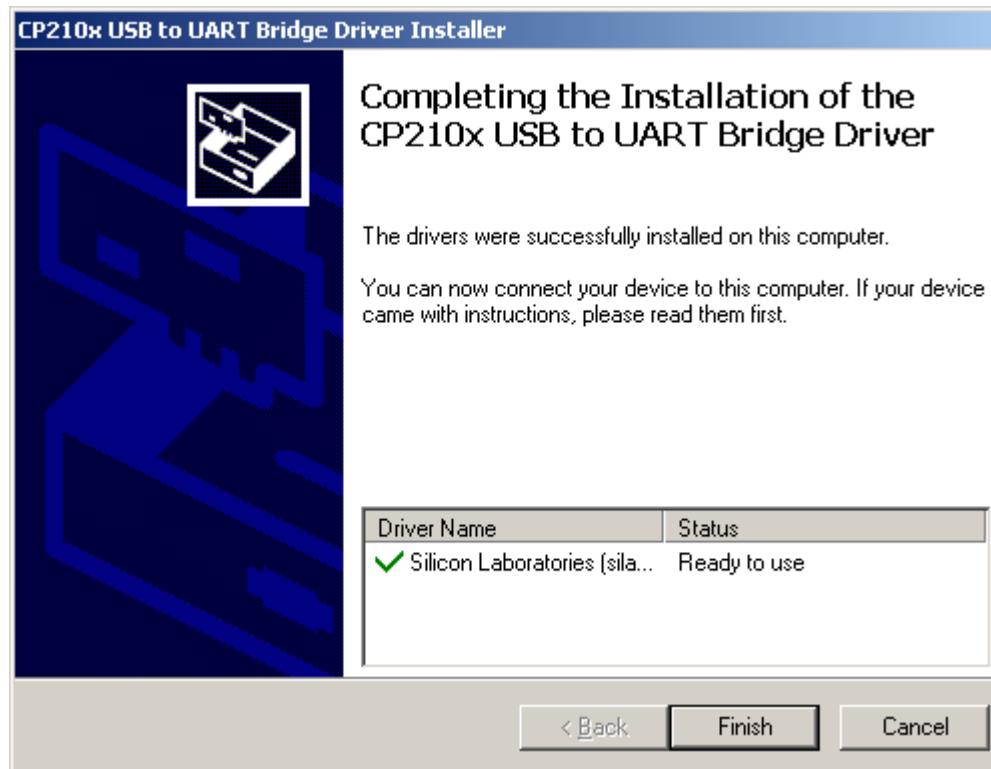


- ▶ **Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the KC705 board**
 - Connect this cable to your PC
 - Power on the KC705 board for UART Drivers Installation

KC705 Setup

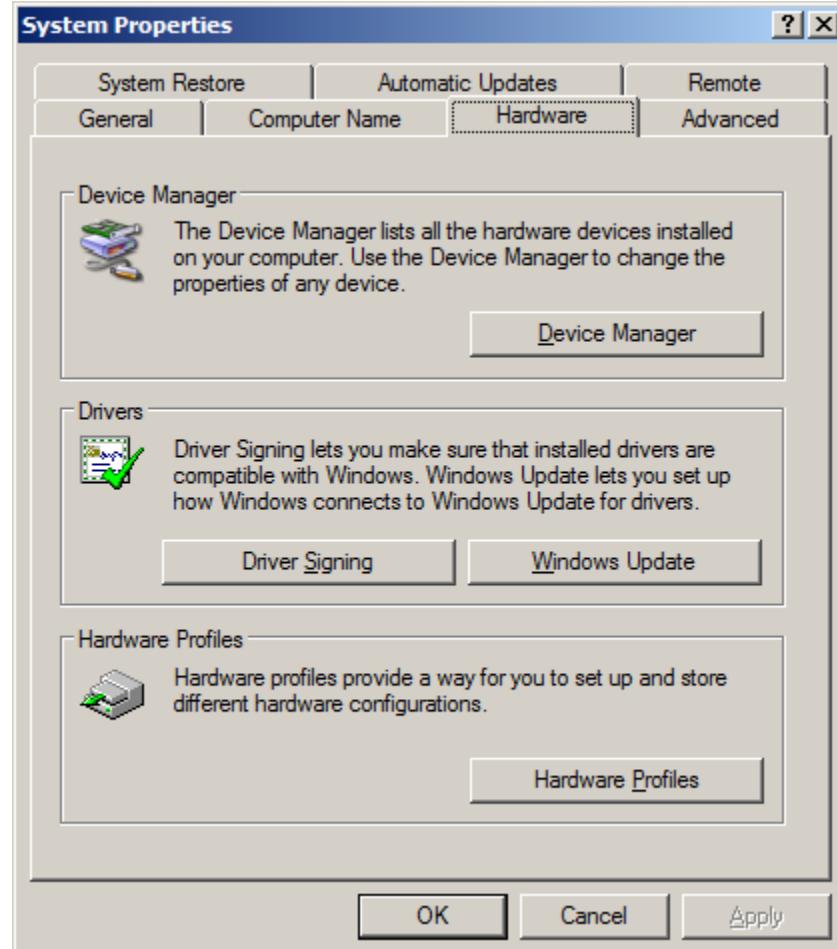
► Install USB UART Drivers

- Refer to [UG1033](#) for details on installing the USB to UART Drivers



KC705 Setup

- Reboot your PC if necessary
- Right-click on My Computer and select Properties
 - Select the Hardware tab
 - Click on Device Manager

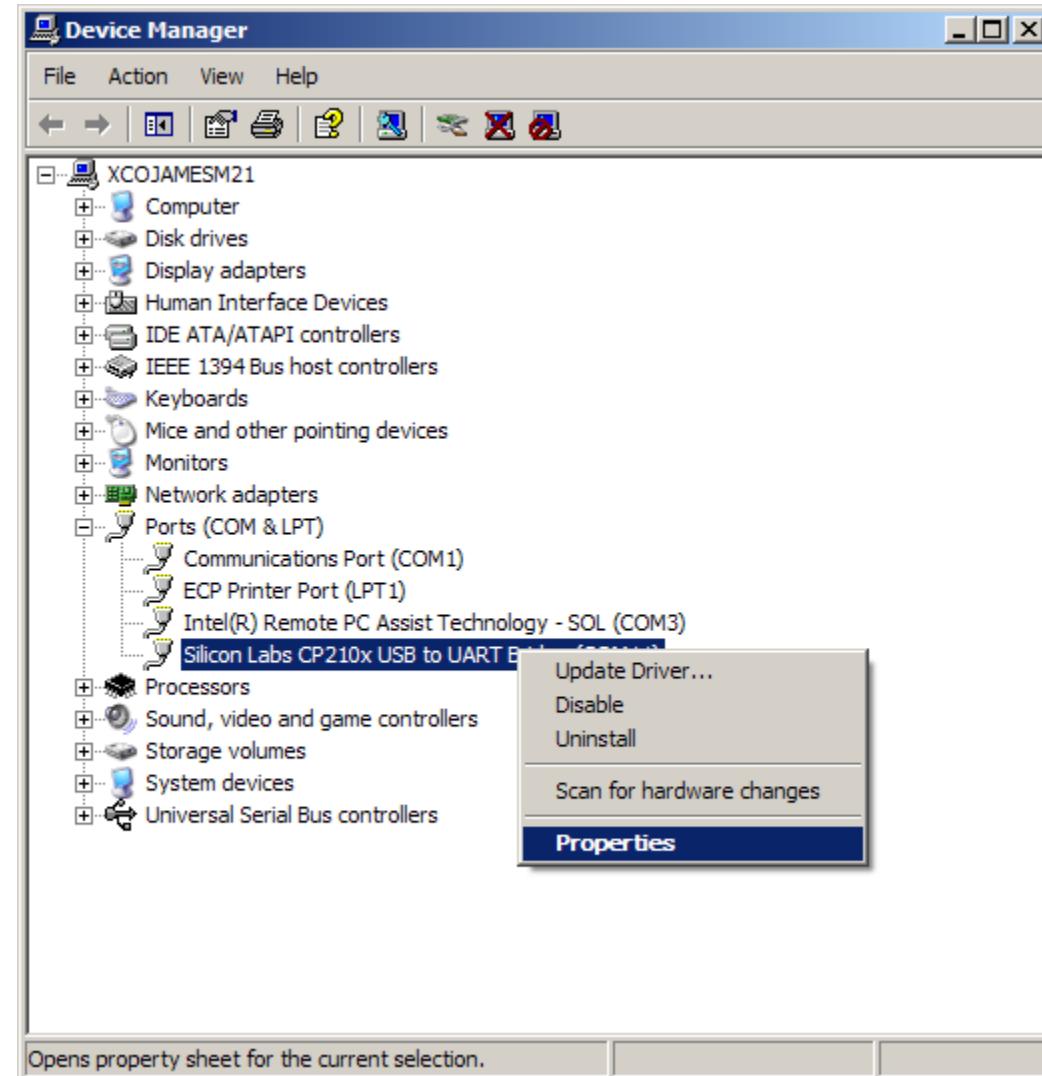


KC705 Setup

► Expand the Ports

Hardware

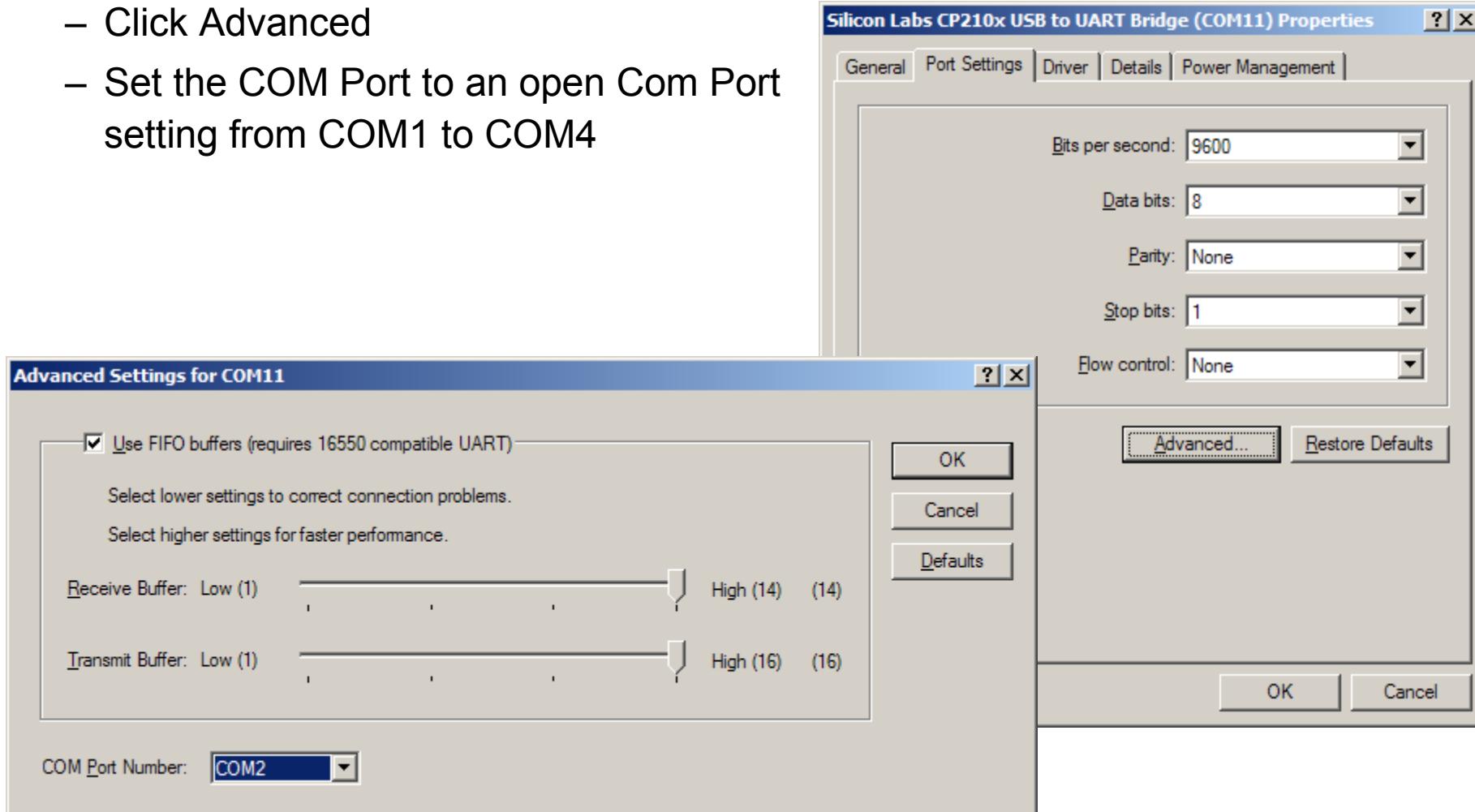
- Right-click on Silicon Labs CP210x USB to UART Bridge and select Properties



KC705 Setup

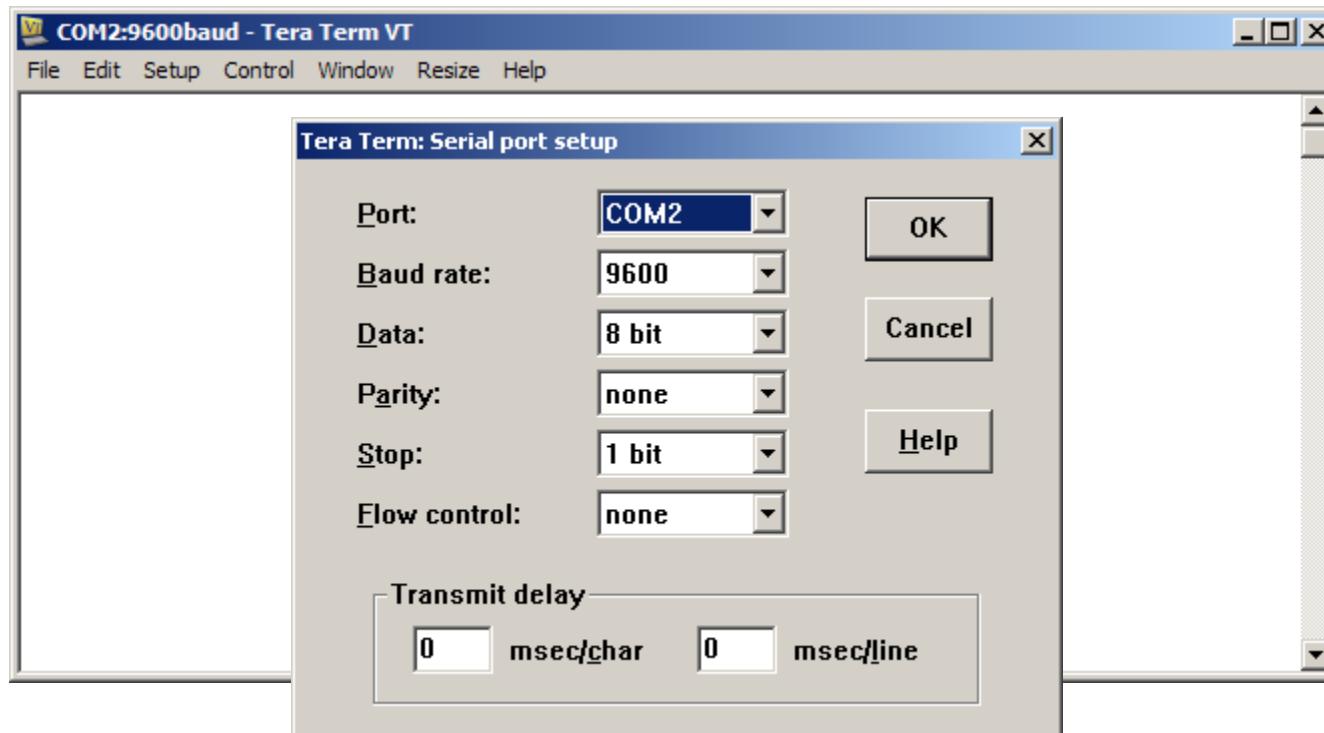
► Under Port Settings tab

- Click Advanced
- Set the COM Port to an open Com Port setting from COM1 to COM4



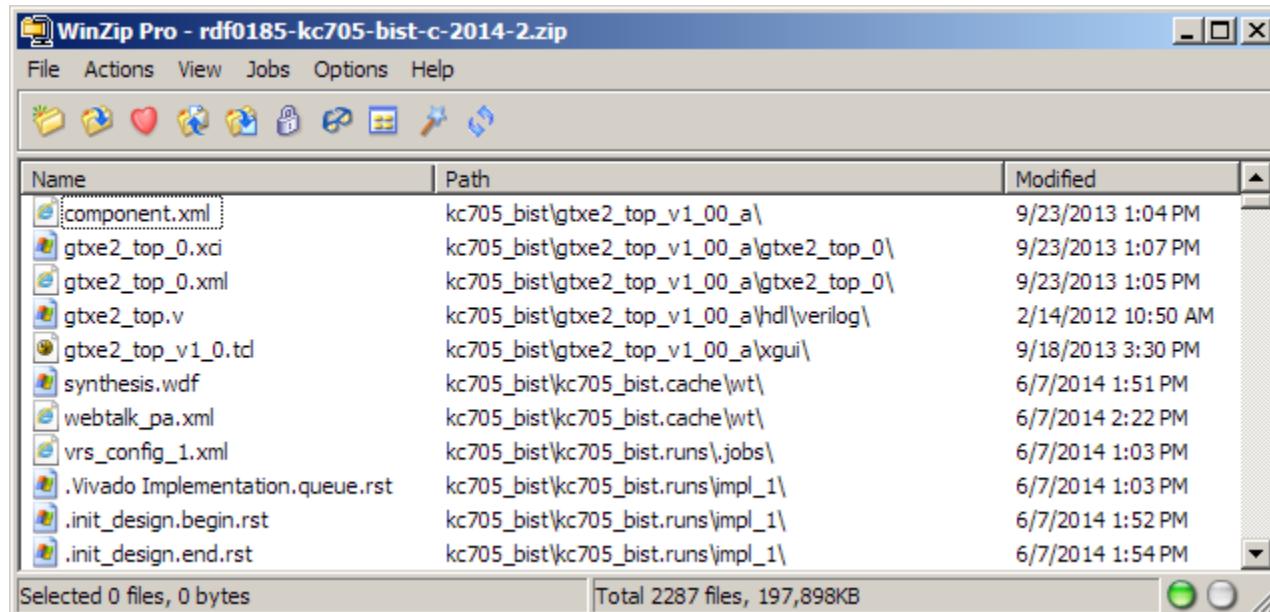
KC705 Setup

- Refer to [UG1036](#) regarding Tera Term installation
- Board Power must be on before starting Tera Term
- Start the Terminal Program
 - Select your USB Com Port
 - Set the baud to 9600



KC705 Setup

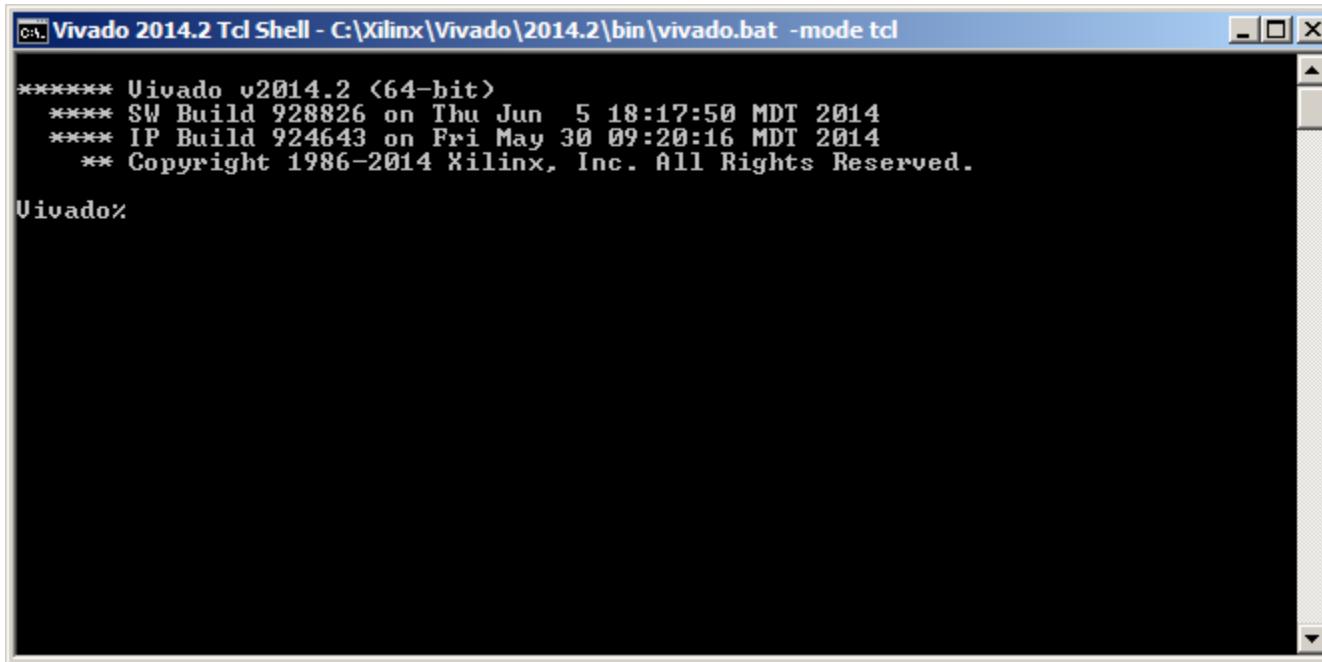
- Unzip the RDF0185 - KC705 BIST Design Files (2014.2 C) zip file
 - Available through <http://www.xilinx.com/kc705>



KC705 BIST

► Open a Vivado Tcl Shell:

**Start → All Programs → Xilinx Design Tools → Vivado 2014.2 →
Vivado 2014.2 Tcl Shell**



The screenshot shows a terminal window titled "Vivado 2014.2 Tcl Shell - C:\Xilinx\Vivado\2014.2\bin\vivado.bat -mode tcl". The window displays the following startup information:

```
***** Vivado v2014.2 (64-bit)
***** SW Build 928826 on Thu Jun  5 18:17:50 MDT 2014
***** IP Build 924643 on Fri May 30 09:20:16 MDT 2014
** Copyright 1986-2014 Xilinx, Inc. All Rights Reserved.
```

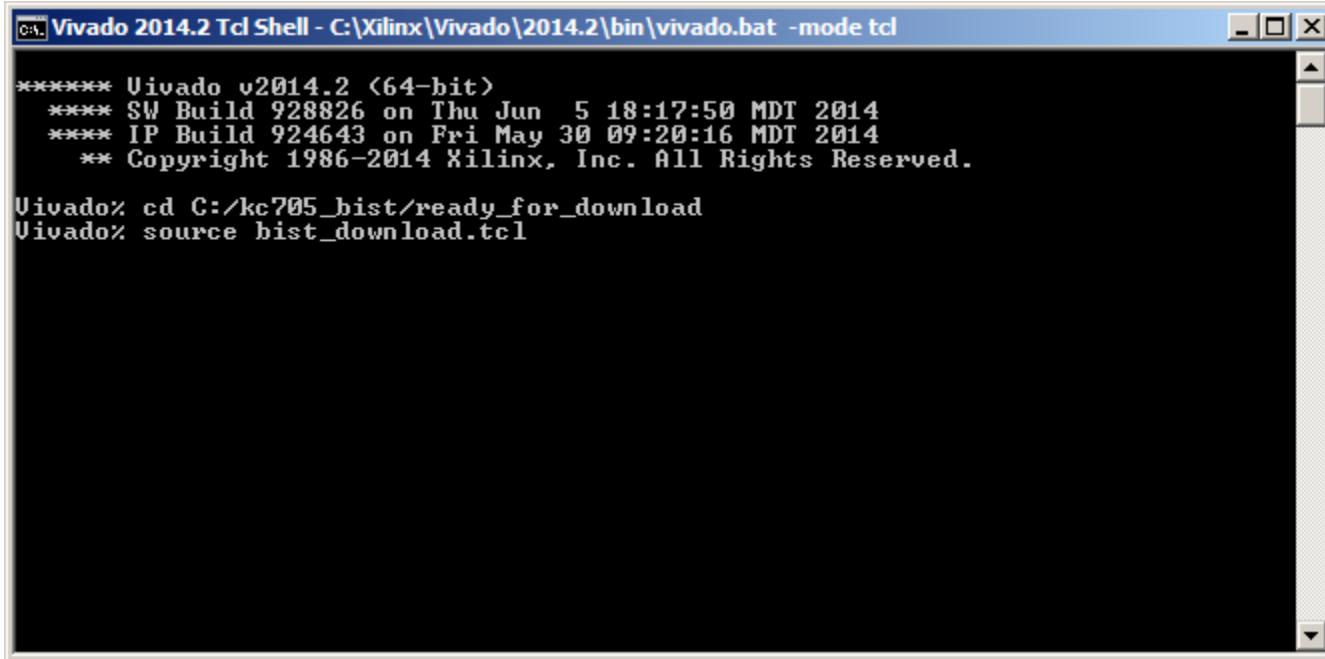
The prompt "Vivado%" is visible at the bottom of the window.

KC705 BIST

► Download the BIST bitstream

► In the Vivado Tcl Shell type:

```
cd C:/kc705_bist/ready_for_download  
source bist_download.tcl
```

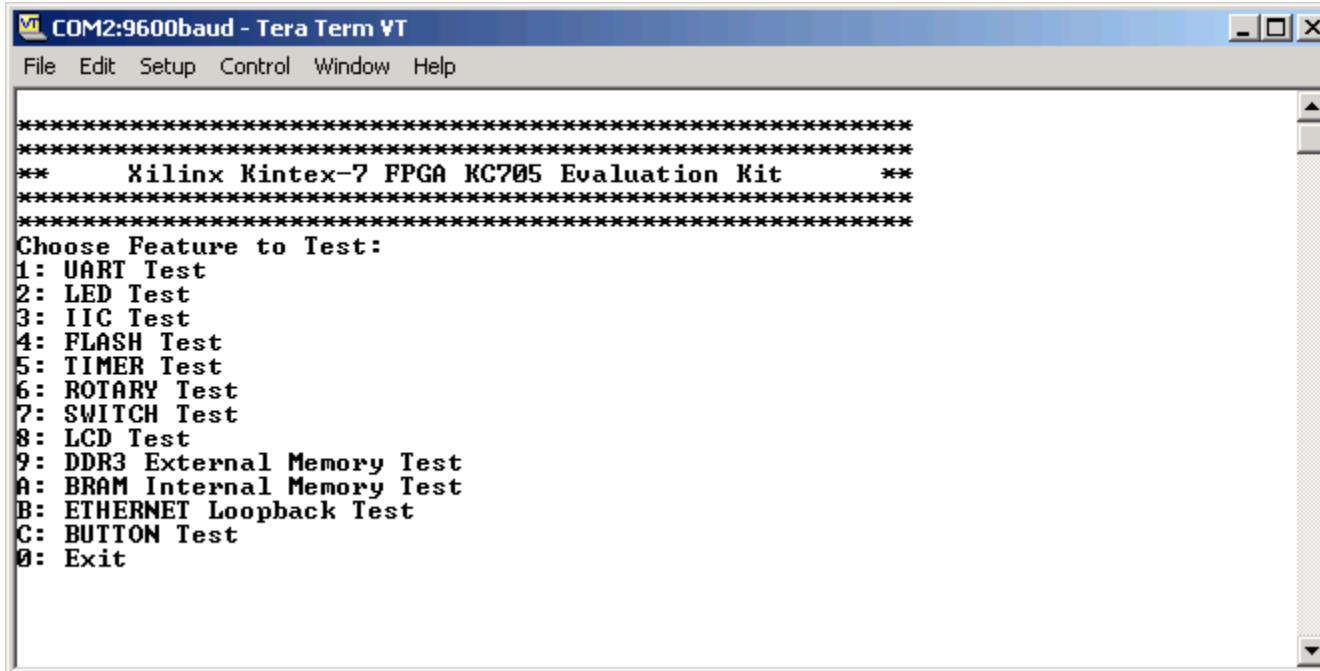


The screenshot shows a terminal window titled "Vivado 2014.2 Tcl Shell - C:\Xilinx\Vivado\2014.2\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2014.2 (64-bit)  
***** SW Build 928826 on Thu Jun  5 18:17:50 MDT 2014  
***** IP Build 924643 on Fri May 30 09:20:16 MDT 2014  
** Copyright 1986-2014 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/kc705_bist/ready_for_download  
Vivado> source bist_download.tcl
```

KC705 BIST

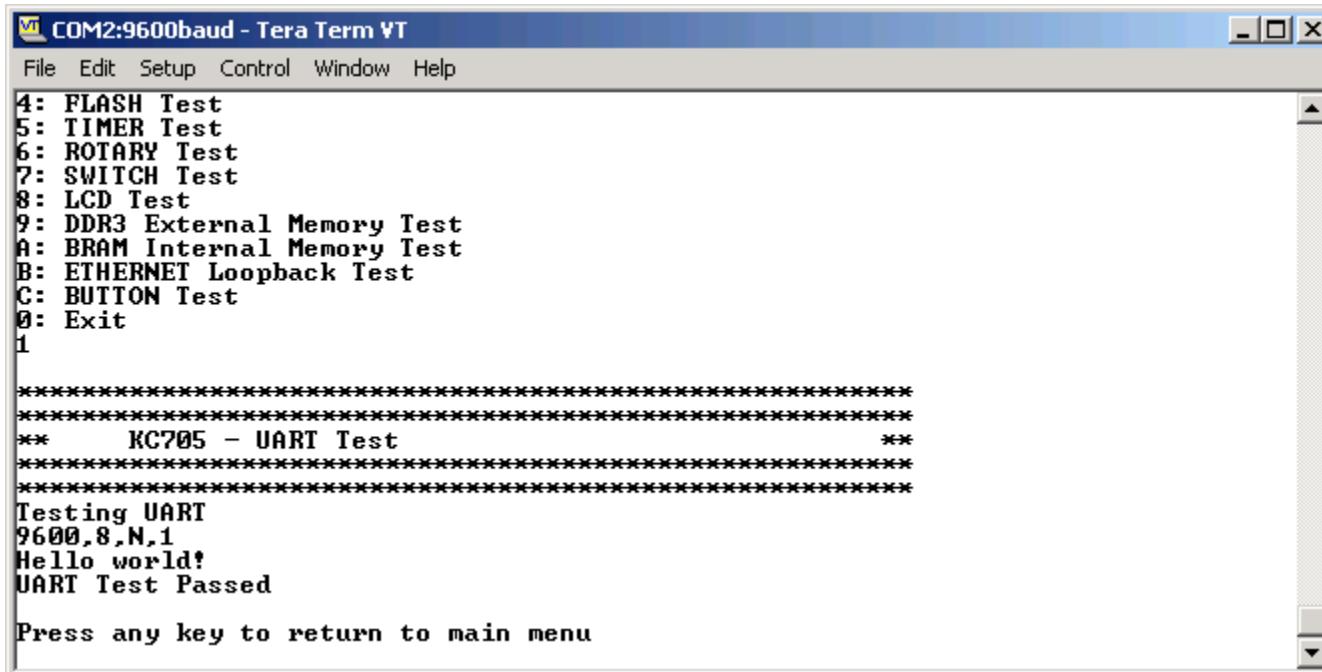
► View initial BIST screen



KC705 BIST

➤ UART Test

- Type “1” to start the UART Test
- After each test, press any key to return to the main menu



The screenshot shows a terminal window titled "COM2:9600baud - Tera Term VT". The menu bar includes File, Edit, Setup, Control, Window, and Help. The main window displays a test menu and the results of a UART test.

```
File Edit Setup Control Window Help
4: FLASH Test
5: TIMER Test
6: ROTARY Test
7: SWITCH Test
8: LCD Test
9: DDR3 External Memory Test
A: BRAM Internal Memory Test
B: ETHERNET Loopback Test
C: BUTTON Test
0: Exit
1

*****
** KC705 - UART Test **
*****
Testing UART
9600,8,N,1
Hello world!
UART Test Passed

Press any key to return to main menu
```

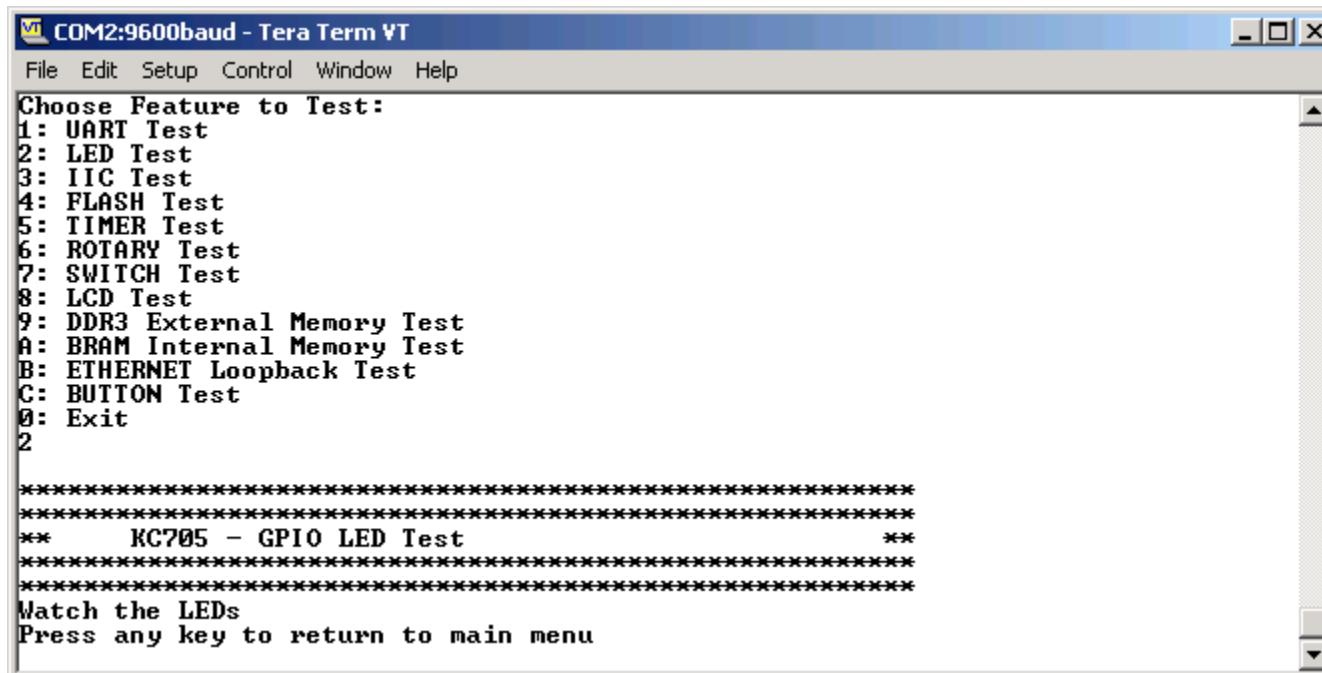
KC705 BIST

► LED Test

- Type 2 to begin LED Test

► View Walking 1's pattern on GPIO LEDs

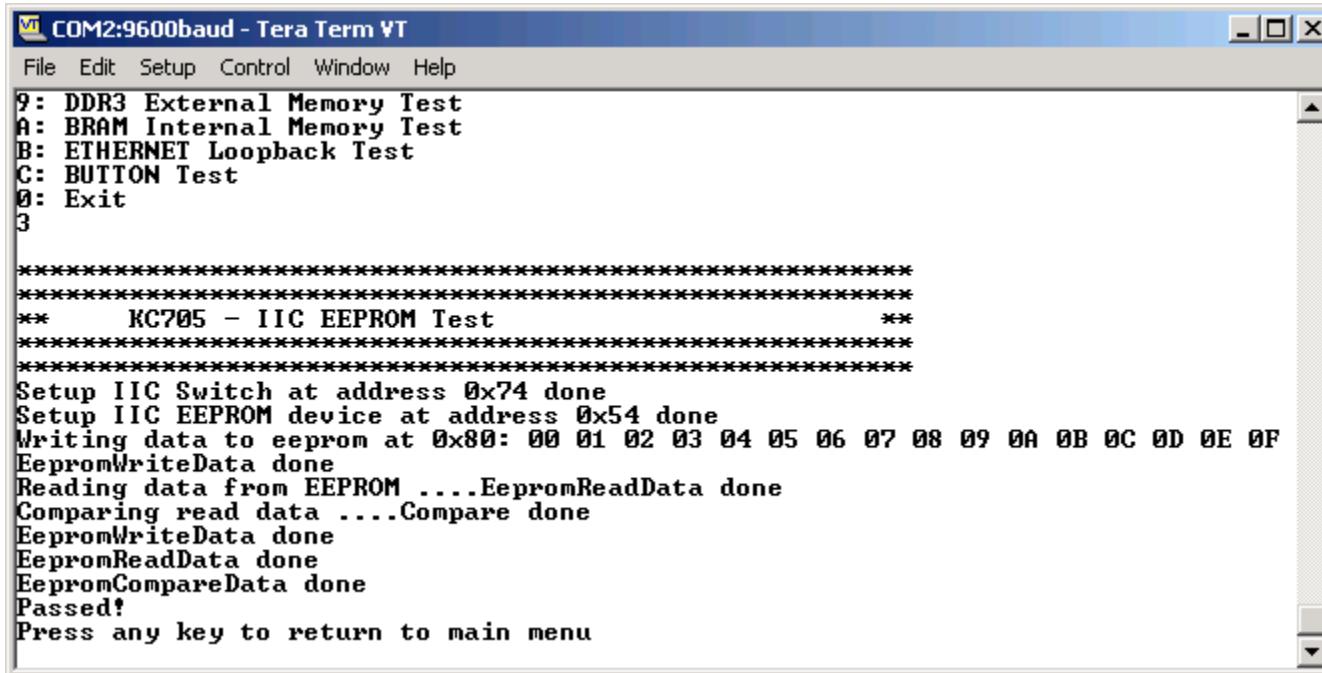
- Sequence repeats twice



KC705 BIST

► IIC Test

- Type 3 to begin IIC Test



The screenshot shows a terminal window titled "COM2:9600baud - Tera Term VT". The menu bar includes File, Edit, Setup, Control, Window, and Help. The main window displays a test menu:

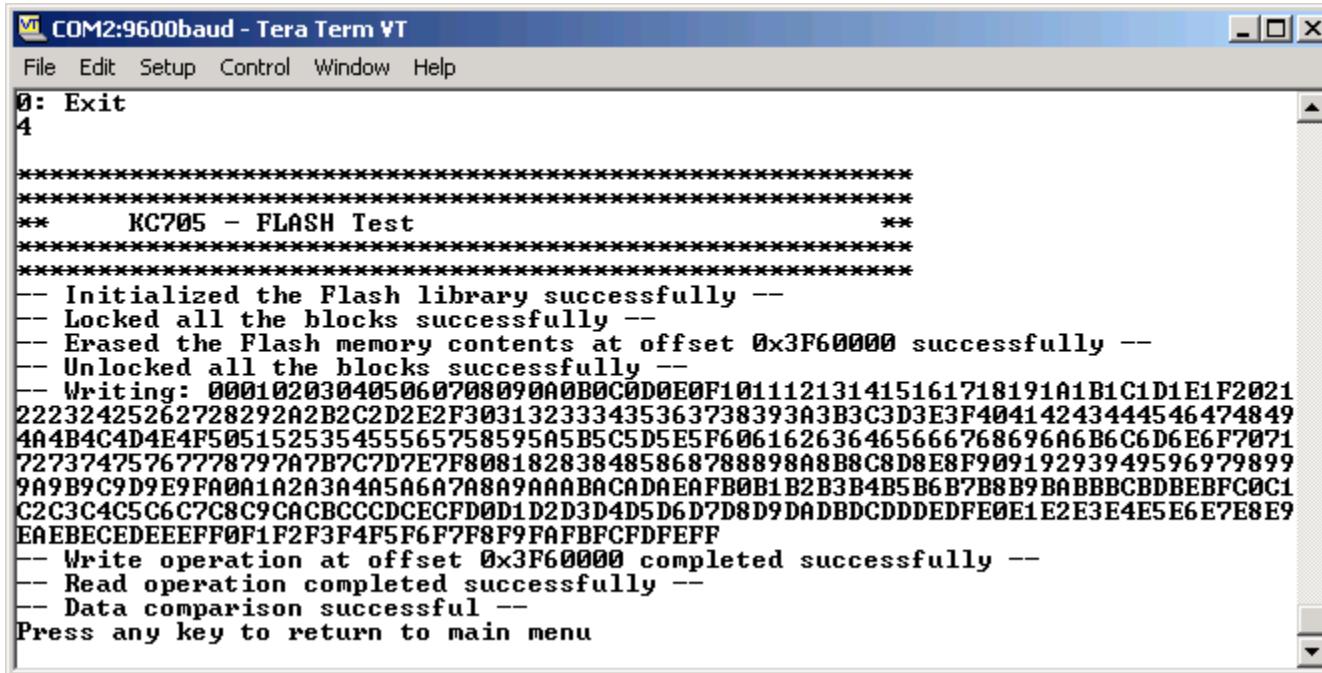
```
File Edit Setup Control Window Help
9: DDR3 External Memory Test
A: BRAM Internal Memory Test
B: ETHERNET Loopback Test
C: BUTTON Test
0: Exit
3

*****
**      KC705 - IIC EEPROM Test      **
*****
Setup IIC Switch at address 0x74 done
Setup IIC EEPROM device at address 0x54 done
Writing data to eeprom at 0x80: 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
EepromWriteData done
Reading data from EEPROM ....EepromReadData done
Comparing read data ....Compare done
EepromWriteData done
EepromReadData done
EepromCompareData done
Passed!
Press any key to return to main menu
```

KC705 BIST

► Flash Test

- Type 4 to begin Flash test

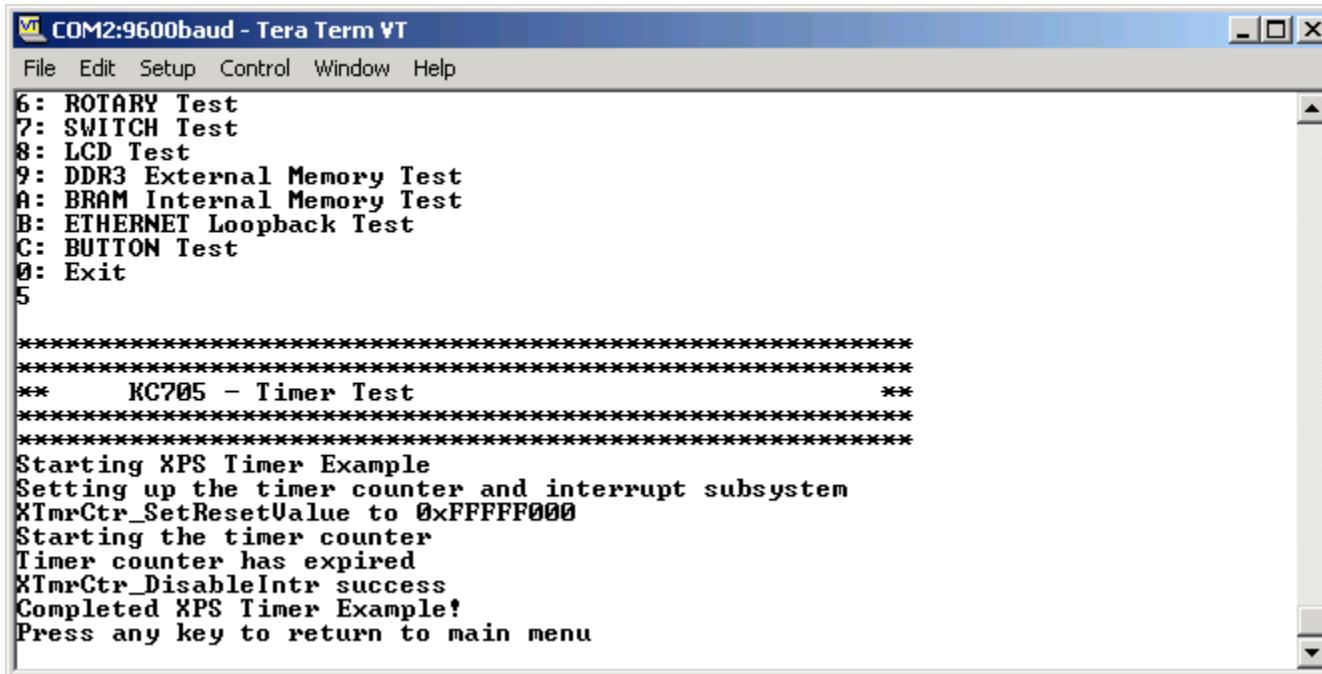


The screenshot shows a terminal window titled "COM2:9600baud - Tera Term VT". The window contains a log of a KC705 Flash Test. The log starts with "0: Exit" and "4", followed by a series of asterisks. It then displays the test steps: "KC705 - FLASH Test", "Initialized the Flash library successfully", "Locked all the blocks successfully", "Erased the Flash memory contents at offset 0x3F60000 successfully", "Unlocked all the blocks successfully", "Writing" followed by a long string of hex data (000102030405060708090A0B0C0D0E0F101112131415161718191A1B1C1D1E1F2021 22232425262728292A2B2C2D2E2F303132333435363738393A3B3C3D3E3F40414243444546474849 4A4B4C4D4E4F505152535455565758595A5B5C5D5E5F606162636465666768696A6B6C6D6E6F7071 72737475767778797A7B7C7D7E7F8008182838485868788898A8B8C8D8E8F90919293949596979899 9A9B9C9D9E9FA0A1A2A3A4A5A6A7A8A9AAABACADAEAFB0B1B2B3B4B5B6B7B8B9BABBBCDBEBFC0C1 C2C3C4C5C6C7C8C9CACBCCCCDCECFD0D1D2D3D4D5D6D7D8D9DADBDCCDDDEDFFE0E1E2E3E4E5E6E7E8E9 EAEBECEDEEEFF0F1F2F3F4F5F6F7F8F9FAFBFCFDFEFF). Finally, it shows "Write operation at offset 0x3F60000 completed successfully", "Read operation completed successfully", "Data comparison successful", and "Press any key to return to main menu".

KC705 BIST

► Timer Test

- Type 5 to begin Timer Test



The screenshot shows a terminal window titled "COM2:9600baud - Tera Term VT". The menu options listed are:

- 6: ROTARY Test
- 7: SWITCH Test
- 8: LCD Test
- 9: DDR3 External Memory Test
- A: BRAM Internal Memory Test
- B: ETHERNET Loopback Test
- C: BUTTON Test
- 0: Exit
- 5

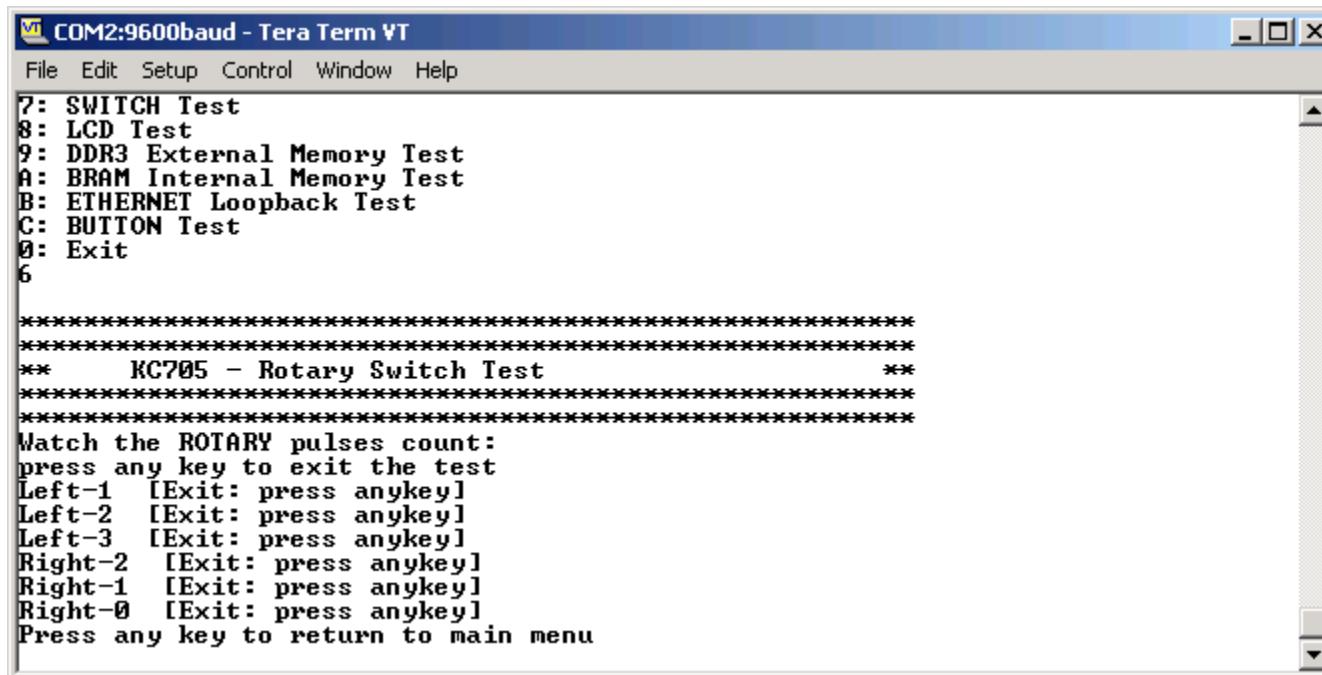
After selecting option 5, the following log output is displayed:

```
*****
**      KC705 - Timer Test      **
*****
Starting XPS Timer Example
Setting up the timer counter and interrupt subsystem
XTmrCtr_SetResetValue to 0xFFFFF000
Starting the timer counter
Timer counter has expired
XTmrCtr_DisableIntr success
Completed XPS Timer Example!
Press any key to return to main menu
```

KC705 BIST

► Rotary Test

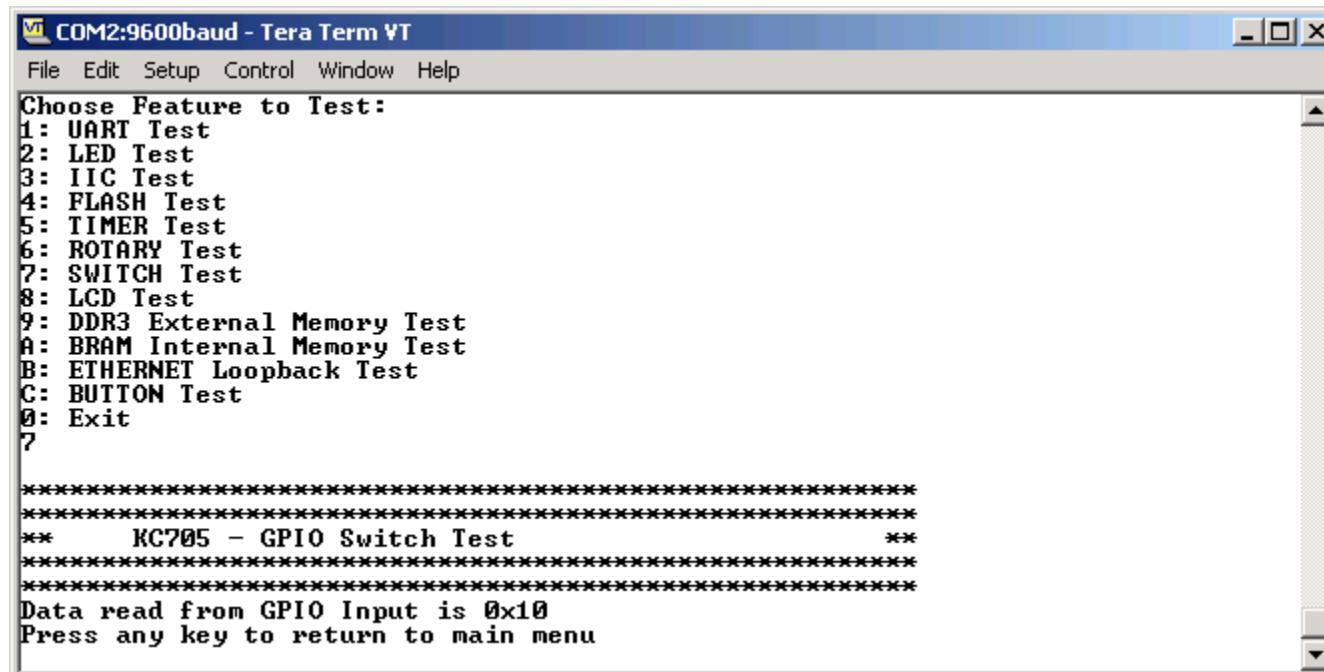
- Type 6 to begin Rotary Test
- Turn the rotary switch (under the LCD) back and forth
- Push the rotary switch inwards to actuate the push button switch



KC705 BIST

► GPIO Switch Test

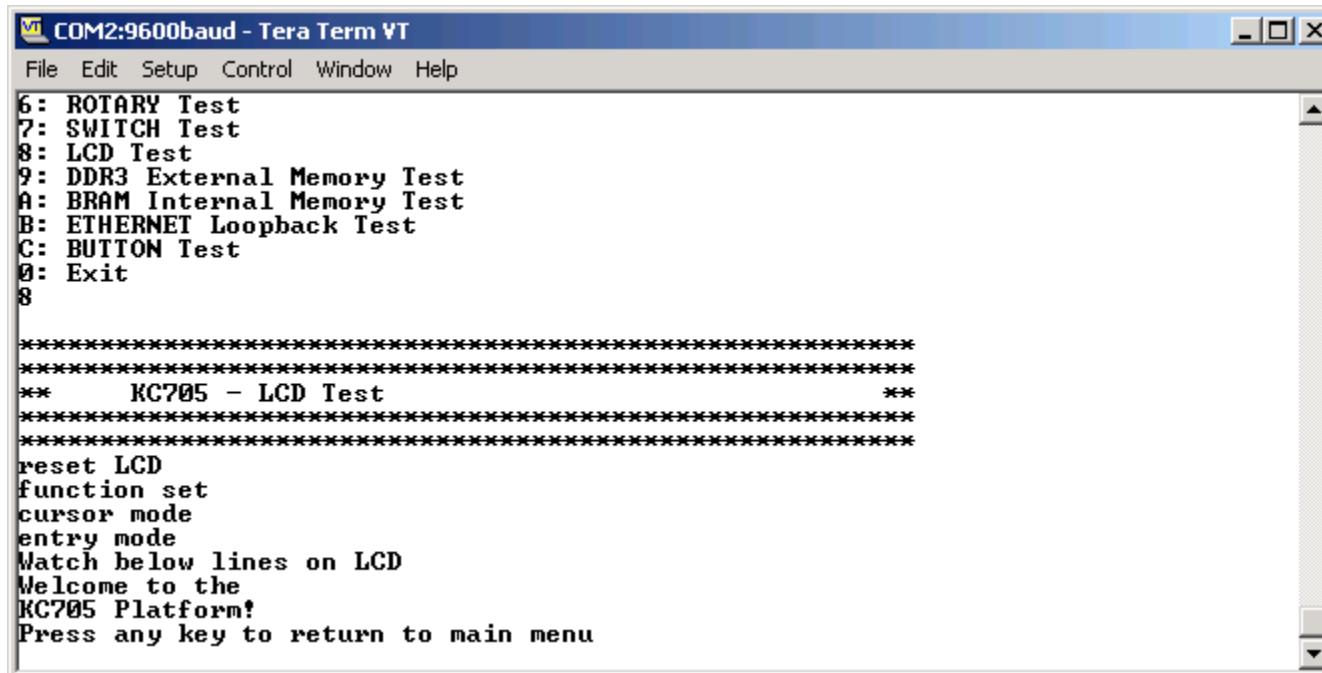
- Set 4-position GPIO DIP Switch (SW4)
- Type 7 to begin GPIO Switch Test
 - Reads switch settings



KC705 BIST

► LCD Test

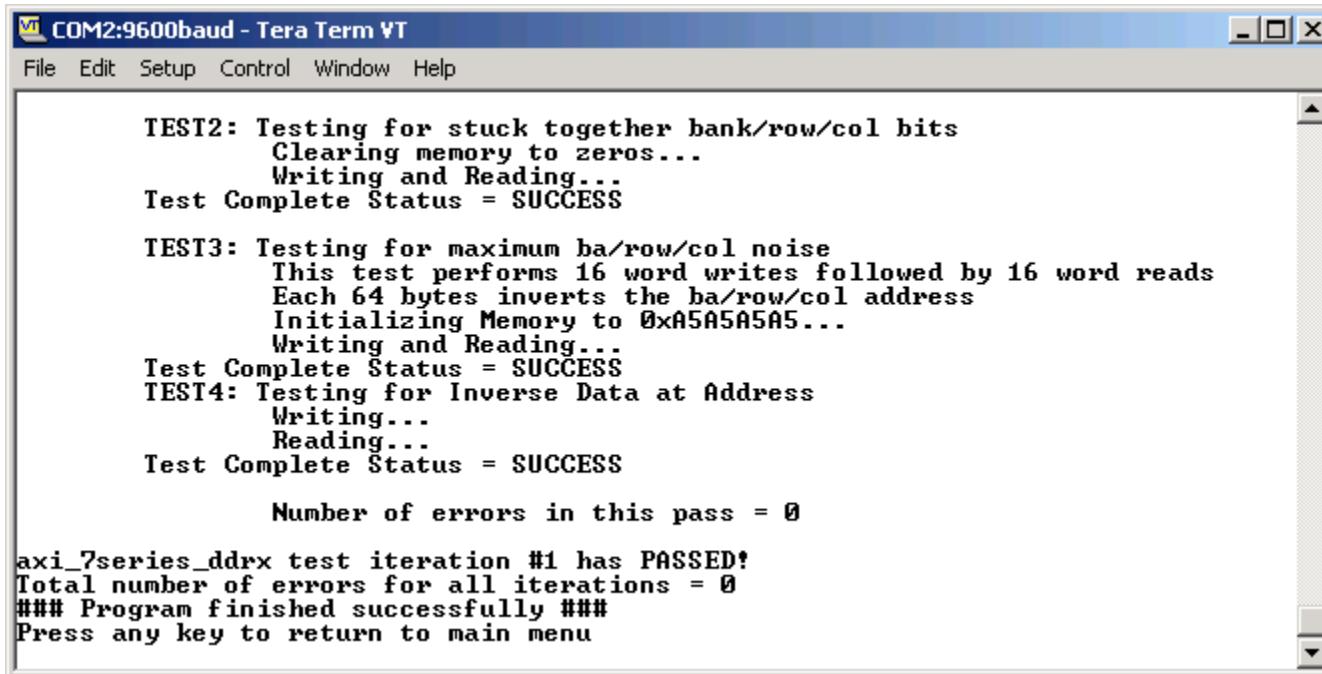
- Type 8 to begin LCD Test



KC705 BIST

► External Memory Test

- Type 9 to begin External Memory Test



COM2:9600baud - Tera Term VT

File Edit Setup Control Window Help

```
TEST2: Testing for stuck together bank/row/col bits
Clearing memory to zeros...
Writing and Reading...
Test Complete Status = SUCCESS

TEST3: Testing for maximum ba/row/col noise
This test performs 16 word writes followed by 16 word reads
Each 64 bytes inverts the ba/row/col address
Initializing Memory to 0xA5A5A5A5...
Writing and Reading...
Test Complete Status = SUCCESS
TEST4: Testing for Inverse Data at Address
Writing...
Reading...
Test Complete Status = SUCCESS

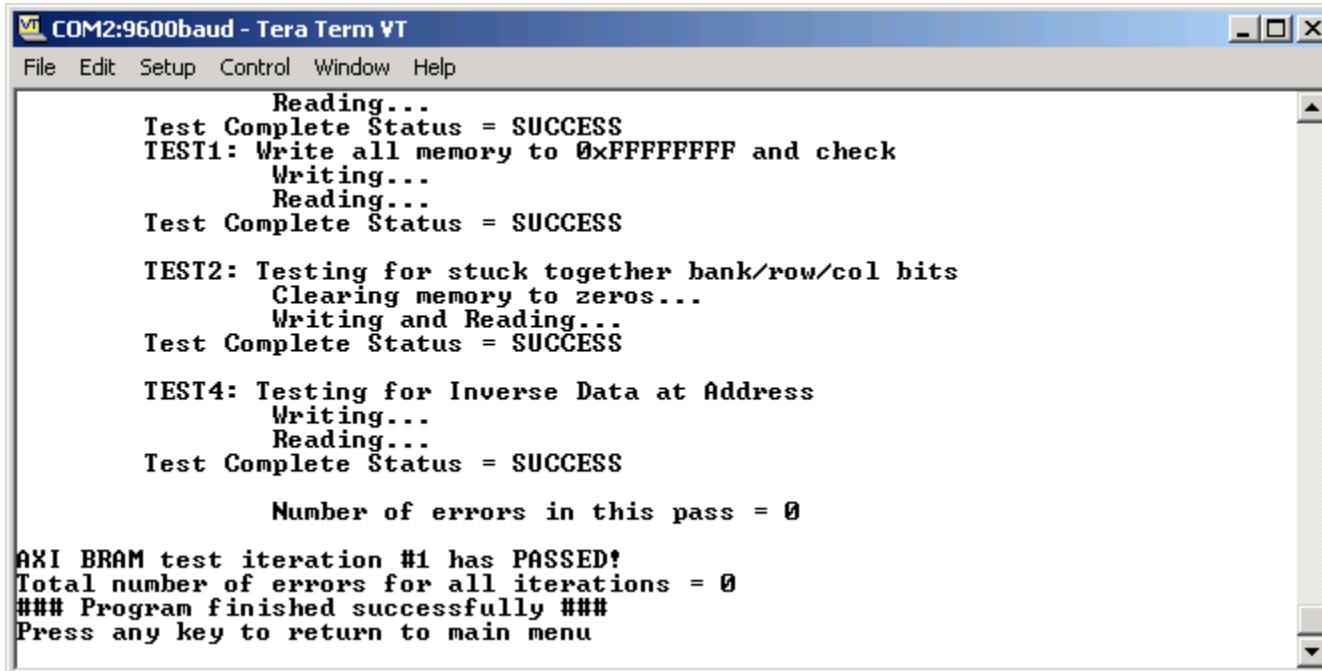
Number of errors in this pass = 0

axi_7series_ddrx test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### Program finished successfully ####
Press any key to return to main menu
```

KC705 BIST

► Internal Memory Test

- Type A to begin BRAM Memory Test



COM2:9600baud - Tera Term VT

```
Reading...
Test Complete Status = SUCCESS
TEST1: Write all memory to 0xFFFFFFFF and check
      Writing...
      Reading...
Test Complete Status = SUCCESS

TEST2: Testing for stuck together bank/row/col bits
      Clearing memory to zeros...
      Writing and Reading...
Test Complete Status = SUCCESS

TEST4: Testing for Inverse Data at Address
      Writing...
      Reading...
Test Complete Status = SUCCESS

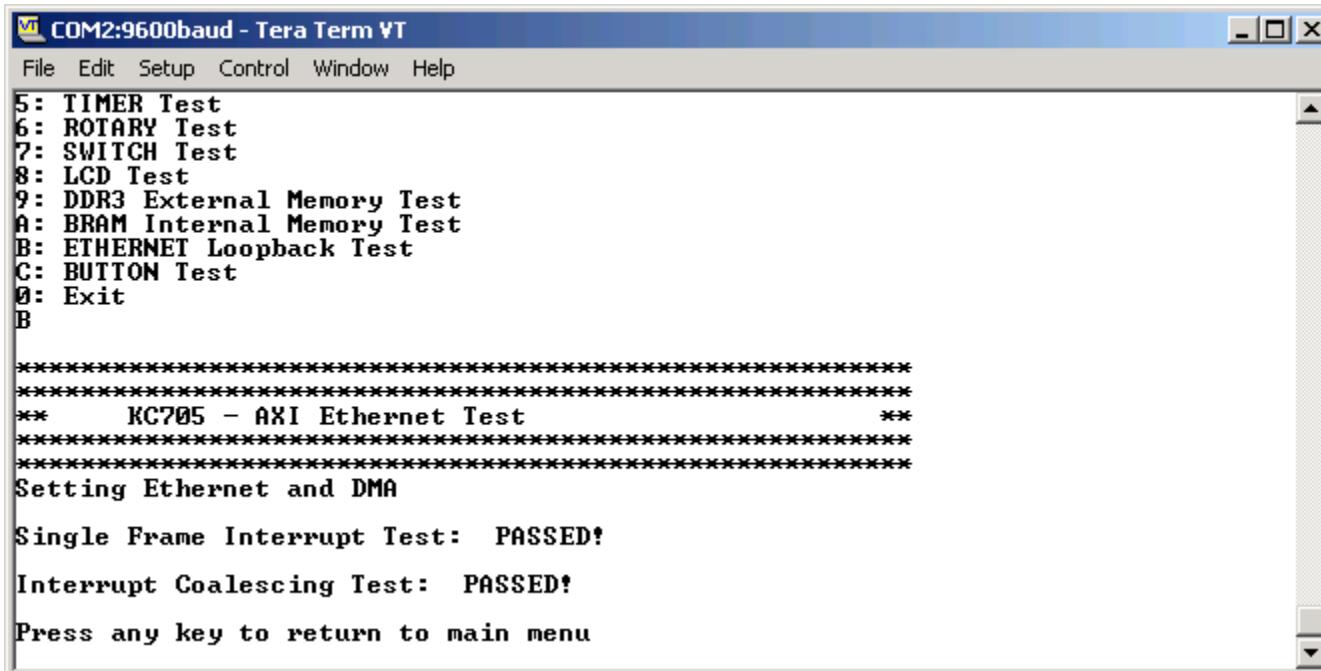
      Number of errors in this pass = 0

AXI BRAM test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### Program finished successfully ####
Press any key to return to main menu
```

KC705 BIST

► Ethernet Test

- Type B to begin AXI Ethernet Test



COM2:9600baud - Tera Term VT

File Edit Setup Control Window Help

```
5: TIMER Test
6: ROTARY Test
7: SWITCH Test
8: LCD Test
9: DDR3 External Memory Test
A: BRAM Internal Memory Test
B: ETHERNET Loopback Test
C: BUTTON Test
0: Exit
B

*****
**      KC705 - AXI Ethernet Test      **
*****
Setting Ethernet and DMA

Single Frame Interrupt Test: PASSED!
Interrupt Coalescing Test: PASSED!
Press any key to return to main menu
```

KC705 BIST

► Button Test

- Type C to begin Button Test



```
VI COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help
B: ETHERNET Loopback Test
C: BUTTON Test
Q: Exit
C

*****
**      KC705 - Button Test      **
*****
Press west button
Press south button
Press east button
Press north button
Press center button
Press any button
Press any key to return to main menu
```

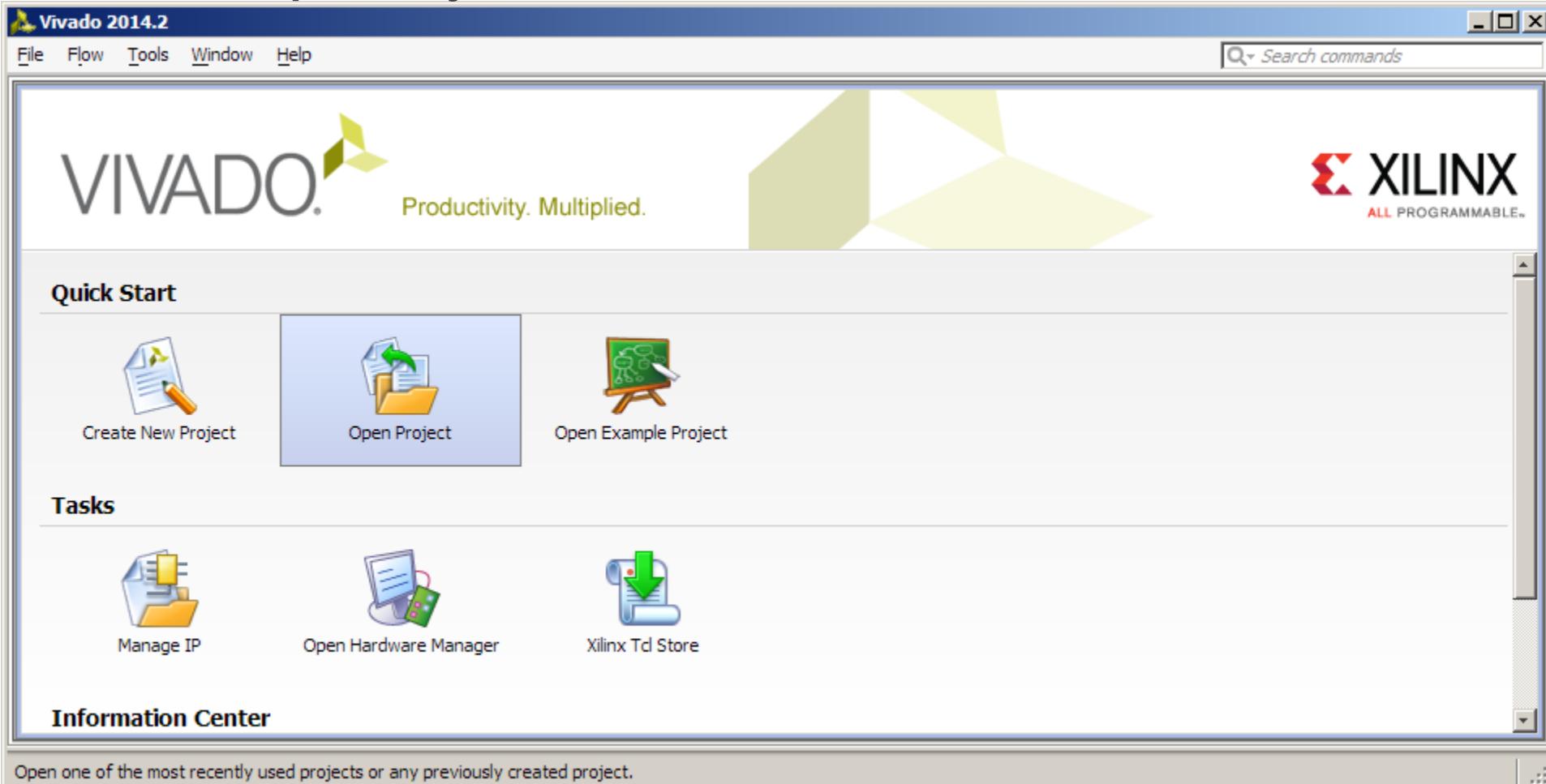
Compile KC705 BIST Design

Compile KC705 BIST Design

► Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2014.2 → Vivado

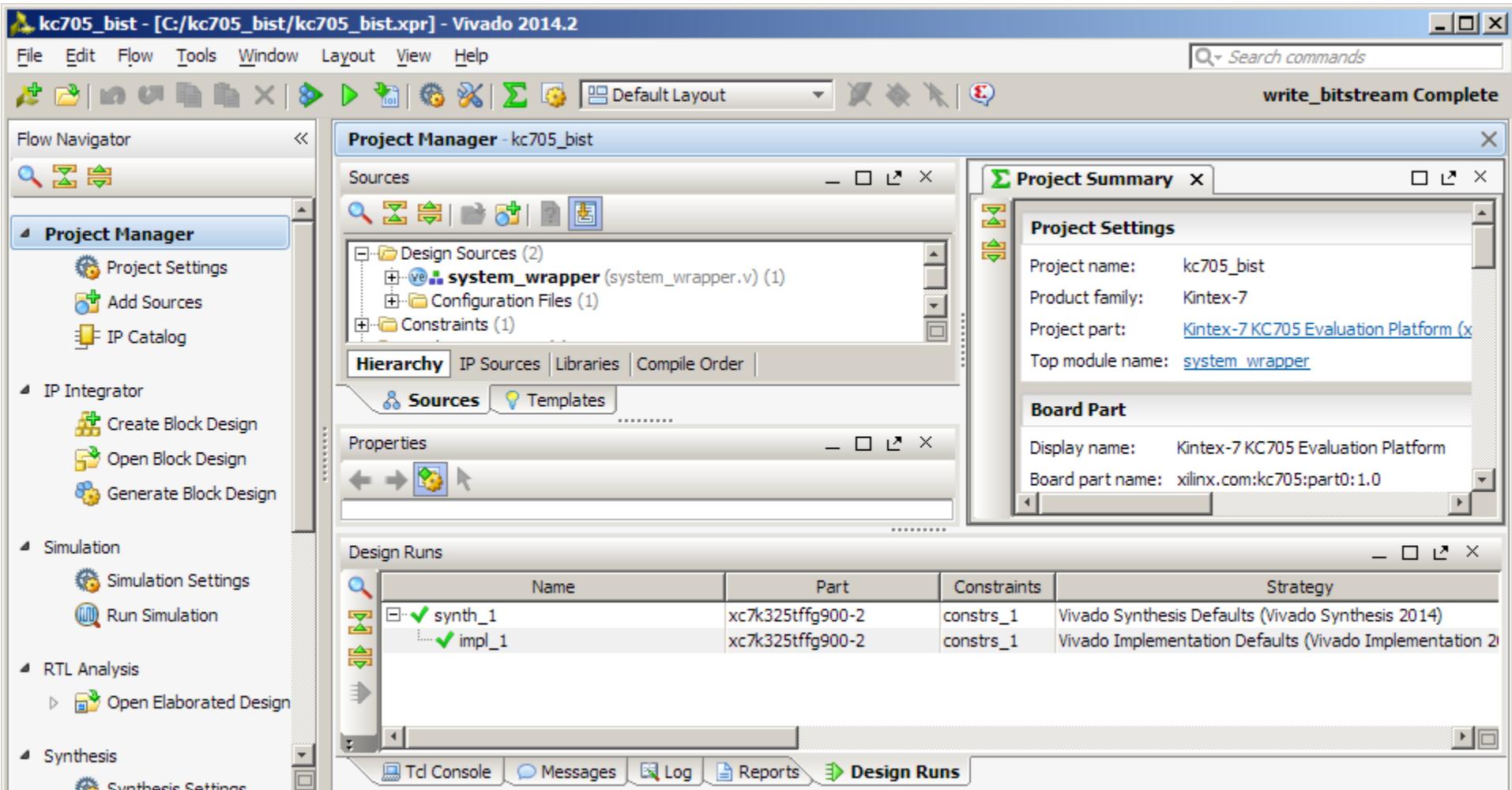
► Select Open Project



Compile KC705 BIST Design

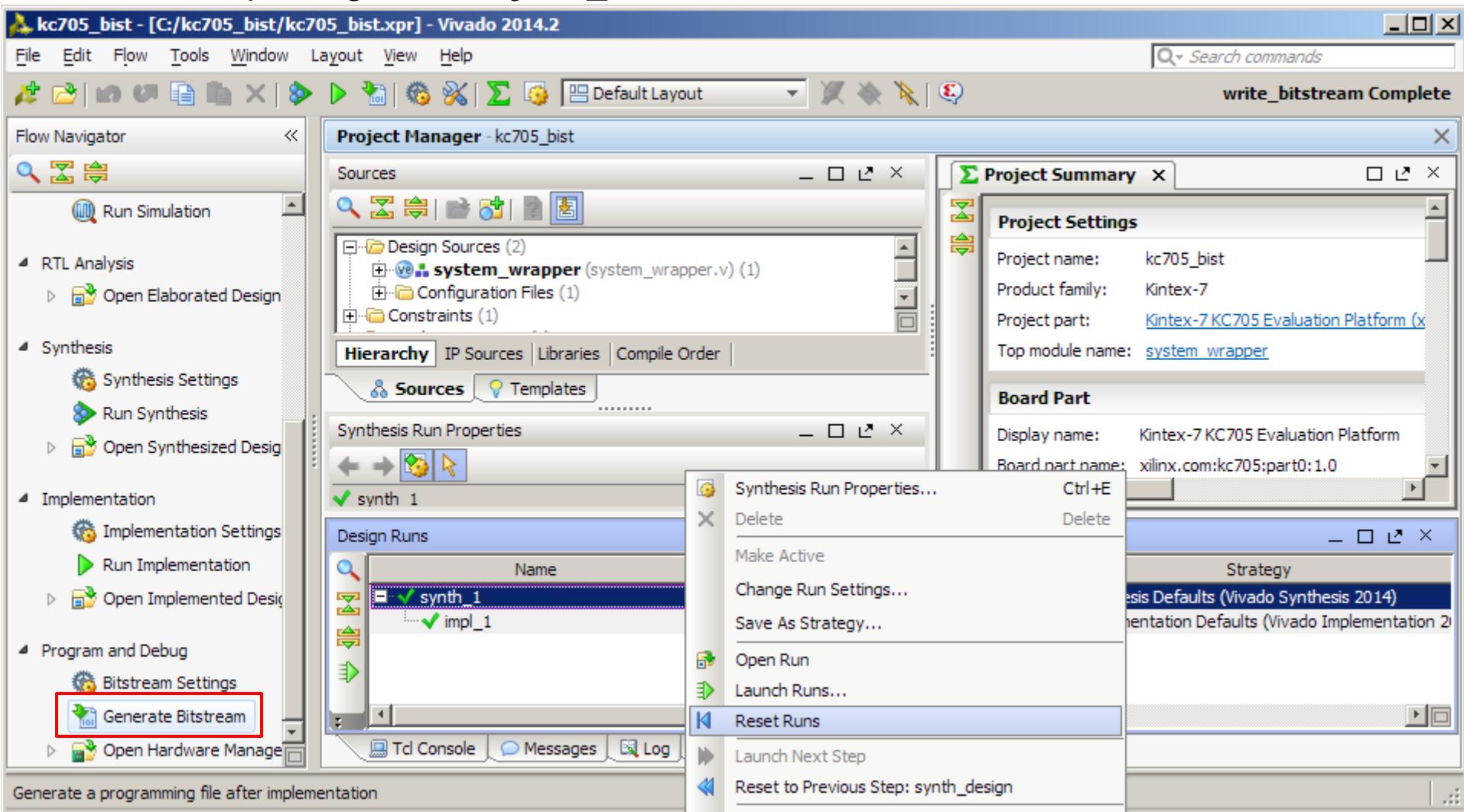
► Open the KC705 Design:

- <Design Name>\kc705_bist\kc705_bist.xpr



Compile KC705 BIST Design

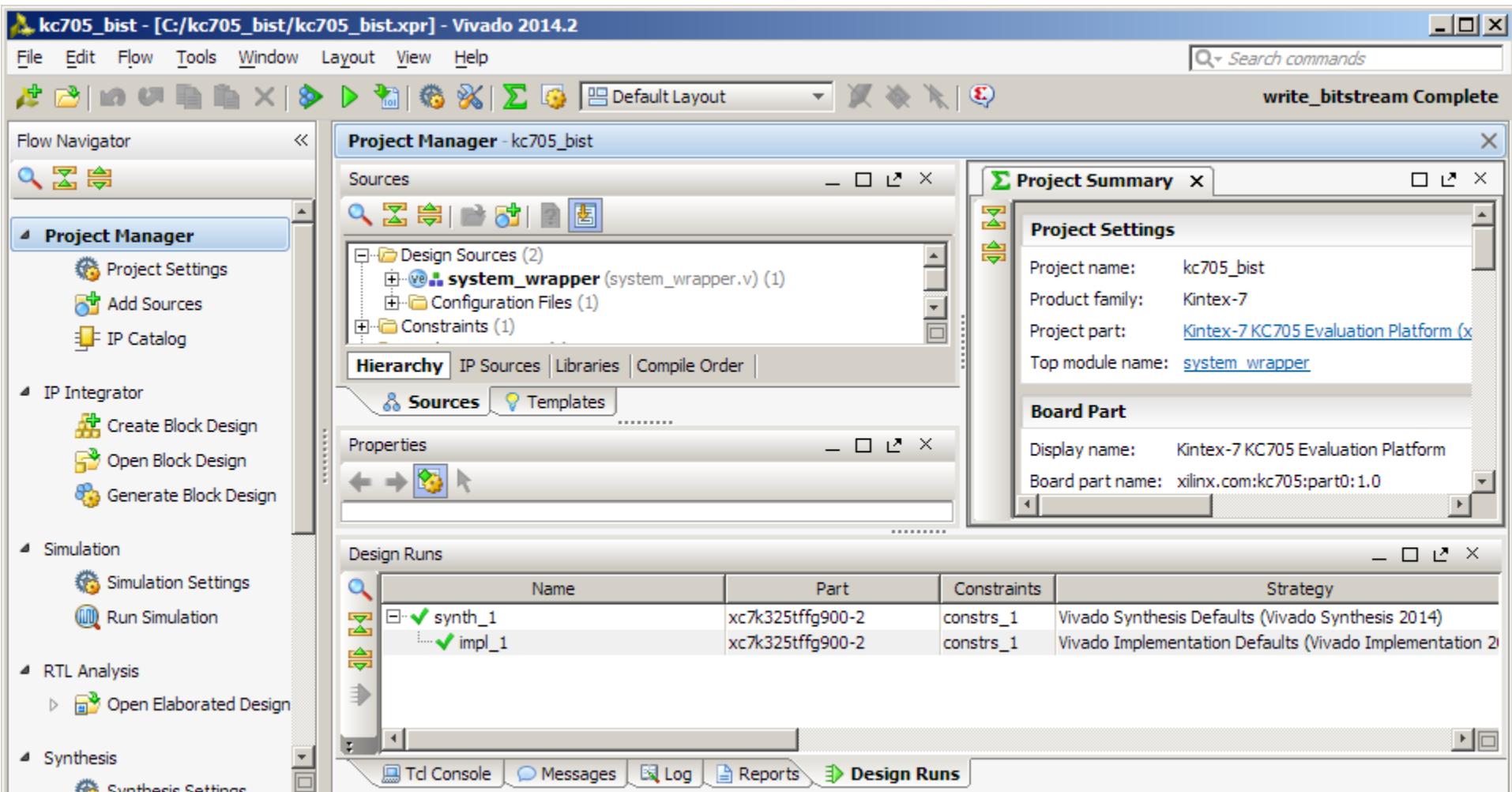
- The design is fully implemented; you can recompile, or export to SDK
 - To recompile, right-click **synth_1**, select **Reset Runs** then **Generate Bitstream**



Note: Presentation applies to the KC705

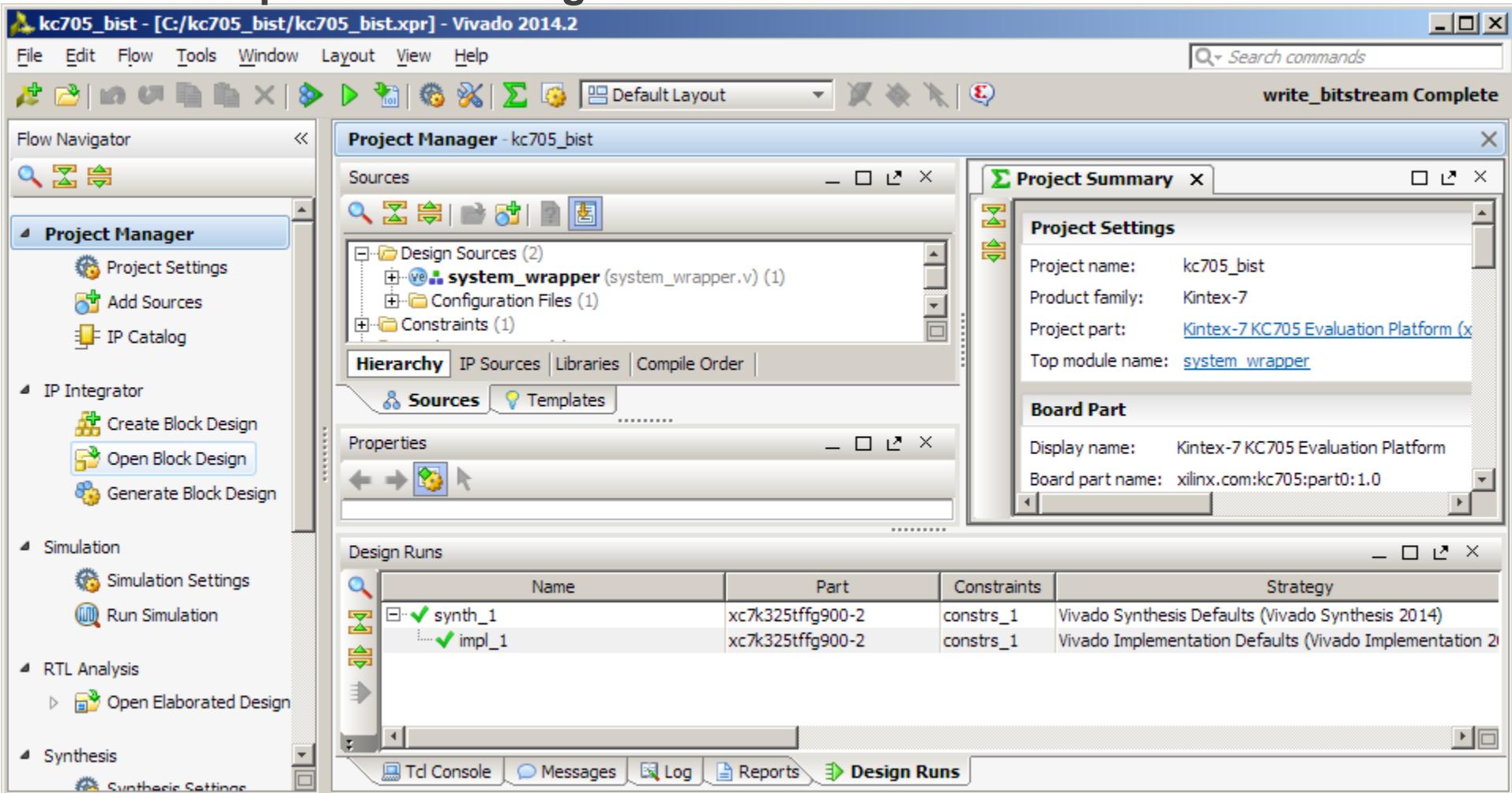
Compile KC705 BIST Design

- Once done, both the Synthesis and Implementation will have green check marks



Compile KC705 BIST Design

- The BIST Design has been implemented with IP Integrator (IPI)
- Click Open Block Design



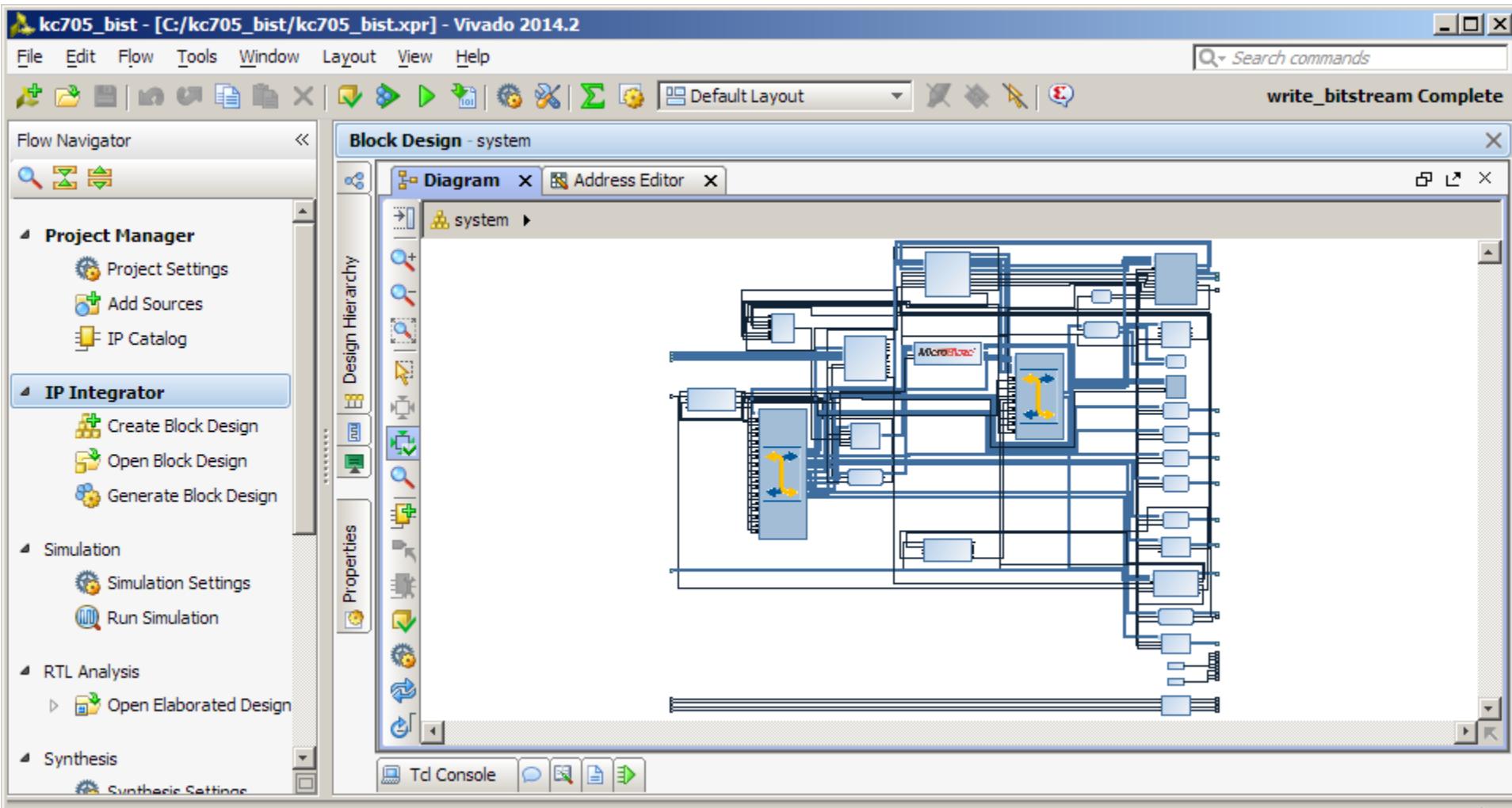
Open an IP subsystem from the current project

Note: Presentation applies to the KC705

XILINX ➤ ALL PROGRAMMABLE

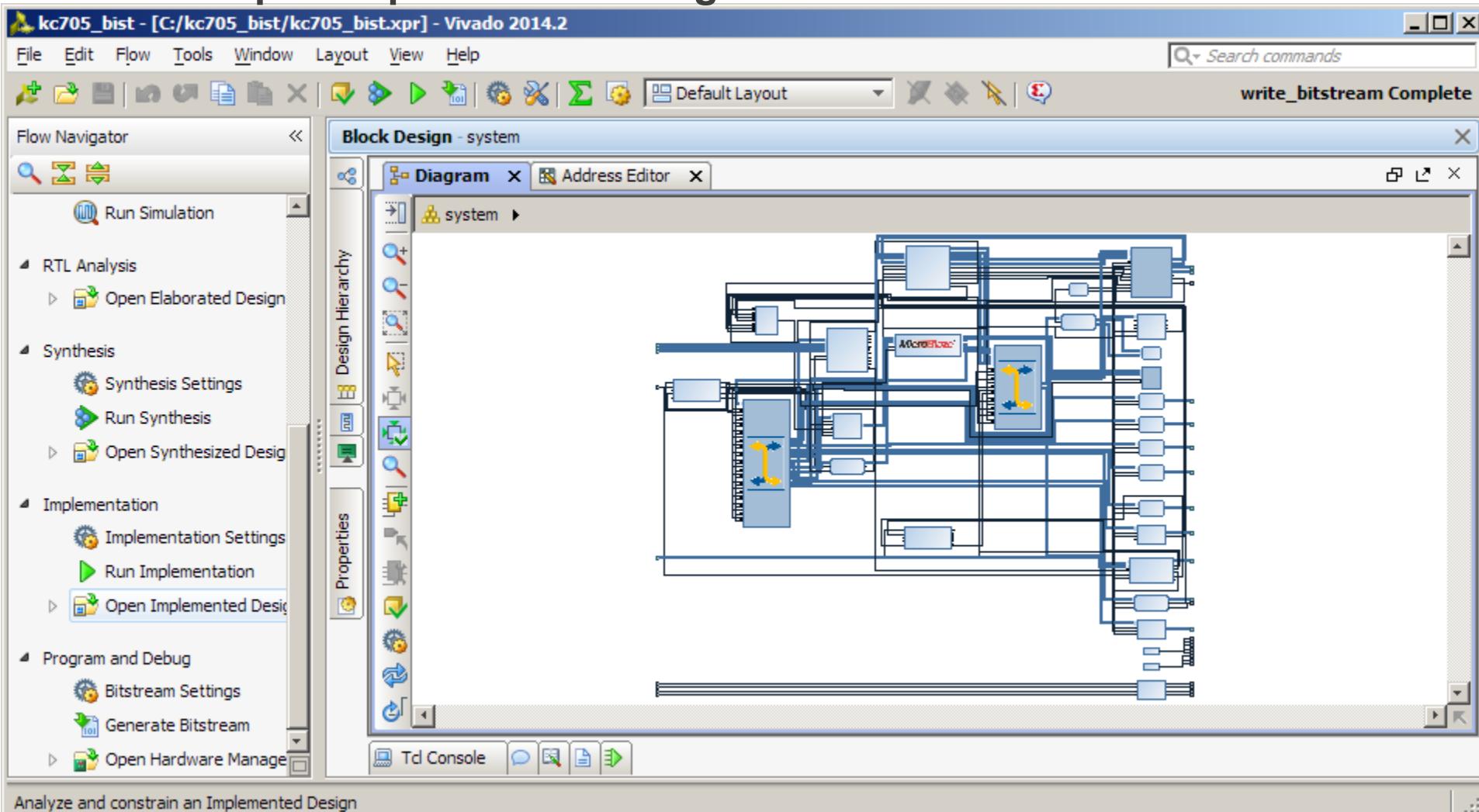
Compile KC705 BIST Design

► All the IP Blocks used in the design can be seen in this view



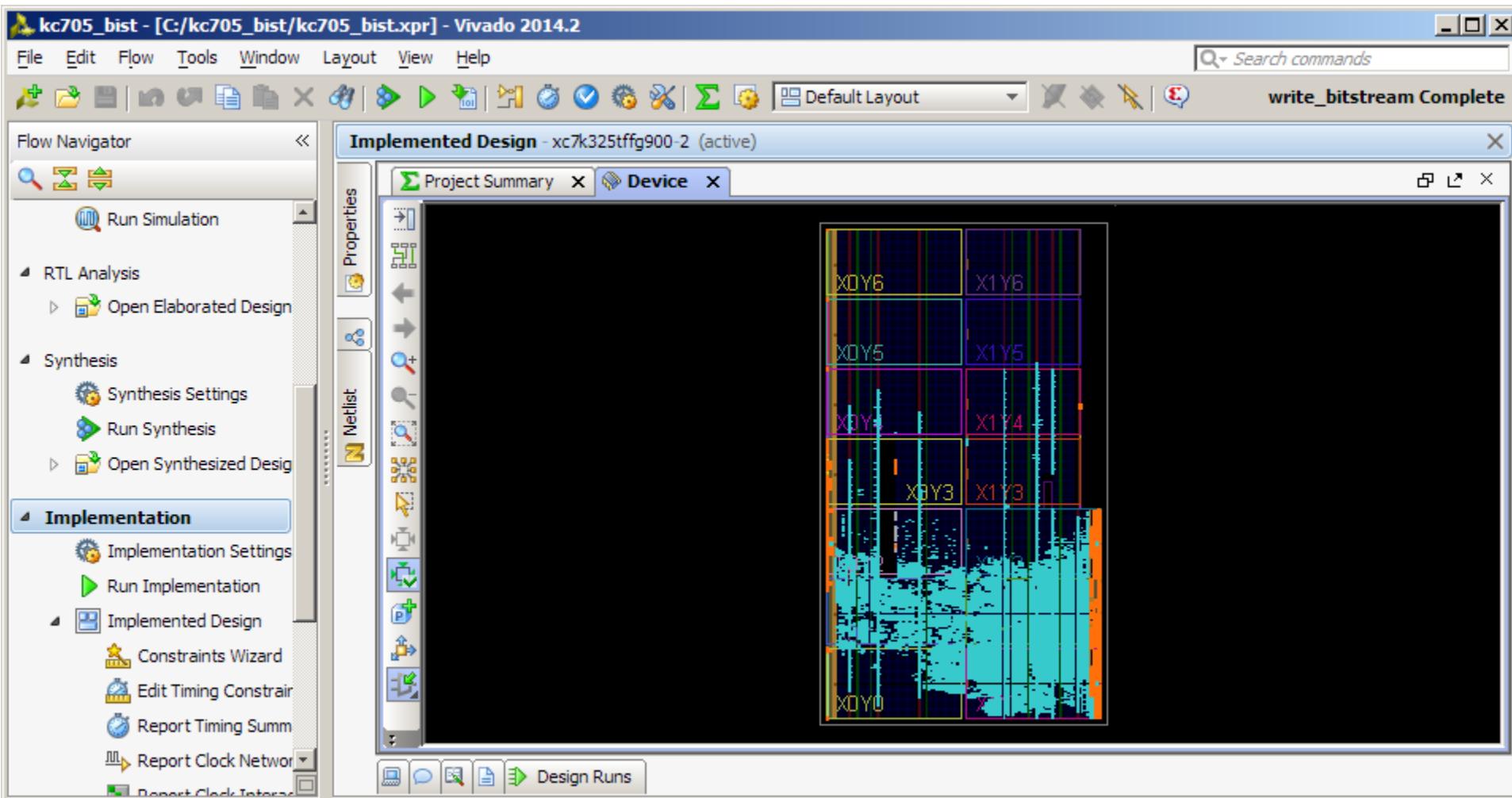
Compile KC705 BIST Design

- To export to SDK, the Block and Implemented designs must be open
- Click Open Implemented Design



Compile KC705 BIST Design

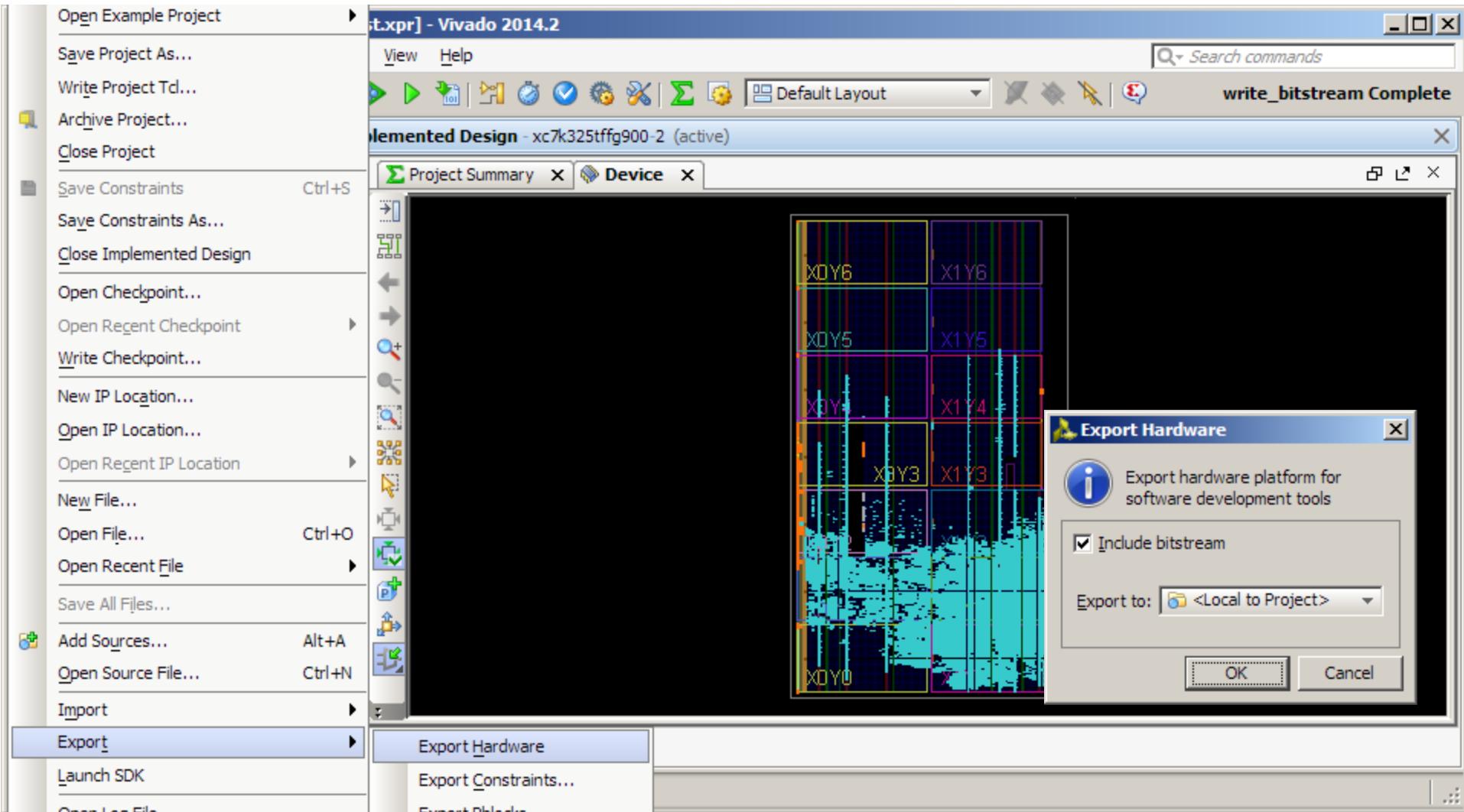
► View Implemented Design



Compile KC705 BIST Design

► Select File → Export → Export Hardware

► Click OK



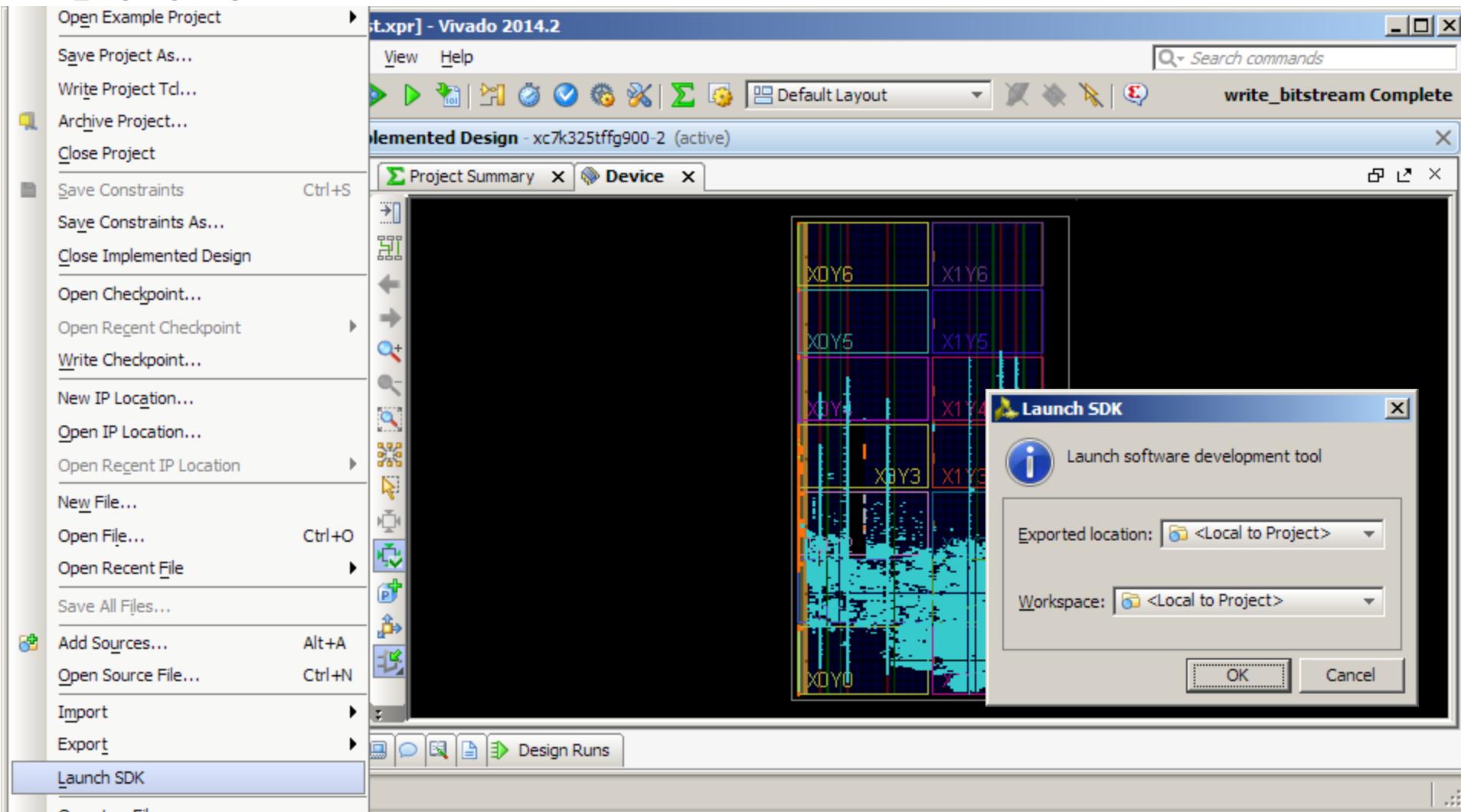
Note: Presentation applies to the KC705

XILINX ALL PROGRAMMABLE™

Compile KC705 BIST Design

► Select File → Launch SDK

► Click OK



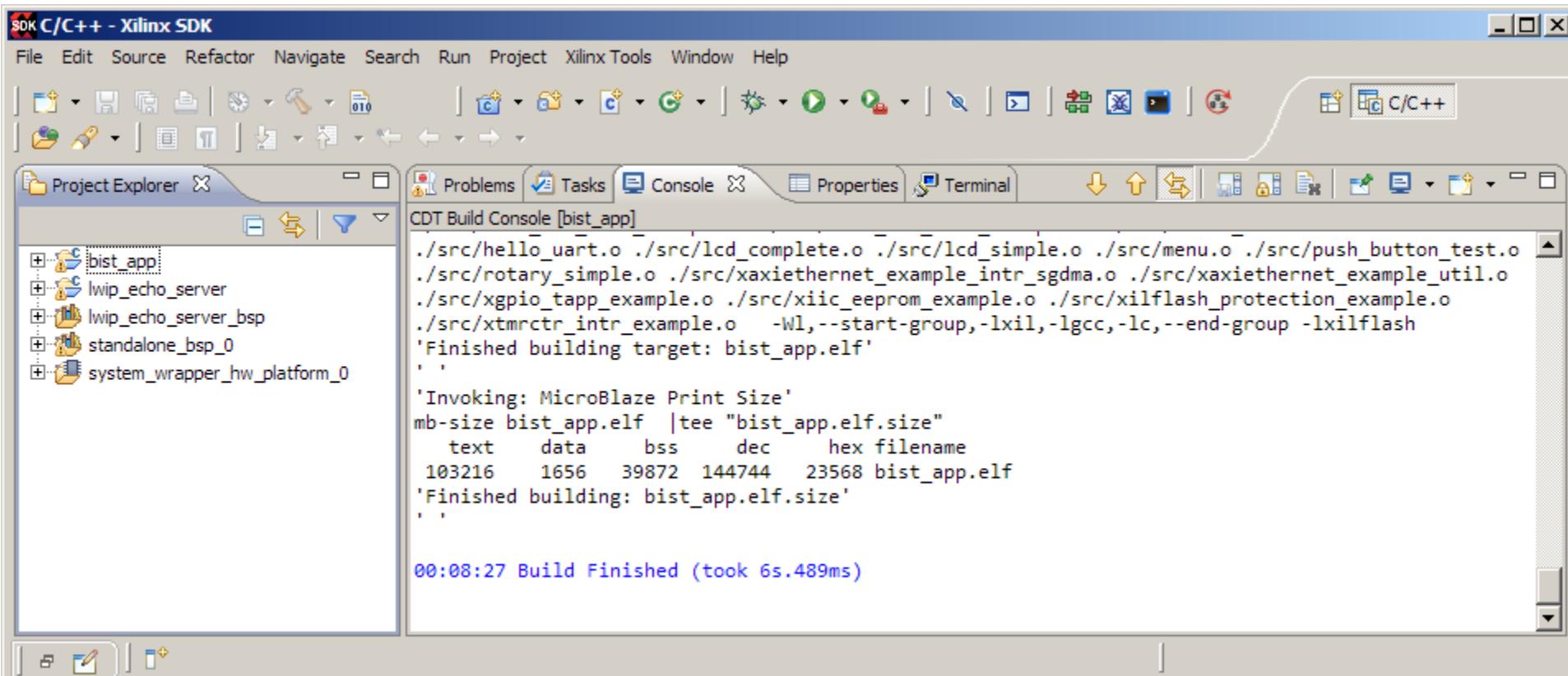
Note: Presentation applies to the KC705

XILINX ➤ ALL PROGRAMMABLE™

Compile KC705 Software in SDK

► SDK Software Compile - Build ELF files in SDK

- Project builds automatically
- When done, close SDK and return to Vivado



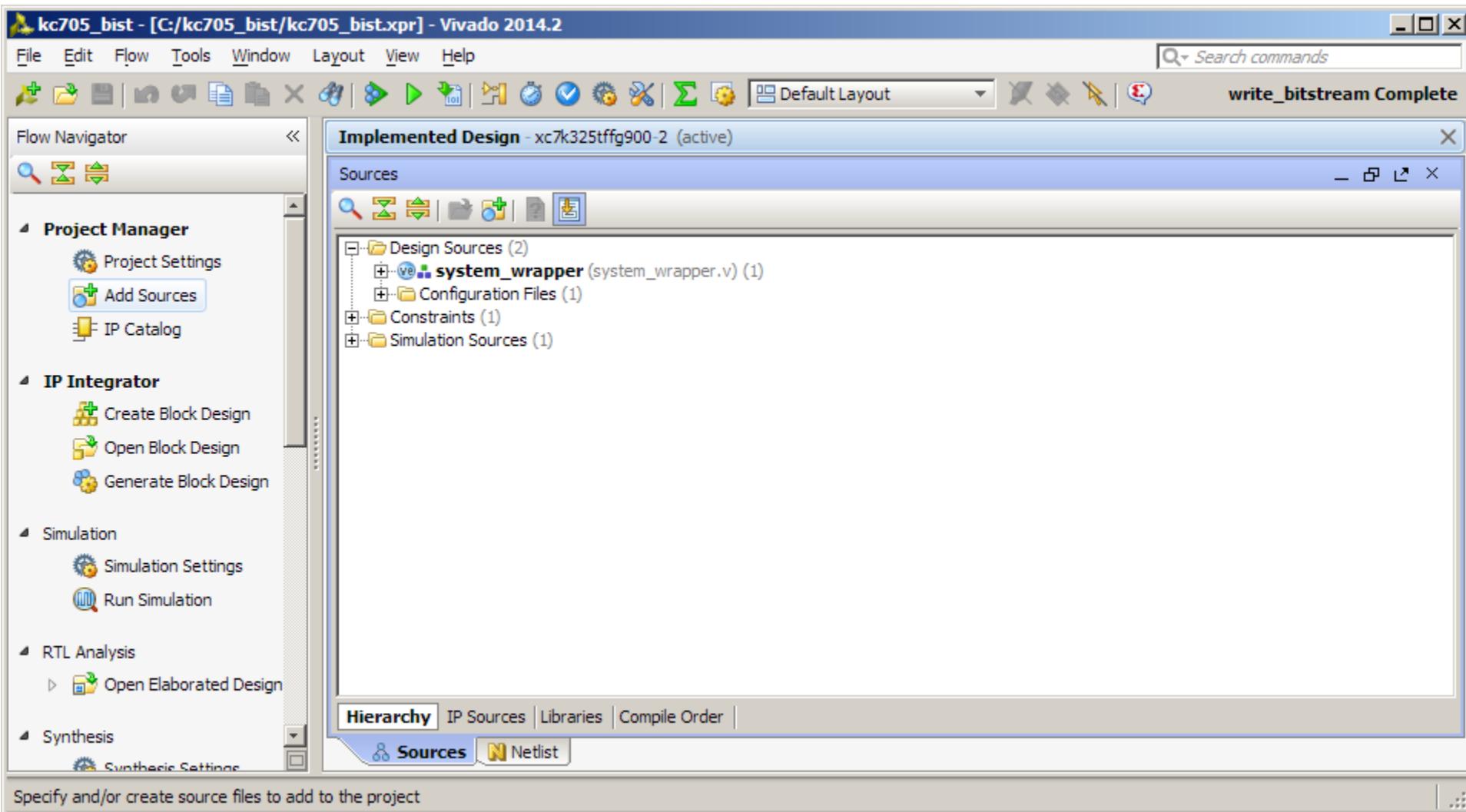
The screenshot shows the Xilinx SDK C/C++ interface. The title bar reads "SDK C/C++ - Xilinx SDK". The menu bar includes File, Edit, Source, Refactor, Navigate, Search, Run, Project, Xilinx Tools, Window, and Help. The toolbar has various icons for file operations like Open, Save, and Build. The "Project Explorer" view on the left lists several projects: "bist_app" (selected), "lwip_echo_server", "lwip_echo_server_bsp", "standalone_bsp_0", and "system_wrapper_hw_platform_0". The main workspace contains a "CDT Build Console [bist_app]" tab showing the build log:

```
./src/hello_uart.o ./src/lcd_complete.o ./src/lcd_simple.o ./src/menu.o ./src/push_button_test.o  
./src/rotary_simple.o ./src/xaxiethernet_example_intr_sgdma.o ./src/xaxiethernet_example_util.o  
./src/xgpio_tapp_example.o ./src/xiic_eeprom_example.o ./src/xilflash_protection_example.o  
./src/xtmrctr_intr_example.o -Wl,--start-group,-lxil,-lgcc,-lc,--end-group -lxilflash  
'Finished building target: bist_app.elf'  
  
'Invoking: MicroBlaze Print Size'  
mb-size bist_app.elf |tee "bist_app.elf.size"  
text data bss dec hex filename  
103216 1656 39872 144744 23568 bist_app.elf  
'Finished building: bist_app.elf.size'  
  
00:08:27 Build Finished (took 6s.489ms)
```

Program KC705 with BIST Design

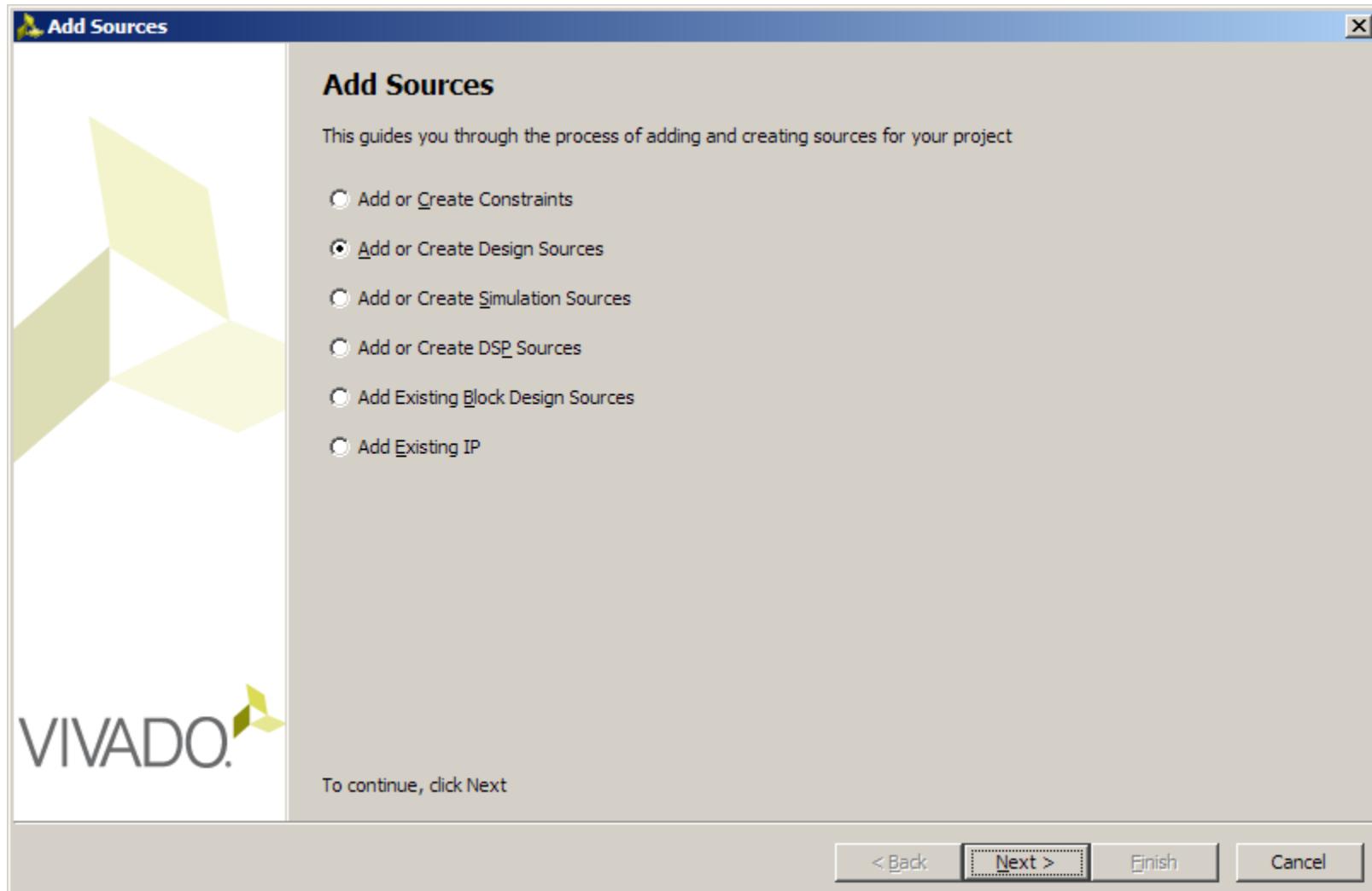
Program KC705 with BIST Design

► Select Add Sources



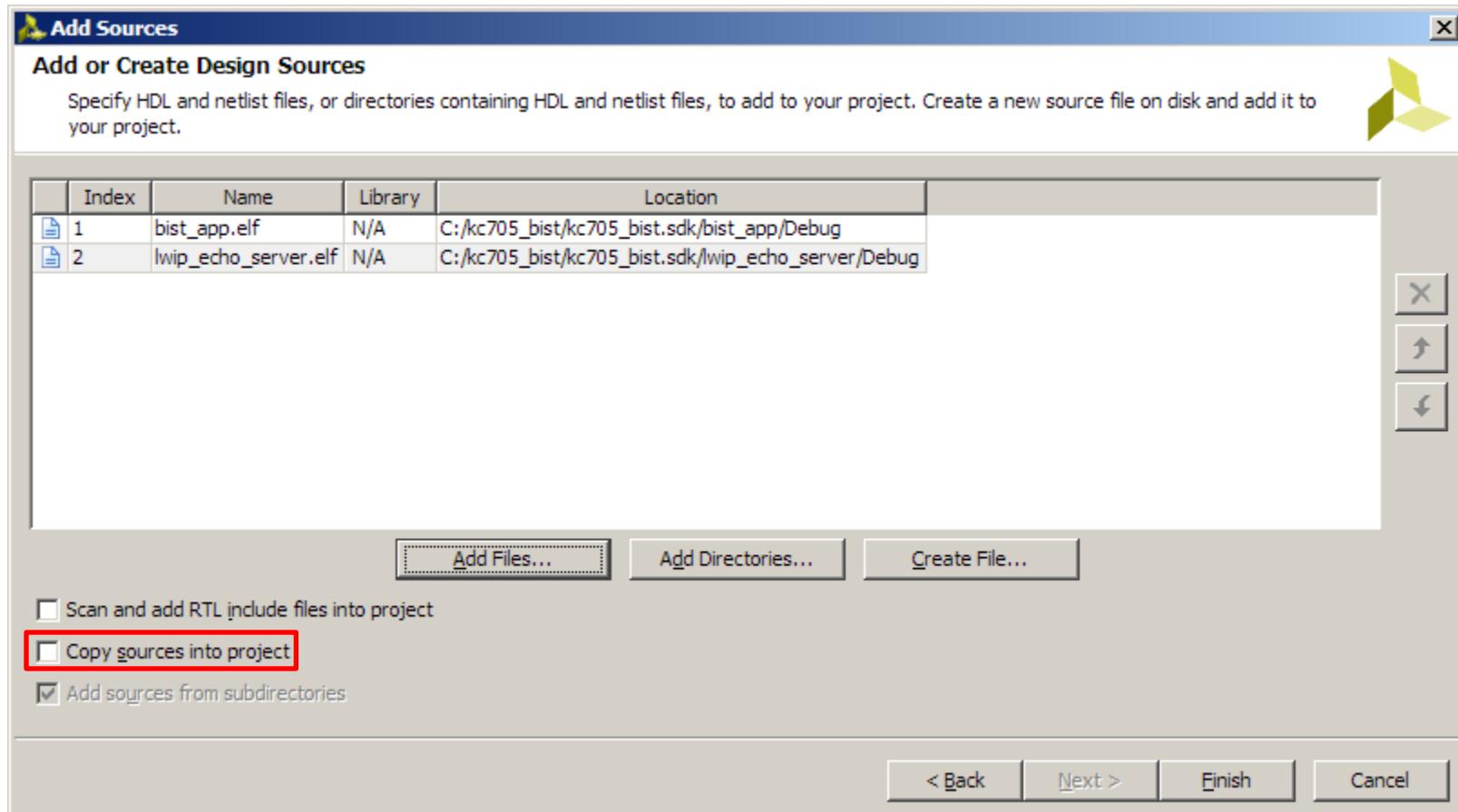
Program KC705 with BIST Design

► Select Add or Create Design Sources



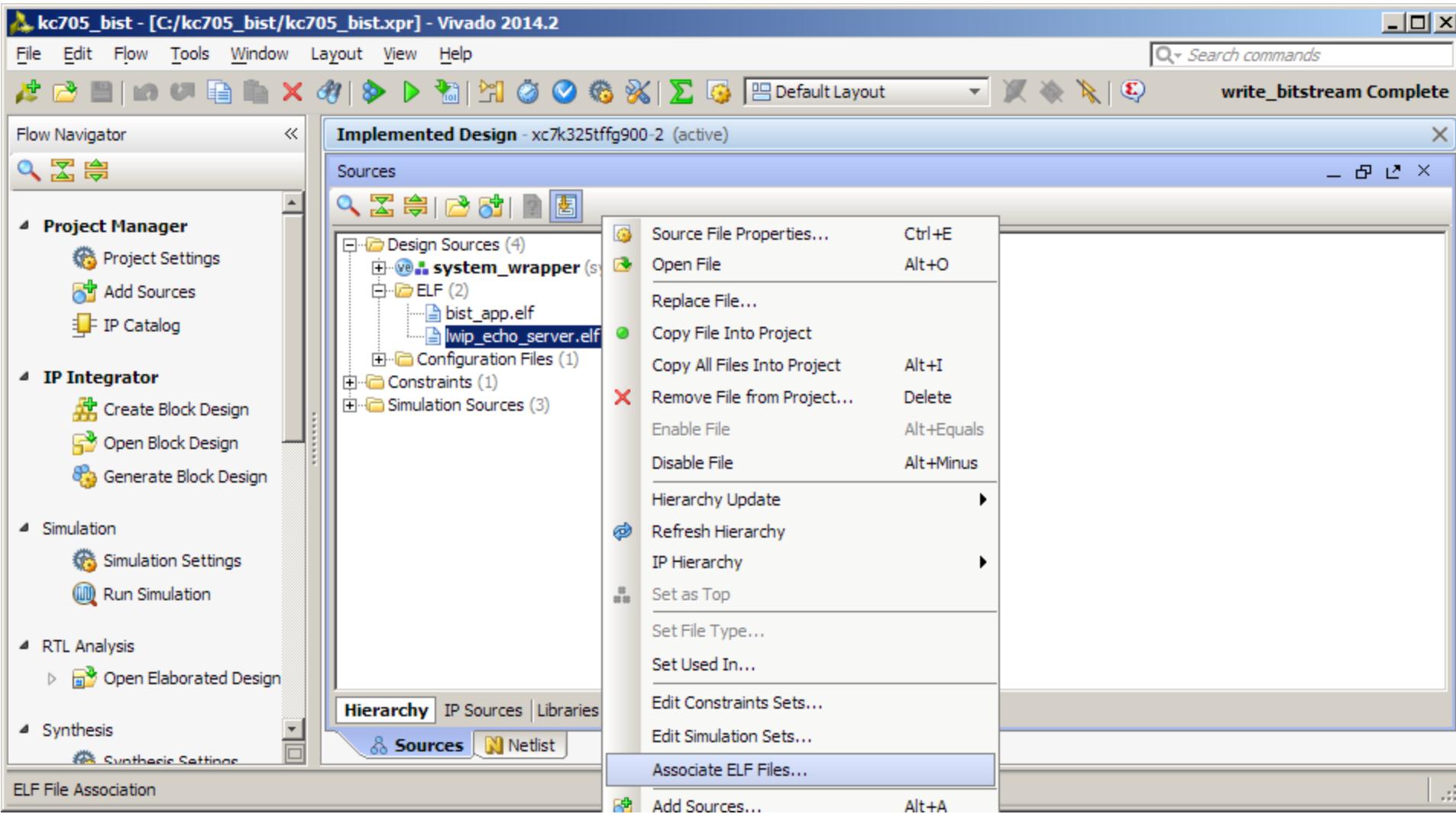
Program KC705 with BIST Design

- Add `bist_app.elf` and `lwip_echo_server.elf` from the SDK tree
- Make sure Copy sources into project is deselected
- Click Finish



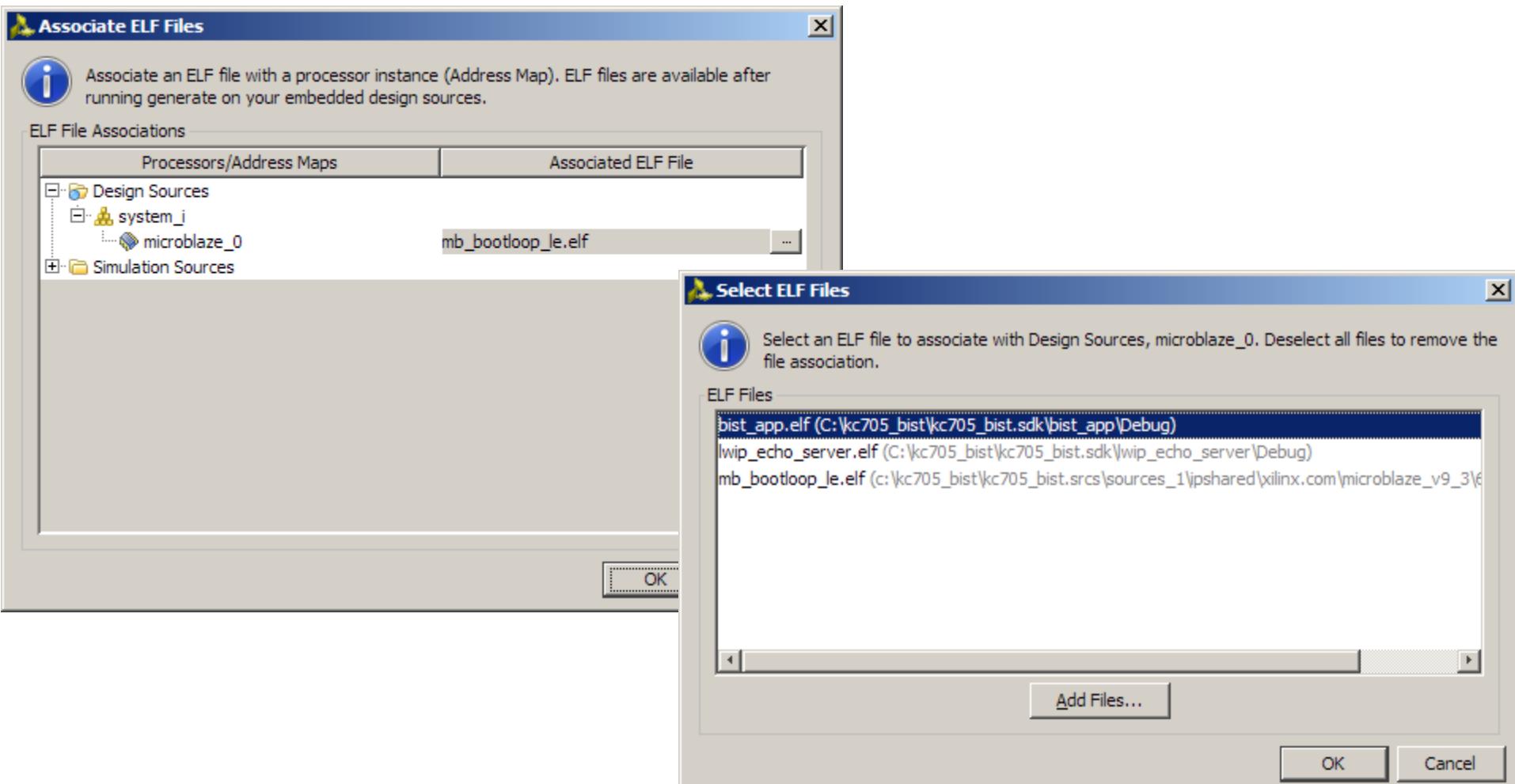
Program KC705 with BIST Design

► Right-click on one of the ELF files and select Associate ELF files



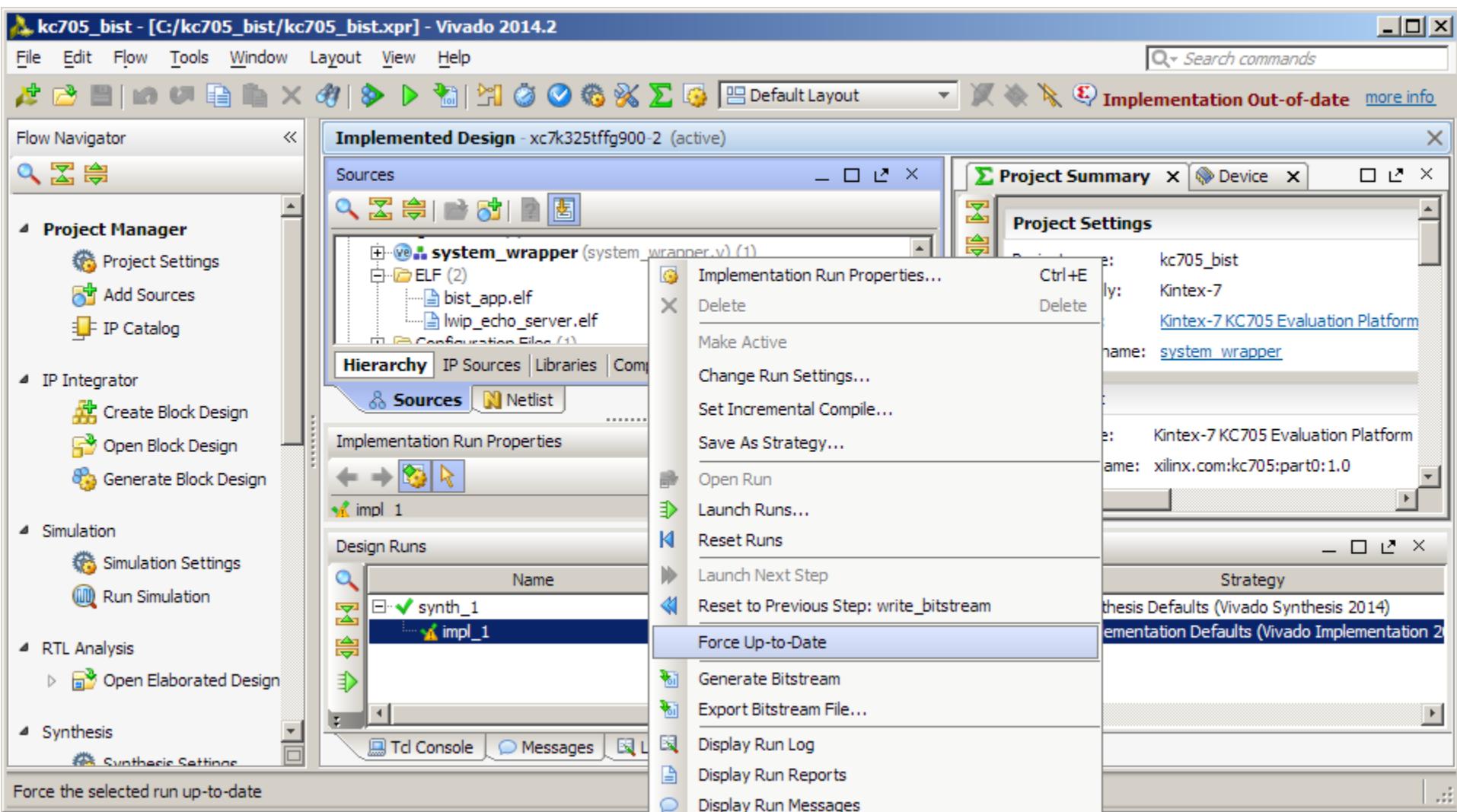
Program KC705 with BIST Design

- Click the button to the right; select the `bist_app.elf` then click OK twice



Program KC705 with BIST Design

- Right-click on `impl_1` and select Force Up-to-Date



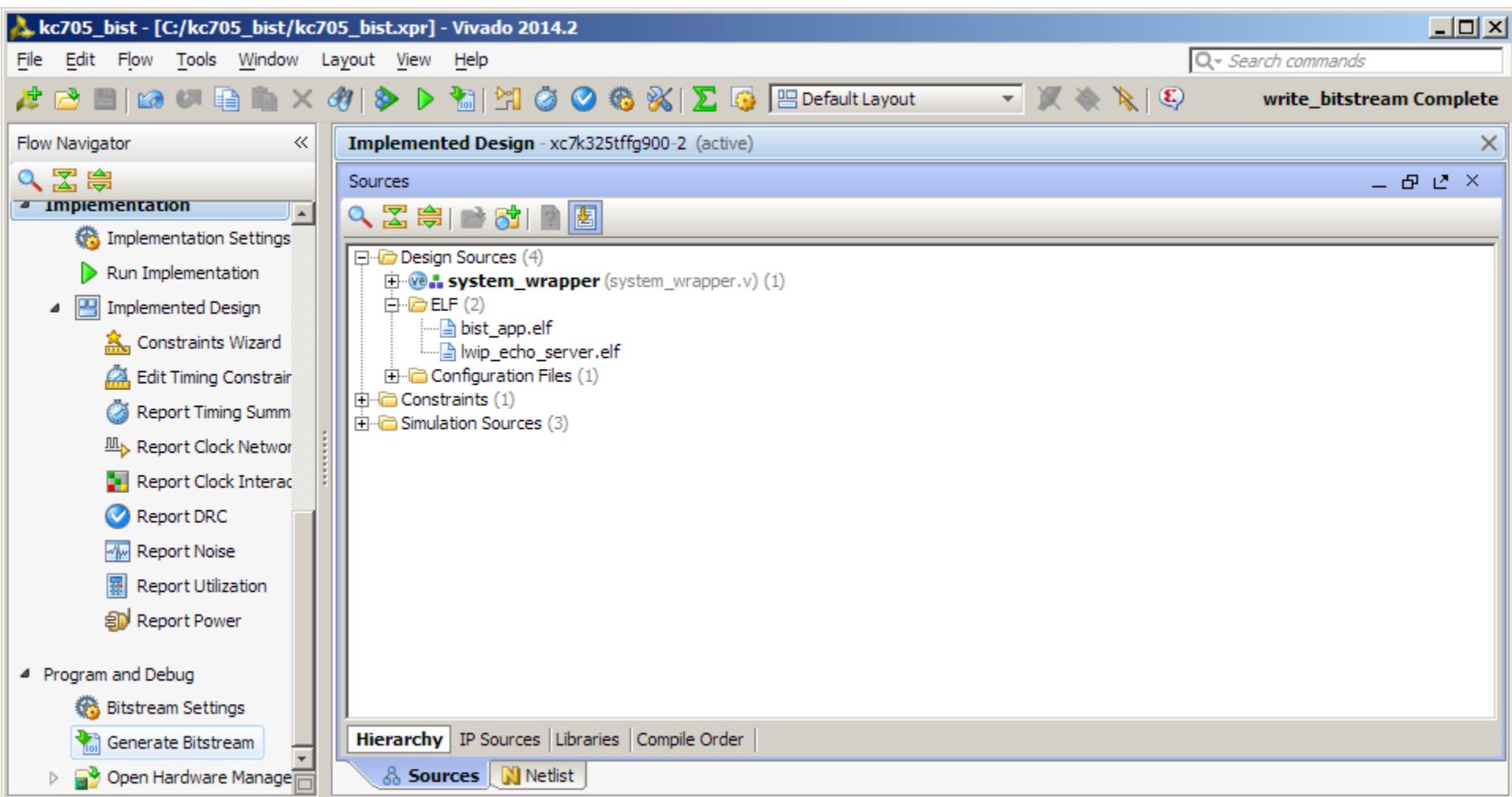
Note: Presentation applies to the KC705

XILINX ➤ ALL PROGRAMMABLE™

Program KC705 with BIST Design

► Select Generate Bitstream

- This creates a bitstream with the BIST ELF file



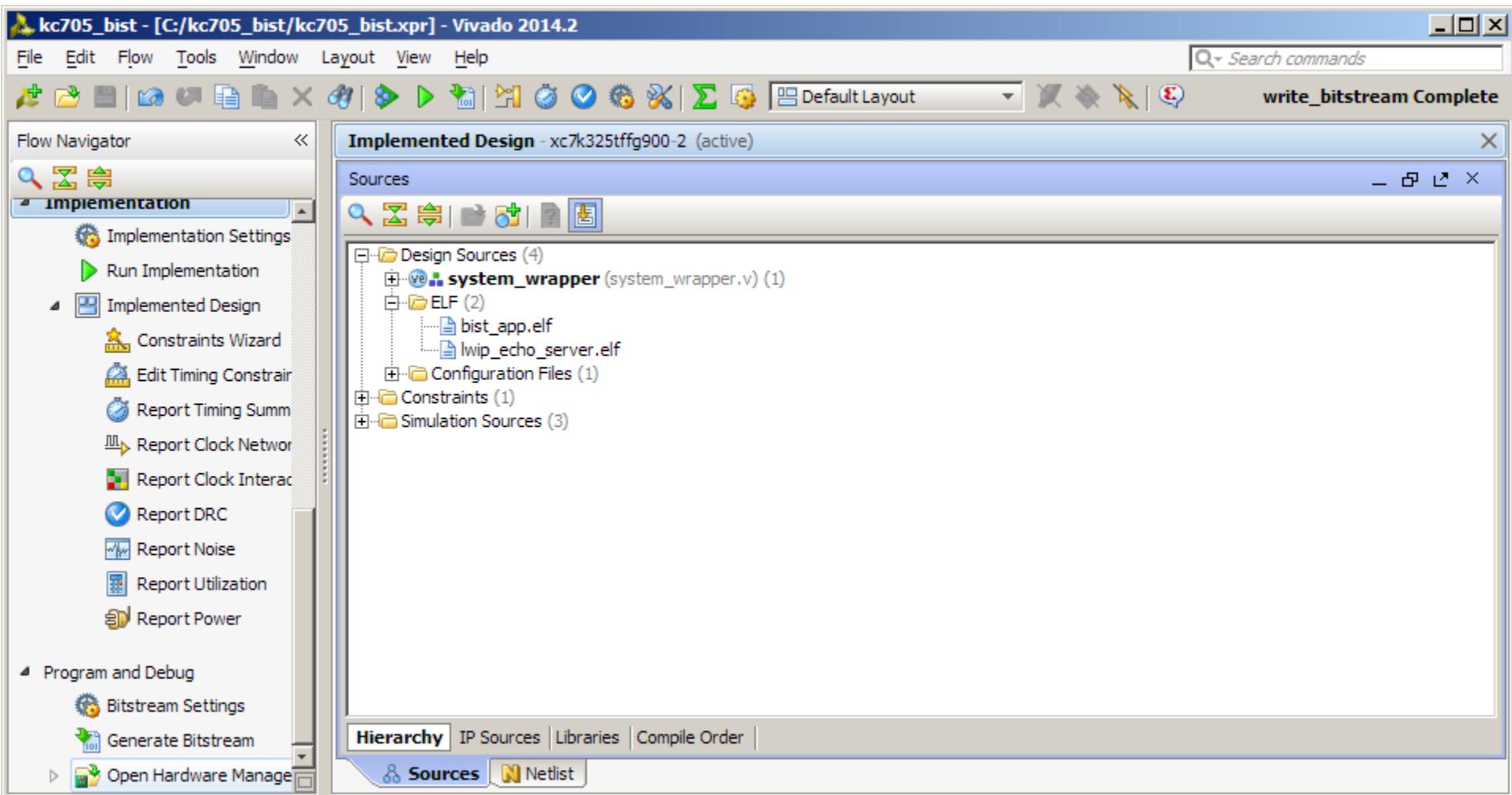
Generate a programming file after implementation

Note: Presentation applies to the KC705

 XILINX  ALL PROGRAMMABLE

Program KC705 with BIST Design

► Click Open Hardware Manager

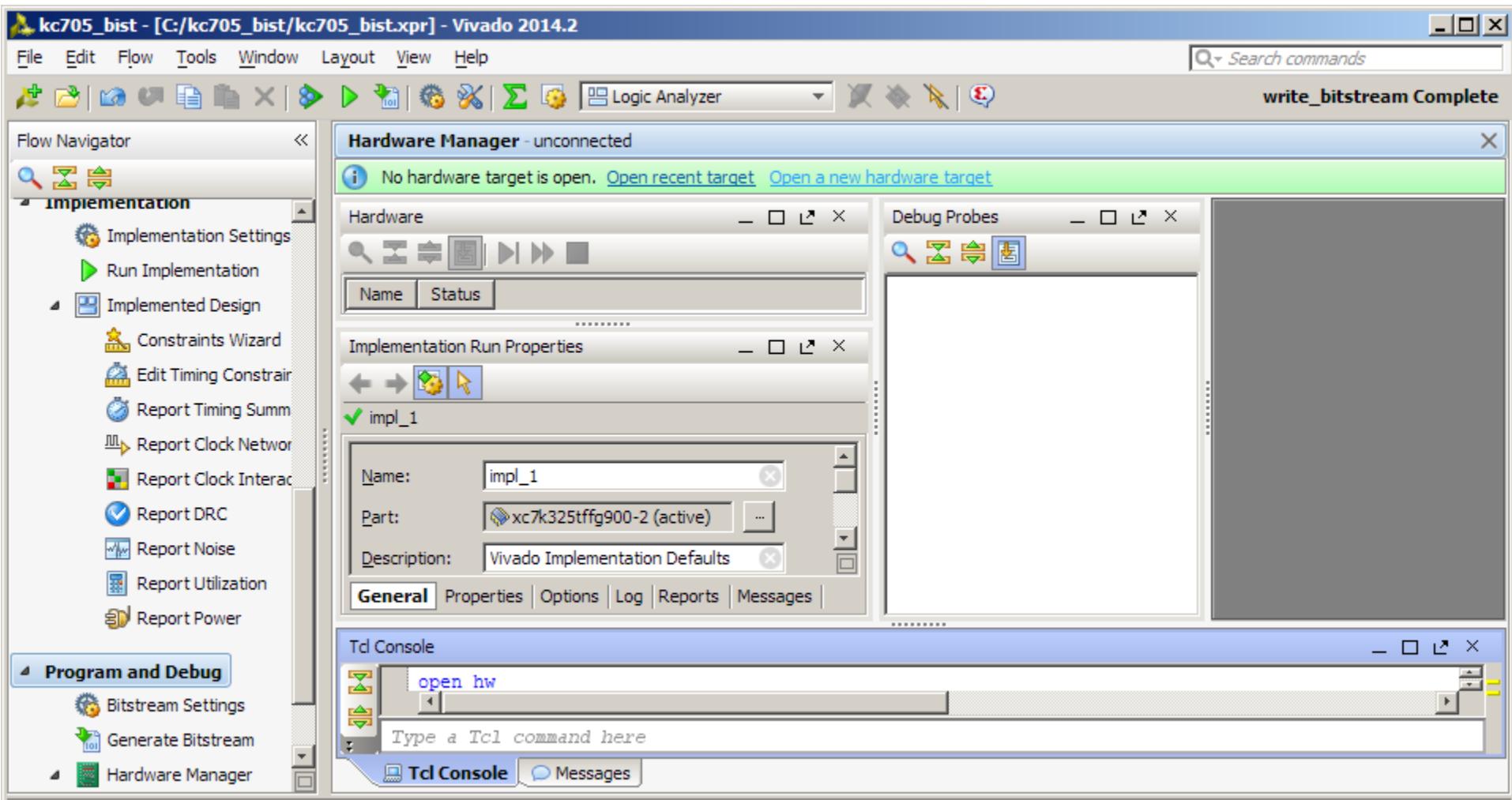


Note: Presentation applies to the KC705

XILINX ➤ ALL PROGRAMMABLE™

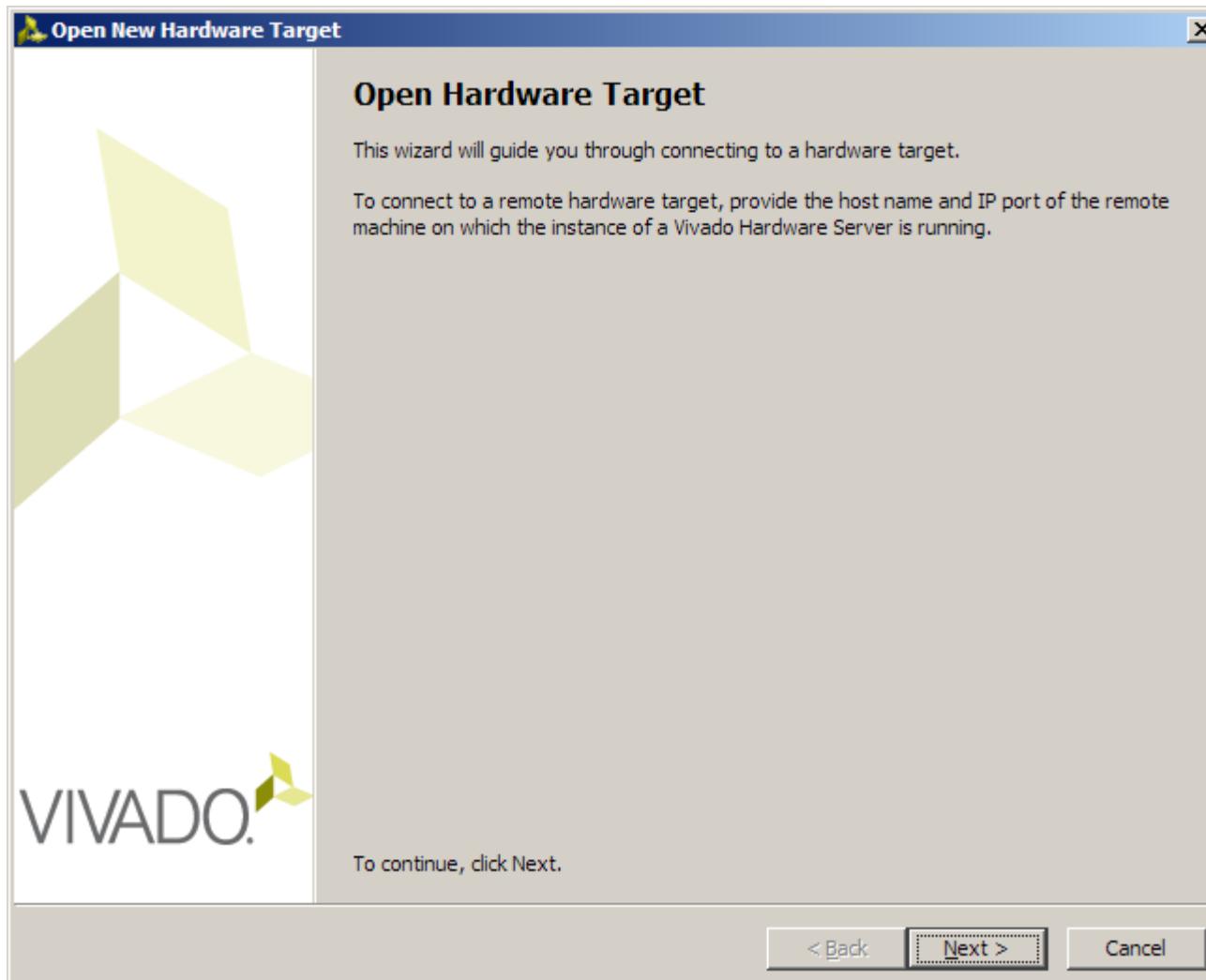
Program KC705 with BIST Design

► Click Open New Hardware Target



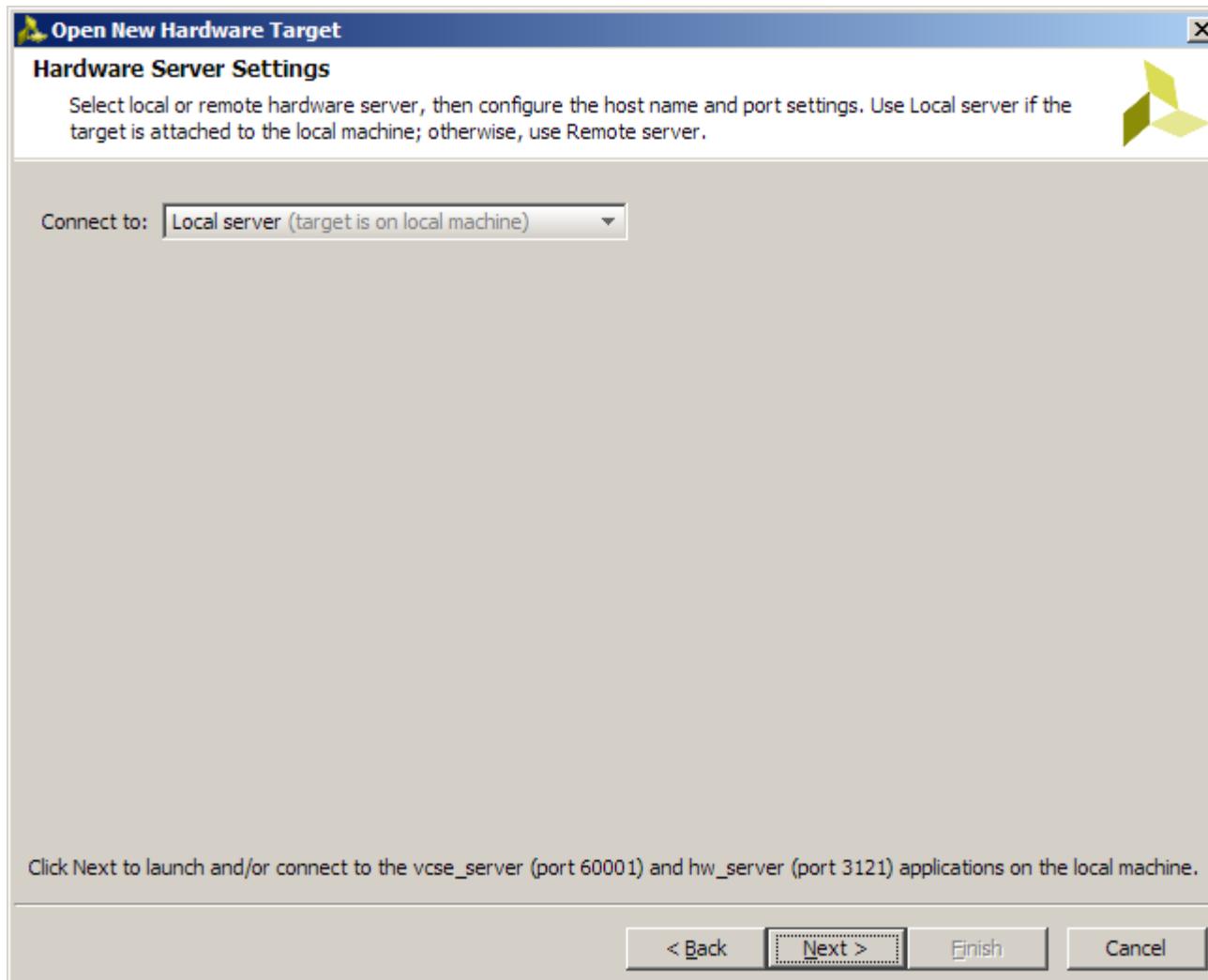
Program KC705 with BIST Design

► Click Next



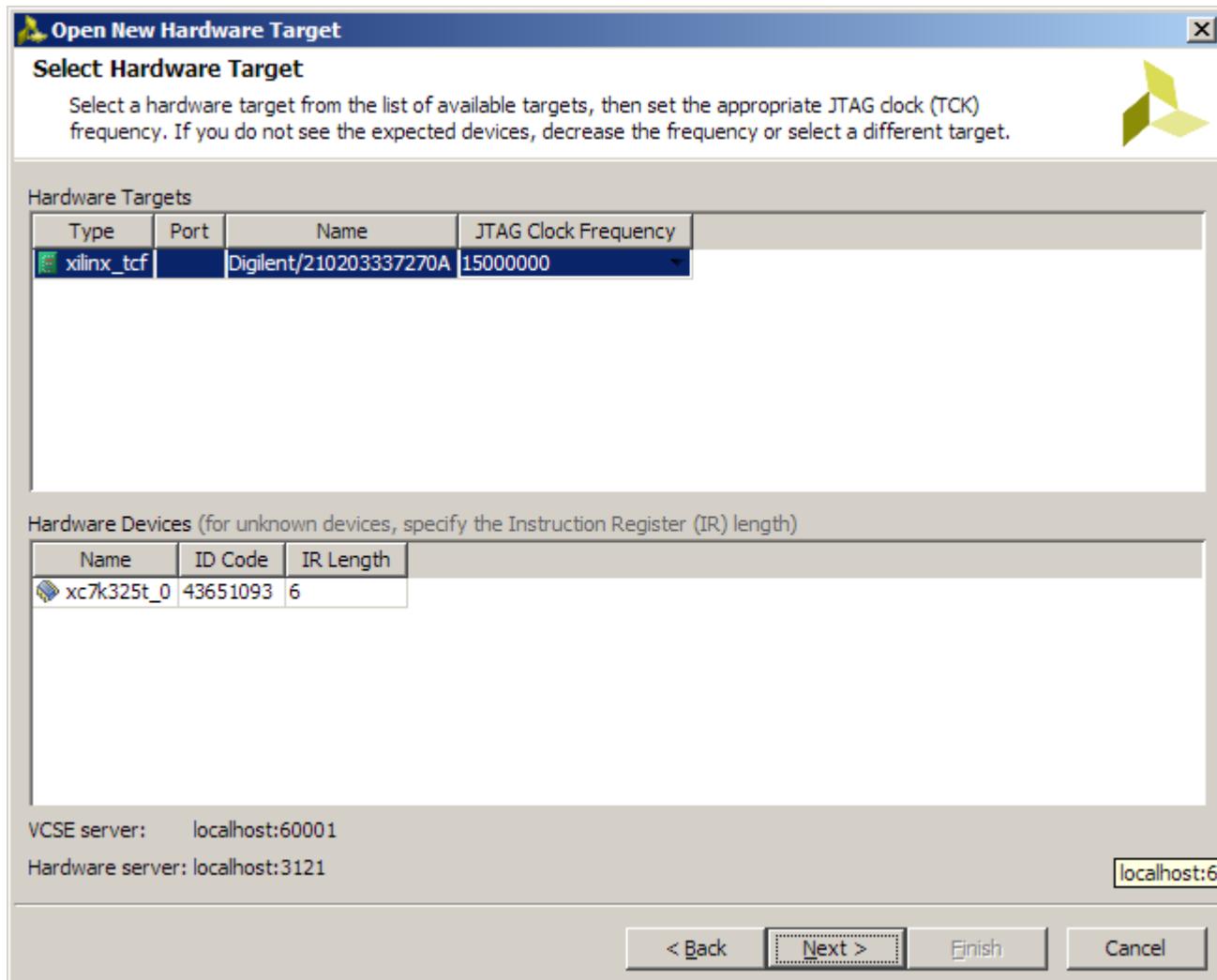
Program KC705 with BIST Design

► Click Next



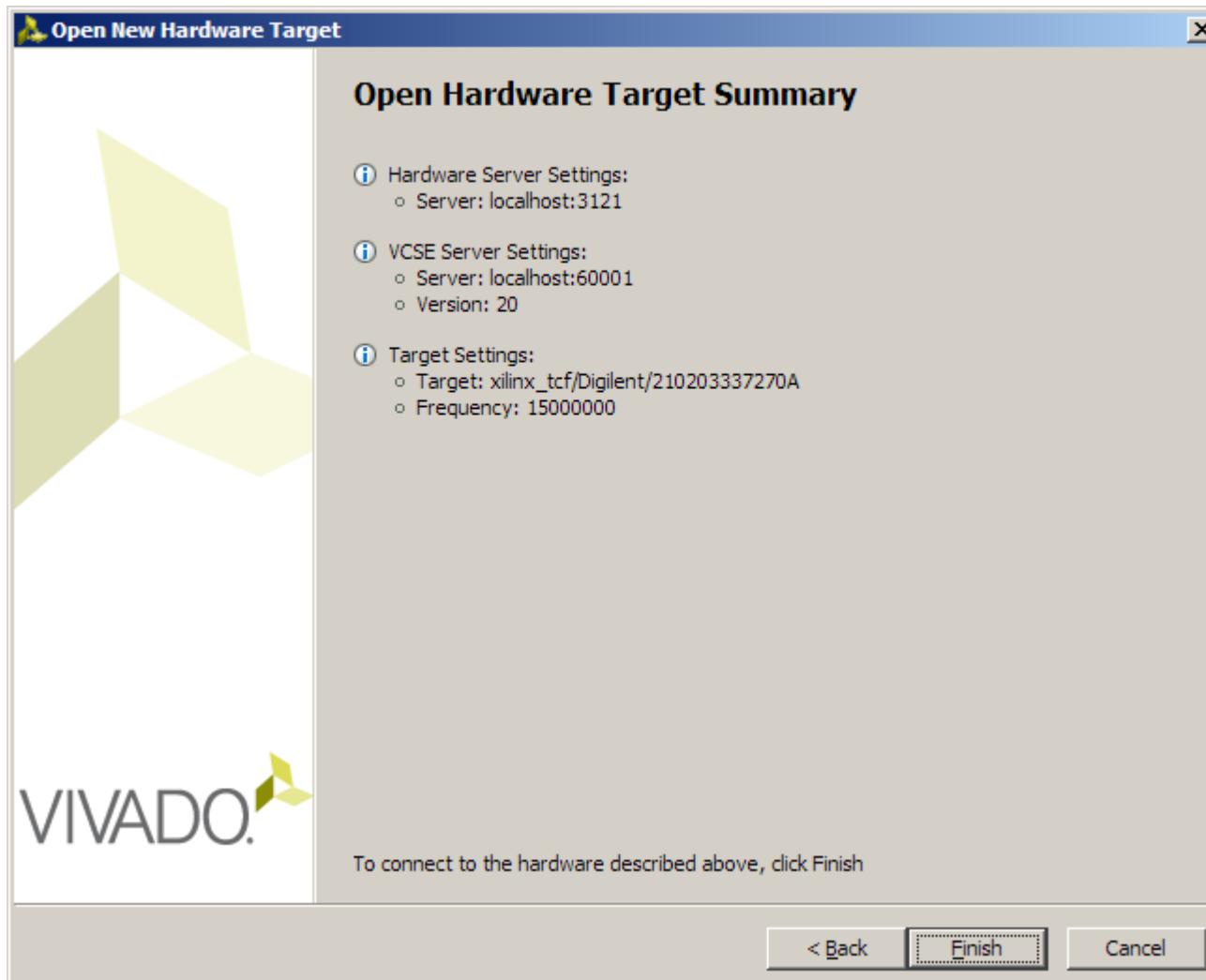
Program KC705 with BIST Design

► Click Next



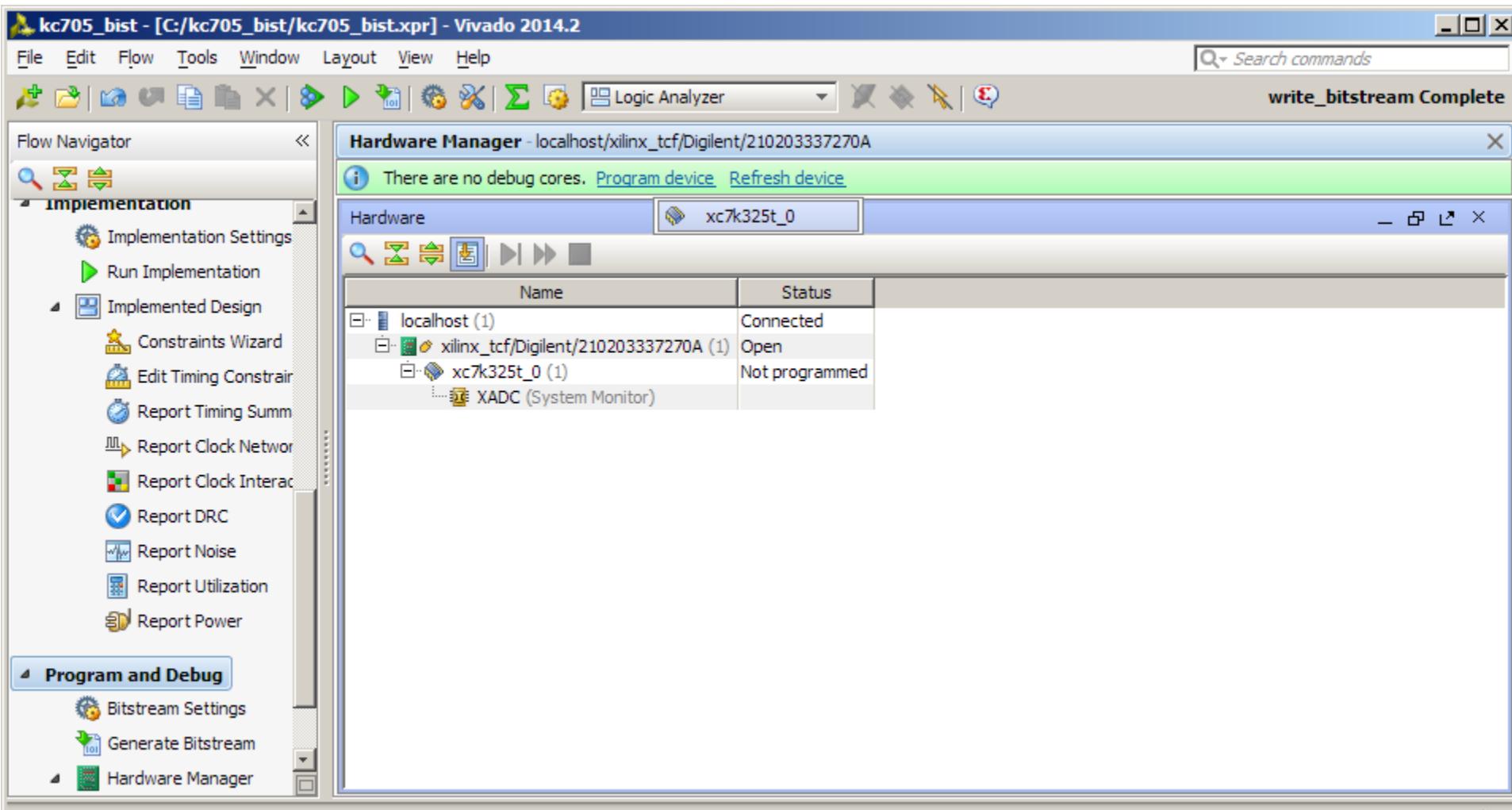
Program KC705 with BIST Design

► Click Finish



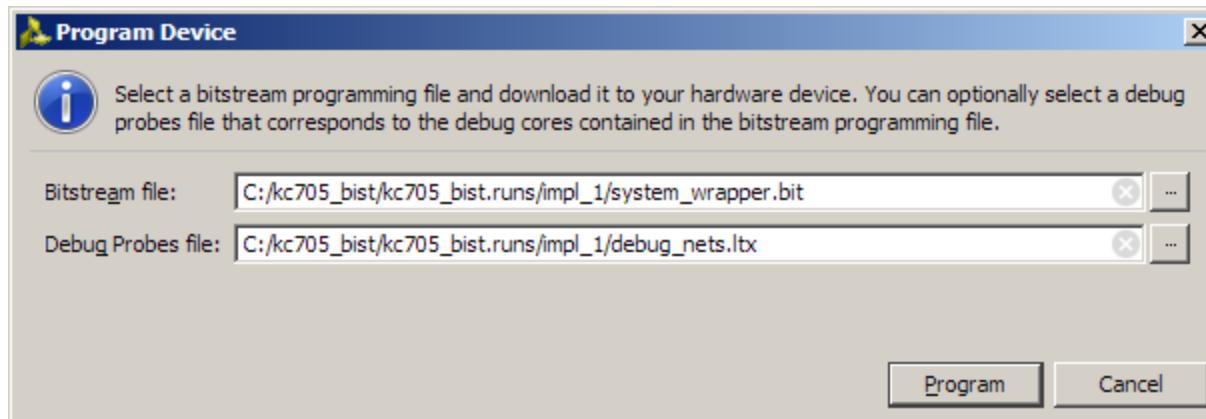
Program KC705 with BIST Design

► Select Program device → xc7k325t_0



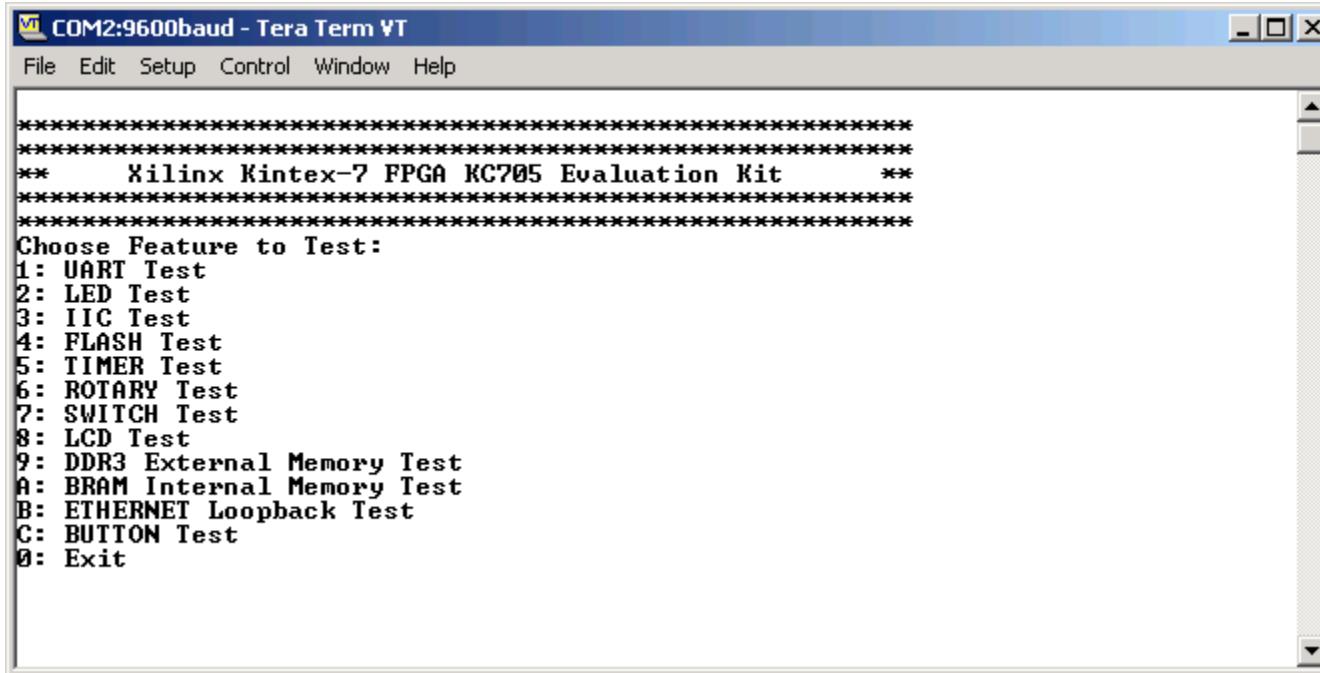
Program KC705 with BIST Design

- Program Device defaults to impl_1 bitstream
- Click Program



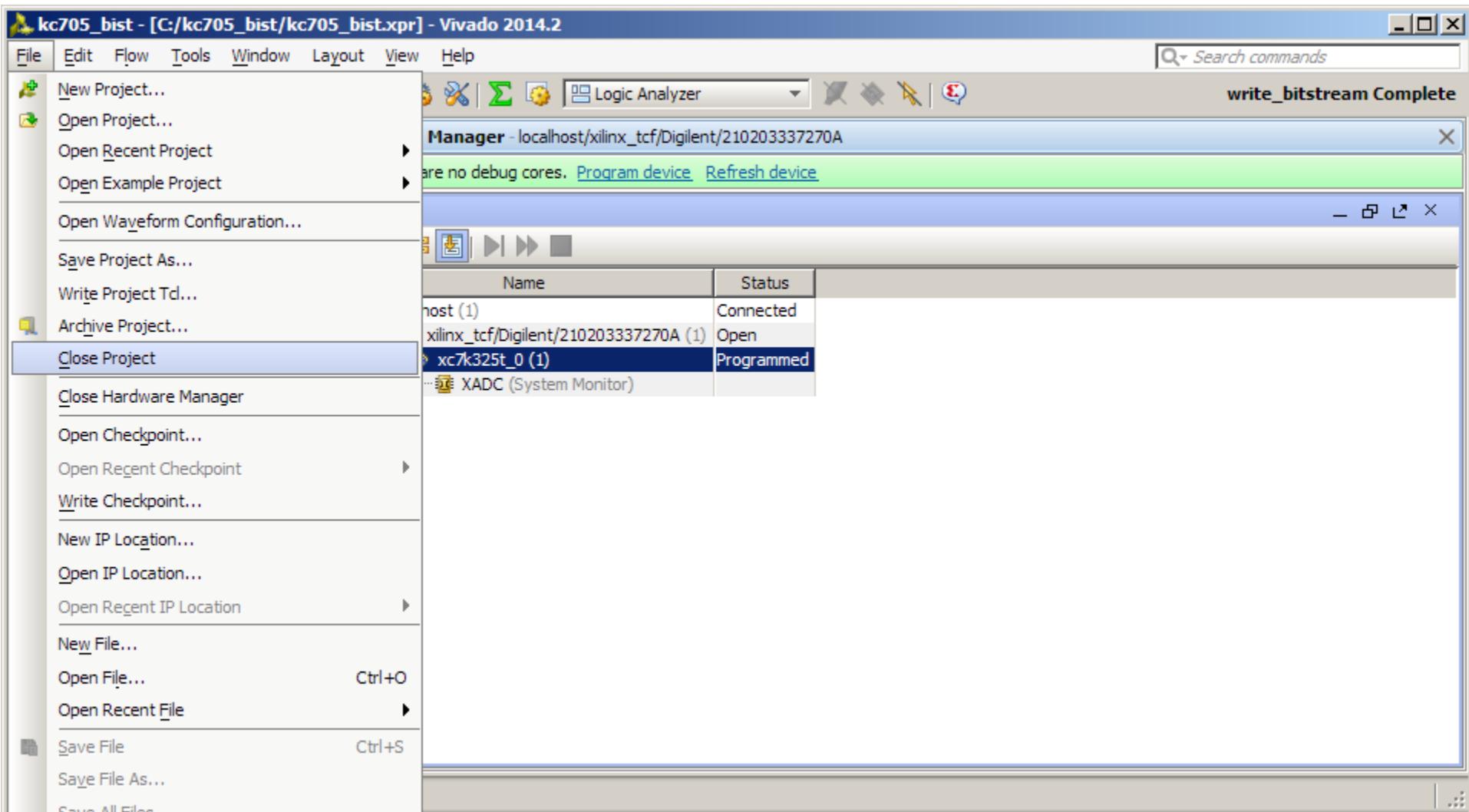
Program KC705 with BIST Design

- BIST Application runs in the terminal window



Program KC705 with BIST Design

► Close the Project



Note: Presentation applies to the KC705

 XILINX  ALL PROGRAMMABLE

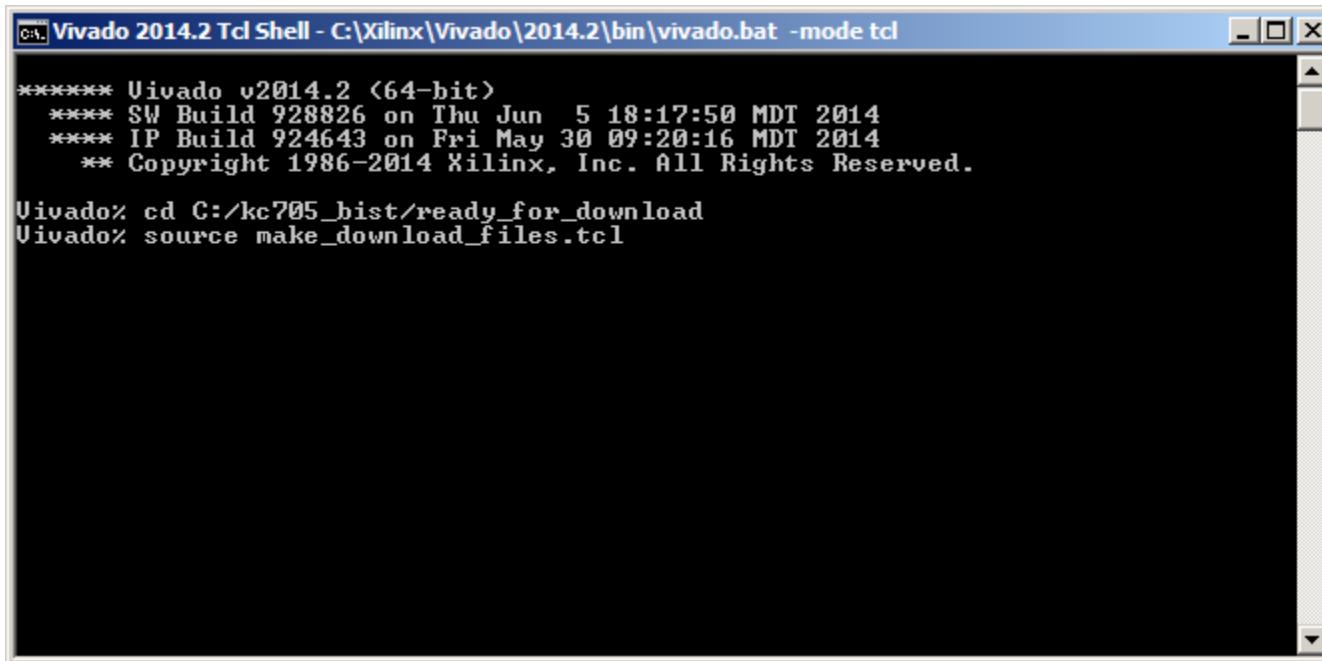
Program KC705 with BIST Design

➤ Repeat this process using Tcl scripts

➤ Open a Vivado Tcl shell and type:

```
cd C:/kc705_bist/ready_for_download  
source make_download_files.tcl
```

➤ This script uses Tcl commands to add the ELF files to the BIST project , then generate both the BIST and LwIP bitstreams



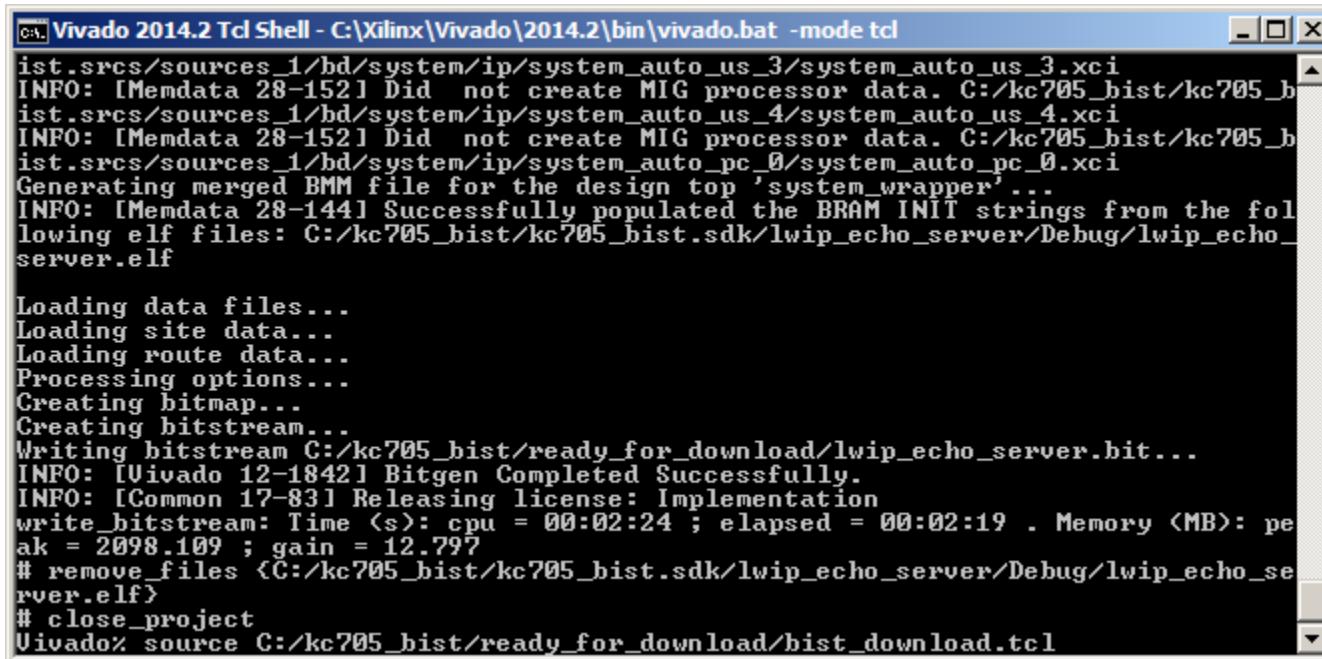
The screenshot shows a Windows command-line interface titled "Vivado 2014.2 Tcl Shell - C:\Xilinx\Vivado\2014.2\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2014.2 (64-bit)  
**** SW Build 928826 on Thu Jun  5 18:17:50 MDT 2014  
**** IP Build 924643 on Fri May 30 09:20:16 MDT 2014  
** Copyright 1986-2014 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/kc705_bist/ready_for_download  
Vivado> source make_download_files.tcl
```

Program KC705 with BIST Design

- Download the BIST bitstream
- In the Vivado Tcl Shell type:

```
source C:/kc705_bist/ready_for_download/bist_download.tcl
```

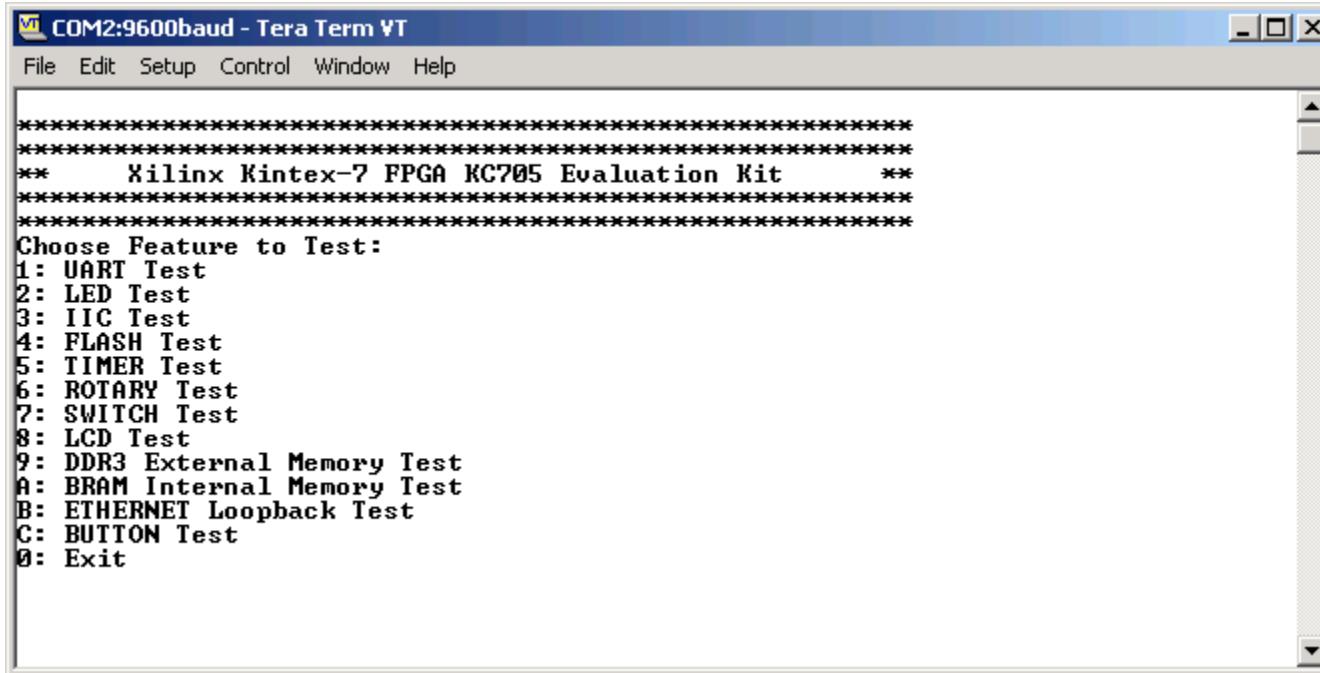


The screenshot shows a command-line interface window titled "Vivado 2014.2 Tcl Shell - C:\Xilinx\Vivado\2014.2\bin\vivado.bat -mode tcl". The window displays the output of a Tcl script named "bist_download.tcl". The script performs several tasks: it sources a configuration file ("C:/kc705_bist/ready_for_download/bist_download.tcl"), loads data files, site data, and route data; processes options, creates a bitmap, and generates a bitstream ("C:/kc705_bist/ready_for_download/lwip_echo_server.bit"). It also releases a license, writes the bitstream, removes temporary files, closes the project, and finally sources the same configuration file again.

```
ist.srcs/sources_1/bd/system/ip/system_auto_us_3/system_auto_us_3.xci  
INFO: [Memdata 28-152] Did not create MIG processor data. C:/kc705_bist/kc705_b  
ist.srcs/sources_1/bd/system/ip/system_auto_us_4/system_auto_us_4.xci  
INFO: [Memdata 28-152] Did not create MIG processor data. C:/kc705_bist/kc705_b  
ist.srcs/sources_1/bd/system/ip/system_auto_pc_0/system_auto_pc_0.xci  
Generating merged BMM file for the design top 'system_wrapper'...  
INFO: [Memdata 28-144] Successfully populated the BRAM INIT strings from the fol  
lowing elf files: C:/kc705_bist/kc705_bist.sdk/lwip_echo_server/Debug/lwip_echo_  
server.elf  
  
Loading data files...  
Loading site data...  
Loading route data...  
Processing options...  
Creating bitmap...  
Creating bitstream...  
Writing bitstream C:/kc705_bist/ready_for_download/lwip_echo_server.bit...  
INFO: [Vivado 12-1842] Bitgen Completed Successfully.  
INFO: [Common 17-83] Releasing license: Implementation  
write_bitstream: Time <s>: cpu = 00:02:24 ; elapsed = 00:02:19 . Memory <MB>: pe  
ak = 2098.109 ; gain = 12.797  
# remove_files {C:/kc705_bist/kc705_bist.sdk/lwip_echo_server/Debug/lwip_echo_se  
rver.elf}  
# close_project  
Vivado% source C:/kc705_bist/ready_for_download/bist_download.tcl
```

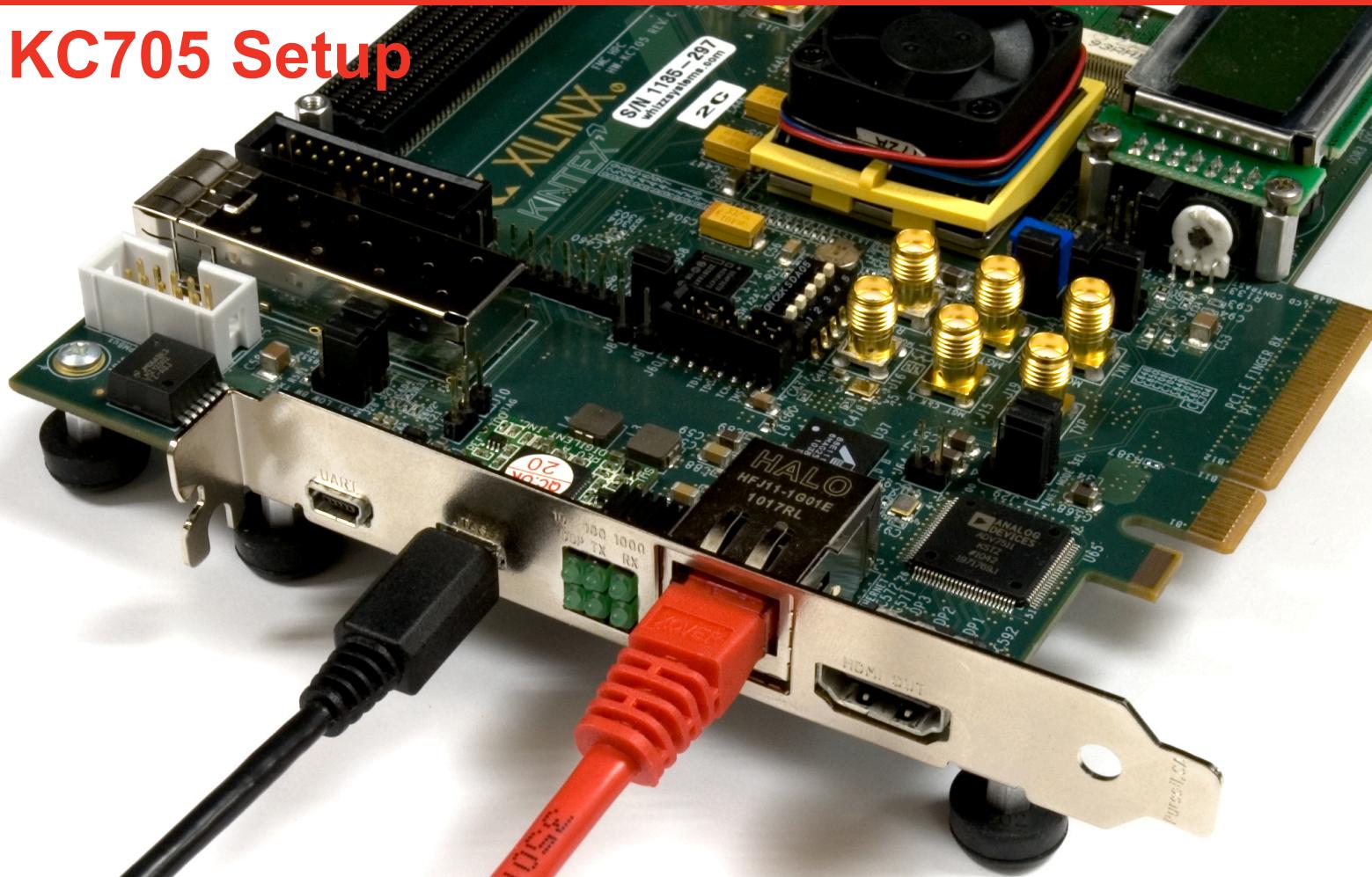
Program KC705 with BIST Design

- BIST Application runs in the terminal window



Run the LwIP Ethernet Design

KC705 Setup

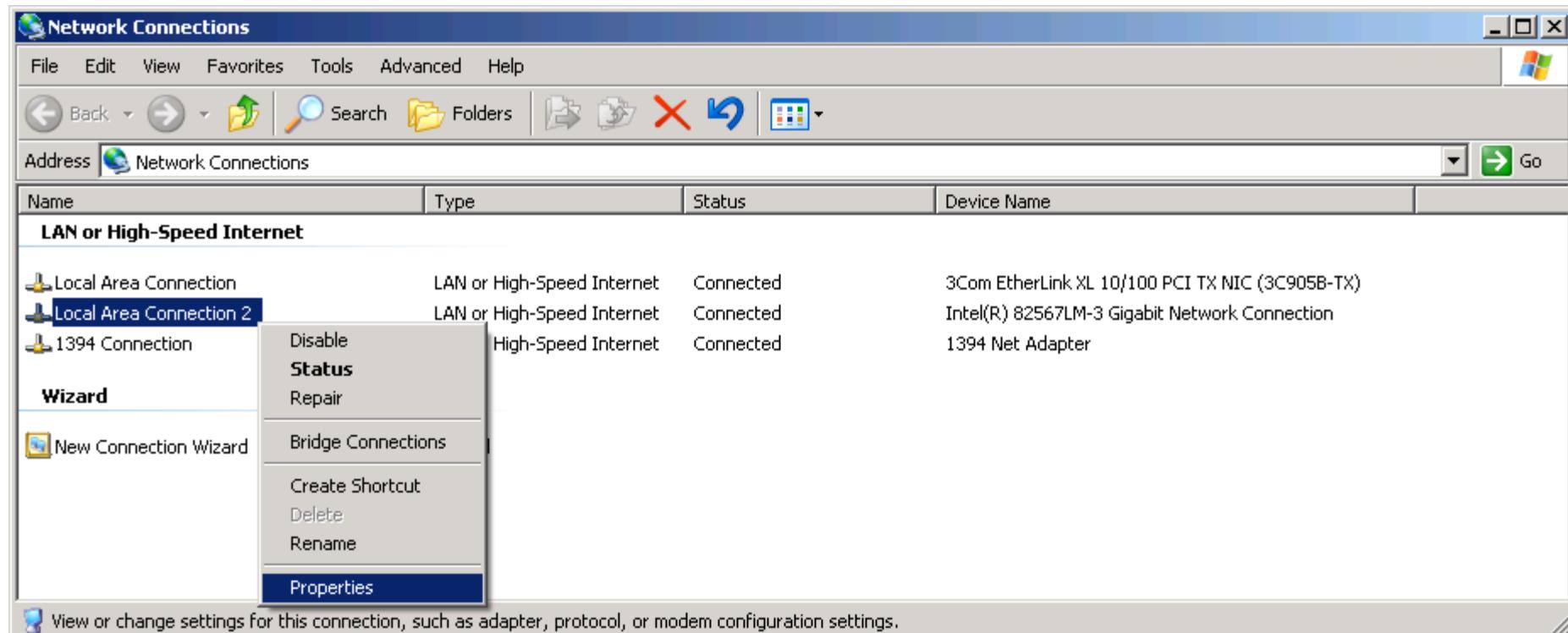


▶ Connect a Ethernet cable to the KC705

- Connect this cable to your PC
- Not shown, the UART should be connected

Run the LwIP Ethernet Design

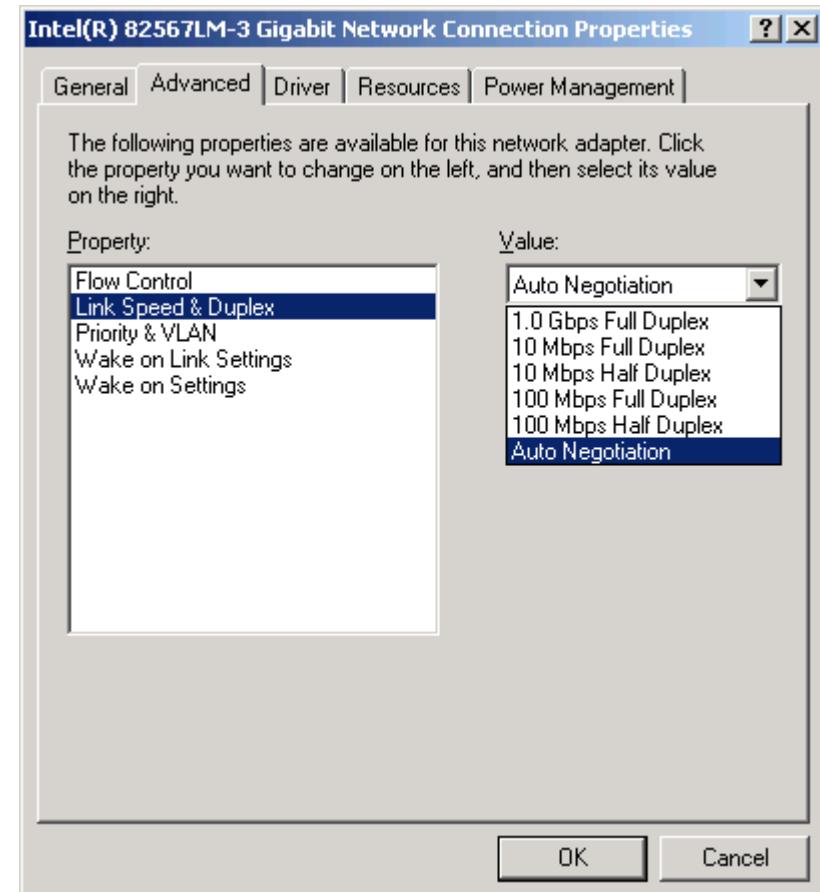
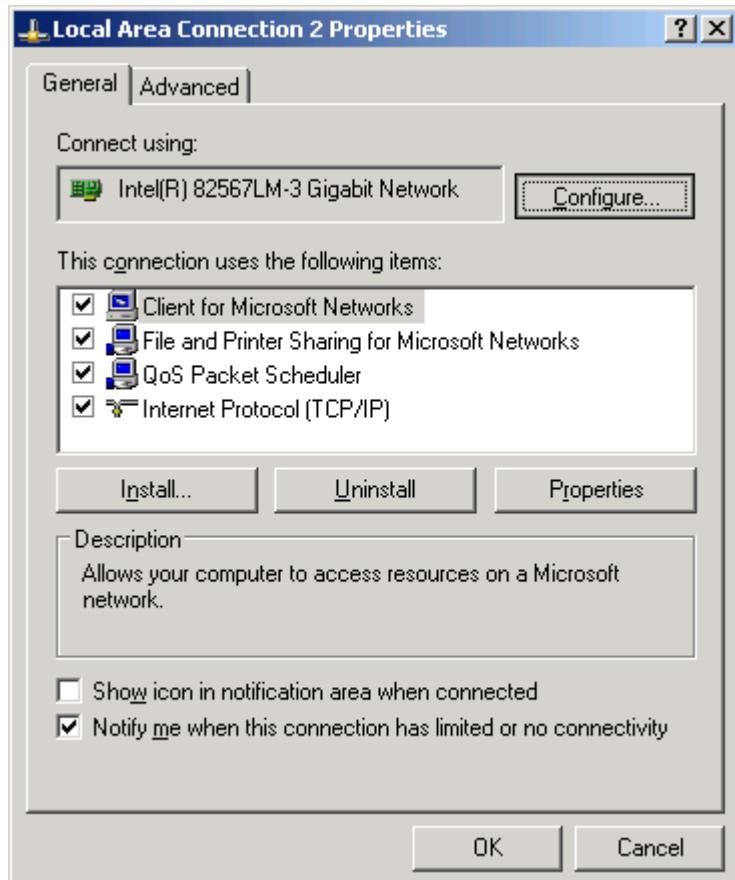
- From the Windows Control Panel, open Network Connections
- Right-click on the Gigabit Ethernet Adapter and select Properties



Run the LwIP Ethernet Design

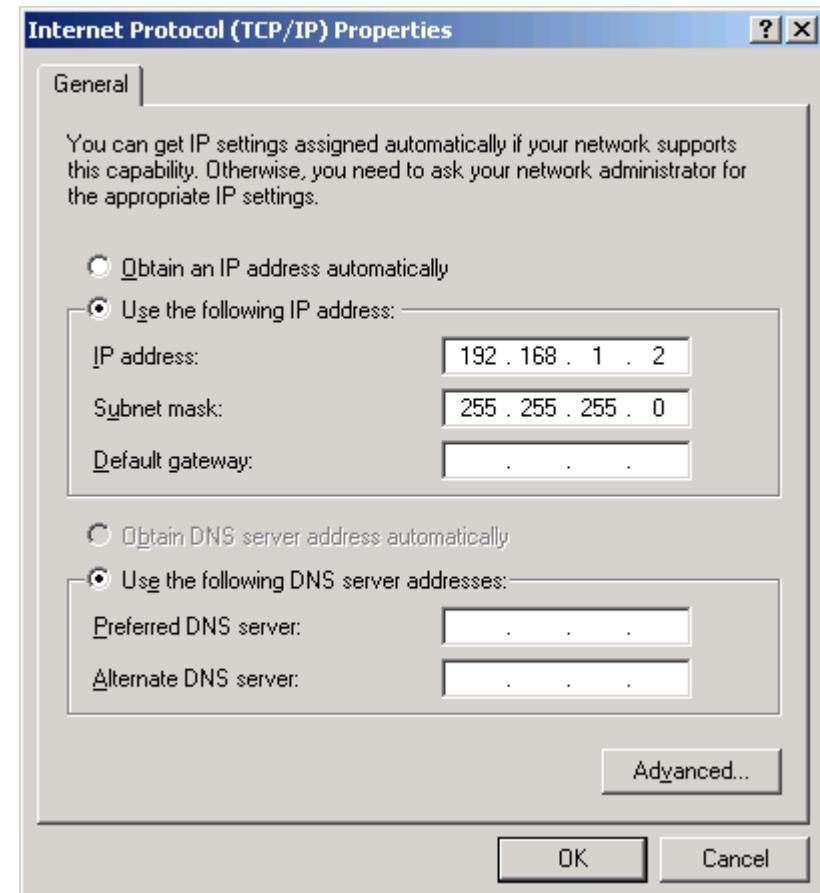
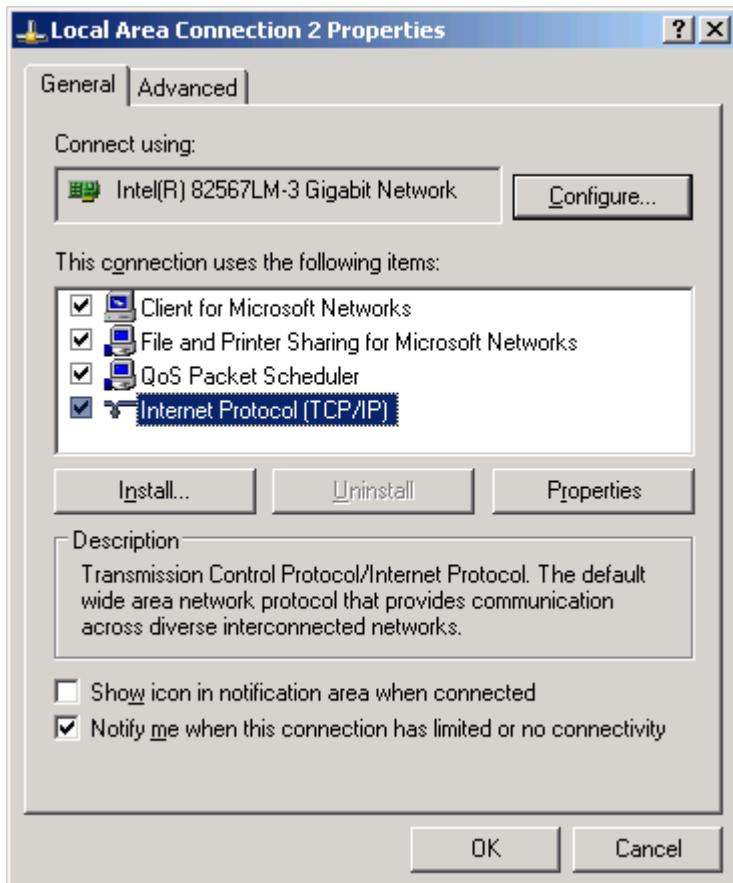
► Click Configure

- Set the Media Type to Auto for 1 Gbps then click OK



Run the LwIP Ethernet Design

- Reopen the properties after the last step
- Set your host (PC) to this IP Address:

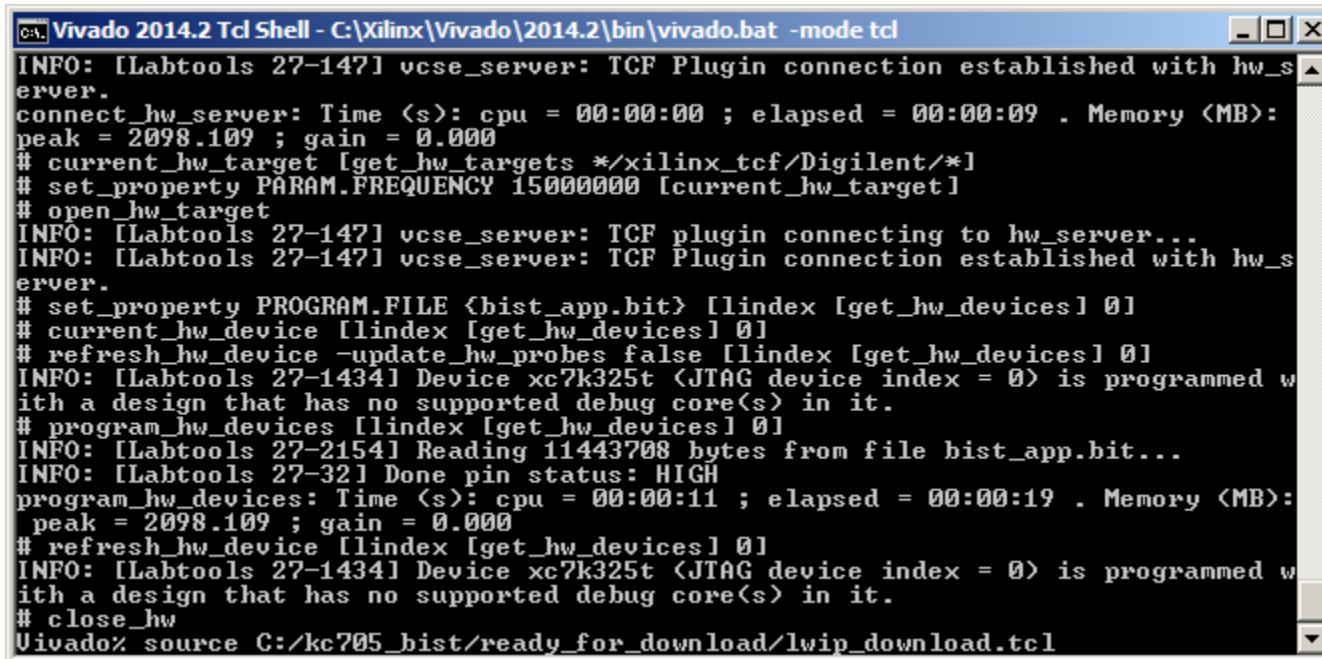


Run the LwIP Ethernet Design

► Download the LwIP bitstream

► In the Vivado Tcl Shell type:

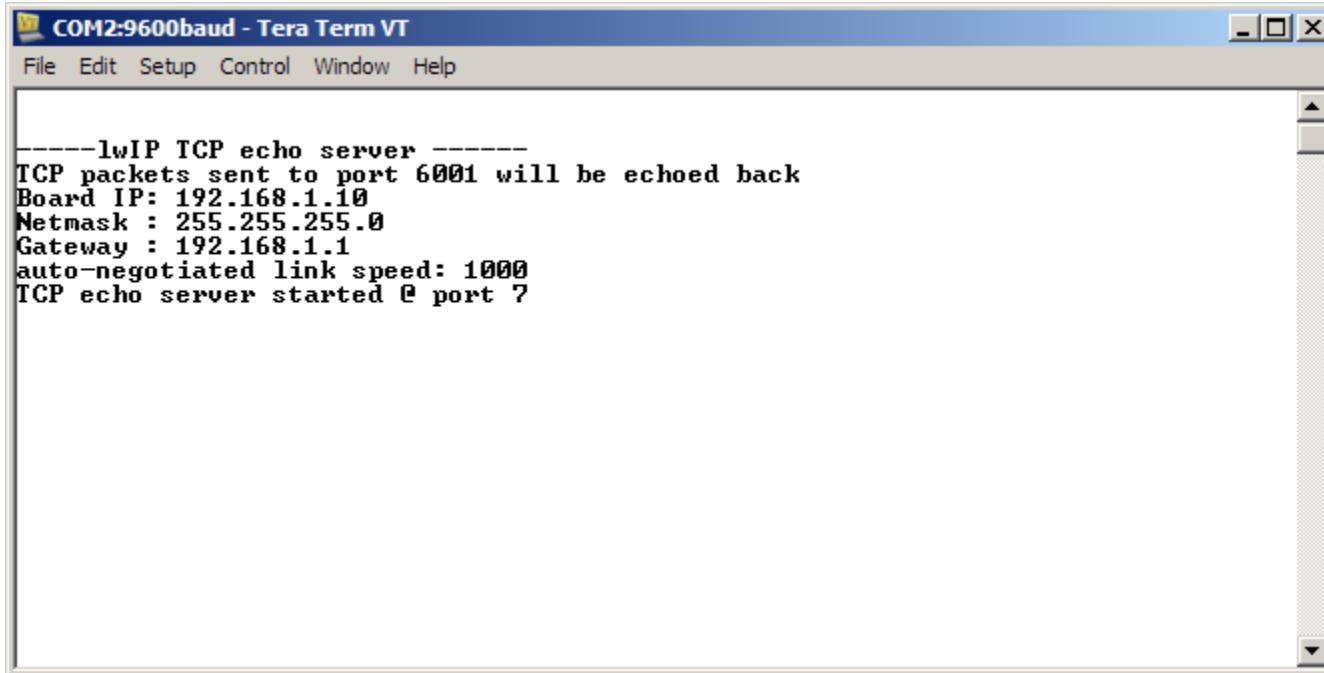
```
source C:/kc705_bist/ready_for_download/lwip_download.tcl
```



```
INFO: [Labtools 27-147] vcse_server: TCF Plugin connection established with hw_server.
connect_hw_server: Time <s>: cpu = 00:00:00 ; elapsed = 00:00:09 . Memory <MB>:
peak = 2098.109 ; gain = 0.000
# current_hw_target [get_hw_targets */xilinx_tcf/Digilent/*]
# set_property PARAM.FREQUENCY 15000000 [current_hw_target]
# open_hw_target
INFO: [Labtools 27-147] vcse_server: TCF plugin connecting to hw_server...
INFO: [Labtools 27-147] vcse_server: TCF Plugin connection established with hw_server.
# set_property PROGRAM.FILE {bist_app.bit} [lindex [get_hw_devices] 0]
# current_hw_device [lindex [get_hw_devices] 0]
# refresh_hw_device -update_hw_probes false [lindex [get_hw_devices] 0]
INFO: [Labtools 27-1434] Device xc7k325t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it.
# program_hw_devices [lindex [get_hw_devices] 0]
INFO: [Labtools 27-2154] Reading 11443708 bytes from file bist_app.bit...
INFO: [Labtools 27-32] Done pin status: HIGH
program_hw_devices: Time <s>: cpu = 00:00:11 ; elapsed = 00:00:19 . Memory <MB>:
peak = 2098.109 ; gain = 0.000
# refresh_hw_device [lindex [get_hw_devices] 0]
INFO: [Labtools 27-1434] Device xc7k325t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it.
# close_hw
Vivado% source C:/kc705_bist/ready_for_download/lwip_download.tcl
```

Run the LwIP Ethernet Design

► View LwIP echo server screen



The screenshot shows a terminal window titled "COM2:9600baud - Tera Term VT". The window contains the following text output from a LwIP TCP echo server:

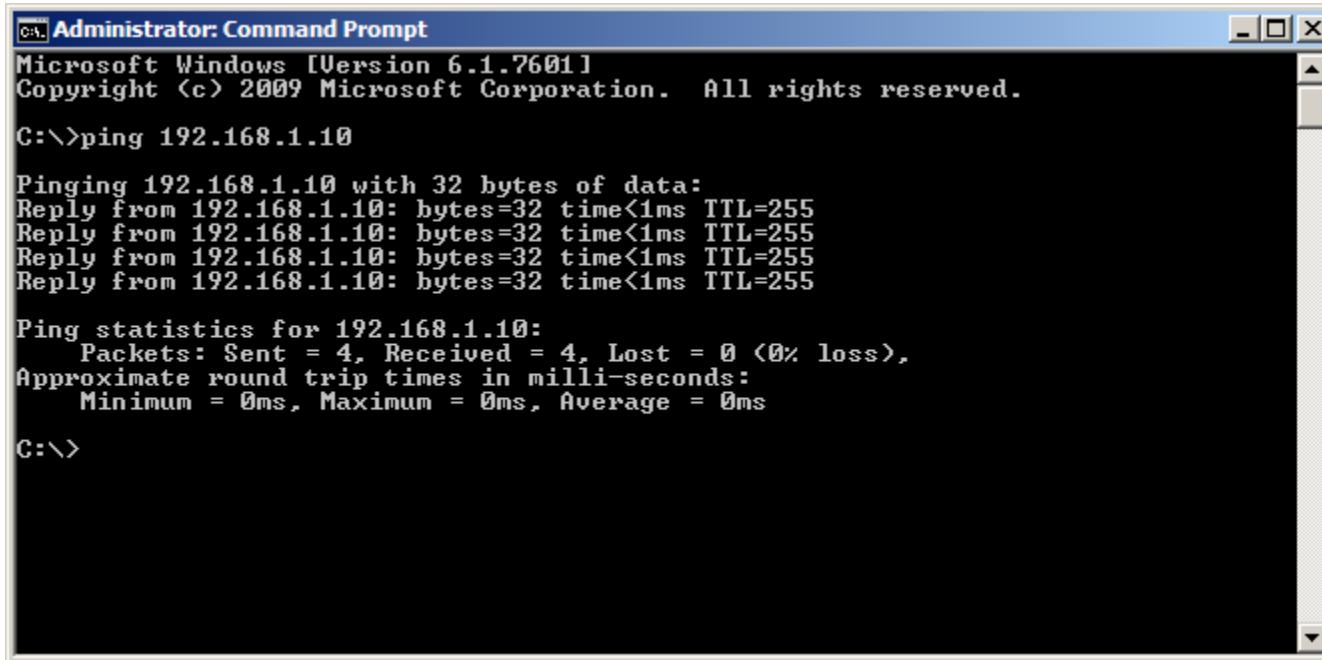
```
----lwIP TCP echo server ----
TCP packets sent to port 6001 will be echoed back
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1
auto-negotiated link speed: 1000
TCP echo server started @ port 7
```

Run the LwIP Ethernet Design

► From a DOS window on the PC Host, enter the command:

ping 192.168.1.10

- Ping from PC host 192.168.1.2 to KC705 target 192.168.1.10



```
Administrator: Command Prompt
Microsoft Windows [Version 6.1.7601]
Copyright <c> 2009 Microsoft Corporation. All rights reserved.

C:\>ping 192.168.1.10

Pinging 192.168.1.10 with 32 bytes of data:
Reply from 192.168.1.10: bytes=32 time<1ms TTL=255

Ping statistics for 192.168.1.10:
    Packets: Sent = 4, Received = 4, Lost = 0 (0% loss),
    Approximate round trip times in milli-seconds:
        Minimum = 0ms, Maximum = 0ms, Average = 0ms

C:\>
```

References

References

► IP Integrator Documentation

- Vivado Design Suite Tcl Command Reference Guide
 - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_2/ug835-vivado-tcl-commands.pdf
- Designing IP Subsystems Using IP Integrator
 - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_2/ug994-vivado-ip-subsystems.pdf

► 7 Series Configuration

- 7 Series FPGAs Configuration User Guide
 - http://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf

Documentation

Documentation

► Kintex-7

- Kintex-7 FPGA Family
 - <http://www.xilinx.com/products/silicon-devices/fpga/kintex-7/index.htm>
- Design Advisory Master Answer Record for Kintex-7 FPGAs
 - <http://www.xilinx.com/support/answers/42946.htm>

► KC705 Documentation

- Kintex-7 FPGA KC705 Evaluation Kit
 - <http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm>
- KC705 Getting Started Guide
 - http://www.xilinx.com/support/documentation/boards_and_kits/kc705/2013_2/ug883_K7_KC705_Eval_Kit.pdf
- KC705 User Guide
 - http://www.xilinx.com/support/documentation/boards_and_kits/kc705/ug810_KC705_Eval_Bd.pdf