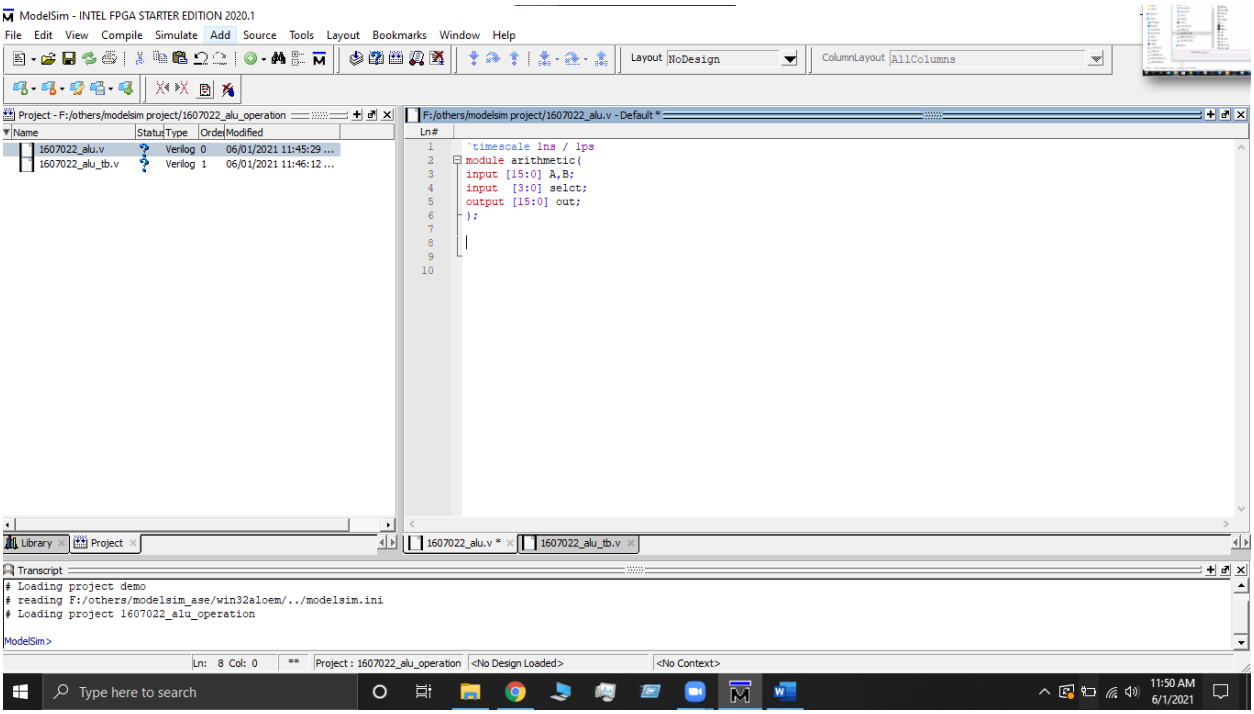
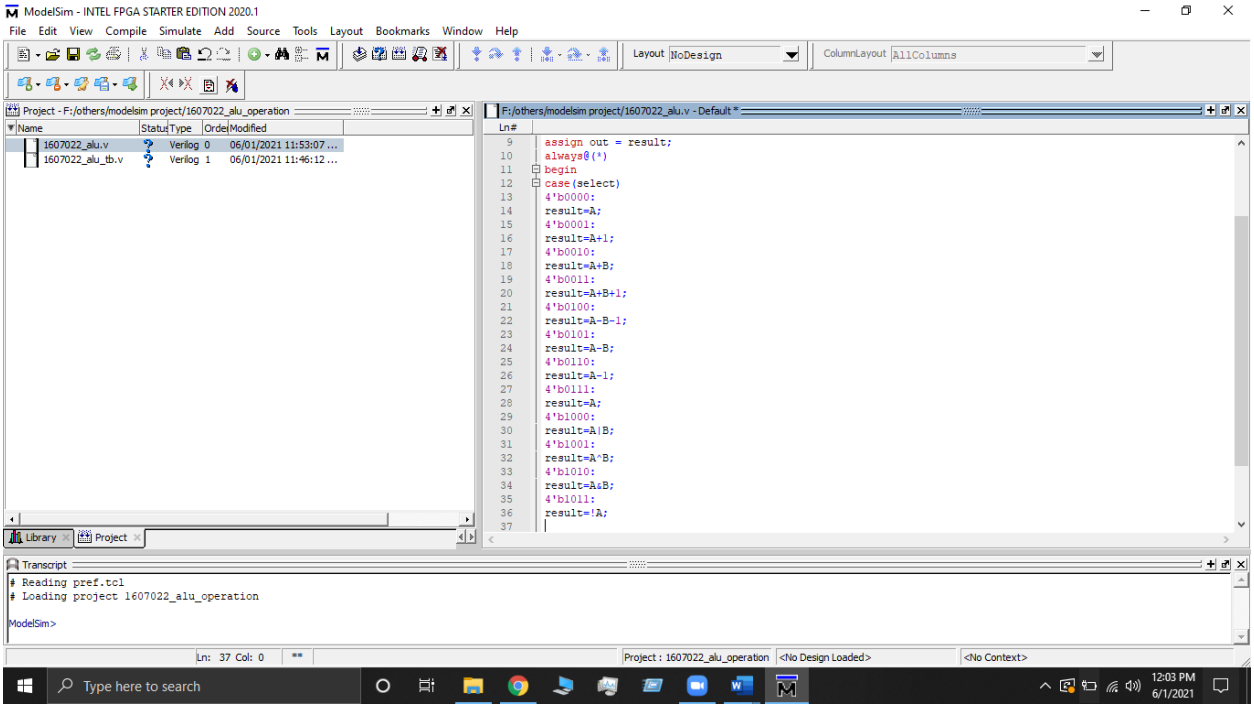
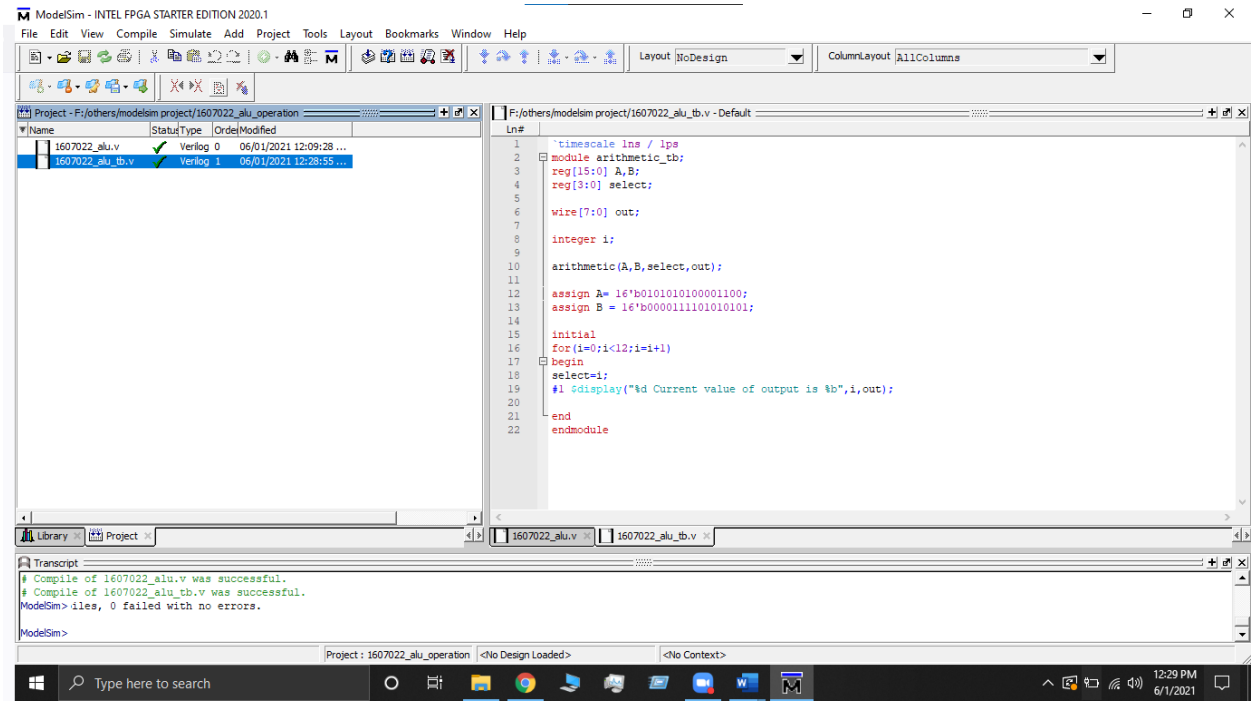
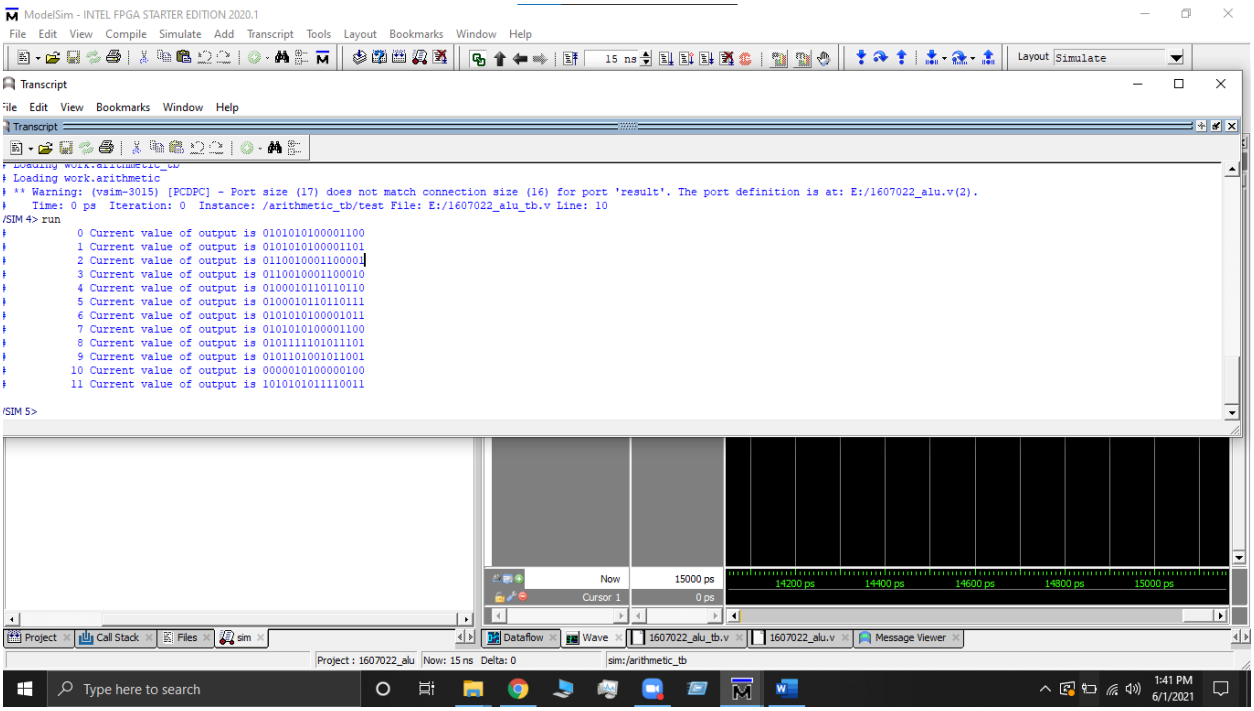
SS:


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Project - F:/others/modelsim project/1607022_alu_operation
1607022_alu.v
1607022_alu_tb.v
F:/others/modelsim project/1607022_alu.v - Default *
`timescale 1ns / 1ps
module arithmetic(
input [15:0] A,B;
input [3:0] selct;
output [15:0] out;
);
Transcript
Loading project demo
reading F:/others/modelsim_ase/win32aloem/../modelsim.ini
Loading project 1607022_alu_operation
ModelSim>
Type here to search
11:50 AM
6/1/2021


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Project - F:/others/modelsim project/1607022_alu_operation
1607022_alu.v
1607022_alu_tb.v
F:/others/modelsim project/1607022_alu.v - Default *
assign out = result;
always@(*)
begin
case(select)
4'b0000:
result=A;
4'b0001:
result=A+1;
4'b0010:
result=A+B;
4'b0011:
result=A+B+1;
4'b0100:
result=A-B-1;
4'b0101:
result=A-B;
4'b0110:
result=A-1;
4'b0111:
result=A;
4'b1000:
result=A|B;
4'b1001:
result=A^B;
4'b1010:
result=A&B;
4'b1011:
result=!A;
Transcript
Reading pref.tcl
Loading project 1607022_alu_operation
ModelSim>
Type here to search
12:03 PM
6/1/2021



Results:(for 12 operations)



Code:

ALU.v:

```
`timescale 1ns / 1ps
module arithmetic(A,B,select,result);
input [15:0] A,B; // 16  bit data
input  [3:0] select; // 4 bit select lines
output [16:0] result; // 16 bit results
reg [16:0] result;
always@(*)
begin
case(select) //12 operations
4'b0000:
result=A;
4'b0001:
result=A+1;
4'b0010:
result=A+B;
4'b0011:
result=A+B+1;
4'b0100:
result=A-B-1;
4'b0101:
result=A-B;
4'b0110:
result=A-1;
4'b0111:
result=A;
4'b1000:
result=A|B;
```

```
4'b1001:
result=A^B;
4'b1010:
result=A&B;
4'b1011:
result=~(A);
endcase
end
endmodule
```

ALU_tb: //test bench

```
`timescale 1ns / 1ps
module arithmetic_tb();
reg[15:0] A,B;
reg[3:0] select;
wire[15:0] out;
integer i;
arithmetic test(A,B,select,out);
assign A= 16'b0101010100001100;  //16 bit random data for A
assign B = 16'b0000111101010101;  //16 bit random data for B

initial
for(i=0;i<12;i=i+1) //for 12 operations
begin
select=i;
#1 $display("%d Current value of output is %b",i,out); //print

end
endmodule
```