ECE 551

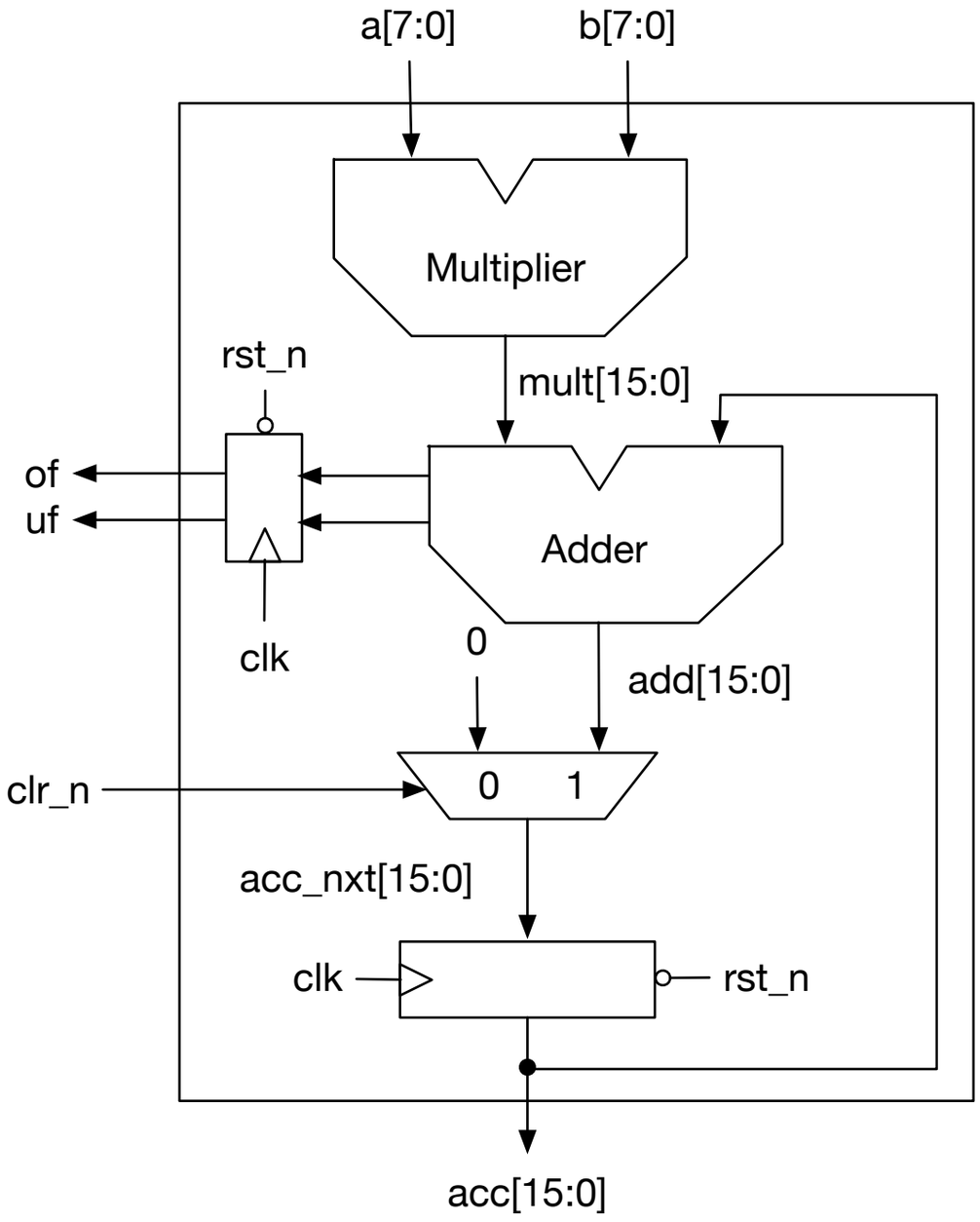
Exercise 7

Spring ’18

March 16

Due March 21, 11:00am

MAC module



Signal	Dir.	Wid.	Description
`a`	I	8	Operand A (signed)
`b`	I	8	Operand A (signed)
`of`	O	1	Overflow indicator
`uf`	O	1	Underflow indicator
`clr_n`	I	1	Clear (active low)
`acc`	O	16	Accumulator output

- Signed 8-bit MAC module
- Use dataflow Verilog for the datapath
- Use behavioral Verilog only for the registers
- clk and rst_n are implicit

Overflow and underflow

- Sign extend the input by 1 bit
  - e.g., +7 = 0111 → 00111, +1 = 0001 → 00001
  - e.g., -8 = 1000 → 11000, -1 = 1111 → 11111
- Add
- Compare 2 MSBs
  - 01 = Overflow
    - e.g., 7 + 1 = 00111 + 00001 = 01000 = 8. Overflow occurs since 8 cannot be represented in 4 bits.
  - 10 = Underflow
    - e.g., -8 - 1 = 11000 + 11111 = 10111 = -9. Underflow occurs -9 cannot be represented in 4 bits.
  - Otherwise, no over/underflow.

Testbench

- Write a testbench that keeps monitoring **of** and **uf** and display a message if any detected
  - No need to display any message if no of/uf detected
- Calculate the following:
  2*5 + (-2)*5 + (-3)*8
  - Does an overflow or underflow occurs?
- Calculate the following:
  126*126 + 126*126 + 126*126
  - Does an overflow or underflow occurs?
- Write an example that generates an underflow

Submit

- **mac.sv**
- **mac_tb.sv** exercising the MAC with the three input pairs
- **screenshot.png** showing one overflow and one underflow case

Team formation

- Make a team of 4 by noon Wednesday 3/21
- Register at https://goo.gl/forms/bpXPNHNtfywqrcYq2
- Let me know if you fail to make a team of 4
  - We have 78 students. One of the current teams of 2 should be split and make two teams of 3.
  - Teams of 3 get a small extra credit.