

Computer Architecture and Organisation Laboratory Report

Exercise 3: Designing the one input and one output sequential circuit that implements the given state transition and output tables

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1. **Requirements**

Design the one input and one output sequential circuit that implements the following state transition and output tables.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **Input** | |  |  | **Input** | |
| **State** | **0** | **1** | **State** | **0** | **1** |
| S1 | S2 | S3 | S1 | 0 | 0 |
| S2 | S2 | S3 | S2 | 1 | 0 |
| S3 | S3 | S1 | S3 | 0 | 1 |

You can use flip-flops from the breadboard (i.e. 7474, 7476) and NAND gates only. The output of the circuit and the output of each used flip-flop have to be connected to LED bar. Validate if the circuit behaves according to state transition and output tables.

1. **The resulting transition and output tables**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **State** | | **Input** | **Next State** | | **Output** | **Flip - Flop** | | **Flip - Flop** | |
| **Q1** | **Q0** | **X** | **Q1\*** | **Q0\*** | **Y** | **J1** | **K1** | **J2** | **K2** |
| **S0** | X | X | 0 | X | X | X | X | X | X | X |
| X | X | 1 | X | X | X | X | X | X | X |
| **S1** | 0 | 0 | 0 | 1 | 0 | 0 | 1 | X | 0 | X |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | X | 1 | X |
| **S2** | 1 | 0 | 0 | 1 | 0 | 1 | X | 0 | 0 | X |
| 1 | 0 | 1 | 0 | 1 | 0 | X | 1 | 1 | X |
| **S3** | 0 | 1 | 0 | 0 | 1 | 0 | 0 | X | X | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | X | X | 1 |

1. **The Karnaugh maps used for minimization of all needed logical functions**

**J1 = \*0 K1 = X**

**X**

**X**

|  |  |  |
| --- | --- | --- |
| **Q1Q0** | **0** | **1** |
| **00** | 1 | 0 |
| **01** | 0 | 0 |
| **11** | X | X |
| **10** | X | X |

|  |  |  |
| --- | --- | --- |
| **Q1Q0** | **0** | **1** |
| **00** | X | X |
| **01** | X | X |
| **11** | X | X |
| **10** | 0 | 1 |

**J0 = X K0 = X**

**X**

**X**

|  |  |  |
| --- | --- | --- |
| **Q1Q0** | **0** | **1** |
| **0** | 0 | 1 |
| **01** | X | X |
| **11** | X | X |
| **10** | 0 | 1 |

|  |  |  |
| --- | --- | --- |
| **Q1Q0** | **0** | **1** |
| **00** | X | X |
| **01** | 0 | 1 |
| **11** | X | X |
| **10** | X | X |

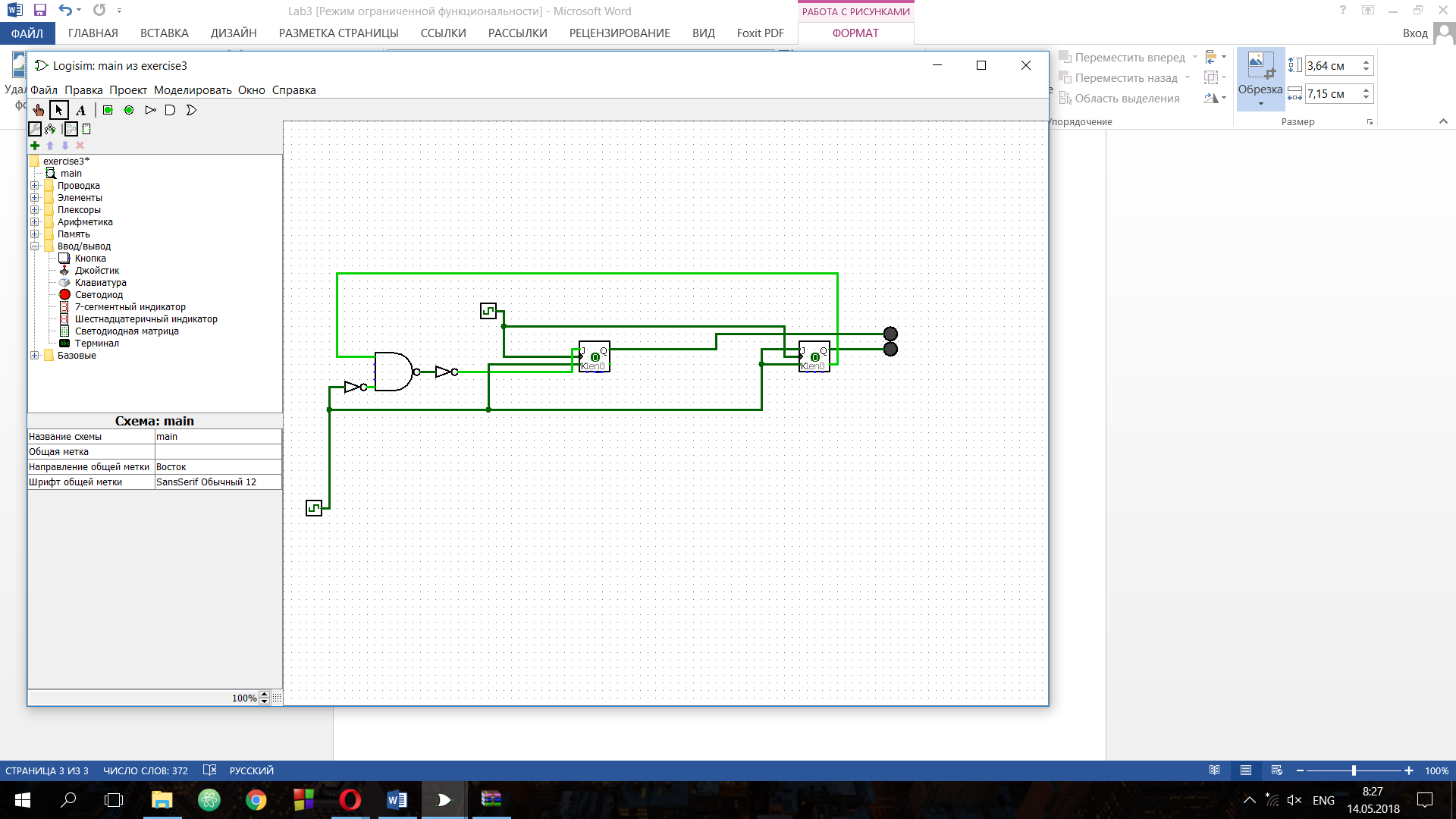
**Y = X\*Q0 + \*Q1 = NOT(0 \* 1)**

**X**

|  |  |  |
| --- | --- | --- |
| **Q1Q0** | **0** | **1** |
| **0** | 0 | 0 |
| **01** | 0 | 1 |
| **11** | X | X |
| **10** | 1 | 0 |

*Note: Groupings in the Karnaugh maps are marked by coloring the cells in the tables in red.*

1. **Obtained logic circuit and connection scheme**

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