Lab 4

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State Transition Diagram:

S0

S1

S2

S3

0

0

1

1

0

1

1

0

S0 = 00; S1 = 01; S2 = 10; S3 = 11

State Transition Table:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| State | | Input | Next State | | Flip-Flops | | | |
| Q1 | Q0 | x | Q1 | Q0 | J1 | K1 | J0 | K0 |
| 0 | 0 | 0 | 0 | 1 | 0 | X | 1 | X |
| 0 | 0 | 1 | 1 | 1 | 1 | X | 1 | X |
| 0 | 1 | 0 | 1 | 0 | 1 | X | X | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | X | X | 1 |
| 1 | 0 | 0 | 1 | 1 | X | 0 | 1 | X |
| 1 | 0 | 1 | 0 | 1 | X | 1 | 1 | X |
| 1 | 1 | 0 | 0 | 0 | X | 1 | X | 1 |
| 1 | 1 | 1 | 1 | 0 | X | 0 | X | 1 |

Karnaugh Maps:

1) For J1:

x

|  |  |  |
| --- | --- | --- |
| q1/q0 | 0 | 1 |
| 00 | 0 | 1 |
| 01 | 1 | 0 |
| 11 | X | X |
| 10 | X | X |

J1 = x\*q0 + x\*q0

2)For K1:

x

|  |  |  |
| --- | --- | --- |
| q1/q0 | 0 | 1 |
| 00 | X | X |
| 01 | X | X |
| 11 | 1 | 0 |
| 10 | 0 | 1 |

K1 = x\*q0 + x\*q0

3)For J0:

x

|  |  |  |
| --- | --- | --- |
| q1/q0 | 0 | 1 |
| 00 | 1 | 1 |
| 01 | X | X |
| 11 | X | X |
| 10 | 1 | 1 |

J0 = 1

4)For K0:

x

|  |  |  |
| --- | --- | --- |
| q1/q0 | 0 | 1 |
| 00 | X | X |
| 01 | 1 | 1 |
| 11 | 1 | 1 |
| 10 | X | X |

K0 = 1

Design of the circuit using logic gates

NAND, NOT, and JK flip-flops

