Lab 5

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State Transition Diagram:

S0/0

S1/0

S2/0

S3/1

1

0

1

0

0

1

0

1

S0 = 00; S1 = 01; S2 = 10; S3 = 11

State Transition Table:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| State | | Input | Output | Next State | | Flip-Flops | | |
| Q1 | Q0 | x | y | Q1 | Q0 | J1 | K1 | D0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | 0 | |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | X | 1 | |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | X | 0 | |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | X | 1 | |
| 1 | 1 | 0 | 1 | 1 | 0 | X | 0 | 0 | |
| 1 | 1 | 1 | 1 | 0 | 1 | X | 1 | 1 | |
| 1 | 0 | 0 | 0 | 0 | 0 | X | 1 | 0 | |
| 1 | 0 | 1 | 0 | 1 | 1 | X | 0 | 1 | |

Karnaugh Maps:

1) For J1:

x

|  |  |  |
| --- | --- | --- |
| q1/q0 | 0 | 1 |
| 00 | 0 | 0 |
| 01 | 1 | 0 |
| 11 | X | X |
| 10 | X | X |

J1 = x\*q0

2)For K1:

x

|  |  |  |
| --- | --- | --- |
| q1/q0 | 0 | 1 |
| 00 | X | X |
| 01 | X | X |
| 11 | 0 | 1 |
| 10 | 1 | 0 |

J1 = x\*q0 + x\*q0

3)For D0:

x

|  |  |  |
| --- | --- | --- |
| q1/q0 | 0 | 1 |
| 00 | 0 | 1 |
| 01 | 0 | 1 |
| 11 | 0 | 1 |
| 10 | 0 | 1 |

D0 = x

4)For y: → function for output

x

|  |  |  |
| --- | --- | --- |
| q1/q0 | 0 | 1 |
| 00 | 0 | 1 |
| 01 | 0 | 1 |
| 11 | 0 | 1 |
| 10 | 0 | 1 |

Y = x

Design of the circuit using logic gates

NAND, NOT, JK flip-flop, and D flip-flop