CVSD Final Project

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1 Algorithm

1.1 QR Decomposition Algorithm Introduction

There are many algorithms for QR decomposition, such as Householder transformation, Givens rotation, and modified Gram-Schmidt. Since modified Gram-Schmidt algorithm computes the results faster and it is more intuitive for implementation compared to other algorithms, we adopt modified Gram-Schmidt to implement the hardware for QR decomposition in this final project.

Modified Gram-Schmidt is an iterative algorithm that starts with the original matrix H and produces the orthogonal matrix Q and the upper triangular matrix R. It works by iteratively orthogonalizing the columns of H to create Q while simultaneously updating R. In each iteration, Modified Gram-Schmidt computes the orthogonal projection of the current column onto the previously processed columns, ensuring that Q remains orthogonal. This process continues until all columns have been orthogonalized, resulting in the QR decomposition of the original matrix H.

$$H = [h_1|h_2|h_3|h_4] = [e_1|e_2|e_3|e_4] \begin{bmatrix} h_1 \cdot e_1 & h_2 \cdot e_1 & h_3 \cdot e_1 & h_4 \cdot e_1 \\ 0 & h_2 \cdot e_2 & h_3 \cdot e_2 & h_4 \cdot e_2 \\ 0 & 0 & h_3 \cdot e_3 & h_4 \cdot e_3 \\ 0 & 0 & 0 & h_4 \cdot e_4 \end{bmatrix} = QR \tag{1}$$

2 Hardware Implementation

2.1 Hardware Scheduling

In our design, the result of one RE data will be calculated after twenty six cycles, and the calculation will be started in the 17^{th} cycle (counter equals 16) of this RE. Figure(1) shows the flow for the 1^{st} RE calculation and the details of each cycle. For the 1^{st} RE, we start our calculations at the 17^{th} cycle of the 1^{st} RE input. After twenty six cycles of calculations, the result can be obtained at the 3^{rd} cycle (counter equals 2) of the 3^{rd} RE input. Since our calculation process takes more than twenty cycles, we parallel part of our design to allow all REs to start the process at the 17^{th} cycle of each RE. Please note that we only show the 1^{st} RE calculation in Figure(1). In our real design, the process for 2^{nd} RE will be started at the 17^{th} cycle of the 2^{nd} RE while the process for the 1^{st} RE have not been done.

The notations in Figure(1) are referred to the final introduction. The * superscript means the multiplications needed for the intermediate value of the certain notation. Since the modified Gram-Schmidt needs many multiplications and the frequency requirement is above 200MHz, we have to pipeline the hardware into many stages. According to Figure(1), we can observe that we only do one stage calculations in most cycles in order to reach the higher frequency more than 200MHz. Because the multiplication delay is strict for high frequency design, we separate the multiplication from addition and subtraction to reduce the latency of each timing path.

input	RE1				RE2								
counter	16	17	18	19	0	1	2	3	4	5	6	7	8
	R_{11}^*	R_{11}	e_1	R_{12}^*	R_{12}	R_{13}	R_{14}	$R_{14}e_1$	$h_4^{(1)}$	e_2	R_{23}^*	R_{23}	R_{24}
					R_{13}^*	R_{14}^*	$R_{13}e_1$	$h_3^{(1)}$	R_{22}	y_hat_1	$y\_hat_2^*$	y_hat_2	$R_{23}e_2$
						$R_{12}e_1$	$h_2^{(1)}$	R_{22}^*	$y\_hat_1^*$			R_{24}^*	
input	RE2											RE3	
counter	9	10	11	12	13	14	15	16	17	18	19	0	1
	$R_{24}e_2$	$h_4^{(2)}$	R_{33}	e_3	R_{34}^*	R_{34}	$R_{34}e_3$	$h_4^{(3)}$	R_{44}^*	R_{44}	e_4	$y\_hat_4^*$	y_hat_4
	$h_3^{(2)}$	R_{33}^*			$y\_hat_3^*$	y_hat_3							

Figure 1: Flow Chart

2.2 Hardware Block Diagram

Figure(2) shows the block diagram of our design. In our design, we don't use SRAM since we want to fetch the data faster. There are other three modules designed by ourselves to simplify the code and improve the readability. There is a module functioning as a lookup table for square root value and reciprocal value. The other two modules functioning as complex multiplier with different fix-point format.

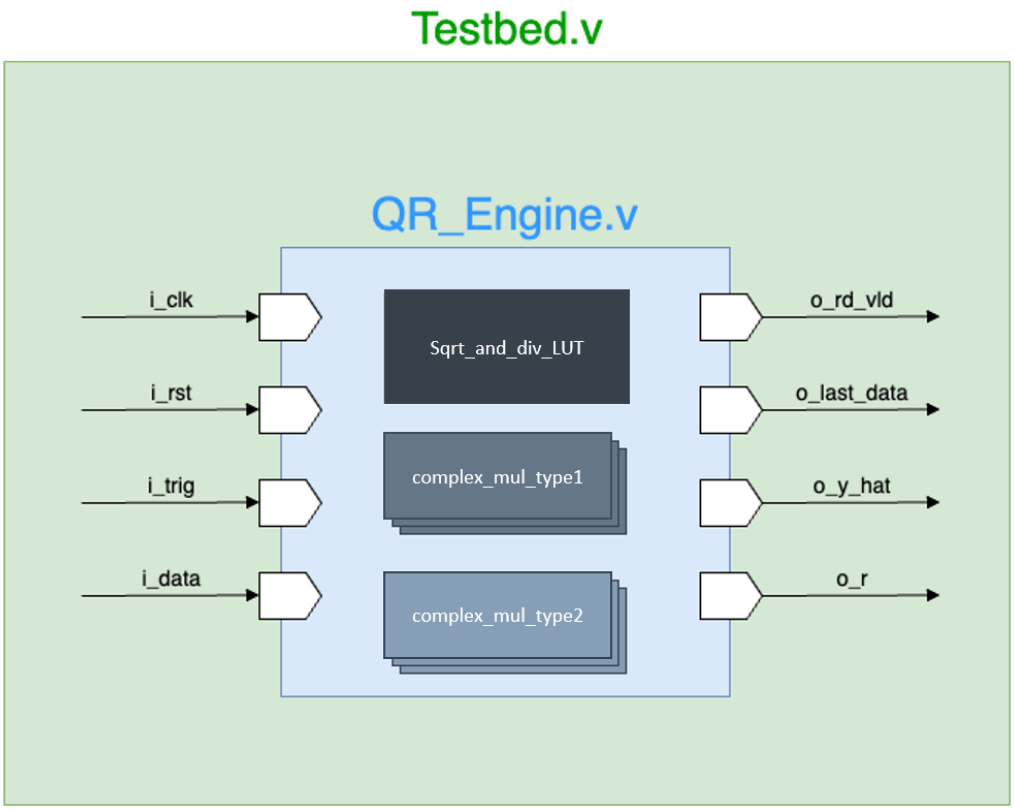

Figure 2: Block Diagram

2.3 Fixed Point Setting

The input data is in s1,22 fix point format, and the output data should be in s3,16 format. Since the precision for intermediate calculation directly affects the register needed and the output precision, selecting number of bits for each intermediate step should be considered carefully. Since the LUT

for square root and reciprocal will be quite large if we keep all precision, we only consider ten bits in this LUT. According to the result by means of implementing the LUT, we can get about 1.23 performance gain while there are still margins for 10SNR and 15SNR cases. Thus, we reduce the width of some registers to minimize the area while maintain the same performance gain. In the end, we use about two thousand registers.

2.4 Area / Power / Latency Reports

```
****************************************
Report : area
Design : QR_Engine
Version: U-2022.12
Date   : Sun Dec 17 00:37:51 2023
****************************************

Library(s) Used:

    slow (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/slow.db)

Number of ports:                         1405
Number of nets:                         34105
Number of cells:                        30892
Number of combinational cells:          28239
Number of sequential cells:              2376
Number of macros/black boxes:               0
Number of buf/inv:                       5928
Number of references:                     472

Combinational area:             466793.486211
Buf/Inv area:                    45848.471327
Noncombinational area:           80139.344679
Macro/Black Box area:                0.000000
Net Interconnect area:         3304949.922974

Total cell area:                546932.830889
Total area:                    3851882.753863
1
```

(a) Synthesis Area Report

```
************************ Analyze Floorplan *************************
    Die Area(um^2)            : 607217.50
    Core Area(um^2)           : 575885.39
    Chip Density (Counting Std Cells and MACROs and IOs): 94.840%
    Core Density (Counting Std Cells and MACROs): 100.000%
    Average utilization       : 100.000%
    Number of instance(s)     : 58795
    Number of Macro(s)        : 0
    Number of IO Pin(s)       : 533
    Number of Power Domain(s) : 0
************************ Estimation Results ************************
********************************************************************
```

(b) APR Area Report

Figure 3: Area Report

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 20
Design : QR_Engine
Version: U-2022.12
Date   : Sun Dec 17 00:37:56 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: DP_OP_585J1_126_9153/i_clk_r_REG909_S20
              (rising edge-triggered flip-flop clocked by i_clk)
  Endpoint: i_clk_r_REG482_S9
            (rising edge-triggered flip-flop clocked by i_clk)
  Path Group: i_clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  QR_Engine          tsmc13_wl10           slow

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock i_clk (rise edge)                                 0.00       0.00
  clock network delay (ideal)                             1.00       1.00
  DP_OP_585J1_126_9153/i_clk_r_REG909_S20/CK (DFFRX4)     0.00       1.00 r
  DP_OP_585J1_126_9153/i_clk_r_REG909_S20/Q (DFFRX4)      0.47       1.47 f
  U27636/CO (ADDFHX4)                                     0.36       1.83 f
  U10690/Y (XOR2X4)                                       0.12       1.95 r
  U10647/Y (XOR2X4)                                       0.20       2.15 f
  U10646/Y (NOR2X6)                                       0.18       2.33 r
  U8177/Y (OA21X4)                                        0.21       2.54 r
  U10669/Y (NAND3X8)                                      0.19       2.73 f
  U10666/Y (AOI21X4)                                      0.15       2.88 r
  U5290/Y (XNOR2X2)                                       0.21       3.09 f
  U9855/Y (NOR2X4)                                        0.17       3.26 r
  s1/sum[11] (square_root_relate)                         0.00       3.26 r
  s1/U2752/Y (INVX12)                                     0.13       3.39 f
  s1/U359/Y (INVX4)                                       0.18       3.57 r
  s1/U2317/Y (OR2X4)                                      0.23       3.80 r
  s1/U213/Y (INVX3)                                       0.15       3.95 f
  s1/U803/Y (INVX3)                                       0.30       4.25 r
  s1/U580/Y (NOR2X2)                                      0.18       4.43 f
  s1/U581/Y (INVX1)                                       0.27       4.70 r
  s1/U14/Y (NAND3X1)                                      0.20       4.91 f
  s1/U1069/Y (AOI21X1)                                    0.29       5.20 r
  s1/U3/Y (OAI21X2)                                       0.25       5.45 f
  s1/sqrt_val[17] (square_root_relate)                    0.00       5.45 f
  i_clk_r_REG482_S9/D (DFFRX1)                            0.00       5.45 f
  data arrival time                                                  5.45

  clock i_clk (rise edge)                                 4.80       4.80
  clock network delay (ideal)                             1.00       5.80
  clock uncertainty                                      -0.10       5.70
  i_clk_r_REG482_S9/CK (DFFRX1)                           0.00       5.70 r
  library setup time                                     -0.25       5.45
  data required time                                                 5.45
  --------------------------------------------------------------------------
  data required time                                                 5.45
  data arrival time                                                 -5.45
  --------------------------------------------------------------------------
  slack (MET)                                                        0.00
```

(a) Max

```
****************************************
Report : timing
        -path full
        -delay min
        -max_paths 20
Design : QR_Engine
Version: U-2022.12
Date   : Sun Dec 17 00:37:56 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: i_clk_r_REG868_S16
              (rising edge-triggered flip-flop clocked by i_clk)
  Endpoint: i_clk_r_REG868_S16
            (rising edge-triggered flip-flop clocked by i_clk)
  Path Group: i_clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  QR_Engine          tsmc13_wl10           slow

  Point                                   Incr       Path
  ----------------------------------------------------------
  clock i_clk (rise edge)                 0.00       0.00
  clock network delay (ideal)             1.00       1.00
  i_clk_r_REG868_S16/CK (DFFRX4)          0.00       1.00 r
  i_clk_r_REG868_S16/QN (DFFRX4)          0.31       1.31 r
  U10115/Y (OAI2BB2X2)                    0.11       1.42 f
  i_clk_r_REG868_S16/D (DFFRX4)           0.00       1.42 f
  data arrival time                                  1.42

  clock i_clk (rise edge)                 0.00       0.00
  clock network delay (ideal)             1.00       1.00
  clock uncertainty                       0.10       1.10
  i_clk_r_REG868_S16/CK (DFFRX4)          0.00       1.10 r
  library hold time                       0.03       1.13
  data required time                                 1.13
  ----------------------------------------------------------
  data required time                                 1.13
  data arrival time                                 -1.42
  ----------------------------------------------------------
  slack (MET)                                        0.29
```

(b) Min

Figure 4: Synthesis Timing Report

```
report_power
****************************************
Report : Time Based Power
Design : QR_Engine
Version: T-2022.03
Date   : Mon Dec 18 09:42:37 2023
****************************************


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                          Internal  Switching  Leakage    Total
Power Group               Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network           2.814e-03 5.159e-04 8.190e-06 3.338e-03 (12.87%)
register                3.502e-03 1.290e-04 6.391e-05 3.695e-03 (14.24%)  i
combinational              0.0116 6.956e-03 3.234e-04    0.0189 (72.89%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 7.601e-03   (29.30%)
  Cell Internal Power  =    0.0179   (69.17%)
  Cell Leakage Power   = 3.955e-04   ( 1.52%)
                         ---------
Total Power            =    0.0259  (100.00%)

X Transition Power     = 3.595e-05
Glitching Power        = 1.169e-04

Peak Power             =    0.5933
Peak Time              =   524.761
```

Figure 5: Power Report

```
Pattern    1# ~  100# are written
Pattern  101# ~  200# are written
Pattern  201# ~  300# are written
Pattern  301# ~  400# are written
Pattern  401# ~  500# are written
Pattern  501# ~  600# are written
Pattern  601# ~  700# are written
Pattern  701# ~  800# are written
Pattern  801# ~  900# are written
Pattern  901# ~ 1000# are written
$finish called from file "./testfixture-3.v", line 422.
$finish at simulation time             98138650
           V C S   S i m u l a t i o n   R e p o r t
Time: 98138650 ps
CPU Time:    282.490 seconds;       Data structure size:   6.9Mb
```

Figure 6: Latency

```
------------------------------------------------------------
     timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+--------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all  | reg2reg |reg2cgate| in2reg  | reg2out | in2out  | default |
+--------------------+--------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.341 |  0.341  |  0.829  |  0.481  |  2.437  |   N/A   |  0.000  |
|           TNS (ns):|  0.000 |  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0   |    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  4959  |  2105   |   247   |  2697   |   478   |   N/A   |    0    |
+--------------------+--------+---------+---------+---------+---------+---------+---------+

+----------------+-----------------------------+------------------+
|                |             Real            |       Total      |
|    DRVs        +------------------+----------+------------------|
|                |  Nr nets(terms)  | Worst Vio|  Nr nets(terms)  |
+----------------+------------------+----------+------------------+
|   max_cap      |      0 (0)       |   0.000  |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000  |      0 (0)       |
|   max_fanout   |      0 (0)       |     0    |     10 (10)      |
|   max_length   |      0 (0)       |     0    |      0 (0)       |
+----------------+------------------+----------+------------------+

Density: 71.994%
      (100.000% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------
```

(a) Setup

```
------------------------------------------------------------
     timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_max

+--------------------+--------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all  | reg2reg |reg2cgate| in2reg  | reg2out | in2out  | default |
+--------------------+--------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.674 |  0.674  |  1.121  |  1.173  |  1.776  |   N/A   |  0.000  |
|           TNS (ns):|  0.000 |  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0   |    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  4959  |  2105   |   247   |  2697   |   478   |   N/A   |    0    |
+--------------------+--------+---------+---------+---------+---------+---------+---------+

Density: 71.994%
      (100.000% with Fillers)
------------------------------------------------------------
```

(b) Hold

Figure 7: Route Timing Report