Min-Hsin (Sam) Liu 劉旻鑫

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Education

National Taiwan University

- **M.S.** in *Graduate Institute of Electronics Engineering*, major in **EDA** *Sep. 2023 – Jun. 2025*
  - **Advisor**：James Chien-Mo Li - **Research Areas**：VLSI Testing and Diagnosis
  - **Thesis**：Debugging and Preventing Abnormally high V_{min} During Logic Scan Test Bring-up - GPA: 4.10/4.30
- **B.S.** in *Engineering Science and Ocean Engineering* focus on **Digital IC Design** *Sep. 2019 – Jun. 2023*
  - GPA：4.05/4.30 - Rank：3/47 - **Awards:** Dean's List Award (3 times)
- **Courses**
  Introduction to EDA | VLSI Testing | Algorithms | Computer-aided VLSI System Design
  Logic Synthesis and Verification | Logic Circuit Design | Circuits and Electronics | Physical Design for Nanometer ICs

Experience

ILITEK, Physical Design Intern *Jun. 2023 – Aug. 2023*

- Applied ICC throughout APR flow: Floorplan → Placement → CTS → Routing in two ongoing industry projects
- Skilled in advanced techniques for every step of APR, including fixing timing with PrimeTime and Tweaker

Qualcomm, Product Test Engineer Intern *May 2024 – Jun. 2025*

- Solved the over-testing problem caused by high V_{min} pattern sets with DFT and PTE teams in the U.S. and India
- Debugged root cause of high V_{min} and propose two methods to improve V_{min} with little pattern count inflation

National Taiwan University, Algorithm Teacher Assistant *Sep. 2024 – Dec. 2024*

- Guided students to solve problems and improving average grades to be the highest among three classes

Skills

- **Programming Language** C/C++, Python, Java, Verilog, MATLAB, Tcl
- **CAD Tools** Cadence Innovus/NC-Verilog/VCS, PSpice, Altium Designer
  Synopsys Design Compiler/PrimeTime/ICC, Siemens Tessent
- **English Ability** TOEFL-105

Publication

Debugging and Preventing Abnormally High V_{min} During Logic Scan Test Bring-up | Tessent, Python

- Found out the root cause of high V_{min} pattern sets for an industry design by Qualcomm
- Proposed pre-silicon and post-silicon methods with Tessent to prevent high V_{min} pattern sets
- Improved V_{min} by **28.83mV** to **39.33mV** with **0%** to **0.5%** pattern count inflation
- Master Thesis collaborating with Qualcomm, Accepted paper of **2025 International Test Conference**

ML-based Adaptive Wafer Sort to Preserve Diagnostic Information | Python

- Propose a new adaptive test to preserve diagnostic information and save test time on various types of test suites
- Reduce up to **39%** test time with 185 ppm test quality loss and preserve up to **338 times** diagnostic information
- Collaborate with Qualcomm, Accepted paper of **2025 VLSI Test Symposium**

Projects

Power and Timing Optimization Using Multibit Flip-Flop | C++ *Feb. 2024 – Jun. 2024*

- Proposed a three-step method to optimize performance, including power, timing and area
- In charge of multi-bit flip-flop legalization using modified BFS considering bin utilization rate
- Improved **30%** performance score compared with input data

QR Decomposition Hardware Implementation | Verilog *Dec. 2023 – Jan. 2024*

- Constructed QR decomposition with modified Gram-Schmidt algorithm for TX/RX with Verilog
- Applied pipeline technique to reduce critical path, and parallel technique to improve throughput
- Simplified complex computation, such as square root and square, to a few LUTs
- Implemented digital IC design flow: RTL design → Verification → Synthesis → APR
- Computer-aided VLSI System Design final project (performance **ranked 9** out of 50 groups)

N-Detect Transition-Delay-Fault ATPG and Test Compression | C++ *May. 2023 – Jun. 2023*

- Implemented a transition delay fault (TDF) ATPG based on launch-on-shift (LOS) mode
- Generated N-detected test pattern set for better test quality
- Adopted static test compression (STC) and dynamic test compression (DTC) to reduce **30%** test length in average