**SET LOW CBX**

**Inputs Needed:**

* Target Frequency
* Data Rate
* Integer N Mode
* Device Sub Function
* Destination

**Input Values:**

1. Target Frequency - Integer Value (Eg. 2000000000)

2. Data Rate - Integer Value (Eg. 200000000)

3. Integer N Mode - True or False flag

4. Device Sub Function -

* 0 for TX
* 1 for RX/Default

5. Destination -

* Radio\_Perif\_0
* Radio\_Perif\_1
* Global
* Radio\_0\_I2C
* Radio\_1\_I2C
* Global\_I2C
* Radio\_0\_SPI
* Radio\_1\_SPI
* Global\_SPI

6. **Constant Registers are needed in Input --> Not passed as Input but defined in the function.**

Constant Register 0:

|  |  |
| --- | --- |
| **Field** | **Value** |
| INT\_MODE | False |
| INT | 125 |
| FRAC | 0 |
| C3 | False |
| C2 | False |
| C1 | False |

Constant Register 1:

|  |  |
| --- | --- |
| **Field** | **Value** |
| CPOC | False |
| CPL | 1 |
| CPT | 0 |
| Phase | 1 |
| MOD | 4095 |
| C3 | False |
| C2 | False |
| C1 | True |

Constant Register 2:

|  |  |
| --- | --- |
| **Field** | **Value** |
| LDS | False |
| SDN | 3 |
| MUX | 1 |
| DBR | False |
| RDIV2 | False |
| R | 1 |
| REG4BD | False |
| CP | 8 |
| LDF | False |
| LDP | False |
| PDP | True |
| SHDN | False |
| TRI | False |
| RST | False |
| C3 | False |
| C2 | True |
| C1 | False |

Constant Register 3:

|  |  |
| --- | --- |
| **Field** | **Value** |
| VCO | 0 |
| VAS\_SHDN | False |
| RETUNE | True |
| CDM | 0 |
| CDIV | 1 |
| C3 | False |
| C2 | True |
| C1 | True |

Constant Register 4:

|  |  |
| --- | --- |
| **Field** | **Value** |
| FB | True |
| DIVA | 0 |
| BS | 0 |
| BDIV | True |
| RFB\_EN | False |
| BPWR | 0 |
| RFA\_EN | True |
| APWR | 3 |
| C3 | True |
| C2 | False |
| C1 | False |

Constant Register 5:

|  |  |
| --- | --- |
| **Field** | **Value** |
| F01 | True |
| LD | 1 |
| MUX | False |
| C3 | True |
| C2 | False |
| C1 | True |

**Sub Modules:**

* CreateMax2870Packets (Stand alone program for possible reusability)

**Inputs Needed:**

1. Constant Register 5

2. Constant Register 4

3. Constant Register 3

4. Constant Register 2

5. Constant Register 1

6. Constant Register 0

7. Device Sub Function

8. Destination

CreateMax2870Packets module also internally calls DestinationEncoding(Stand alone program for possible reusability) module to Encode the Destination Value.

* construct\_radio\_register from FormatRadioCommand module to create the Input Stream for each packet seperately**.**
* Encode\_Process from EncodingStream to create 64 bit format for each packet of the Input Stream.

**Output:**

* LO Frequency
* Coerce Frequency
* Packets (7 packets - 1 header packet, 6 constant register packets respectively)
* Each Packet will have 5 packets in the encoded stream(35 packets)
* Each packet is converted to its 64 bit stream(35 packets)

**Packet 1 Information:**

|  |  |
| --- | --- |
| Destination | Refer Page 1 |
| Address | 36 |
| Data | If TX = [1 OR 1610612736]  If RX = [2 OR 1610612736] |

**All data values for the registers are calculated by constructing an array of index 32 and True or False values, these true and false values are converted to their binary equivalent(True = 1 and False = 0) and then converted to its decimal form.**

**Input to the binary form is specified in the tables.**

**Packet 2 Information: Register 5**

|  |  |
| --- | --- |
| Destination | Refer Page 1 |
| Address | 40 |
| Data | |  |  | | --- | --- | | C1 Register Value | True or False | | C2 Register Value | True or False | | C3 Register Value | True or False | |  | False | |  | False | |  | False | |  | False | |  | False | |  | False | |  | False | |  | False | |  | False | |  | False | |  | False | |  | False | |  | False | |  | False | |  | False | | MUX Register Value | True or False | |  | False | |  | False | |  | False | | LD Register Value(2 bits) | Last 2 LS bits of the binary representation of the Value  (Ex: If reg value is 2, then binary form is 10, therefore True, False) | | F01 Register Value | True or False | |  | False | |  | False | |  | False | |  | False | |  | False | |  | False | |  | False | |

**Packet 3 Information: Register 4**

|  |  |
| --- | --- |
| Destination | Refer Page 1 |
| Address | 40 |
| Data | |  |  | | --- | --- | | C1 Register Value | True or False | | C2 Register Value | True or False | | C3 Register Value | True or False | | APWR Register Value | Last 2 LS bits of the binary representation of the Value | | RFA\_EN Register Value | True or False | | BPWR Register Value | Last 2 LS bits of the binary representation of the Value | | RFB\_EN Register Value | True or False | | BDIV Register Value | True or False | |  | False | |  | False | | BS Register Value | Last 8 LS bits of the binary representation of the Value | | DIVA Register Value | Last 3 LS bits of the binary representation of the Value | | FB Register Value | True or False | | BS Register Value | LS Bit 9 and LS Bit 10's binary representation of the value | |  | False | |  | False | |  | False | |  | True | |  | True | |  | False | |

**Packet 4 Information: Register 3**

|  |  |
| --- | --- |
| Destination | Refer Page 1 |
| Address | 40 |
| Data | |  |  | | --- | --- | | C1 Register Value | True or False | | C2 Register Value | True or False | | C3 Register Value | True or False | | CDIV Register Value | Last 12 LS bits of the binary representation of the Value | | CDM Register Value | Last 2 LS bits of the binary representation of the Value | |  | False | |  | False | |  | False | |  | False | |  | False | |  | False | |  | False | | RETUNE Register Value | True or False | | VAS\_SHDN Register Value | True or False | | VCO Register Value | Last 6 LS bits of the binary representation of the Value | |

**Packet 5 Information: Register 2**

|  |  |
| --- | --- |
| Destination | Refer Page 1 |
| Address | 40 |
| Data | |  |  | | --- | --- | | C1 Register Value | True or False | | C2 Register Value | True or False | | C3 Register Value | True or False | | RST Register Value | True or False | | TRI Register Value | True or False | | SHDN Register Value | True or False | | PDP Register Value | True or False | | LDP Register Value | True or False | | LDF Register Value | True or False | | CP Register Value | Last 4 LS bits of the binary representation of the Value | | REG4DB Register Value | True or False | | R Register Value | Last 10 LS bits of the binary representation of the Value | | RDIV2 Register Value | True or False | | DBR Register Value | True or False | | MUX Register Value | Last 3 LS bits of the binary representation of the Value | | SDN Register Value | Last 2 LS bits of the binary representation of the Value | | LDS Register Value | True or False | |

**Packet 6 Information: Register 1**

|  |  |
| --- | --- |
| Destination | Refer Page 1 |
| Address | 40 |
| Data | |  |  | | --- | --- | | C1 Register Value | True or False | | C2 Register Value | True or False | | C3 Register Value | True or False | | MOD Register Value | Last 12 LS bits of the binary representation of the Value | | PHASE Register Value | Last 12 LS bits of the binary representation of the Value | | CPT Register Value | Last 2 LS bits of the binary representation of the Value | | CPL Register Value | Last 2 LS bits of the binary representation of the Value | | CPOC Register Value | True or False | |

**Packet 7 Information: Register 0**

|  |  |
| --- | --- |
| Destination | Refer Page 1 |
| Address | 40 |
| Data | |  |  | | --- | --- | | C1 Register Value | True or False | | C2 Register Value | True or False | | C3 Register Value | True or False | | FRAC Register Value | Last 12 LS bits of the binary representation of the Value | | INT Register Value | Last 16 LS bits of the binary representation of the Value | | INT MODE Register Value | True or False | |