Photovoltaic Inverter Model in Simulink

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I. INTRODUCTION

The 2020 National Renewable Energy Lab (NREL) Solar District Cup is a collegiate design competition that challenges undergraduates to design a realistic and buildable solar photovoltaic (PV) plus battery storage system for one of several urban districts. Multiple Lane Department of Electrical Engineering and Computer Science Seniors participated in this competition in lieu of their capstone as competitors in the New Mexico State University (NMSU) district division, and placed second overall.

NMSU wishes to reduce their energy impact and maximize utility savings by investing in a commercial solar PV plus battery storage system. To this end, the team designed two different solar PV installations on the NMSU campus that collectively supply approximately 30% of the campus' yearly energy consumption. The installation of interest to this project is a 278.2 kWDC roof-mounted installation on the Corbett Center Student Union.

This installation, like most PV plus storage systems, necessitates the use of a power inverter, of which there are two in the Corbett Center installation, as can be seen in the **one-line diagram in the appendix**. It is important to note that local zoning laws in the region of Las Cruces, New Mexico that the university is located presently prohibit net metering. Due to this situation, the overall campus PV system was designed such that power generation does not result in net power exports back into the grid.

However, the PV plus storage system must be designed to be 'grid ready' and is interconnected onto the Geothermal Substation of the Western Interconnection region. Like in many jurisdictions, net-metering is slated to gain legislative ground in the coming years. If and when net metering is permitted, it will require that the utility that services the campus credits the campus for the solar power that is supplied to the grid.

When it begins net metering, the Corbett Center Student Union roof-mounted installation's power inverter; being the electronic system that converts the DC power generated by the PV array into AC usable by the grid, must output power that has been processed such that it is sufficiently cleared of distorting harmonic contents. Thus, the design of the inverter must seek to minimize both real power losses and total harmonic distortion (THD).

In this paper, the team presents a "reverse engineering" and redesign of **one of the two** *SMA Sunny Tripower Core1 50-US/62-US* grid-tie inverters utilized in the PV installation designed for the Corbett Student Union rooftop by the team in the 2020 NREL Solar District Cup. This inverter is boxed in red in the one-line diagram in the appendix.

II. CIRCUIT TOPOLOGY AND DEVICES

The chief design principle in question for the creation of any power electronic converter is the circuit topology. The team's PV inverter utilizes power MOSFETs as the primary active circuit components within the H-bridge, specifically the Mouser Silicon Carbide Power MOSFET C2M0025120D. Unlike current-controlled switching elements such as BJTs, MOSFETs are voltage-controlled, providing the advantage of considerably lower overall real power losses, and thereby lower costs associated with their operation as a power device.

Additionally, MOSFETs with SiC substrate were selected due to the fact that they "switch faster, maintain a higher current density, and possess a lower on-state impedance" compared to even most insulated-gate BJTs. [1]

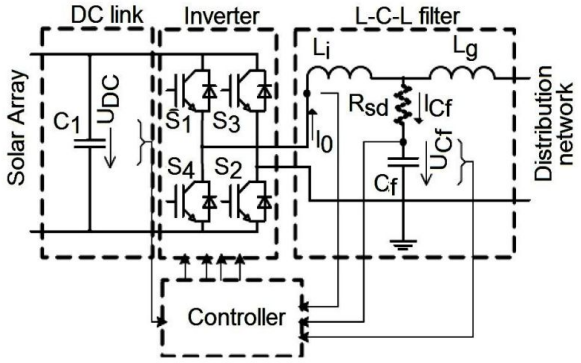

Fig. 1: General One-Line Diagram of a Grid-Tie Inverter (Single Phase) [2]

As shown in Figure 1, before the H-bridge section of the inverter is a DC-link capacitor placed in parallel over the photovoltaic array to act as a "pre-inverter filter", in an attempt to smooth the inherently volatile and noisy DC signal of the PV array and limit its fluctuations even under heavy current absorption. This capacitor essentially acts as a filter to reduce current ripple [2].

Following the H-bridge, the output of the circuit, still being primarily a distorted sinusoid in nature, (i.e. possessing various harmonics) requires an extensive filtering scheme to produce a more pure sinusoidal output. This is accomplished primarily with a resonant filter

consisting of an inductor in series with the output terminal, and a capacitor in parallel with the output terminals. This is called an LC filter, which acts similar to the DC link, but instead functions on the output of the inverter.

Downsides of this LC filter include a marginal attenuation of the output current, and the potential for resonances and unstable states in the system [4]. Following the LC filter, the voltage must be stepped up via a high frequency transformer to a little above the grid voltage before it can be connected. Because of the fact that Las Cruces, New Mexico does not currently allow net metering, the PV system and its corresponding inverter were modeled as operating in "Island Mode", and the modeling of the interconnection to the grid was neglected for the purpose of this analysis, although the inclusion of it in future works would be relatively simple.

An additional measure included in the inverter design, to work in tandem with the H-bridge, is a pulse width modulation (PWM) scheme. Naturally, the frequency of the output must be a practically pure 60 Hz, and therefore must also be synchronized with grid phase delay.

III. DEVICE PROTECTION AND CALCULATIONS

The single inverter in the Corbett Hall PV System simulated by the team is fed by 12 strings of 16 PV modules. By referring to the specification sheet of the selected solar module, [3], the nominal, maximum, and worst case scenario specifications for the input of the solar array into the inverter were calculated as follows, utilizing the data for the CS32-420PB-AG Module:

Currents:

$$I_{nominal} = I_{mp} * 12\ strings = 127.68\ A,$$

$$where\ I_{mp} = 10.64\ A$$

$$I_{max} = I_{sc} * 12\ strings = 135.12\ A,$$

$$where\ I_{sc} = 11.26\ A$$

Voltages:

$$V_{nominal} = V_{mp} * 16\ modules = 632\ V,$$

$$where\ V_{mp} = 39.5\ V$$

$$V_{max} = V_{oc} * 16\ modules = 768\ V,$$

$$where\ V_{oc} = 48\ V$$

By simulation, these values were confirmed to be successfully input into the inverter model via the PV array Simulink component.

Applying a 15% buffer, the "worst case scenario" for inverter inputs were calculated to be:

$$I_{max} = 135.12\ A\ *\ 1.15 = 155.38\ A$$

$$V_{max} = 768\ V\ * 1.15 = 883.2\ V$$

$$P_{max} = 155.38\ A * 883.2\ V\ = 137.23\ kW$$

In actuality, at the nominal operating points, total power for n strings of m PV modules can be calculated as follows:

$$P_{array} = I_{nominal} * V_{nominal} * n * m$$

$$= 10.64 * 39.5 * 12 * 16 = 80.69\ kW$$

Which was verified by the team via simulation.

A relatively unintuitive component of power electronics design is that of filter parameter selection. In order to filter the noisy sinusoidal PWM signal output by the h-bridge containing harmonics, a variety of protection filter schemes were utilized as described in section II.

As described previously, a lowpass RLC filter was implemented, utilizing a capacitor connected in parallel with the resistive load, and an inductor connected in series with the parallel combination. The overall thevenin equivalent of this is then connected to the H-bridge.

The desired output of the frequency of the inverter is 60 Hz, that is,

$$f_0 = 60\ Hz\ .$$

Referencing Rashid's *Power Electronics: Devices, Circuits, and Applications,* the concept of quality factor, Q is described. This factor can be used in calculations for the various filter components of the inverter. From [5]:

$$Q = \frac{V_{Lp}}{V_{Lp(fund)}}\ ,$$

where V_{Lp} is the peak voltage across the load, and $V_{Lp(fund)}$ is the peak of the fundamental voltage component across the load.

From [6], a formulation for the inductance and capacitance values for the LC filter of a three-phase PV inverter can be given as:

$$L_f = \frac{0.1V^2}{2\pi f_0 P}$$

and

$$C_f = \frac{0.05P}{2\pi f_0 V^2}$$

A quality factor, Q, of 1.07 was calculated using results from the simulation. Values of L_f and C_f were calculated to be 76 mH and 46 μF, respectively. Although no breakers were used throughout the simulation, in practice, breakers would be installed to provide layers of protection for devices that could be affected by a short circuit or arc flash.

Another possible mode of protection to prevent the MOSFETs from malfunctioning is to set a limit on the values of change in current and voltage per time, or $\frac{dv}{dt}$ and $\frac{di}{dt}$ limits. This can be accomplished via a snubber circuit, which can include multiple resistors and inductors and a capacitor. Complex snubber circuits utilize these passive components to introduce convergences within the turn on $\frac{di}{dt}$ value and turn off $\frac{dv}{dt}$ value. The RLC circuit is typically made to be critically damped to decrease effects of oscillations. With complex snubber circuits, resistors can also be placed across the main capacitor to avoid the capacitor from discharging across the MOSFET. In the team's simulation, the chosen universal bridge utilizes a simple RC snubber in parallel with each switching device.

A. *Conduction Losses*

According to [7], the average value of the conduction losses for a power MOSFET, denoted as $P_{C,M}$, can be calculated utilizing the following equation:

$$P_{C,M} = R_{DS,on} * I_{D,rms}{}^2$$

Thus, referencing the datasheet for the selected Mouser SiC Power MOSFET [4], the conduction losses for the 4 MOSFETs utilized in the H-bridge can be computed as shown below, ensuring to account for current division on input current into the H-bridge:

$$P_{ave,conduction} = (\frac{I_{max}}{2})^2 * R_{ds,on}$$

$$= (\frac{155.38}{2}\ A) * (25\ m\Omega) = 150.89\ W$$

This value will later be used in the thermal characterization of the device, and motivate the selection of a heatsink.

B. *Switching Losses*

In addition to conduction losses, switching losses are also prevalent in the circuit. The MOSFETs used incur losses due to the nonlinearities present during the mode switching. A reference document was used to aid in the calculations of switching losses for MOSFETs, [7]. Utilizing the datasheets from the solar modules and MOSFETs used, the information required to calculate energy lost during switching can be observed via graphs and tables. The first step in the process is to analyze the Gate Charge Characteristic graph (Fig. 2), which details the relationship between gate charge and gate-source voltage. Using the graph, the plateau voltage can be seen to hold a value of 10 V ($V_{plateau}$).

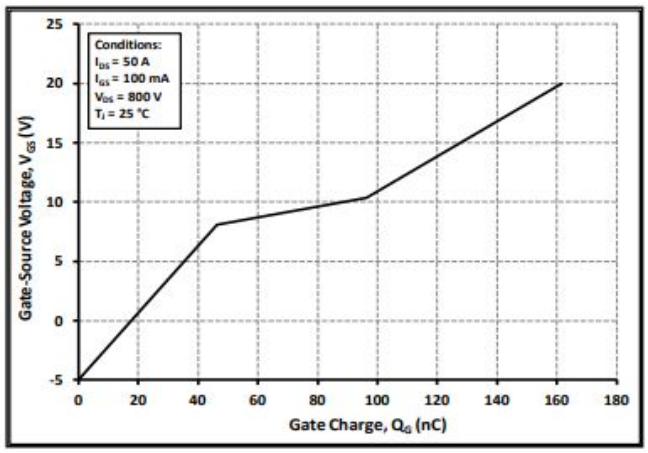

Fig. 2: Gate Charge Characteristic

Due to the Miller effect, the drive voltage must be taken at a higher value than that in the plateau region, taken as 13 V (V_{Dr}) which is used to turn on the MOSFET [7]. The next step is to take note of the gate resistance from the MOSFET datasheet (R_g = 1.1Ω) and then calculate the gate currents during rise and fall times:

$$I_{G,on} = \frac{V_{Dr} - V_{plateau}}{R_g} = 2.73A\ ,$$

$$I_{G,off} = \frac{-V_{plateau}}{R_g} = -9.1A\ .$$

Following the gate current calculations, the time it takes for the voltage needs to be calculated. To start this calculation, the capacitance needs to be observed from the graphs that plot capacitance vs drain-source voltage (Figure 3). Follow the graph given the supply voltage of 150 V and find that the capacitance value (C_{rss}) is 25 pF. Half of the supply voltage produces capacitance (C_{oss}) of around 550 pF.

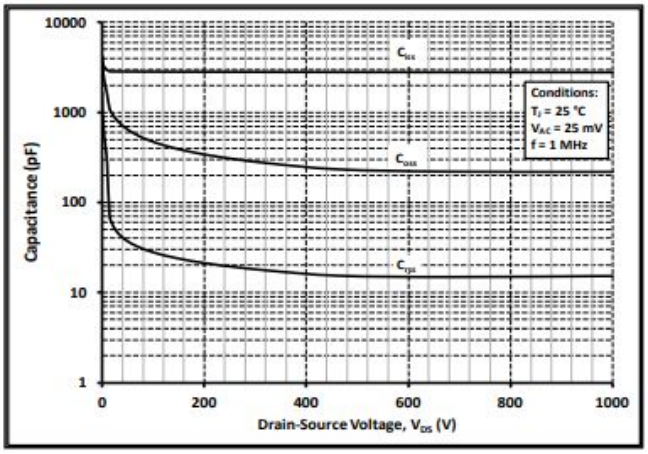

Fig. 3: Capacitances vs Drain-Source Voltage

After observing the capacitance values, the times it takes for the voltages to drop and rise along with corresponding averages are calculated:

$$t_{OFFv,1} = (V_{DD} - R_{DS,on} * I_{D,on}) * \frac{25\,pF}{I_{G,on}} = 13.63\ ns\ ,$$

$$t_{OFFv,2} = (V_{DD} - R_{DS,on} * I_{D,on}) * \frac{550\,pF}{I_{G,on}} = 214.23\ ns\ ,$$

$$t_{OFFv,avg} = \frac{t_{OFFv,1} + t_{OFFv,2}}{2} = 115.43\ ns\ ,$$

$$t_{ONv,1} = (V_{DD} - R_{DS,on} * I_{D,on}) * \frac{25\,pF}{I_{G,off}} = 4.09\ ns\ ,$$

$$t_{ONv,2} = (V_{DD} - R_{DS,on} * I_{D,on}) * \frac{550\,pF}{I_{G,off}} = 64.29\ ns\ ,$$

$$t_{ONv,avg} = \frac{t_{ONv,1} + t_{ONv,2}}{2} = 34.19\ ns\ .$$

Due to the fact that the current fall and rise times are included in the datasheet, they do not need to be re-calculated. After gathering the corresponding times, losses from switching need to be calculated. The equations used below are gathered from [7].

$$E_{loss,on} = V_{DD} * I_{D,on} * \frac{(i\ rise\ time) + (v\ fall\ time)}{2} + Q_{rr} * V_{DD},$$

$$= 131.23\ \mu J\ ,$$

$$E_{loss,off} = V_{DD} * I_{D,off} * \frac{(i\ fall\ time) + (v\ risel\ time)}{2} = 1.3\ pJ\ .$$

Due to the built-in freewheeling diode in the MOSFET, some losses will need to be estimated and included into the overall switching losses within the circuit. The equation for total power losses due to switching is as follows:

$$(E_{loss,on} + E_{loss,off}) * f_{sw} + \tfrac{1}{4} * Q_{rr} * V_{DD} * f_{sw}\ .$$

Following these calculations, a conservative estimate for switching losses from the inverter are around 24.6 W.

C. *Thermal Characterization*

Generally, the goal of the heatsink design is to limit the thermal impedance from the junction of the device to the ambient air. Therefore, the selection of a heatsink onto which the device will be mounted is primarily dependent on the thermal impedance of the sink to the ambient air, $R_{\theta sa}$. In order to analyze the thermal characteristics of the overall device, a "thermal circuit" can be created with thermal impedances supplied by the average power of the system to find the thermal impedance between the case and the ambient air. After finding the case to ambient thermal impedance, this along with other various parameters can be utilized to find a suitable commercially available heat sink.

By referring to the specification sheet of the selected Mouser C2M0025120D SiC Power MOSFET [4], the upper limit of the thermal impedance from the sink to the ambient air can be estimated with the equations and corresponding parameters as follows:

The overall temperature at the junction is given as:

$$T_J = P_{ave}(R_{\theta cs} + R_{\theta sa} + R_{\theta jc}) + T_A$$

Therefore, the upper limit of the thermal impedance from the sink to the ambient air can be given as:

$$R_{\theta sa} < \frac{T_J - T_a}{P_{avg}} - R_{\theta cs} - R_{\theta jc}\ ,$$

$$where\ R_{\theta cs,max} = 0.27\frac{^\circ C}{W}\ ,\ T_J = 150\ ^\circ C,\ T_A = 40\ ^\circ C,$$
$$and\ R_{\theta jc} \approx 0.075\frac{^\circ C}{W}$$

The average power dissipated in an active component, P_{avg}, such as that experienced by the SiC power MOSFET selected by the team, is given by the sum of the average conduction losses and average switching losses.

To estimate the "worst case" P_{avg} value experienced by one of the team's selected Power MOSFETs, the worst case values for the conduction and switching losses computed in sections A and C are utilized:

$$P_{ave} = P_{ave,conduction} + P_{ave,switching}$$
$$= 150.89\ W + 24.6\ W = 175.49\ W$$

Thus, the upper limit of the thermal impedance from the sink to the ambient air can be calculated as follows:

$$R_{\theta sa} < \frac{T_J - T_a}{P_{avg}} - R_{\theta cs,max} - R_{\theta jc}$$
$$\Rightarrow R_{\theta sa} < 0.2818\frac{^\circ C}{W}$$

Given this limit, the team sought a heatsink that stayed below this thermal impedance limit even in the "worst case" thermal impedance of the heatsink itself. A heatsink that meets this constraints was identified, specifically the Fischer Elektronik LA 6/100 12V, [8], which was deemed favorable by the team due to its compact construction, and its ability to retain a thermal impedance less than $R_{\theta sa} = 0.2818\ ^\circ C/W$, and is relatively simple in cooling operation, utilizing a fan and forced air.

Thus, using the upper limit of $R_{\theta sa}$ calculated previously, the total thermal impedance of the packaged inverter, that is, the overall thermal impedance from the junction to the ambient air, in the worst case, can be calculated as:

$$R_\theta = R_{\theta jc} + R_{\theta cs} + R_{\theta sa}$$
$$= 0.075\frac{^\circ C}{W} + 0.27\frac{^\circ C}{W} + 0.2818\frac{^\circ C}{W} = 0.6268\frac{^\circ C}{W}$$

IV. PACKAGING ARRANGEMENT

Throughout the device selection process, design phase of the inverter, and thermal calculations, the physical container for the circuit was considered. The circuit will be mounted on an insulating material and put into an aluminum housing. The housing could include small fins on the outer layer of the aluminum box to help with radiating heat as well as the heat sinks and their fans. Other possibilities for packaging could include liquid cooling and further improvements on the forced air ventilation.

The overall packaging architecture of the inverter is crucial to its longevity. If not properly cooled and maintained, the devices within will likely burn up, or at least dramatically shorten their lifetime. Choosing equipment that is rated to withstand well above given thermal characteristics is essential and will save money in the long run, as devices will last longer.

V. DRIVE CIRCUIT AND CONTROL

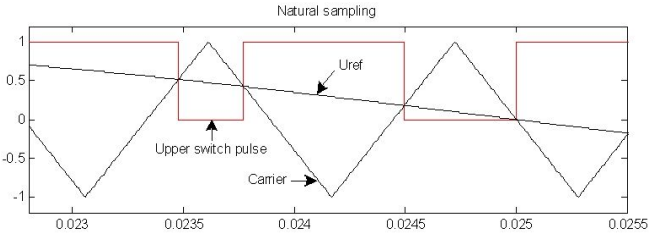

Fig. 4: Two-level PWM example in Natural Sampling mode [9]

The team utilizes a two-level pulse width modulation (PWM) scheme to drive the inverter, simulating it using the two-level PWM generator available in Simulink. This technique utilizes a sinusoidal sawtooth carrier signal, which is compared against a reference signal U_{ref}, also called a modulating signal. When the reference signal value is greater than the carrier, the pulse for the upper switching device is logic high, and the pulse for the lower switching device is logic low [9]. This is summarized in Figure 4.

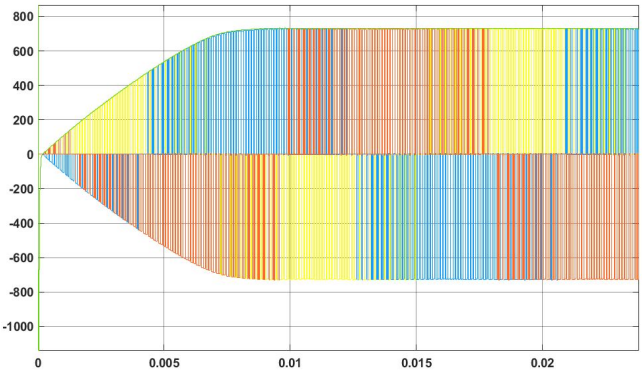

Fig. 5: Pulse width modulated phase-to-phase inverter output voltage waveforms before filtering (Red, Blue, Yellow). Input PV voltage envelope shown in green.

A challenge arose in designing the PWM scheme for the inverter regarding how to properly modify the two level PWM reference voltage when the load experienced by the inverter changes. As a solution, the team implemented a three-stage closed-loop control scheme to ensure accurate operation of the PWM scheme regardless of the load.

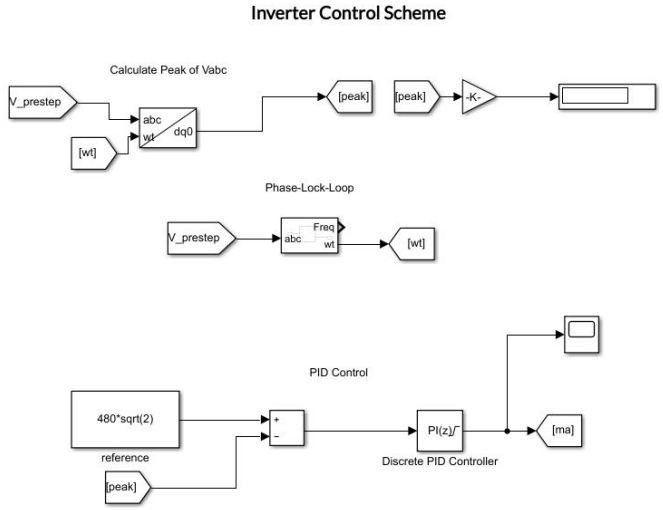

Fig. 6: Topology of the team's inverter PWM control scheme

The three stages of the team's control scheme can be summarized as follows, which are depicted in Fig. 6:

1. The measured three-phase output voltage of the inverter V_{abc} is fed into a Phase-Lock-Loop to extract the current value of ωt.
2. The PLL-calculated value of ωt and the three-phase output voltage signal V_{abc} are input into a Park Transformation in order to calculate the peak value of the three-phase output voltage [10].
3. The extracted peak value of the three-phase output voltage is subtracted from the desired "reference" peak value of the three-phase output voltage. This difference is fed into a PID controller.
    a. The output of the PID controller is multiplied by a "dummy" three-phase waveform with magnitude 1 and 120 degrees apart to form the new three-phase reference voltage for the PWM generator.

The resultant three-phase U_{ref} signal is then fed into the PWM generator, and the above control process is repeated iteratively at every time step. Favorable results were observed with this control scheme, generating the desired output waveforms while within rated load constraints, with an overall favorable total harmonic distortion of less than 5%, with the nominal load of 80 kW yielding a THD of approximately 1.8%.

VI. DISCUSSION

Some common industry practices used in the design of grid-tie inverters that were not utilized in the team's final model were researched, to be considered for utilization in future work. Chief among these is Maximum Power Point Tracking (MPPT).

In short, an MPPT device, which is essentially a microcontroller, attempts to keep the PV panels operating at the point on their i-v curves such that maximum power is generated. This is an optimizing technique that ensures the full capability of the PV array is being utilized. Finding this operation point requires extensive sensor schemes, and an algorithmic controller that increases operating voltage and decreases operating current, or vice versa, and a corresponding closed loop control system that iteratively produces these changes.

Additionally, the team determined that, if and when Las Cruces, NM allows net metering, this PV inverter would need the addition of a "**DC Gain Stage**" in order to assist with grid-tie operations.

VII. RESULTS AND CONCLUSION

The team's model was simulated for three different loads that could realistically be encountered by the inverter during a year of operation of the Corbett Student Union PV system. The results of the three simulated loads are summarized below in Table 1, and are explained further throughout the section.

Table 1: Summary of Simulation Results For All Loads

Load per phase	$P_{i,3\phi}$	$P_{o,3\phi}$	η	THD_{avg}
40 kW	67.72 kW	57.15 kW	84.39%	1.78%
80 kW (rated)	119.84 kW	100.5 kW	83.86%	1.75%
100 kW	135.97 kW	112.85 kW	82.99%	1.76%

A. Rated Load

Accounting for the single phase nature of the PV source, the total three-phase input power than can be delivered by the portion of the Corbett Center Student Union PV system simulated was found to be:

$$P_{i,3\phi} = \sqrt{3} V_{pv} I_{pv} pf = 119.84\ kW$$

On the rated **per-phase** load of 80 kW, the measured **three-phase** power dissipated was simulated as 100.5 kW, yielding an efficiency of:

$$\eta = \frac{P_o}{P_i} * 100 = 83.86\%$$

Additionally, the total harmonic distortion per phase was measured as:

$$THD_A = 1.733\%\ ,\ THD_B = 1.760\%\ ,\ THD_C = 1.756\%$$

All of which fall below the grid interconnection standard for THD specified by IEEE Standard 519, which limits harmonic voltage distortion on power systems to 3%. The average phase THD is given by:

$$THD_{avg} = \frac{THD_A + THD_B + THD_C}{3} = 1.750\%$$

Figure 7, below, depicts various outputs at the start of the simulation for the per-phase load of 80 kW. Note that the presence of a "**settling time**" for the PID controller produces unacceptable harmonics for approximately nine millisecond during startup time as the PV voltage responds. Future research is needed to determine how to reduce this spike in harmonics.

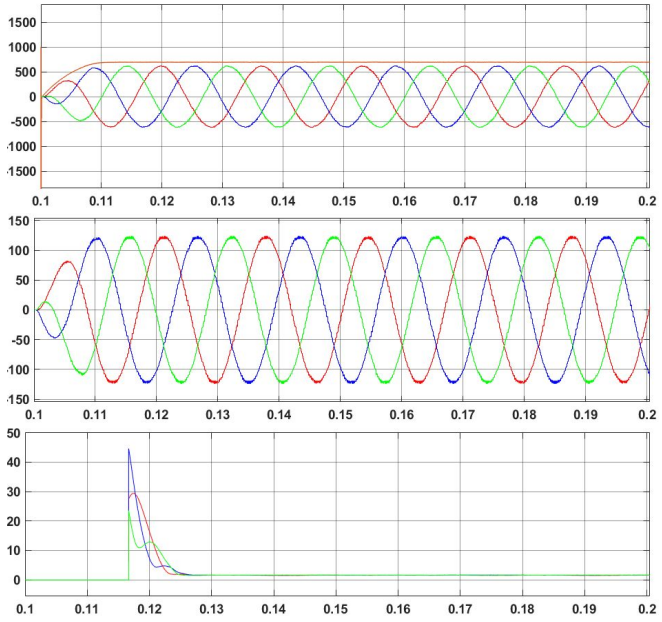

Fig. 7: 80 kW per-phase loading results. All plots versus time. From top top bottom: 1. Phase-to-phase output voltages of the inverter after step-up transformer (Red, Blue, Green) and the PV voltage (Orange) 2. Output phase currents of the inverter 3. THD values of the phase-to-phase output voltages.

B. Heavy Load

A "heavy" load of 100 kW **per-phase** was simulated to observe the effects of exceeding the rated per-phase load of 80 kW. From the simulation, the total three-phase input power was found to be:

$$P_{i,3\phi} = \sqrt{3} V_{pv} I_{pv} pf = 135.97\ kW$$

At a per-phase load of 100 kW, the measured three-phase power dissipated was simulated as 112.85 kW, yielding an efficiency of:

$$\eta = \frac{P_o}{P_i} * 100 = 82.99\%$$

Additionally, the total harmonic distortion per phase was measured as:

$$THD_A = 1.811\%\ ,\ THD_B = 1.780\%\ ,\ THD_C = 1.66\%$$

Yielding an average THD of 1.76%. The output graphs for this simulation are shown below in Figure 8.

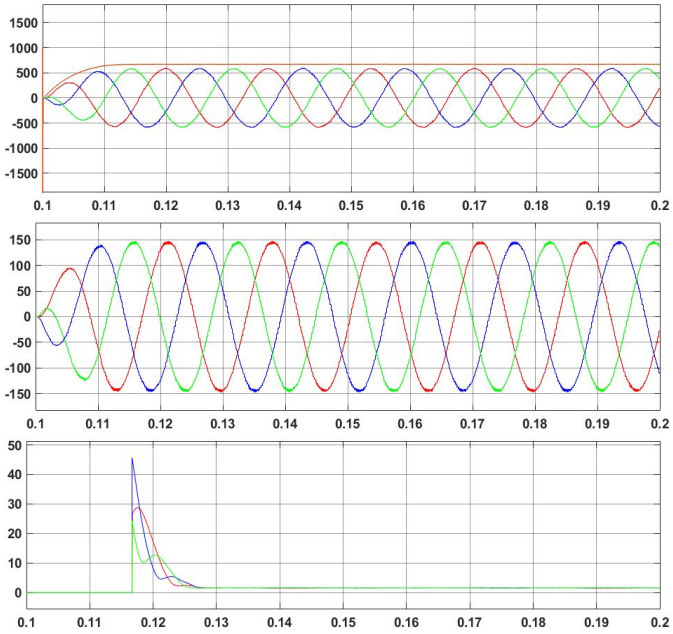

Fig. 8: 100 kW per-phase load results. All plots versus time. From top top bottom: 1. Phase-to-phase output voltages of the inverter after step-up transformer (Red, Blue, Green) and the PV voltage (Orange) 2. Output phase currents of the inverter 3. THD values of the phase-to-phase output voltages.

C. Light Load

A "light" load of 40 kW **per-phase** was simulated to observe the effects of a load below the rated per-phase load of 80 kW. A practical example of such a load could be nighttime operation. From the simulation, the total three-phase input power was found to be:

$$P_{i,3\phi} = \sqrt{3} V_{pv} I_{pv} pf = 67.7\ kW$$

At a per-phase load of 40 kW, the measured three-phase power dissipated was simulated as 57.15 kW, yielding an efficiency of:

$$\eta = \frac{P_o}{P_i} * 100 = 84.39\%$$

Additionally, the total harmonic distortion per phase was measured as:

$$THD_A = 1.778\%\ ,\ THD_B = 1.791\%\ ,\ THD_C = 1.790\%$$

Yielding an average THD of 1.78%. The output graphs for this simulation are shown below in Figure 9.

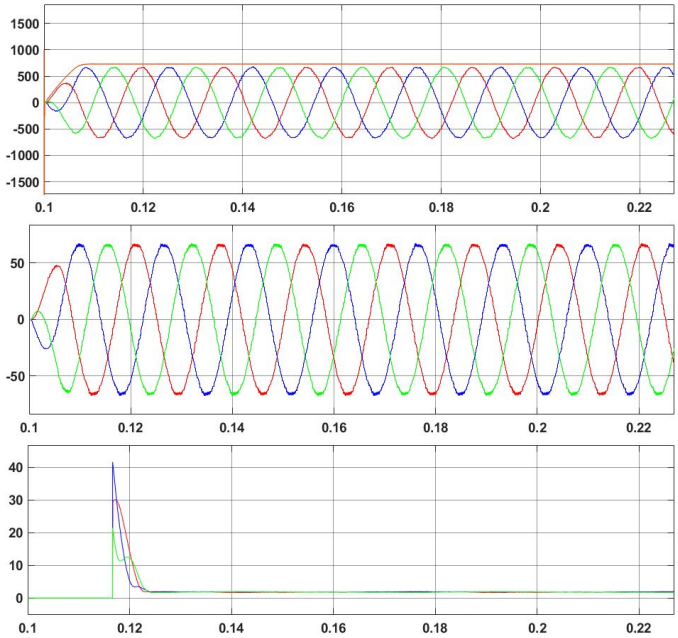

Fig. 9: 40 kW per-phase load results. All plots versus time. From top top bottom: 1. Phase-to-phase output voltages of the inverter after step-up transformer (Red, Blue, Green) and the PV voltage (Orange) 2. Output phase currents of the inverter 3. THD values of the phase-to-phase output voltages.

Some remarks regarding the results of the simulations can be made. As expected, an increase in load resulted in a proportional increase in the magnitude of drawn output current.

In regards to output voltage, as the load approached the rated values of the panels, some voltage regulation challenges were encountered. Specifically, the magnitude of the output voltage began to very slightly decrease as the load approached the rated value, and was unable to be perfectly regulated to grid voltage by the control system. The team hypothesized that this was likely due to non-linear losses incurred due to the filter components, or a need for improvements in the control system. The importance of this was further verified by additional research by the team that found, according to [11], that modern "high-quality" sine wave PV inverters typically possess efficiencies of around 90-95%. Inverters deemed of lower quality were said to have efficiencies of approximately 75-85% [11].

Preliminary calculations were performed to attempt to quantify the unexplained non-linear losses observed in the simulation. Using the calculated efficiencies for the 80 kW and 100 kW per phase loads, η_{80} and η_{100}, the non-linear losses due to the filter and reactive components of the H-bridge were attempted to be calculated as:

$$\frac{loss}{dec} = \frac{\eta_{80} - \eta_{100}}{dec^{-1}} * 100, \; where\ dec = log(\frac{80}{100})$$

$$= (83.86 - 82.99) * 0.0969 * 100 = 8.5\% \frac{loss}{dec}$$

In conclusion, this project was instrumental in introducing the team to the iterative process of designing power electronic systems. Not only was it a phenomenal learning experience, but it also exposed the team to the breadth and depth of design considerations and problems that are encountered throughout the design and modeling of a grid-tie photovoltaic inverter.

VIII. REFERENCES

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IX. APPENDIX

- Corey Buchanan: Simulink model, device research and selection, heatsink calculations, control theory, LC filter and calculations, loss calculations and protections research
- Samuel Talkington: Simulink model, circuit topology, device research and selection, MPPT research, PWM design, loss calculations, control theory, control system design, LC filter calculations, and troubleshooting