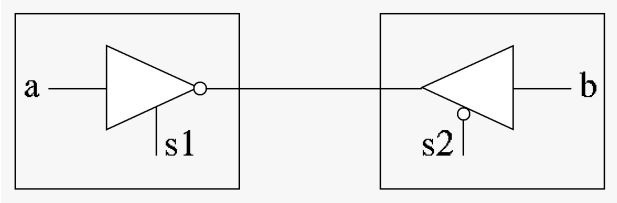
Exam 1

Remember ::

A. **Once you hit "submit" you CANNOT return to the exam.** So you should hit "submit" only when you are sure you are done.
   - **Your exam will auto-submit at 9:00pm**
B. **For each question, there is an empty text box right below it, for you to mention HOW/WHY you got/chose the answer, and provide the reasoning you used to get your answer. If you do not mention HOW/WHY you got/chose your answer, you WILL lose points.**
   - **If you give me more than one WHY/HOW for the same question, I will grade all your answers, and score your points for the answer which obtained the least points**
C. Questions marked [749 only]
   - ECEN 449 students: DO NOT answer these questions. You will receive these points for free if you attempt the exam.
   - ECEN 749 students: You MUST answer these questions.
D. TOTAL POINTS are 125 points for both ECEN 449 and ECEN 749 students
E. ————————————————————Some constants/notation.
   ————————————————————
   A. 1 millisecond = 10^{-3} sec
   B. 1 microsecond = 10^{-6} sec
   C. 1 nanosecond = 10^{-9} sec
   D. 1 picosecond = 10^{-12} sec
   E. 1 byte = 8 bits
   F. 1 kilobyte = 10^{3} byte
   G. 1 megabyte = 10^{6} byte
   H. 1 gigabyte = 10^{9} byte
   I. 1 cm = 10^{-2} m
   J. The speed of light is c = 3 x 10^{8} m/s
   K. Use "**abar**" to refer to the complement of logical variable "**a**"

1 Essay 15 points Question

Consider the circuit shown below. It consists of two built-in Verilog gates. The output of the gate on the left is connected to the output of the gate on the right.



a) What is the name of the built-in gate on the left?
b) What is the name of the built-in gate on the right?
c) Assuming that the signals s1, s2, a and b can have their values selected from the set {0, 1, X}, where "X" refers to the "don't care" condition. Write down all (s1, s2, a, b) values, one per line, that will not cause the circuit to be damaged electrically. Type your answer in the text box below.

For example if you think that (s1, s2, a, b) = 0 0 1 1 and 1 X X 1 will not cause the circuit to be damaged, you would write your answer as:
0 0 1 1
1 X X 1

a) notif1 (output is inverting. control input is not inverting)
b) bufif0 (output is not inverting, control input is inverting)
c) electrical damage occurs if both buffers are driving, and their values are different

No damage if
0 x x x // notif1 is hiZ
x 1 x x // bufif1 is hiZ
1 0 0 1 // both drive same value (1)
1 0 1 0 // both drive same value (0)

2 File Upload 20 points Question

This question type cannot be printed

I am designing the Verilog code for a microprocessor that I would like to design. Assume that I have following Verilog code fragment in my design. The idea is that the software programmer who is using the microprocessor (once the manufacturer is fabricated and sold) will provide the variable k.

```
for (i = 0; i < k; i = i + 1) begin
   not inv[i]  (x[i+1], x[i]);
end
```

Draw the circuit that is realized when the above code is synthesized, and upload your answer in the answer box below.

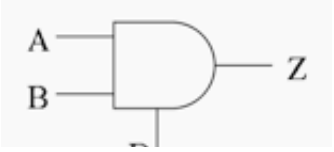
Drag n' Drop here or Browse

Cant synthesize a varrable k on-demand. Hardware can only have a fixed number of inverters, cant make up k inverters as the software demands. So, this verilog cant be synthesized.

3 File Upload 25 points Question

This question type cannot be printed

Suppose I have an AND gate G with two inputs A and B, and an output Z. This AND gate has a delay 10 when a third input D is 1, and a delay of 20 when D is 0. The only purpose that input D serves is to change the delay of the AND gate G.
I have a circuit S which uses one or more instances of G. I would like to perform event driven timing simulation (EDTS) on this circuit S. Clearly EDTS, as we studied in class, does not handle gates with variable delays like G.
I propose to fix this issue by converting gate G into a new circuit G*, and replacing every occurrence of G in S by G*. With this change, EDTS (as we studied in class) will work seamlessly without any changes.
I have shown a cartoon of gate G below. Derive a circuit G* (with the same inputs, outputs and logical/timing behavior as G). Draw your circuit G*, take a picture of it, and upload it as your answer.



D

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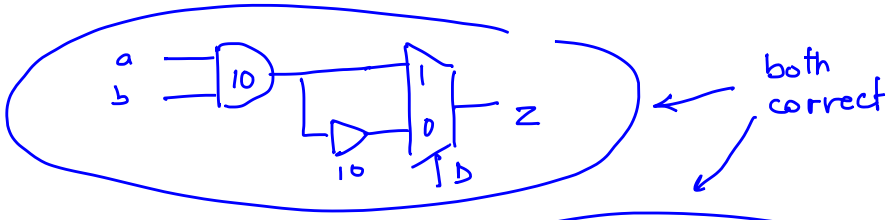
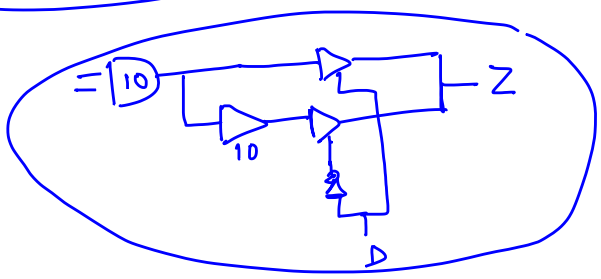


4 Essay 10 points Question



Suppose that C = 5'b010X0.
A) What is the result of ^c,
B) What is the result of |c,
C) What is the result of ^(c >> 2)
Type your answer into the text box below.

If you check the Verilog notes (page 45 & beyond) you will find this material there...

These are unary (one operand) operators. They perform the operation on the bits of the operand.

a) ^c = 0^1^0^x^0 = x

c)
b) |c = 0|1|0|x|0 = 1

c>>2 = 00010

^(c>>2) = 0^0^0^1^0 = 1

5 Essay 15 points Question

Consider my desktop computer. It has a latency of 10^7 clock cycles when data is accessed from the Hard Disk Drive (HDD). It takes a latency of 200 clock cycles to access data from the DRAM (if the data is present in DRAM). If the data is not present in the DRAM, the DRAM sends back a signal "DRAM-miss" (after 200 cycles) indicating that it does not have the data. It takes a latency of 1 clock cycle to access data from the cache (if the data is present in the cache). If the data is not present in the cache, the cache

sends back a signal “Cache-miss” (in 1 cycle) indicating that it does not have the data. When I use the word “latency”, I refer to the quantity t2 - t1, where t2 is the time when the requested data arrives at the CPU, and t1 is the time when the data request is issued by the CPU. The clock frequency of the CPU in my desktop computer is 2 GHz.

Suppose I am executing a program P, which requests data from the memory system.

A) Program P first requests data from the cache. What is the latency (in seconds) incurred if the data is present in the cache?

B) If the data is not found in the cache, program P next requests the data from the DRAM. What is the cumulative latency (in seconds) incurred if the data is not present in cache, but present in the DRAM?

C) If the data is not found in the DRAM, program P requests the data from the HDD. What is the cumulative latency (in seconds) incurred if the data is not present in the cache and DRAM, but is present in the HDD?

Type your answers into the text box below.

Clock period: $\frac{1}{F} = \frac{1}{2\times10^9} = 5\times10^{-10}$ sec

a) 1 cycle : so $1 \times 5\times10^{-10}$ sec

b) 1 cycle + 200 cycle = $201 \times 5\times10^{-10}$ sec
(cache miss) (dram access) $= 1.005\times10^{-7}$ sec

c) $1 + 200 + 10^7$ cycles $= (10^7+200+1)\times 5\times10^{-10}$ sec
$= 5.0001005\times10^{-3}$ sec

(note @ the end of 1(200) cycles I have the data from the cache (DRAM) or the miss indication)

6 Essay 15 points Question

I have two programs that I am considering for hardware acceleration using an FPGA board.

The first program is Microsoft Word. The serial portion of this code takes up 94% of the runtime. The remaining 6% of the code is parallelizable. When I accelerate the parallelizable code on the FPGA, I get a speedup of 30X.

The second program is Vivado. It has about 80% of the code which can be parallelized, and 20% of the code is serial in nature. When I accelerate the parallelizable code on the FPGA, I get a speedup of 40X.

A) What is the overall speedup that I obtain for Microsoft Word if I accelerate it on an FPGA?

B) What is the overall speedup that I obtain for Vivado if I accelerate it on an FPGA?

Type your answers into the text box below.

speedup = old runtime / new runtime = $\frac{S+P}{S+P/F}$

where S = serial part runtime
P = parallelizable part runtime
F = speedup factor

A) speedup = $\frac{100}{94+6/30} = \frac{100}{94.2} = 1.0615$

B) speedup = $\frac{100}{20+80/40} = \frac{100}{22} = 4.5454$

7 Essay 25 points Question

<<< [749 question] >>> <<< [749 question] >>> <<< [749 question] >>> <<< [749 question] >>>
Consider a digital circuit S which consists of a total of N gates. The fanout of a gate G is defined as the set of gates $\{h_i\}$ which the output of G drives. In a circuit S, assume that on average, any gate has F gates in its fanout. Also assume that during any clock cycle, a fraction A of the gates of S have events on them.
A) When performing event driven timing simulation (EDTS) on circuit S, how many new rows (on average) are generated in the event table, for every clock cycle?
B) How many of the rows in part A (on average) are such that the corresponding gate for that row has the same logic value at t+ and at t-?
Type your answers into the text box below.

a) number of gates w/ events every cycle = NA
each event gets propagated to F other gates
Number of rows created in EDTS table
= NAF

b) But we know that there are statistically NA events every cycle (ie NA gates with different values at t^+ & t^-)
So # rows with same value @ t^+ & t^- is
NAF − NA