HW4 - SOLUTIONS

Due No due date **Points** 0 **Questions** 6 **Time Limit** None
Allowed Attempts Unlimited

Instructions

IMPORTANT

This quiz is here so that you can see the solutions to HW4. This quiz is ungraded.

Submit an empty quiz. The solutions to HW4 will be displayed below each question when you view your attempt.

Take the Quiz Again

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	less than 1 minute	0 out of 0 *

* Some questions not yet graded

Score for this attempt: **0** out of 0 *
Submitted May 3 at 5:14pm
This attempt took less than 1 minute.

Unanswered

Question 1

Not yet graded / 0 pts

Suppose I have a DVD with 5 GB capacity. I want to store a movie on this disk. The screen is 2000 pixels wide, and 1000 pixels high. Each pixel has 8 bits to represent its red, blue, and green color intensity. Images on the screen are refreshed 60 times a second to generate the effect of a movie. How many minutes of the movie can I store on the disk?

IMPORTANT

Please follow the instruction (Description 1) for submitting your answer to the question

The number of bits in one static image is
$2000 \times 1000 \times 8 \times 3 = 48000000\ bits$.
So the bit rate is
$48000000\ bits \times 60\ Hz = 2880000000\ bits/s$.
Also, $5\ GB = 5 \times 2^{30}\ bytes = 40 \times 2^{30}\ bits$

The duration of a movie that can be stored on this DVD is
$\frac{40 \times 2^{30}\ bits}{2880000000\ bits/s} = 14.9\ s$

Note that without compression we can only store about 15 seconds of video on a DVD. This question illustrates the need to do compression for video.

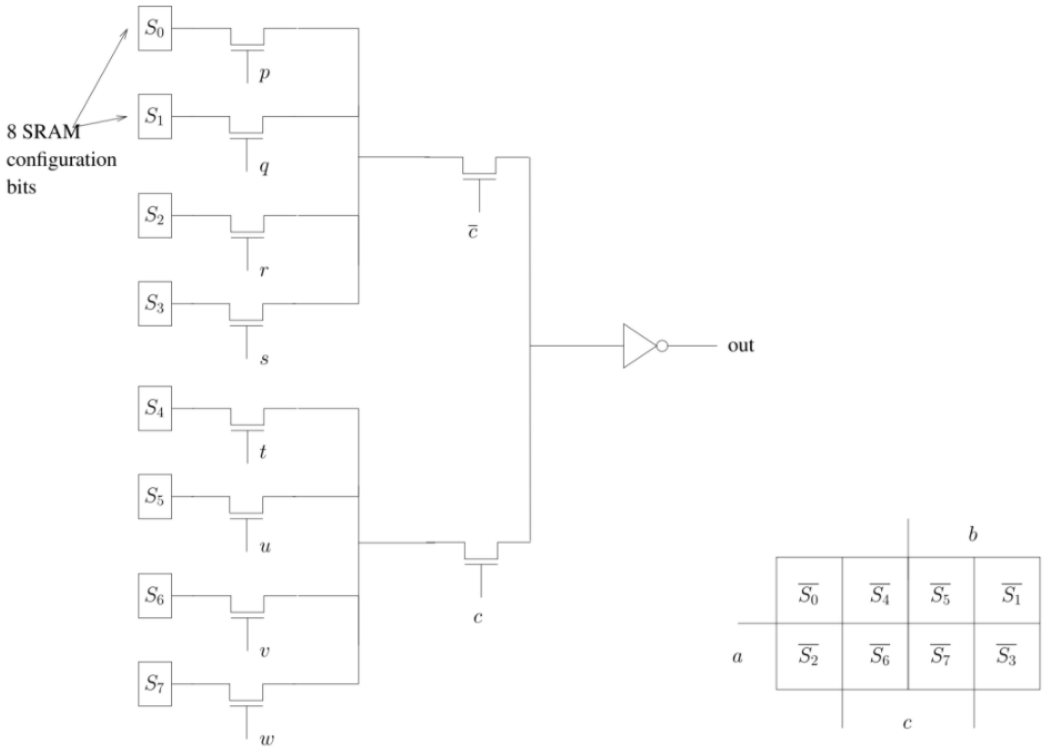
Unanswered

Question 2

Not yet graded / 0 pts

Consider the circuit drawn below (in Figure a)). I want to use it to implement a 3-input LUT, which depends on variables a, b and c. The corresponding K-map for the LUT circuit is shown beside the circuit (in

Figure b)).



A) 3−input LUT circuit b) K−map for 3−input LUT

(a)

Write down the logic functions for the gate terminal of the 8 NMOS transistors shown (these logic functions are labeled p, q, r, s, t, u, v and w in the figure).

(b)

Why is the LUT circuit shown above faster than the traditional LUT circuit which we discussed in class?

(c)

What is the disadvantage of the LUT circuit shown above, compared to the traditional LUT circuit which we discussed in class?

IMPORTANT

Please follow the instruction (Description 1) for submitting your answer to the question

(a)

Minterms of the SRAM configuration bits based on K-map:

$$\overline{S_0} = \bar{a}\bar{b}\bar{c} \quad \overline{S_1} = \bar{a}b\bar{c} \quad \overline{S_2} = a\bar{b}\bar{c} \quad \overline{S_3} = ab\bar{c}$$

$$\overline{S_4} = \bar{a}\bar{b}c \quad \overline{S_5} = \bar{a}bc \quad \overline{S_6} = a\bar{b}c \quad \overline{S_7} = abc$$

Minterms of the SRAM configuration bits based on LUT circuit:

$$\overline{S_0} = p\bar{c} \quad \overline{S_1} = q\bar{c} \quad \overline{S_2} = r\bar{c} \quad \overline{S_3} = s\bar{c}$$

$$\overline{S_4} = tc \quad \overline{S_5} = uc \quad \overline{S_6} = vc \quad \overline{S_7} = wc$$

From the K-map, $\bar{S_0} = \bar{a}\bar{b}\bar{c}$. From the LUT circuit, $\bar{S_0} = p\bar{c}$. Hence $p\bar{c} = \bar{a}\bar{b}\bar{c}$, and $p = \bar{a}\bar{b}$. From above discussion, we can write down the logical functions for the gate terminal of the 8 NMOS transistors as follows:

$$p = \bar{a}\bar{b} \quad q = \bar{a}b \quad r = a\bar{b} \quad s = ab$$

$$t = \bar{a}\bar{b} \quad u = \bar{a}b \quad v = a\bar{b} \quad w = ab$$

(b)

Assuming that p,q,r,s,t,u,v are already available, the LUT given in the question is faster than the traditional LUT because in the traditional LUT circuit, we have 3 levels of NMOS transistors to traverse, compared to 2 levels of NMOS transistors for the LUT given in the question.

(c)

The LUT given in this circuit is more complex than a traditional LUT. It consumes more area and power than the traditional LUT. This is because 4 AND gates (each requiring 6 transistors) are required to generate $\bar{a}\bar{b}, \bar{a}b, a\bar{b}, ab$.

Unanswered

Question 3

Not yet graded / 0 pts

Suppose a printed circuit board is made of a material having a relative dielectric constant κ = 4 and a characteristic impedance of 60 Ohm. The length of wire from source voltage to load is 0.2 m. Suppose the source resistance is 10 ohm and load resistance is 100 ohm.
(a) Find the velocity of wave propagation in PCB.
(b) Find the inductance (L) per unit length of wire.
(c) Find the capacitance (C) per unit length of wire

IMPORTANT
Please follow the instruction (Description 1) for submitting your answer to the question

(a) The velocity (v) of wave propagation is given by:

$v = \frac{c}{\sqrt{\kappa}} = 1.5 \cdot 10^8$ m/s

(b) The inductance (L) per unit length of the wire is given by:

$L = \frac{Z_0}{\sqrt{v}} = 4 \cdot 10^{-7}$ H/m, where Z0 is the characteristic impedance.

(c) The capacitance (C) per unit length of the wire is given by

$C = \frac{1}{vZ_0} = 0.11 \cdot 10^{-9}$ F/m

Unanswered

Question 4

Not yet graded / 0 pts

Suppose I want to transmit several full-duplex audio signals simultaneously via an optical fiber. The bandwidth of the optical fiber is 30 Gb/s and the frequency of any audio signal varies between 2 - 16 KHz. A PPM scheme is used to sample and transmit these audio signals, and the PPM scheme transmits one of 16 values per sample.

(a) What is the maximum number of simultaneous full-duplex audio signals the transmission system can support?

(b) If PCM is used to replace PPM, what is the maximum number of simultaneous full-duplex audio signals the transmission system can support now?

IMPORTANT
Please follow the instruction (Description 1) for submitting your answer to the question

(a) The maximum number of simultaneous audio signals supported will be (the total bandwidth of fiber / data rate of single audio transmission using PPM).
The data rate of single audio transmission using PPM: To effectively sample an audio signal, according to the Nyquist sampling theorem, the sampling frequency should be twice the maximum frequency of the signal. Thus sampling frequency = 2 x 16 KHz = 32 KHz. Also, the audio signals are full-duplex and transmitted using 16 PPM bits.Thus, data rate of single audio transmission using PPM = 32 KHz x 16 x 2 = 1024 Kbps.
Total bandwidth of fiber = 30 Gb/s
Hence, the maximum number of simultaneous audio signals = $\frac{(30 \cdot 10^9)}{1024000} = 29,296$

(b) If PCM is used to replace PPM, then only 4 bits are needed to represent 16 values. Thus, data rate of single audio transmission using PPM = 32 KHz x 4 x 2 = 256 Kbps.
Hence, the maximum number of simultaneous audio signals = $\frac{(30 \cdot 10^9)}{256000} = 117,187$

Unanswered

Question 5

Not yet graded / 0 pts

Consider an FPGA with 50 IO pads. Each of these IO pads can be configured as input/output/inout, and the total number of combinations of

configurations for each IO pad is 13. The FPGA consists of 250,000 4-input LUTs. The switchboxes in the FPGA contain 25 wires in the horizontal direction, and 30 wires in the vertical direction.

I use this FPGA to implement my radar signal processing algorithm. The radar processor needs 32 input pins for data, 12 output pins for the result and 6 inout pins for control information. It uses 65% of the LUTs and 79% of the switchboxes.

A) Can you suggest a reason why the switchboxes contain more wires in the vertical direction than in the horizontal direction?

B) What is the size of the bitstream for this FPGA?

C) What fraction of the bits in the bitstream for my radar signal processing algorithm are unspecified (don’t care)?

D) How many distinct bitstreams can I construct, each of which implement the radar signal processing algorithm?

IMPORTANT
Please follow the instruction (Description 1) for submitting your answer to the question

A)
There are more vertical wires because we need to connect to the LUT IOs (which use vertical wires)

B)
Size of the bitstream = 50*(ceil(log_2(13))) + (501)^2*25*30 + 500^2 * (2^4+2) +30*5*500^2

= 200 + 188.25075e6 + 4.5e6 + 37.5e6
= 230, 250, 950
= 230.2 M

The first term represents 50 IO pads, each of which have 13 ways to configure them.

The second term represents 501^2 switchboxes, each of which has 25x30 wires

The third term represents 500^2 LUTs, each of whose logic needs 2^4 bits (to program the function) and 2 bits to select tristate and sequential functionality

The fourth term represents the number if bits to connect the 5 IOs of each LUT (4 input plus 1 output) to one of 30 vertical wires, for each of 500^2 LUTs

C)
All bits that control wiring should be 0 and are not don't care. The bits that are don't care are those that are connected to logic (i.e LUTs). This means 87.5e5 LUTs * 18 bits per LUT = 1.575e6 bits. The ratio is 1.575e6/230.2e6 = 0.00684036

D)
2^(1.575e6)

Unanswered

Question 6

Not yet graded / 0 pts

[749 QUESTION]