

ECEN 449 / 749 - Microprocessor System Design

Test #2

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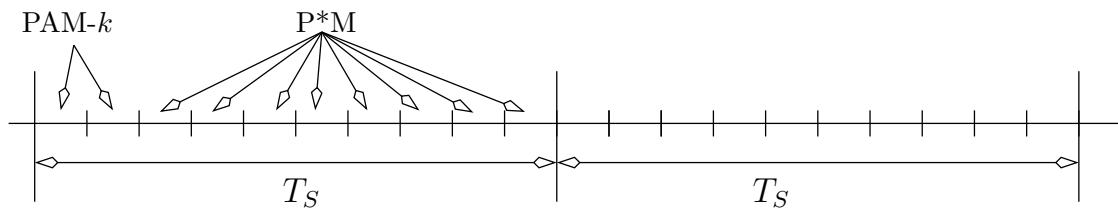
NAME:

SECTION:

Problem	749 points	449 points	Your points
Problem 1	30	30	
Problem 2	30	35	
Problem 3	40	35	
Problem 4 (Graduate)	25	0	
Total	125	100	

- For all your answers which involve Verilog code or C code, you should provide comments in your code for full credit.
- For other answers, you must provide comments about *how* you obtained the answer for full credit.
- If you give me more than one answer for the same question, I will grade all your answers, and score your points for the answer which obtained the least points.
- For a question with N points, I suggest that you budget $1.2 \times N$ minutes for it.
- Write your answers in the box provided. ANYTHING written outside the box will not be graded.
- The speed of light is $c = 3 \times 10^8$ m/s

1. You are designing a pulse modulation scheme, in which each sampling interval T_S consists of 10 equal length sub-intervals as shown below. In the first two sub-intervals, we transmit a PAM- k signal. In the last eight sub-intervals, we transmit data using any of the P*M schemes (i.e. PCM, PPM, or PWM). The P*M scheme is chosen so as to maximize the amount of information transferred. The transmitted signal can vary between 0V and 5V. The sampling interval T_S is 1 μ s.



The transmitter electronics requires that signals must be separated by at least 1V in amplitude. The receiver can resolve signals as long as they are separated by at least 1.25V in amplitude.

- (a) What is the value of k for the PAM- k signal for the first two sub-intervals?

Answer:

5

Reasoning:

- The amplitudes are 0, 1.25, 2.5, 3.75 and 5 (ie 5 amplitudes in all)
- Can't use 0, 1, 2, 3, 4, 5 since rx cannot handle this

- (b) For the data in the last 8 sub-intervals, which would you choose among PCM, PPM and PWM in order to maximize the information transferred between the transmitter and receiver?

Answer:

PCM

Reasoning:

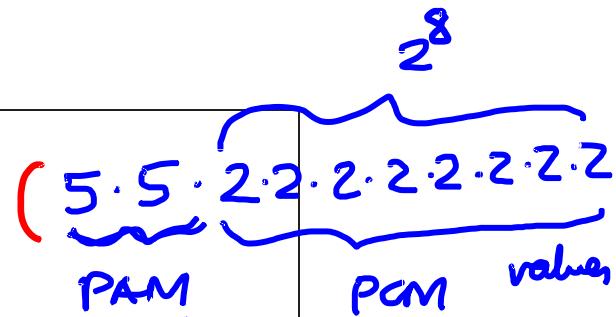
w/ 8 int. PCM can send 2^8 distinct symbols
 w/ 8 int. (PPM) 8 . . .
 and the goal was to maximize the amt of information transferred -

- (c) What is the effective amount of information transferred by your pulse modulation scheme in bits/s?

Answer:

Reasoning:

In 1 μ s, I can send



In 1 μ s I can send $\log_2(25 \cdot 2^8)$ bits

In 1 μ s I can send 12.64 bits

$$\text{info transfer rate} = \frac{12.64 \text{ b}}{1 \mu\text{s}} \in 12.64 \times 10^6 \frac{\text{b}}{\text{s}}$$

- (d) For the pulse modulation scheme above, do you require clock recovery at the receiver?

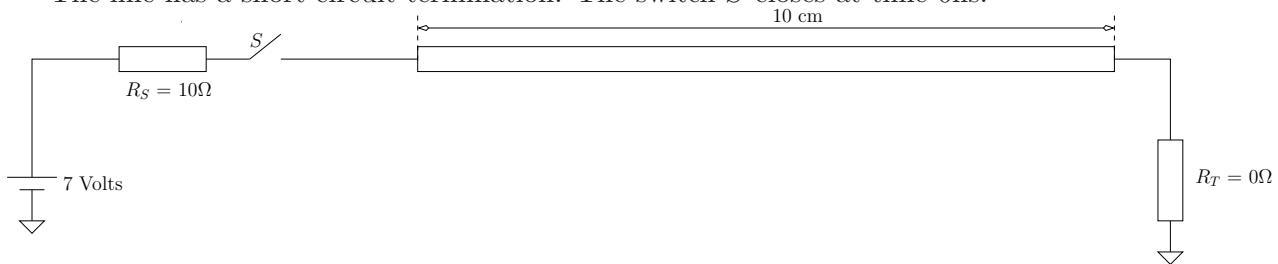
Answer:

yes

Reasoning:

Since transmitter can send 0V (or 5V) in all 10 intervals, causing receiver to lose sync.

2. Consider the circuit shown below. It represents a driver with a 10Ω impedance that drives a PCB trace of length 10cm whose $L = 5.19615 \times 10^{-7} \text{ H/m}$, and $C = 1.443375 \times 10^{-10} \text{ F/m}$. The line has a short circuit termination. The switch S closes at time 0ns.



- (a) How long does the voltage wave take to travel from the source to the destination?

Answer:

Reasoning:

$$v = \frac{1}{\sqrt{LC}} = \frac{L}{t_g} = \frac{0.1 \text{ m}}{t_g} = 1.15 \times 10^8 \text{ m/s}$$

solve for t_g (watch for units!)

- (b) What are the reflection coefficients of the source and destination ends of the wire?

$$t_g = 8.66 \times 10^{-10} \text{ sec}$$

Answer:

$$R_0 = \sqrt{\frac{L}{C}} = 60 \Omega$$

Reasoning:

$$\rho = \frac{R/R_0 - 1}{R/R_0 + 1} \quad \text{for } P_S, R = 10 \Omega \text{ (source end)}$$

$$\rho = \frac{R/R_0 - 1}{R/R_0 + 1} \quad \text{for } P_D, R = \emptyset \Omega \text{ (destination end)}$$

solve for both P_S & P_D

$$\rho_S = -0.71$$

$$\rho_D = -1$$

- (c) What is the characteristic impedance of the PCB trace?

Answer:

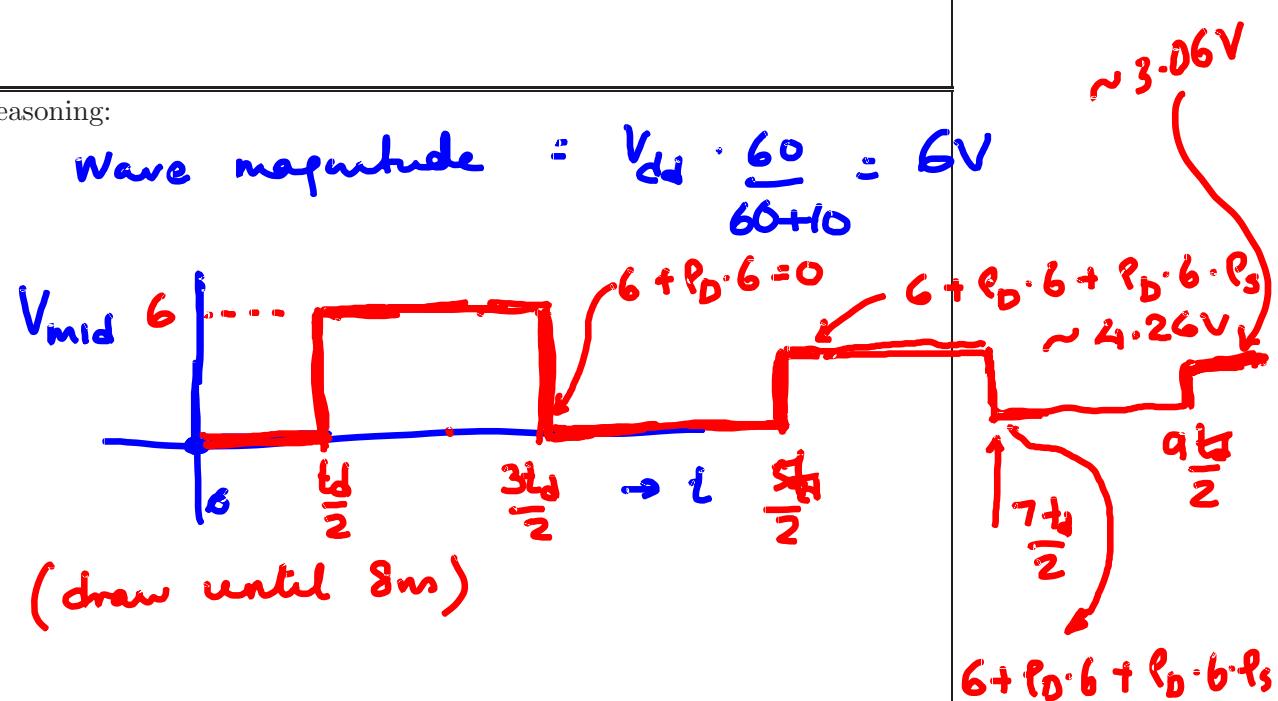
Reasoning:

$$R_0 = \sqrt{\frac{L}{C}} = 60 \Omega$$

- (d) Draw the voltage waveform at the **midpoint** of the wire from time $t = 0\text{ns}$ until $t = 8\text{ns}$.

Answer:

Reasoning:

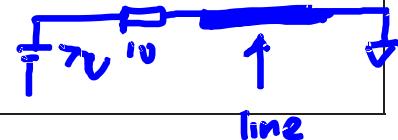


- (e) What is the value of the voltage at the midpoint of the wire at $t \rightarrow \infty$? Why? $+ \rho_i \cdot b \cdot \rho_S \cdot \rho_D = 0$

Answer:

Reasoning:

PSV. Eg. ckt @ $t = \infty$ is

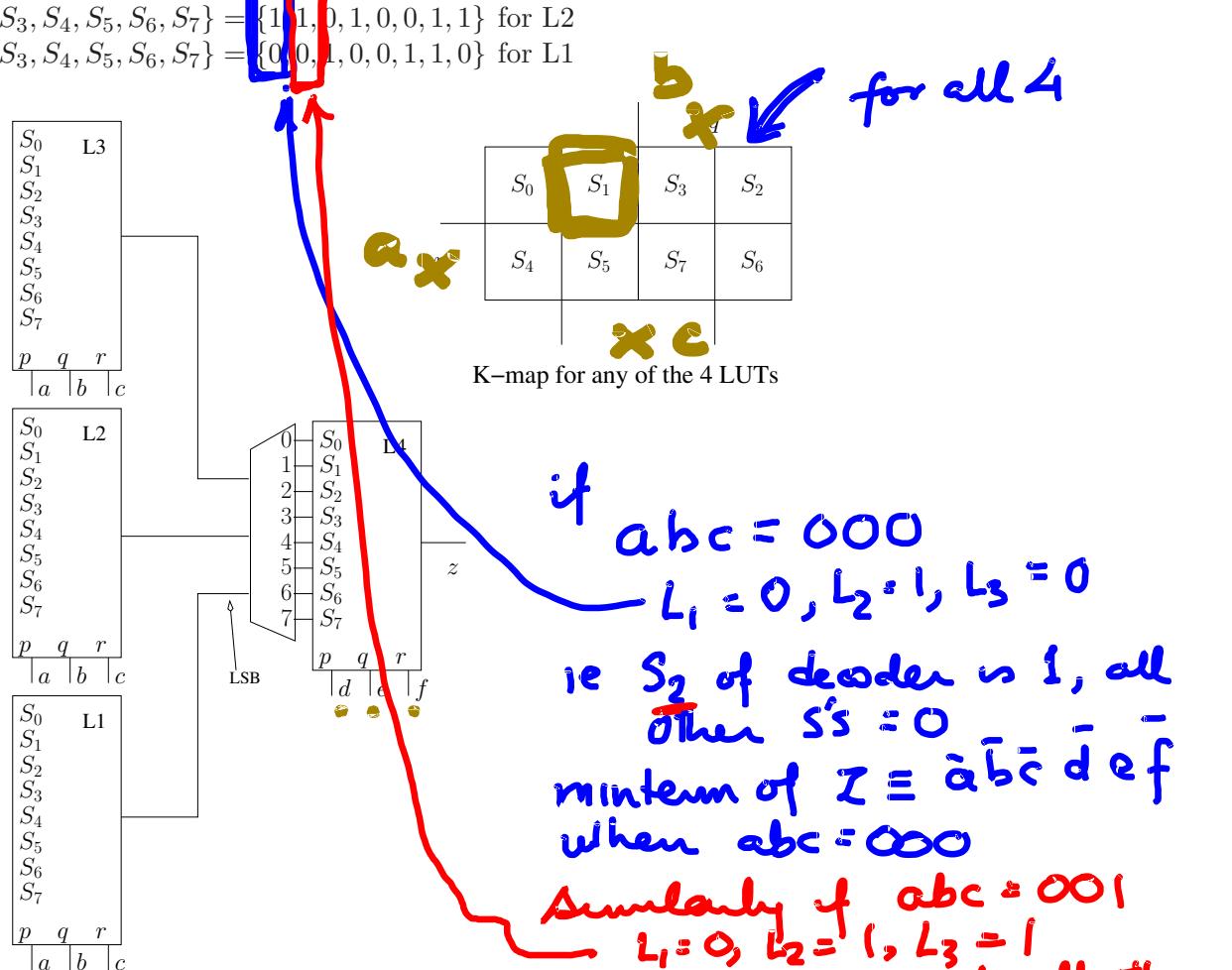


3. Consider the circuit configuration shown below. In this configuration, there are three 3-input LUTs (L1, L2 and L3), each connected to signals a , b and c . The outputs of these 3-input LUTs drive a 3-to-8 binary decoder, whose 8 outputs feed the 8 configuration bits of a 3-input LUT L4, whose inputs are connected to signals d , e , and f as illustrated. The output of LUT L4 is the signal z . The K-map of each LUT is shown at the top right of the circuit. Assume that the configuration bits for LUTs L1, L2 and L3 are respectively:

$$\{S_0, S_1, S_2, S_3, S_4, S_5, S_6, S_7\} = \{0, 1, 0, 1, 0, 1, 0, 1\} \text{ for L3}$$

$$\{S_0, S_1, S_2, S_3, S_4, S_5, S_6, S_7\} = \{1, 0, 1, 0, 1, 0, 0, 1\} \text{ for L2}$$

$$\{S_0, S_1, S_2, S_3, S_4, S_5, S_6, S_7\} = \{0, 0, 1, 0, 0, 1, 1, 0\} \text{ for L1}$$



- (a) Write down the logic function of z in the K-map below, in a sum-of-minterms form. S_i are 0.
 Do not perform logic minimization.

Answer:

$$Z = \bar{a}\bar{b}\bar{c}\bar{d}\bar{e}\bar{f} + \bar{a}\bar{b}\bar{c}d\bar{e}\bar{f} + \dots \text{ 6 more}$$

Hence $Z = 1$ only when $def = 110$,
 Hence minterm
 $\bar{a}\bar{b}\bar{c}d\bar{e}\bar{f}$

Reasoning:

- (b) How many distinct functions of six inputs can you implement on z ?

Answer:
 8^3

Reasoning:

OR
 $2^{8+8+8} = 2^{24}$
since there
one 8 Si in
each of L1, L2,
L3. Any change
in these Si
yields a new
function

for any $\langle abc \rangle$ combination [there are 8 such]
→ the $\langle l_1, l_2, l_3 \rangle$ outputs can have 8 possibilities
→ for each of these a single value of $\langle def \rangle$
produces a function of 2
→ i.e. $\langle def \rangle$ adds no additional functions
So total # fns is $\underbrace{8 \cdot 8 \cdot 8 \dots 8}_{8 \text{ times}} \quad \overbrace{\text{8 ways to select } \langle l_1 l_2 l_3 \rangle}$
8 times, for 8 values of $\langle abc \rangle$

- (c) Suppose you were to replace LUTs L1, L2, L3 and the binary encoder by a SRAM. What is the total size of the SRAM in bits? How wide is the external data bus for this SRAM? How wide is the external address bus for this SRAM?

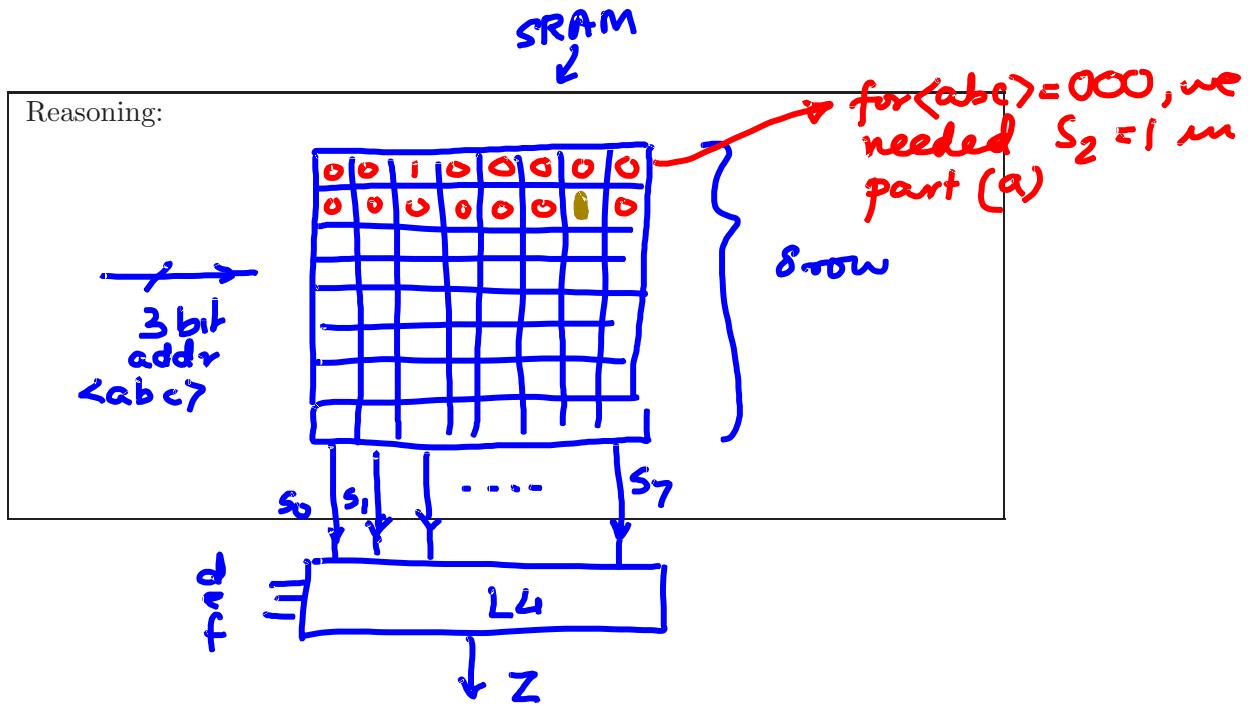
Answer: SRAM needs 8 outputs for $S_0 \dots S_7$

- # bits in the SRAM = $8 \times 8 = 64$
- data bus width = $8b$

, addr bus width = $3b$

see
next
page

Reasoning:



4. [GRADUATE QUESTION GRADUATE QUESTION GRADUATE QUESTION]

Consider a SRAM which stores a total of 2^{30} bits. The SRAM is accessed (read or written) in units of two bytes (16 bits). Each SRAM cell is 4 times as tall as it is wide.

- (a) How wide is the external address bus for the above SRAM?

Answer:

26

Reasoning:

$\frac{2^{30}}{16} = 2^{26}$ entries, each is 16b wide
Hence 26b address bus

- (b) How wide is the external data bus for the above SRAM?

Answer:

16b

Reasoning:

since we access the memory
in units of 16b

- (c) How wide is the column address bus for the above SRAM?

Answer:

12

Reasoning:

We want a square chip, width = height
Each cell is 4x taller than it is wide
Say col address is C bits. Row address is $26-C$
chip width = chip height
 $1 \times (16 \times 2^C) = 2 \times (2^{26-C}) // c+2 = 26 - C$ or
 $C = 12$

- (d) How wide is the row address bus for the above SRAM?

Answer:

14

Reasoning:

see (c)

For rough work. Will NOT be graded

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