HW3 - SOLUTIONS

Due No due date **Points** 0 **Questions** 6 **Time Limit** None
Allowed Attempts Unlimited

Instructions

IMPORTANT

This quiz is here so that you can see the solutions to HW3. This quiz is ungraded.

Submit an empty quiz. The solutions to HW3 will be displayed below each question when you view your attempt.

Take the Quiz Again

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	less than 1 minute	0 out of 0 *

* Some questions not yet graded

Score for this attempt: **0** out of 0 *
Submitted May 3 at 5:13pm
This attempt took less than 1 minute.

Unanswered

Question 1

Not yet graded / 0 pts

Write one line Linux command that performs the required action in each of the problems given below:

(a)
Find the difference in text between two text files `File1.txt` and `File2.txt`

and save the result in a file named `result.txt`

(b)
Change the permissions of the file `remote_driver.c` such that the owner has the permissions
to read, write and execute and anybody other than the owner can only read the file but cannot
write or execute.

(c)
Search for the string `ir_signal` in the file `/home/grad/remote_driver.c` and print on the terminal the number of instances of the given string in the file `/home/grad/remote_driver.c`

(d)
Reboot the system after 5 minutes.

(e)
Display the list of processes currently being run by the user `harvey`.

(f)
Print 3 copies of a file named `my_driver.c` from a printer that has a name `HPLaserJet4300`.

(g)
Put the last 40 lines of the file `driver_log.log` into a new file `final_fault.txt`.

IMPORTANT
Please follow the instruction (Description 1) for submitting your answer to the question.

(a)

```
diff File1.txt File2.txt > result.txt
```

(b)

```
chmod 744 remote_driver.c
```

(c)

```
grep -c ir_signal /home/grad/remote_driver.c
```

(d)

```
shutdown -r +5
```

(e)

```
top -u harvey
```

(f)

```
lpr -PHPLaserJet4300 -#3 my_driver.c
```

(g)

```
tail driver_log.log -n 40 > final_fault.txt
```

Unanswered

Question 2

Not yet graded / 0 pts

Suppose I have a Verilog design, which I synthesize. The resulting synthesized circuit C has exactly 200 2-input gates. Now I perform technology mapping, into an FPGA which has 6-input LUTs.

A) What is the minimum number of LUTs that will result if my circuit C has 5 primary inputs, and 1 primary output?

B) What is the maximum number of LUTs that will result if my circuit C has 5 primary inputs, and 1 primary output?

C) What is the minimum number of LUTs that will result if my circuit C has 5 primary inputs, and 5 primary outputs?

D) What is the maximum number of LUTs that will result if my circuit C has 5 primary inputs, and 5 primary outputs?

IMPORTANT
Please follow the instruction (Description 1) for submitting your answer to

the question.

A. min luts if 5in 1out = 1

B. max luts if 5in 1 out = 1

C. min luts if 5in 5out = 5

D. max luts if 5in 5out = 5

Unanswered

Question 3

Not yet graded / 0 pts

Consider the Makefile below. It resides in my software development folder, along with files x.c, y.c z.c, x.h, y.h, z.h, and w.h. All these files have a timestamp of 11:00am. There are no other files in my software development folder

```
## Makefile for my project
top: x.o y.o z.o
	cc -o top x.o y.o z.o
x.o: x.c w.h
	cc -c x.c
y.o: y.c y.h w.h
	cc -c y.c
z.o: z.c z.h w.h
	cc -c z.c
clean:
	rm -rf *.c *.h *.o
```

a) Now assume we run “make” at 11:15am. The binary **top** is created along with some other files. I test the binary and it works perfectly. I then go to lunch. What other files are created in my software development folder along with **top**?

b) Now at 1:00pm, I run “touch y.h”. I run “make” again at 1:05pm. What files are regenerated as a result of my running “make”?

c) Now at 1:10pm, I make changes to x.h, redefining some fields in a **struct** in the file, and also adding a new **struct**. I run “make” again at 1:14pm. What files are regenerated as a result of my running “make”?

d) After running “make” in the last step, I test the binary again, and it crashes. What is likely possible reason for this crash?

e) Frustrated, at 1:20pm, I decide to recompile the entire project from scratch. I decide to run “make clean”, and then run “make”. I run “make clean” with no errors. When I run “make”, I get several new errors. What is the cause of these errors?

IMPORTANT
Please follow the instruction (Description 1) for submitting your answer to the question.

a) x.o, y,o, z.o

b) y.o, top

c) nothing is regenerated

d) I was editing x.h, but it is not mentioned in the Makefile. So some file (likely x.c) has a dependency on this file, but that’s not mentioned in the Makefile. When nothing is generated in step c, the new structure(s) are not reflected in the top binary, causing it to crash

e) the clean target removes all files including c/h files, so there is nothing left in the directory to compile. Hence there are a lot of errors, with the make utility complaining about missing c/h files.

Unanswered

Question 4

Not yet graded / 0 pts

Consider the following set of processes, with arrival time and execution time reported in milliseconds, along with the priority of each process. Note that P_i has higher priority than P_j if $Priority(P_i) > Priority(P_j)$:

Process	Arrival Time	Execution time	Priority
P_0	0	3	3
P_1	1	1	4
P_2	2	4	0
P_3	3	5	5
P_4	4	2	1
P_5	5	3	2

(a)

Calculate the average turnaround[1] time for the following scheduling algorithms. Assume a scheduling quantum of 1 millisecond. Also draw a timeline (called a Gantt Chart) illustrating the schedule.

i. Round Robin
ii. Priority Scheduling (processes are scheduled in the priority order)
iii. Shortest Remaining Time First (the process with the shortest remaining time is executed first)

(b)

Under what conditions will each of the algorithm result in starvation of a particular process?

IMPORTANT

Please follow the instruction (Description 1) for submitting your answer to the question.

[1]turnaround time for a process is defined as the difference between the time the process finished and the time that it had arrived

(a)

From Fig 1, the time the process P_0 has finished is $6\ ms$ and the arrival time is $0\ ms$. Hence, the turnaround time for this process is $(6-0) = 6\ ms$. Similarly, turnaround times are calculated for each process in each scheduling algorithm and then average turnaround time for each scheduling algorithm is calculated as follows:

i. Average turnaround time for Round Robin Scheduling

$$= \frac{(6-0)+(2-1)+(15-2)+(18-3)+(11-4)+(16-5)}{6} = 8.83ms$$

ii. Average turnaround time for Priority Scheduling

$$= \frac{(9-0)+(2-1)+(18-2)+(8-3)+(14-4)+(12-5)}{6} = 8ms$$

iii. Average turnaround time for Shortest Remaining Time First Scheduling

$$= \frac{(4-0)+(2-1)+(13-2)+(18-3)+(6-4)+(9-5)}{6} = 6.17ms$$

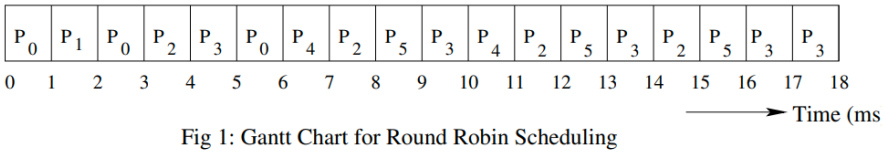

Fig 1: Gantt Chart for Round Robin Scheduling

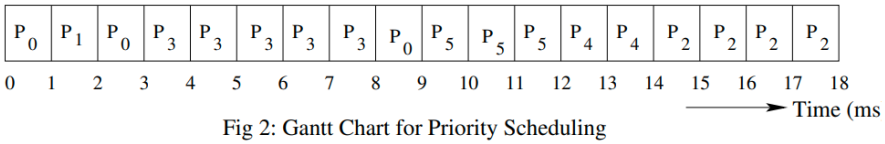

Fig 2: Gantt Chart for Priority Scheduling

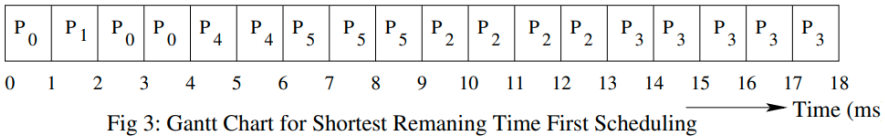

Fig 3: Gantt Chart for Shortest Remaning Time First Scheduling

(b)

i. Every process is given an equal priority and executed for a scheduling quantum of time. Hence, no process goes into starvation in Round Robin Scheduling.

ii. Suppose a process (**P**) with a low priority arrives. After this if only higher priority processes arrive, the low priority process goes into starvation in Priority Scheduling

into starvation in Priority Scheduling.

Unanswered

Question 5

Not yet graded / 0 pts

Consider the circuit shown in Fig. 1.
In the circuit, the OR gates and the inverter have a delay of 5ns. The AND gates and the XOR gates have a delay of 10ns.

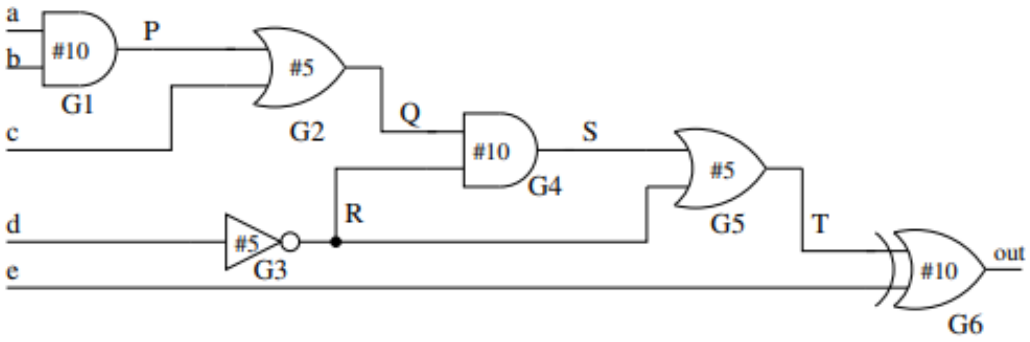

Figure 1

a) Run Static Timing Analysis (STA) on the circuit in Fig. 1. Write down the maximum delay of each node (P, Q, R, S and T) in the circuit.

b) Is the output delay reported by STA accurate? If not, what is the actual maximum delay of the circuit?

IMPORTANT
Please follow the instruction (Description 1) for submitting your answer to the question.

a)

Solution. To run STA on given circuit, we would perform the following steps.

1) Levelize the circuit. The level of any node n with fan-ins $m_1, m_2, \ldots, m_k$ is:

$$level(n) = \max_{1 \le i \le k} [level(m_i) + 1]$$

The level of primary input nodes is 0.

2) Find the cumulative delay C_{delay} for each node n in level order.

$$C_{delay}(n) = \max_{1 \le i \le m} (C_{delay}(m_i)) + Gatedelay(n).$$

The circles in Fig. 2 represent the level of each node, and the squares represent the cumulative delay. The maximum delay reported by STA would be 40ns.

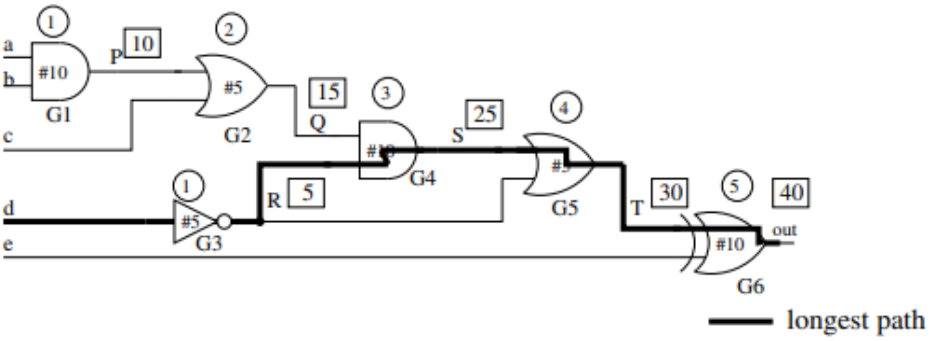

Figure 2

b)

Solution. The maximum delay reported by STA is not accurate as the given circuit has a false path. The logic function of T is RQ+R. This simplifies to R. In other words, the final output is independent of Q, because out = e⊕T = e⊕R = e⊕$\bar{d}$. Note that T does not depend on a, b or c, and hence the delay in computing Q = ab+c does not contribute to the delay of the output. Hence the actual delay of the output is 30ns, because the true longest path (shown in Fig. 2) does not pass through gate G1 and G2.

Unanswered

Question 6

Not yet graded / 0 pts

[749 QUESTION]

I have two programs that I am considering for hardware acceleration using an FPGA board. The first program is Microsoft Word. The serial portion of this code takes up 94% of the runtime. The remaining 6% of the code is parallelizable. When I accelerate the parallelizable code on the FPGA, I get a speedup of 30X. The second program is Vivado. It has about 80% of the code which can be parallelized, and 20% of the code runtime is serial in nature. When I accelerate the parallelizable code on the FPGA, I get a speedup of 40X.