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UNIVERSITY OF ENERGY AND NATURAL RESOURCES, SUNYANI, GHANA

SCHOOL OF ENGINEERING

DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING

MIDSEMESTER EXAMINATION, 2017

Bachelor of Science (Electrical and Electronic Engineering)
Bachelor of Science (Computer Engineering)
Bachelor of Science (Renewable Energy Engineering)

CENG 206: Digital Logic Design

March, 2017 Duration: 1 hr 15mins.

Answer all Questions. [20 Marks]

Question 1 [6 marks]

Consider the mess of gates shown in Fig. 1

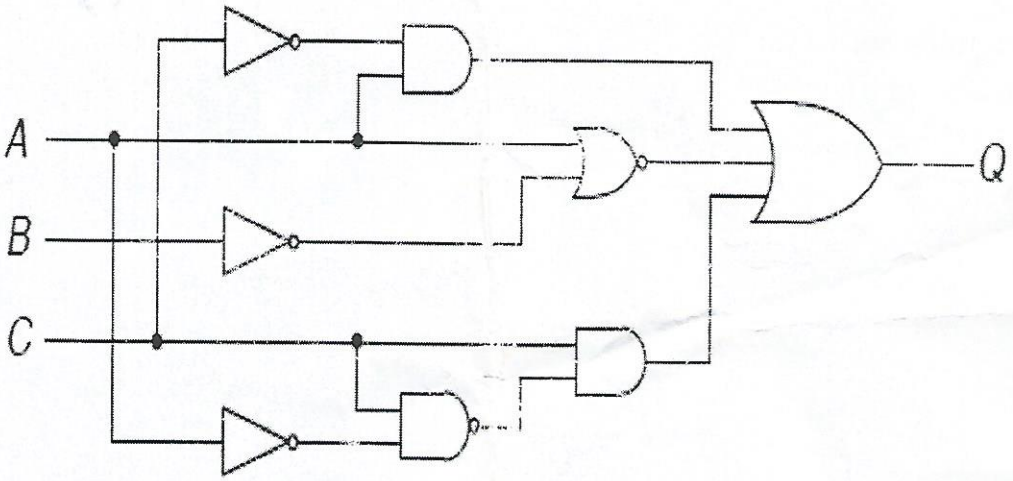

Fig. 1

(a) Convert the mess of gates into the equivalent Boolean expression.

(b) Use Boolean algebra to reduce your Boolean expression.

(c) Express your reduced expression as network of gates.

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Question 2 [5 marks]

Implement the following functions using a decoder and external gates:

$$F_1(x, y, z) = \bar{x}\bar{y}\bar{z} + xy \qquad F_2(x, y, z) = xy\bar{z} + \bar{x}z$$

Question 3 [4 marks]

Reduce the function $\bar{A}.\overline{\left((B.C) + B\right)}.\bar{A}$ and implement it using DTL

Question 4 [5 marks]

A step in a space vehicle checkout depends on four sensors. Every circuit is functioning properly if sensors 'one' and any two of the other three (3) are '1'. If the circuit is not working properly, an alarm should sound. Design a logic circuit to activate the alarm.

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DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING
LEVEL 200: END OF SECOND SEMESTER EXAMINATIONS 2017/2018
Bachelor of Science (Electrical & Electronic Engineering)
Bachelor of Science (Computer Engineering)
Bachelor of Science (Renewable Energy Engineering)

CENG 206: DIGITAL LOGIC DESIGN

May, 2018 Time: 2 hours

Attempt all **FOUR** questions.

Question one [17 Marks]

(a) A long corridor has a single light bulb and two doors with light switch at each door. Design logic circuit for the light; assume that the light is *off* when both switches are in the same position. **[3 marks]**

(b) Draw the CMOS implementation of a three input **OR**-gate. **[3 marks]**

(c) Implement Full Adder using a DECODER. **[5 marks]**

(d) Implement the function $F = AB + B\overline{C}\,\overline{D} + \overline{A}\,\overline{B}D + ACD$ on a Multiplexer using A, B, and C as selection lines. **[6 marks]**

$AB(C+\bar{C})(D+\bar{D})$
$(ABC + AB\bar{C})(D+\bar{D})$
$ABCD + ABC\bar{D} + AB\bar{C}D + AB\bar{C}\bar{D}$

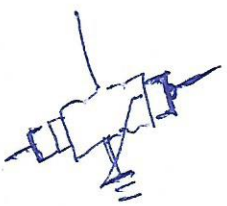
Question Two [11 Marks]

Simply the functions (a) and (b) using Boolean algebra:

(a) $F = AB\overline{C} + A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + \overline{A}\,\overline{B}\,\overline{C} + A\overline{B}$. **[3 marks]**

(b) $X = \overline{\overline{(A+B)} + \overline{(\overline{A}+\overline{B})}}$. **[3marks]**

(c) If $F(a,b,c,d,e) = \overline{b}e$, express F in the form $F(a,b,c,d,e) = \sum m(\ )$ **[5marks]**



Question Three [12 Marks]

(a) An electronic lock has four input keys *A*, *B*, *C*, and *D* for which three combinations is used to open it but not all four. Before the lock can be opened, key *A* must first be in position followed by key *B* and then either *C* or *D* depending on which one is available. Design a logic circuit to implement the opening of the lock if the opening results in a function *F* that produces a '1' for a valid key combination. **[6 marks]**

(b) An engine operates with four essential variables controlling its operation. For the engine to be operating properly, at least two of its control variables must be present at the same time. However, when the machine is not operating correctly we wish to have some signal to alert us to the problem. Design a circuit to implement the state when the alarm signal is present. **[6 marks]**

Question Four [20 Marks]

(a) A counter is designed to go through the sequence: 1, 3, 5, 7, 0, 2, 4, 6, repeat. Using JK flip-flops: **[8 marks]**

(i) Construct the state Table

(ii) Draw the circuit.

(b) A sequential circuit is constructed with one T flip-flop A, one D flip-flop B and one input X. When X=0, the state of the circuit remains the same. When X=1, the circuit goes through the transitions from 00 to 01 to 11 to 10 back to 00, repeat. **[12 marks]**

(i) Draw the state transition diagram

(iii) Construct the state Table

(iv) Draw the circuit.