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Exp
Epitaxial Growth
Oxidation
Diffusion
Film deposition

UNIVERSITY OF ENERGY AND NATURAL RESOURCES, SUNYANI, GHANA

SCHOOL OF ENGINEERING

DEPARTMENT OF COMPUTER AND ELECTRICAL ENGINEERING

MIDSEMESTER EXAMINATION, 2017

Bachelor of Science (Computer Engineering, Electrical and Electronic Engineering)

CENG 303: LINEAR ELECTRONIC CIRCUITS

October, 2017 Duration: 1 hr 20min.

INSTRUCTIONS: Answer all Questions. [20 Marks]

Question 1 [10 marks]

a) List and explain the plannar process technology as applied to IC fabrication

b) A circuit is built around a bi-polar NPN transistor. The Base network has a resistor (R_B) and diode (D_B) in series with the cathode of the diode connected to the base while the collector is connected to a power supply (V_{CC}) through a resistor (R_C). If the emitter is connected to ground:
   i. Draw the circuit
   ii. Provide all the masking layout of the circuit.

Question 2 [10 marks]

For the circuit shown in Fig. 1, the transistor parameters are β =150, V_{BE} =0.7V and V_T =26mV.

a) Determine the operating point parameters
b) Draw the small signal equivalent circuit based on the r_e model
c) Determine:
   i. Gain of the transistor, A_v
   ii. Input impedance, Z_{in}
   iii. Gain with signal, A_{vs}
   iv. Output voltage, given that V_s =30mVSinωt

Photolithography

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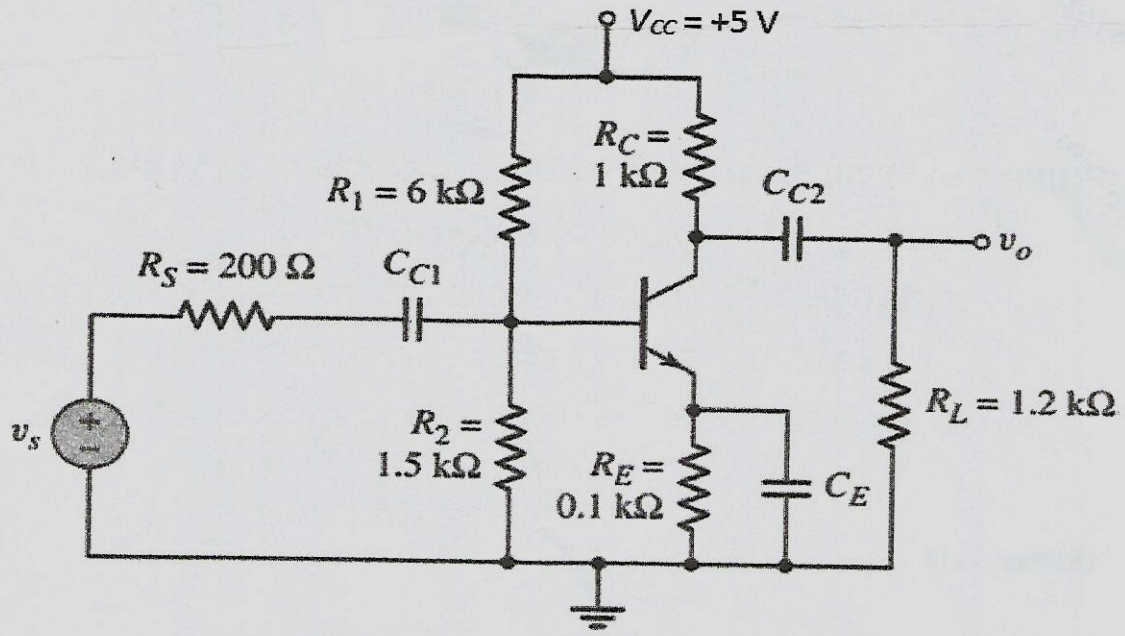

Fig 1