Subthreshold leakage modeling and reduction techniques along with Technology Scaling

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1 Introduction

With technology scaling, the subthreshold current is no longer negligible. To sustain the increasing performance demands, it is fundamental to estimate subthreshold leakage power and to implement new design techniques. It is important to distinguish between standby leakage current, dissipated by MOS devices that are 'off', and active leakage power.

2 Subthreshold leakage reduction techniques

2.1 Source Biasing

With source biasing, a positive bias is applied to the source terminal during the standby state. Since the body effect raises the threshold voltage of the device, the leakage current decreases as a result. Additionally, V_{GS} becomes negative, further reducing the subthreshold current, and it can be reduced even more exploiting the stack effect.

The main disadvantage is that CAD tools must identify the proper stack with enough slack to still meet timing constraints when inserting extra series devices.

2.2 Dual Vt Partitioning

Dual V_t partitioning is a technique that addresses subthreshold conduction by designing transistors with high and low V_t. This solution impacts the timing behavior, so a trade-off between timing performance and leakage current must be found. EDA tools can adopt this technique, using low V_t transistors on critical and quasi-critical paths, and high V_t transistors on the other paths.

The limitation is that the algorithm has to find the best replacement choice. Moreover, Dual V_t partitioning has a natural limit where standby leakage current cannot be reduced sufficiently.

2.3 Domino logic

Domino logic logic technique that operates in two phases: the precharge phase and the evaluation phase. During the precharge phase, GND is detached and the output pin is charged to V_{dd}. Then, during the evaluation phase, the pull-down network is grounded and based on the input valuesthe output pin may either discharge toward GND or remain at a high voltage.

Power dissipation is reduced since, during conduction, the pull-down network is detached from V_{dd}. Even though high performance can be achieved, the difficulty in generating the control signal has to be considered.

3 MTCMOS

MTCMOS is a dual V_t technique for reducing leakage current during standby mode. Given a low V_t computation block, it is possible to interleave standby and active states through sleep devices, which connect the virtual V_{dd} and GND lines to the power supply.

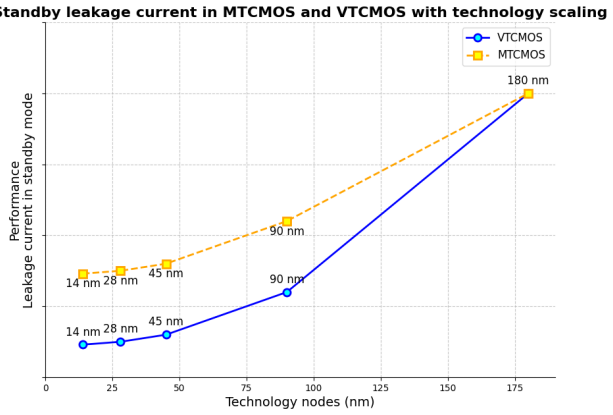
When the low V_t block is turned on, the internal logic computes the result, while when the sleep signal is high, the block is disconnected, and thanks to the high V_t switches, there is low leakage current. One drawback is the sizing of the sleep transistors, as an optimal trade-off must be achieved between performance, area, and energy overhead.

MTCMOS can also be used with sequential circuits, but data stored corruption due to floating nodes should be considered. A MTCMOS flip-flop can be implemented as a solution using a technique called "leakage feedback", which allows to retain the state during standby by using subthreshold leakage current to hold the output, eliminating at the same time current paths from V_{dd} to GND.

4 VTCMOS

VTCMOS is a technique that dynamically adjust V_t. The V_t is changed by biasing the body terminal. By applying maximum reverse bias during standby mode, V_t becomes high, reducing subthreshold leakage current. By contrast, V_t is tuned during active mode to optimize performance. Moreover, with VTCMOS is possible to change both V_{dd} and V_t during active mode, allowing optimal trade-off between performance, dynamic power, and leakage power.

One side effect is the total active power consumed during the active state. To decrease active power, V_{dd} could be scaled, reducing it quadratically, but since V_t has to be scaled accordingly, a higher active leakage current will be experienced.



5 Conclusions

In the following paragraph, the student analyzes the effects of technology scaling on MTCMOS and VTCMOS techniques, evaluating their impact on reducing leakage current in standby mode across different technological nodes. First, to analyze the subthreshold leakage current, it is assumed that in MTCMOS, it primarily depends on the leakage current of the sleep devices, while in VTCMOS, it depends on the leakage current of each transistor, properly biased to be in standby mode. Subsequently, for MTCMOS, the subthreshold current I_{sub} and its scaling factor can be expressed as:

$$I_{sub} = I_t \frac{W}{L} \exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right) \tag{1}$$

$$I'_{sub} \approx S \cdot I_{sub} \exp\left(\left(1 - \frac{1}{S}\right) \cdot \frac{V_{th} - V_{GS}}{nV_T}\right) \tag{2}$$

As can be observed, the higher the scaling factor S, the greater the subthreshold leakage current. Considering that even though sleep switches can be properly sized, they must adhere to the scaling trend. Thus, we can conclude that with technology scaling, the effectiveness of reducing leakage current during standby mode diminishes.

As for VTCMOS, the key point is altering the threshold voltage by properly biasing the body terminal. The threshold voltage and its scaling factor (in the constant electric field era (4) and constant voltage era (5)) can be formulated as follows:

$$V_{th} = V_{th0} + \gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right) \tag{3}$$

$$V'_{th} = V'_{th0} + \frac{t_{ox}/S}{\varepsilon_{0x}}\sqrt{2q\varepsilon_{Si}SN_A}\left(\sqrt{|\frac{V_{SB}}{S} + 2\phi_F|} - \sqrt{|2\phi_F|}\right) \approx \frac{V_{th}}{S} \tag{4}$$

$$V'_{th} = V'_{th0} + \frac{t_{ox}/S}{\varepsilon_{0x}}\sqrt{2q\varepsilon_{Si}S^2N_A}\left(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{|2\phi_F|}\right) \approx V_{th} \tag{5}$$

By biasing the body it is possible to achieve a higher threshold voltage, thereby reducing the subthreshold leakage current, as indicated in (1).

The figure shows the trend of the two techniques across technology nodes, comparing the performance of both in terms of leakage current in standby mode. It highlights how MTCMOS has an increasingly reduced impact on the reduction of subthreshold leakage current in standby mode. The same trend is observed with VTCMOS, albeit with better performance, due to the decrease in threshold voltage. In fact, although the subthreshold leakage current increases, the decrease in threshold voltage mitigates this effect.

In conclusion, MTCMOS and VTCMOS techniques lose effectiveness with technological advancements, although VTCMOS performs better due to the mitigation of the scaling factor by the increase in threshold voltage.