Lab 12: Flip Flops and Timing Diagrams
EECE 2106.05

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Abstract

In Experiment 12, we had to create an SR latch, a gated D latch, a master-slave latch. Circuits were constructed on a breadboard and we had to fill out multiple characteristic tables. One highlight was the 3 bit ripple counter, with seven different LED configurations if done correctly.

Components:

The components utilized to complete the experiment include:

- Gate 7486 (XOR gate)
- Gate 7474 (D flip flop)
- Gate 7476 (JK flip flop)
- 6 resistors
- 6 LED lights
- Breadboard
    - Cable wires
- Power supply (w/ 5v battery)
    - Multimeter

Experiment:

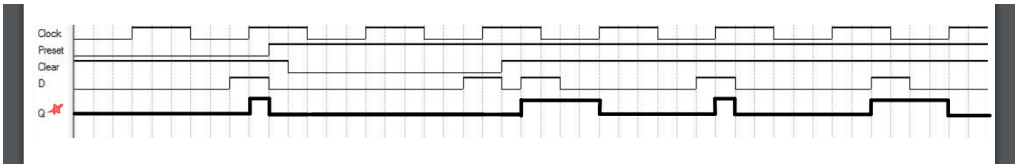
This experiment was divided into 18 problems.

1. Wire the provided D flip-flop making sure to supply 5V to both Preset and Clear. Utilize the function generator to provide a clock signal of 1 Hz. Use a resistor in series with an LED to monitor the output. The provided D flip-flop is a positive-edge-triggered device with asynchronous Preset and Clear.
2. How does output Q behave in response to input D?
    a. if clock = 1 then q = d if clock = 0 then no change occurs.
3. With the information gathered from step 2, fill out the characteristic table corresponding to a D flip-flop.

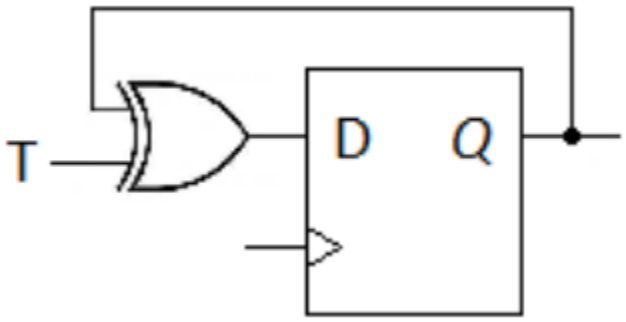
a.

D	Q(t+1)
0	0
1	1

4. Change input Preset to LOW and record the outcome.
    a. Q = 1
5. Change input Clear to LOW and record the outcome.
    a. Q = 0
6. With the information gathered from steps 1 through 5 complete the following timing diagram.

a. 

7. Build the circuit below equivalent to a T flip-flop. Remember to provide 5V to both Preset and Clear for the D flip-flop.

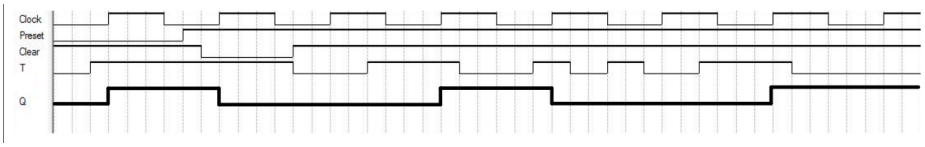
a. 

8. How does output Q behave in response to input T?
    a. If clock = 1 and T = 1 then Q = Q'(t) if T = 0 then Q = Q(t), if clock = 0 then no change occurs.
9. With the information gathered from step 8, fill out the characteristic table corresponding to a T flip-flop.

a.

T	Q(t+1)
0	Q(t)
1	$\overline{Q(t)}$

10. With the information gathered from step 9 complete the following timing diagram.

a. 

11. Wire the provided JK flip-flop making sure to supply 5V to both Preset and Clear. Utilize the function generator to provide a clock signal of 1 Hz. Use a resistor in series with an LED to monitor the output.
12. How does output Q behave in response to all four different combinations of inputs J and K?

a. Only change occurs when clock goes from 1 to 0. (neg. edge)
J = K = 0 ⇒ Q(t)
J = 0, K = 1 ⇒ 0
J = 1, K = 0 ⇒ 1
J = K = 1 ⇒ $\bar{Q}(t)$

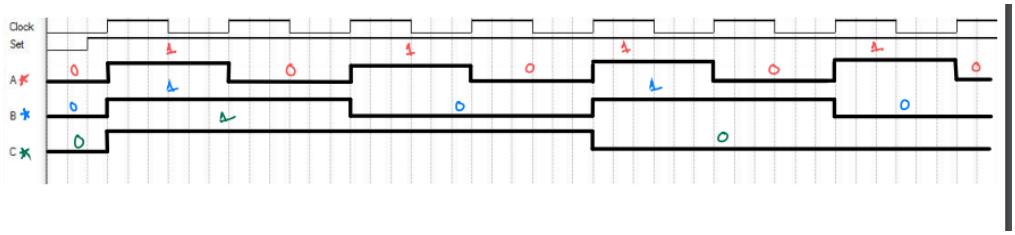
13. With the information gathered from step 12, fill out the characteristic table corresponding to a JK flip-flop.

a.

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\bar{Q}(t)$

14. Change input Preset to LOW and record the outcome.
    a. Q = 1
15. Change input Clear to LOW and record the outcome.
    a. Q = 0
16. With the information gathered from steps 11 through 15 complete the following timing diagram.

17. Build and demonstrate to the lab instructor the circuit shown below using resistors in series with LEDs to monitors outputs A, B and C. When the input signal Set is LOW every output is also LOW; when the input signal Set is HIGH the circuit becomes operational. This circuit is known as a Three-bit Ripple Counter.
18. Observe the behavior of the circuit above and complete the following timing diagram.

a. 

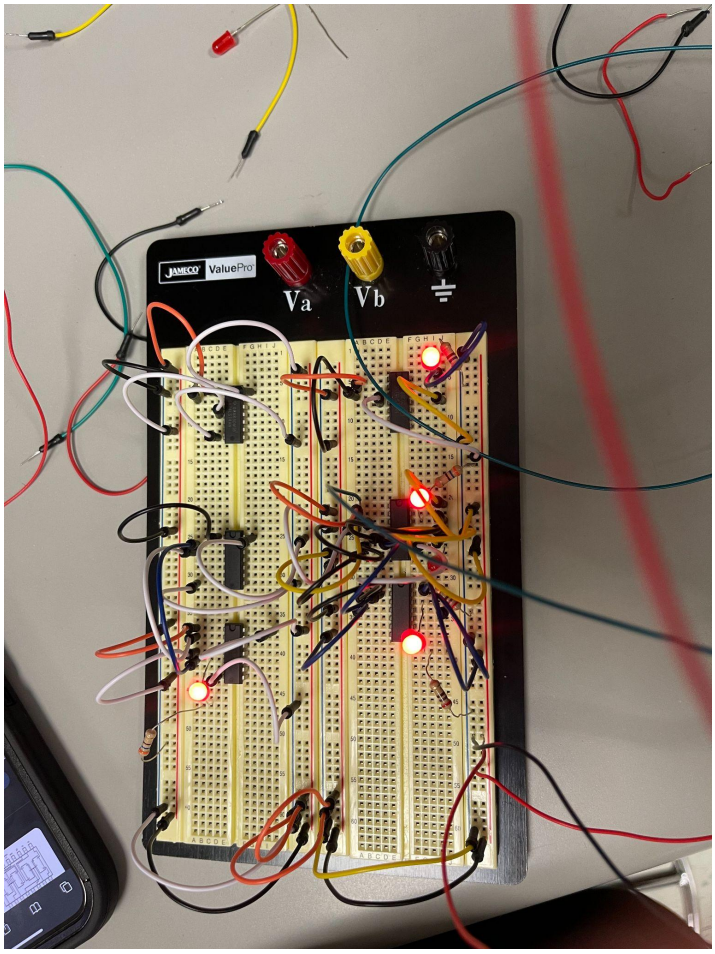
Here is the completed breadboard for all problems.

Carlos Alvizo - Breadboard

The following is a video, requested by the professor:

https://www.youtube.com/shorts/uJsdigEkCP8

Here is an image of our completed breadboard:



Conclusion:

Samuel Lee was responsible for the lab report, Carlos Alvizo was responsible for the prelab and the breadboard. Thankfully circuits seemed to be working, unlike last week. 3 bit ripple counter, JK flip flop, D flip flop construction was successful. 3 bit ripple counter was interesting, had many different inputs/outputs to consider. Samuel Lee was responsible for uploading proof of working breadboard to youtube.