Lab 5: NAND/NOR Conversion
EECE 2106.05

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Abstract

Experiment 5 consisted of two separate breadboards where we'd obtain an SOP and POS equation from a truth-table from a given scenario that would then be implemented on the breadboards utilizing only NAND (7400) and NOR (7402) gates. Schematics were obtained from the equation and then converted to NAND and NOR via the k-mapping method of AND, OR and NOT gates. The costs were then compared between the two finished NAND and NOR breadboards.

Components:

The components utilized to complete the experiment include:

- Gate 7402 (NOR gate)
- Gate 7400 (NAND gate)
- Two resistors
- Two LED lights
- Two Breadboards
    - Cable wires
- Power supply (w/ 5v battery)
    - Multimeter

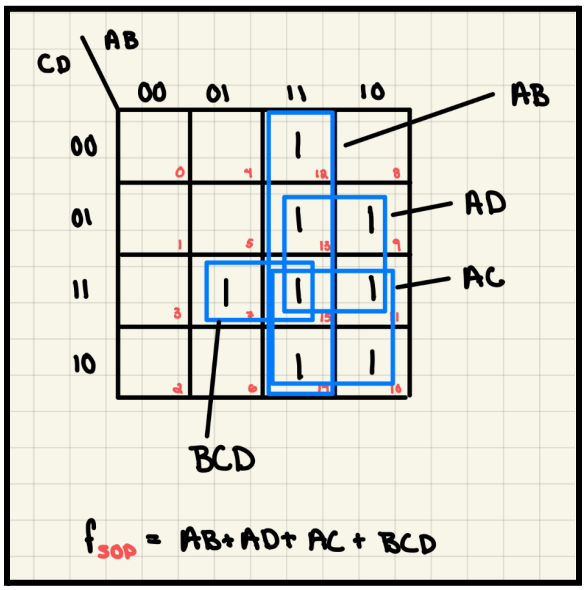
Experiment:

The lab consisted of finding the SOP and POS form of the given truth-table below and drawing both circuits to implement on the breadboard. The output was determined much like a majority-gate where the majority of the inputs must be 1/true in order for the output to be 1. However, the President input is special in which it counts as two inputs (votes) so you can have a combination of a president and another input being 1, or three inputs being 1 (excluding the President) to have an output of 1.

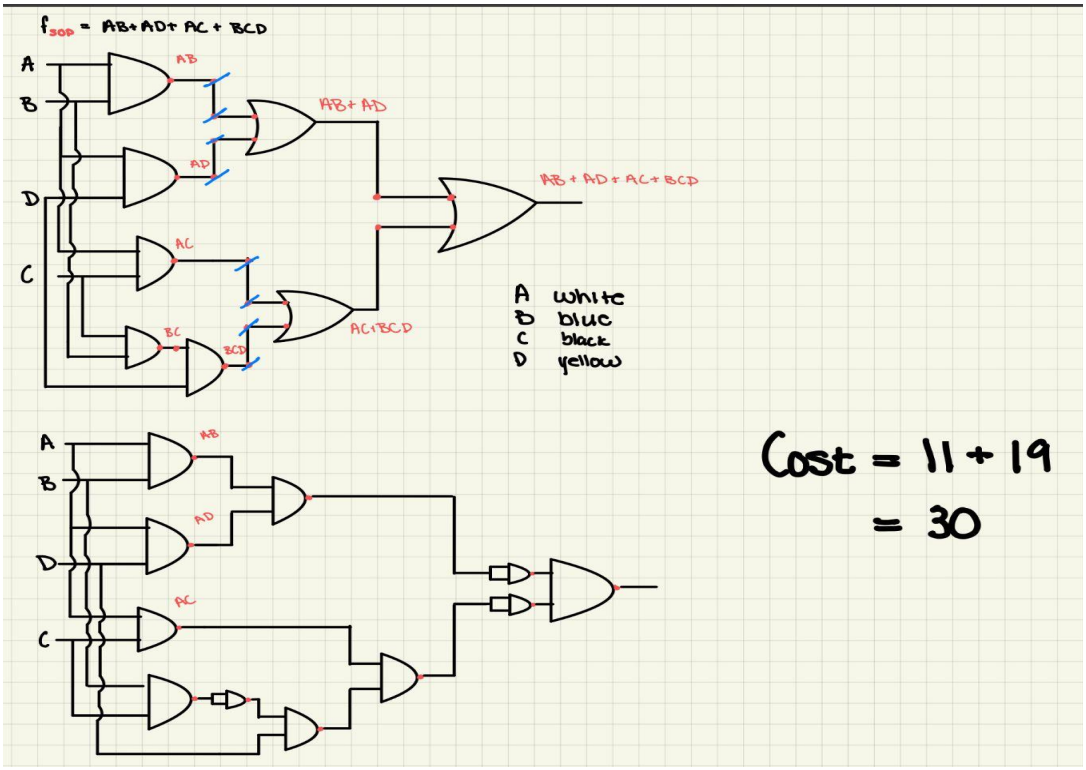
President	Vice President	Secretary	Treasurer	Output
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

After the truth-table was obtained, we then began to derive the SOP and POS equations via a 4-variable Karnaugh map (K-map) in which we got the equations below.

SOP Karnaugh map



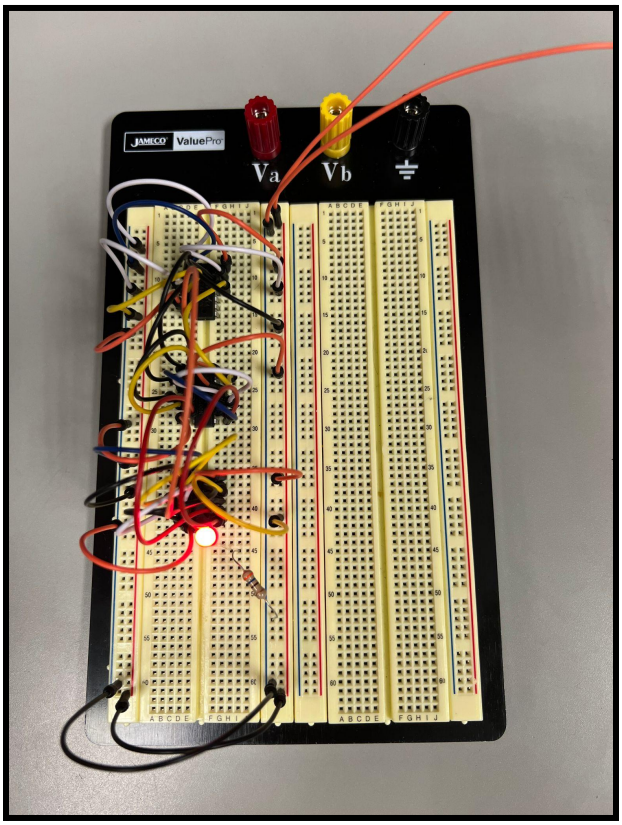
Once the K-map was obtained for SOP, we then drew the schematic using AND and OR gates where we'd use the bubbling process to convert them to their respective NAND forms. Below is shown the bubbling process and the final NAND form.



SOP NAND FORM SCHEMATIC

With the NAND schematic obtained, the only thing left to implement was the said schematic on the breadboard. The procedure was the same as other 2-input gates; however, to form a NOT/inverter on a NAND gate you put a wire to both inputs so that it occupies the two slots and then a given output to one of the inputs to invert a signal.

SOP NAND BREADBOARD



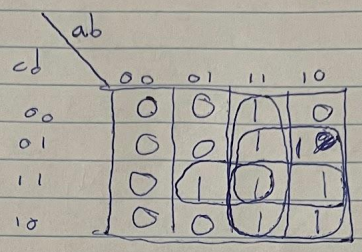
First, we got the k map using the equation obtained from the truth table. Then we bubbled 0s such that as many 0s in our k map were bubbled as possible. Our resulting equation was then drawn as a circuit. This circuit was then converted into a NOR gate circuit.

Truth table to NOR circuit conversion:

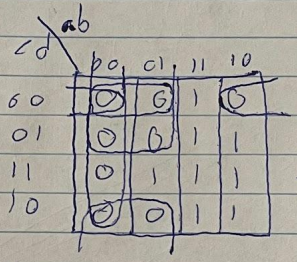
Convert to NOR

	P	VP	S	T	output
1	0	0	0	0	0
2	0	0	0	1	0
3	0	0	1	0	0
4	0	0	1	1	0
5	0	1	0	0	0
6	0	1	0	1	0
7	0	1	1	0	0
8	0	1	1	1	1
9	1	0	0	0	0
10	1	0	0	1	1
11	1	0	1	0	1
12	1	0	1	1	1
13	1	1	0	0	1
14	1	1	0	1	1
15	1	1	1	0	1
16	1	1	1	1	1

(a'bcd)+(ab'c'd)+(ab'cd')
+(ab'cd)+(abc'd')+(abc'd)+
(abcd')+(abcd)



SOP:
ab+ad+bcd
+ac

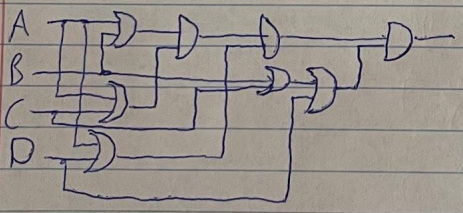


POS:

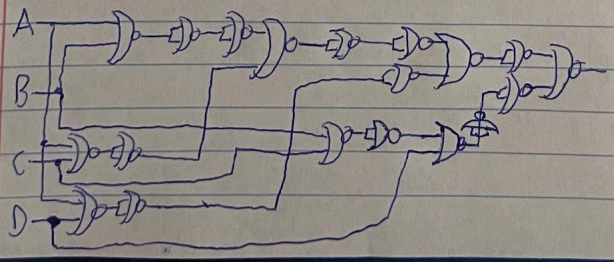
~~b'cd+a'c'+a'd'~~
~~+a'b'~~
~~(b'+c+d)(a'+c')~~
~~(a'+d')(a'+b')~~

POS: (a+b)(a+c)(a+d)(b+c+d)

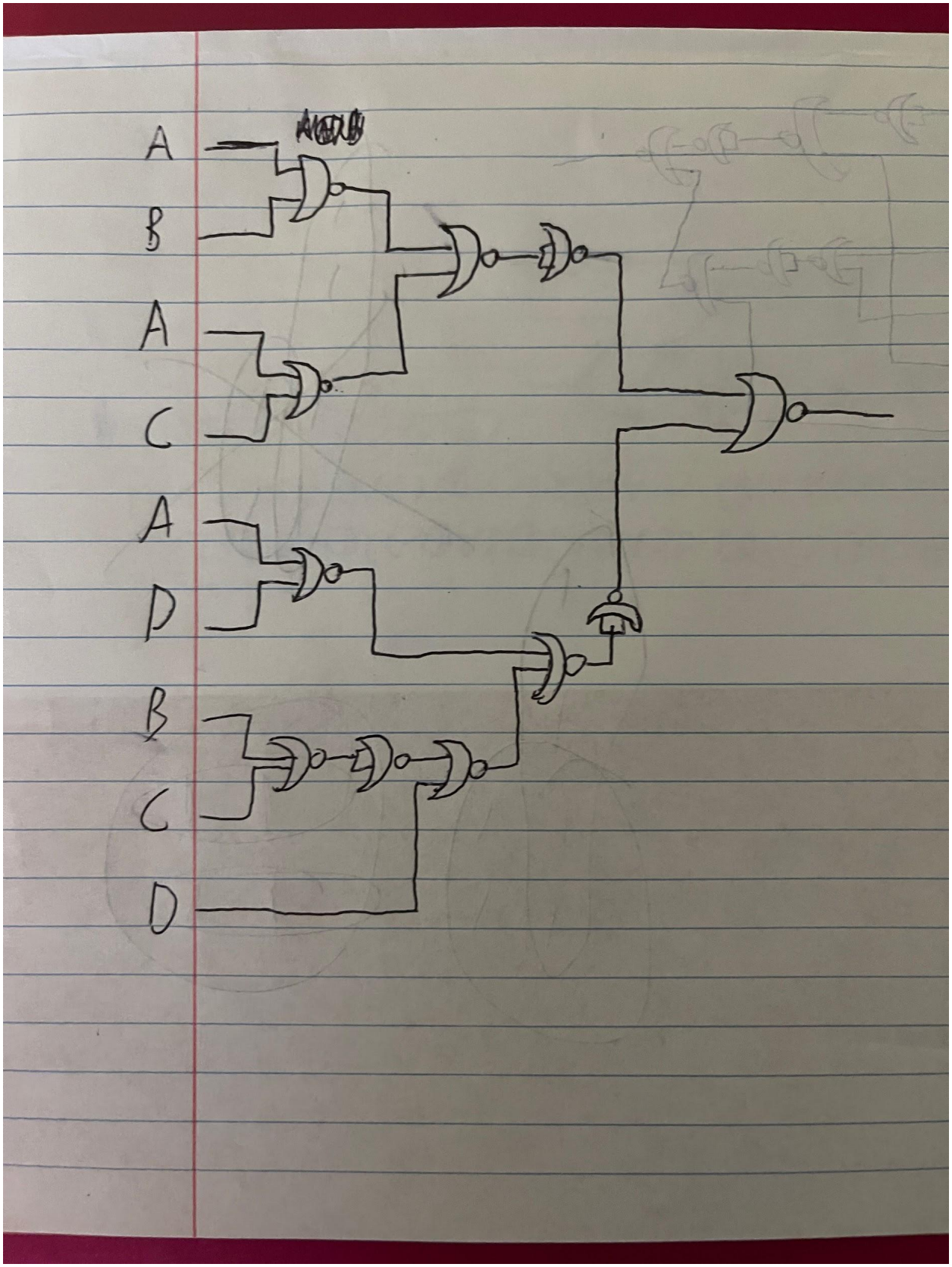
POS minimum cost = 24



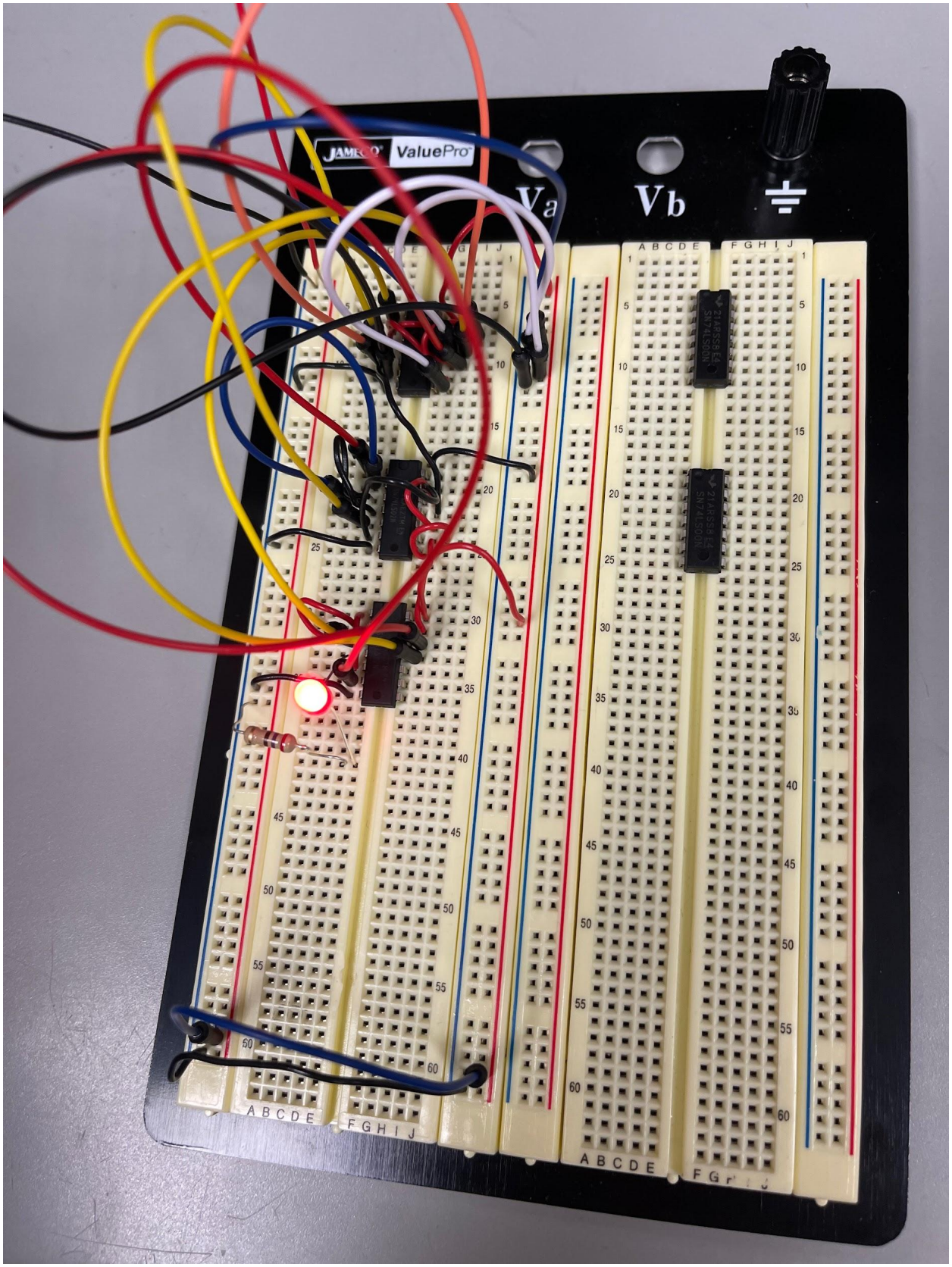
NOR



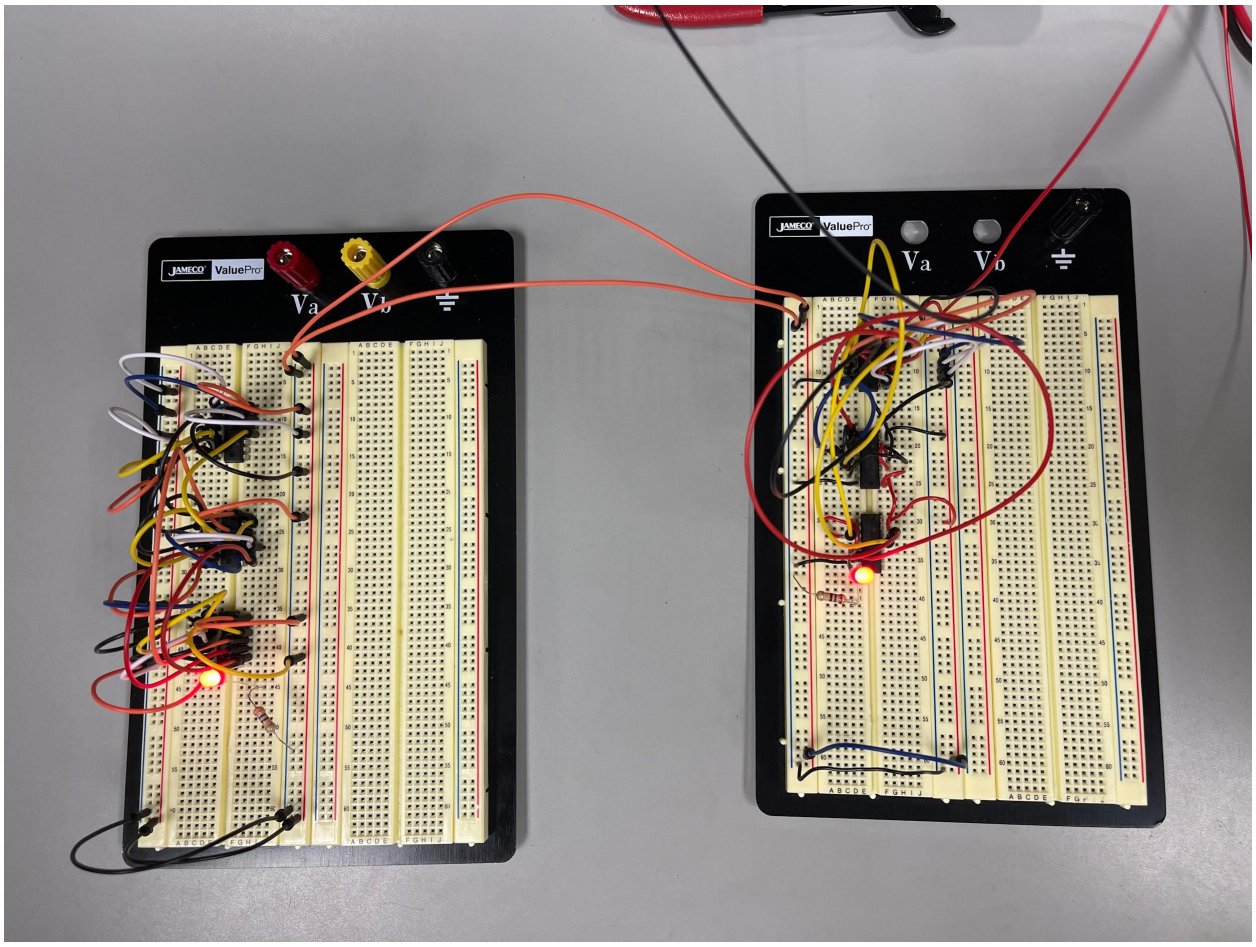
Final POS gate structure


A
B
A
C
A
D
B
C
D

Samuel Lee's POS (NOR) circuit board:


JAMECO
ValuePro
Va
Vb
A B C D E
F G H I J

Both circuit boards. Left is NAND, Right is NOR



Conclusion:

Work was split right down the middle, with Carlos Alvizo responsible for the first breadboard circuit matching the first question on the lab assignment, and his portion of the lab report. Samuel Lee was responsible for the second breadboard circuit matching the second question on the lab assignment, and his portion of the lab report. We learned how to create the SOP and POS equation of a given truth table, how to convert the resulting circuits into NAND/NOR, and how to build NAND/NOR boards.