

Lab 6: Combinatorial Circuit
EECE 2106.05

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Abstract

In Experiment 6 we tested and designed a combinatorial circuit that had a 5 variable k map. So we were given a truth table, and the sop function for our circuit, and we were told to construct this breadboard circuit using NOT, AND, OR, NAND, NOR gates. One highlight was the inclusion of the NAND and NOR gates, which made testing the circuit more difficult. The results from implementing the circuit didn't give us the respective values from its truth table and we are going to present the finished/working breadboard during next week's lab.

Components:

The components utilized to complete the experiment include:

- Gate 7402 (NOR gate)
- Gate 7400 (NAND gate)
- Gate 7408 (AND gate)
- Gate 7404 (NOT gate)
- Gate 7432 (OR gate)
- One resistor
- One LED light
- Two Breadboards (we both tried construction)
 - Cable wires
- Power supply (w/ 5v battery)
 - Multimeter

Experiment:

Experiment 6 consisted of creating a combinatorial circuit using a 5 variable k-map. Or in other words, a multi-function gate that changed what it did depending on what the x and y inputs for this combinatorial circuit were. We were given the equation:

$$F(\text{SOP}) = Y'(ABC) + X'Y(ABC)' + XY'(A+B+C) + Y(A+B+C)'$$

With the POS equation being derived from the SOP equation via utilizing DeMorgan's Theorem on both sides of the former equation.. The POS expression is as follows:

$$F(\text{POS}) = Y(A'+B'+C') + XY'(A+B+C) + X'Y(ABC)' + Y'(ABC)$$

SOP and POS Equations

$X=0$

$X=1$

$$f_{\text{SOP}} = xy'A + x'yA' + xy'B + x'yB' + xy'C + x'yC' + yABC + yA'B'C'$$
$$= y'(ABC) + x'y(A+B+C) + xy'(A+B+C)' + y(A+B+C)'$$

$\therefore A+B+C' = \overline{ABC}$

$\therefore A'B'C' = \overline{A+B+C}$

$$= y'(ABC) + x'y(\overline{ABC}) + xy'(A+B+C) + y(\overline{A+B+C})$$

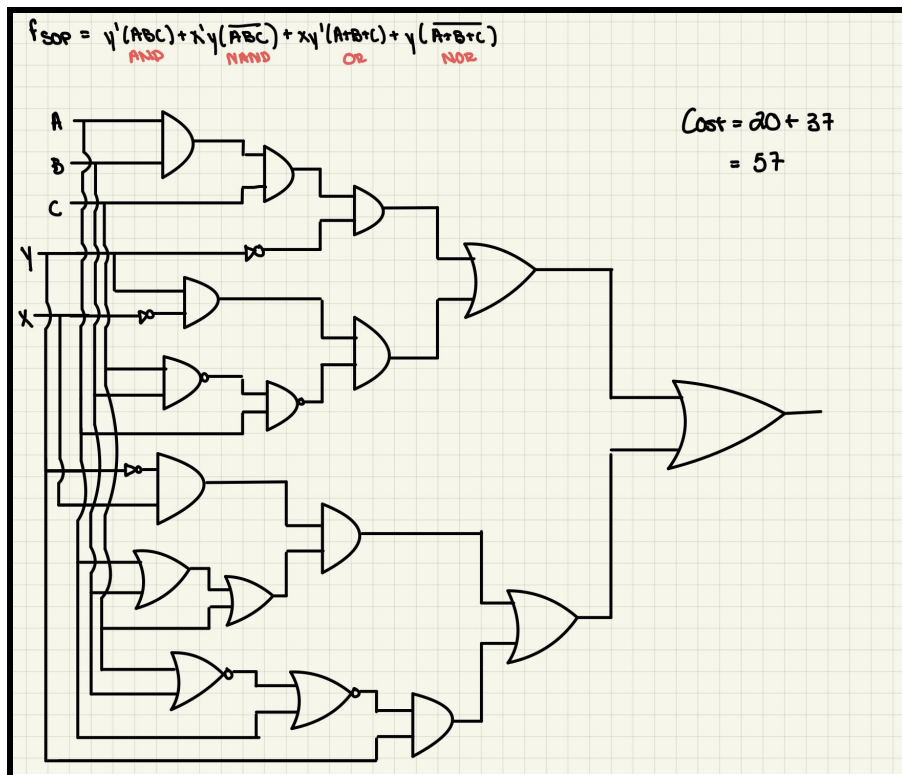
AND NAND OR NOR

$$f_{\text{POS}} = [y + (A+B+C)'] \cdot [x+y+(ABC)] \cdot [x+y+(A'B'C')] \cdot [y' + (A+B+C)]$$
$$= [\underbrace{y + (\overline{ABC})}_{\text{NAND}}] \cdot [\underbrace{x+y}_{\text{AND}}] \cdot [\underbrace{x+y + (\overline{A+B+C})}_{\text{NOR}}] \cdot [\underbrace{y' + (A+B+C)}_{\text{OR}}]$$

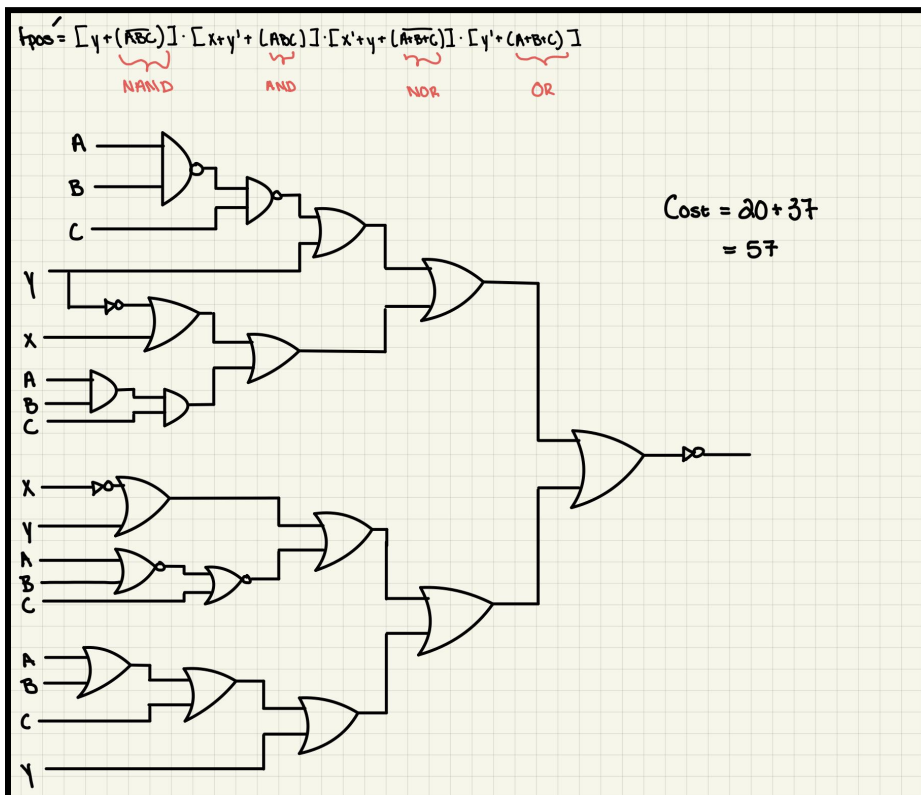
Here is the truth table that was provided:

	x	y	A	B	C	f	
0	0	0	0	0	0	0	
1	0	0	0	0	1	0	
2	0	0	0	1	0	0	
3	0	0	0	1	1	0	
4	0	0	1	0	0	0	
5	0	0	1	0	1	0	
6	0	0	1	1	0	0	
7	0	0	1	1	1	1	AND
8	0	1	0	0	0	1	
9	0	1	0	0	1	1	
10	0	1	0	1	0	1	
11	0	1	0	1	1	1	
12	0	1	1	0	0	1	
13	0	1	1	0	1	1	
14	0	1	1	1	0	1	
15	0	1	1	1	1	0	
16	1	0	0	0	0	0	
17	1	0	0	0	1	1	
18	1	0	0	1	0	1	
19	1	0	0	1	1	1	
20	1	0	1	0	0	1	
21	1	0	1	0	1	1	
22	1	0	1	1	0	1	
23	1	0	1	1	1	1	
24	1	1	0	0	0	1	
25	1	1	0	0	1	0	
26	1	1	0	1	0	0	
27	1	1	0	1	1	0	
28	1	1	1	0	0	0	
29	1	1	1	0	1	0	
30	1	1	1	1	0	0	
31	1	1	1	1	1	0	NOR

Since we were told to construct only the lowest cost circuit, we attempted to construct the SOP circuit since both the SOP and POS equation's circuits had the same cost.



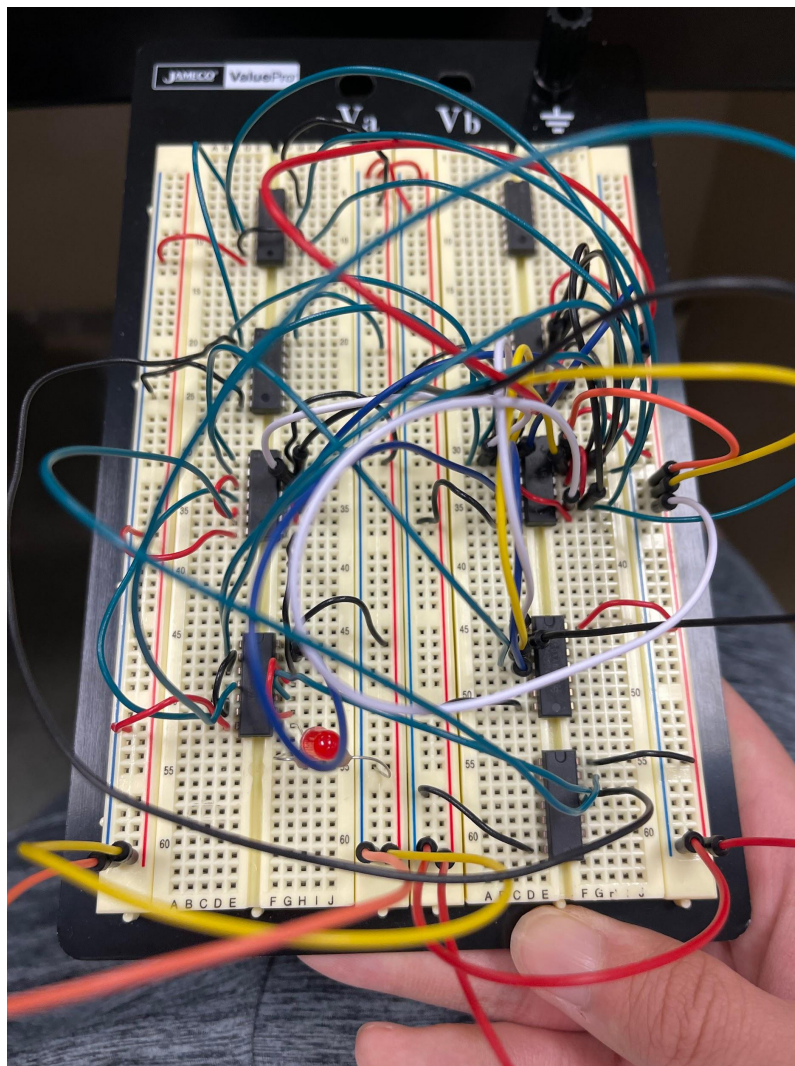
SOP Circuit Schematic



POS Circuit Schematic

Additionally, we were told only to construct the version using NAND and NOR gates, without which we would be penalized. The following image is the attempted SOP circuit that didn't work as intended with its respective truth table values.

Samuel's Attempt at a Breadboard



Conclusion:

Both Samuel and Carlos tried constructing a SOP breadboard based on the equation shown under Lab 6 Sketch NEW, however, both attempts failed as the circuit's outputs didn't match that of its truth table . Although the breadboards did not output the correct equations, we are confident that a correct breadboard will be constructed at the next class meeting. One issue might have been damaged circuits, so after obtaining new undamaged circuits a better working breadboard should be able to be constructed.