Lab 3: Product of Sums Expression
EECE 2106.05

By: Samuel Lee & Carlos Alvizo

Abstract

Lab 3 consisted of a boolean expression, Y = A'B+B'C'D'+BCD+AB'CD that was to be simplified (this time using POS form) and then constructed onto a breadboard using only NOT, AND, and OR gates. Testing was performed to ensure that the output of the breadboard circuit correctly matched the expected truth table of the resulting equation. One item of interest was the addition of another NOT gate, which led to the correct output, once the Y' equation was correctly constructed onto the Breadboard. What this means is that since Y' gives the inverse of the output desired, we simply add a not gate at the end to give the correct output.

Components:

The components utilized to complete the experiment include:

- Gate 7404 (NOT gate)
- Gate 7408 (AND gate)
- Gate 7432 (OR gate)
- One resistor (output)
- LED light
- Breadboard
    - Cable wires
- Power supply (w/ 5v battery)

Experiment:

The purpose of this experiment was to first simplify and then construct the boolean equation Y' = (A+B') * (B+C+D) * (B'+C'+D') * (A'+C'+D')**.** This time we used the POS equation.

Simplification goes as follows:

Original equation: Y = A'B+B'C'D'+BCD+AB'CD

= CD (B + AB') + A'B + B'C'D'

= CD (A+B)

= A'B + B'C'D' + ACD + BCD (**Intended simplification from lab 2**)

Y' = (A'B + B'C'D' + BCD + ACD)' (**DeMorgan's Theorem**)

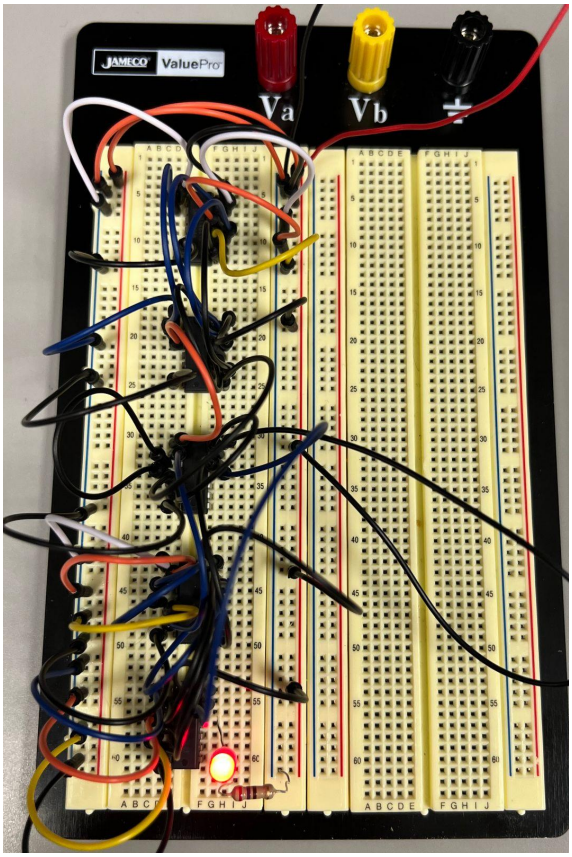
Y' = (A'B)' * (B'C'D')' * (BCD)' * (ACD)'

Y' = (A+B') * (B+C+D) * (B'+C'+D') * (A'+C'+D') (**Final simplification)**

Carlos Alvizo constructed a breadboard based on the equation Y' = (A+B') * (B+C+D) * (B'+C'+D') * (A'+C'+D'), but with another NOT gate at the end to ensure correct logical output to cancel out the Y' from the result of utilizing Demorgan's Theorem on both sides in order to get the POS form (as seen above).

The construction of the POS equation was fairly similar to that of the SOP equation with the major difference being that we utilized more OR gates rather than AND gates (the opposite of SOP form) and the final output being outputted to a NOT gate into the LED. The following breadboard (Figure 1) is the one that was presented to the TA and found that it was logically equivalent to the intended simplified form of the equation if the equation we utilized was correct.

Figure 1: Breadboard w/ Logically Equivalent Simplification



Note: From top to bottom the gates are NOT, OR,

AND, OR & NOT

All three equations being connected to the OR gate and outputted to an LED light with a resistor to test out if our logic aligns with that of the equation's truth tables.

The following is the truth table for the equation Y' = (A+B') * (B+C+D) * (B'+C'+D') * (A'+C'+D') simplified with POS form. The final column shows the output after a NOT gate.

A	**B**	**C**	**D**	**A+B'**	**B+C+D**	**B'+C'+D'**	**A'+C'+D'**	**(A+B') * (B+C+D) * (B'+C'+D') * (A'+C'+D')**	**((A+B') * (B+C+D) * (B'+C'+D') * (A'+C'+D'))'**
1	1	1	1	1	1	0	0	0	1
1	1	1	0	1	1	1	1	1	0
1	1	0	1	1	1	1	1	1	0
1	1	0	0	1	1	1	1	1	0
1	0	1	1	1	1	1	0	0	1
1	0	1	0	1	1	1	1	1	0
1	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	1
0	1	1	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1	0	1
0	1	0	1	0	1	1	1	0	1
0	1	0	0	0	1	1	1	0	1
0	0	1	1	1	1	1	1	1	0
0	0	1	0	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	0
0	0	0	0	1	0	1	1	0	1

Conclusion:

Carlos Alvizo's breadboard was shown to the Teaching Assistant, along with Carlos' pre-lab report. Carlos Alvizo and Samuel Lee both did prelab reports, but Carlos' prelab was shown in class. Carlos was responsible for breadboard construction, Samuel Lee was responsible for the majority of this lab report. We learned about the POS equation and how to construct this onto a breadboard as well as how it differs from its SOP counterpart.