

Lab 10: 7 Segment Display
EECE 2106.05

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Abstract

In Experiment 10 we designed a circuit with a 7 segment display. We tested these circuits based on the partial truth table given in the pdf for this lab, and had to use k maps to find an equation fit for the multiplexer part of this lab. One highlight was the 7 segment display itself, which is a new gate for this lab and was quite different from any other circuit used thus far and visibly showed the output.

Components:

The components utilized to complete the experiment include:

- Gate 74151 (MULT gate)
- Gate 7404 (NOT gate)
- Gate 7486 (XOR gate)
- Gate 7447 (7 segment display decoder)
- 7 segment display
- 1 resistor
- Two Breadboards (we both tried construction)
 - Cable wires
- Power supply (w/ 5v battery)
 - Multimeter

Experiment:

Here is the prelab. We were told to construct a breadboard that used a k map to find the proper equation. Here is the equation, the circuit, and the truth table is at the top of this page.

	^D x_1	^E x_2	^A x_3	^B x_4	^C x_5	No.	y_1	y_2
0	0	0	0	0	0	0	1	0
1	0	0	0	0	1	1	1	0
2	0	0	0	1	0	2	1	0
3	0	0	0	1	1	3	1	0
4	0	0	1	0	0	4	0	1
5	0	0	1	0	1	5	0	1
6	0	0	1	1	0	6	0	1
7	0	0	1	1	1	7	0	1
8	0	1	0	0	0	8	0	1
9	0	1	0	0	1	9	0	1
10	0	1	0	1	0	10	0	1
11	0	1	0	1	1	11	0	1
12	0	1	1	0	0	12	0	1
13	0	1	1	0	1	13	0	1
14	0	1	1	1	0	14	0	1
15	0	1	1	1	1	15	0	1
16	1	0	0	0	0	16	0	0
17	1	0	0	0	1	17	0	0
18	1	0	0	1	0	18	0	0
19	1	0	0	1	1	19	0	0
20	1	0	1	0	0	20	0	0
21	1	0	1	0	1	21	0	0
22	1	0	1	1	0	22	0	0
23	1	0	1	1	1	23	0	0
24	1	1	0	0	0	24	0	0
25	1	1	0	0	1	25	0	0
26	1	1	0	1	0	26	0	0
27	1	1	0	1	1	27	0	0
28	1	1	1	0	0	28	0	0
29	1	1	1	0	1	29	0	0
30	1	1	1	1	0	30	0	0
31	1	1	1	1	1	31	0	0

A blue
B yellow
C black
D white
E orange

BC	DE			
	00	01	11	10
00	1	1	1	1
01		1	1	1
11			1	
10			1	1

A = 0

BC	DE			
	00	01	11	10
00				
01				
11				
10				

A = 1

Expression for Y_2

$$Y_2 = \underline{A'B'C'} + \underline{A'B'E} + \underline{A'B'D} + \underline{A'DE} + \underline{A'C'D}$$

$$Y_2 \mid 1 + E + D + DE + D \Rightarrow 1$$

$$A=0, B=0, C=0$$

$$Y_2 \mid 0 + 0 + 0 + 0 + 0 \Rightarrow 0$$

$$A=1, B=0, C=0$$

$$Y_2 \mid 0 + E + D + DE + D \Rightarrow D + E$$

$$A=0, B=0, C=1$$

$$Y_2 \mid 0 + 0 + 0 + 0 + 0 \Rightarrow 0$$

$$A=1, B=0, C=1$$

$$Y_2 \mid 0 + 0 + 0 + DE + D \Rightarrow D$$

$$A=0, B=1, C=0$$

$$Y_2 \mid 0 + 0 + 0 + 0 + 0 \Rightarrow 0$$

$$A=1, B=1, C=0$$

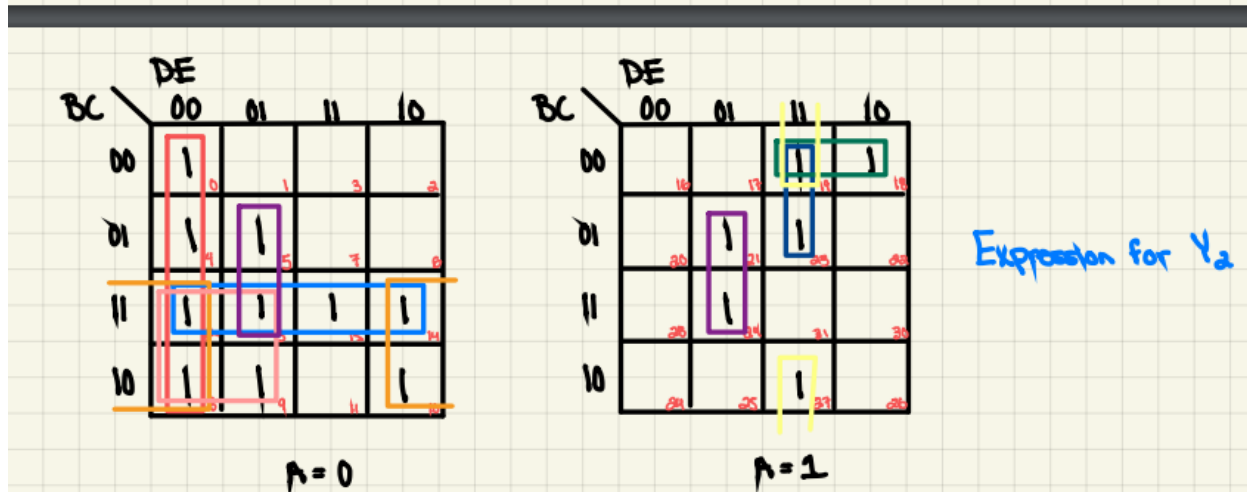
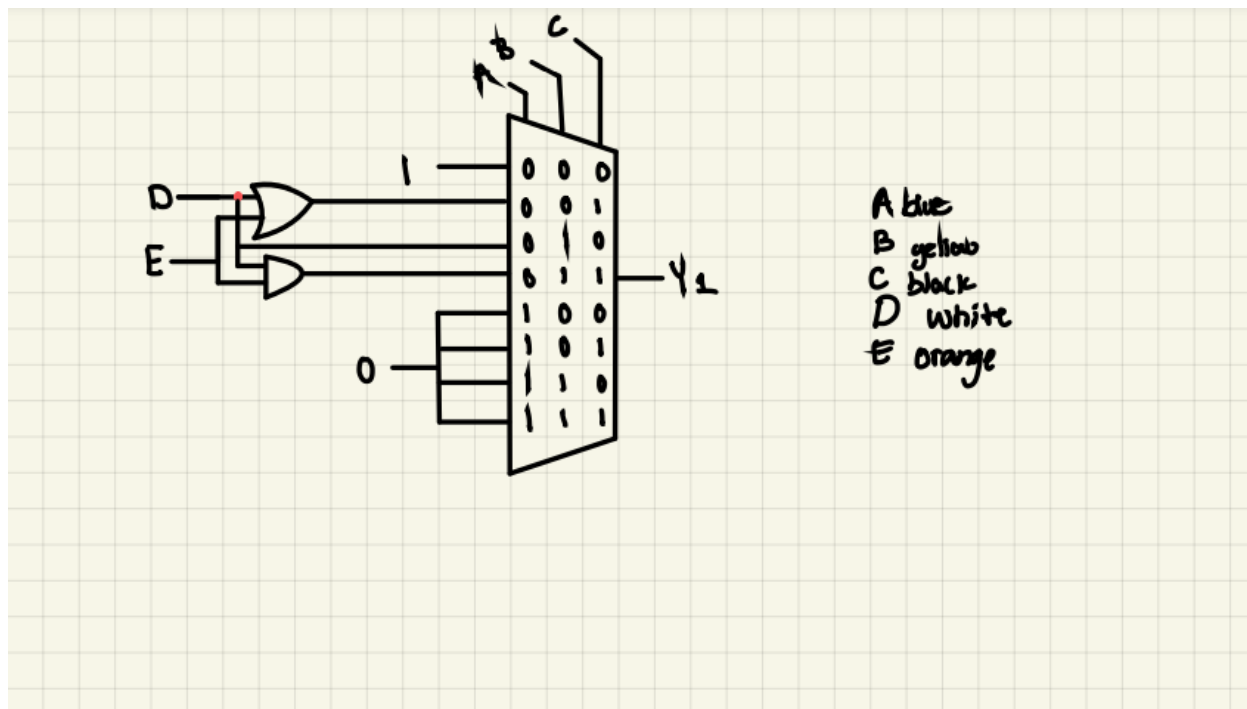
$$Y_2 \mid 0 + 0 + 0 + DE + 0 \Rightarrow DE$$

$$A=0, B=1, C=1$$

$$Y_2 \mid 0 + 0 + 0 + 0 + 0 \Rightarrow 0$$

$$A=1, B=1, C=1$$

Y1 equation and Shannon's Theorem



Y1 schematic (MUX) w/ bottom truth table of Y2

$$Y_2 = \underline{A'D'E'} + \underline{A'BC} + \underline{A'BE'} + \underline{A'BD'} + \underline{CD'E} + \underline{AB'DE} + \underline{ABC'D} + \underline{AC'DE}$$

$$Y_2 \mid \begin{array}{l} D'E' + 0 + 0 + 0 + 0 + 0 + 0 + 0 \\ A=0B=0C=0 \end{array} \Rightarrow D'E'$$

$$Y_2 \mid \begin{array}{l} 0 + 0 + 0 + 0 + 0 + DE + D + DE \\ A=1B=0C=0 \end{array} \Rightarrow D$$

$$Y_2 \mid \begin{array}{l} D'E' + 0 + 0 + 0 + D'E + 0 + 0 + 0 \\ A=0B=0C=1 \end{array} \Rightarrow D'$$

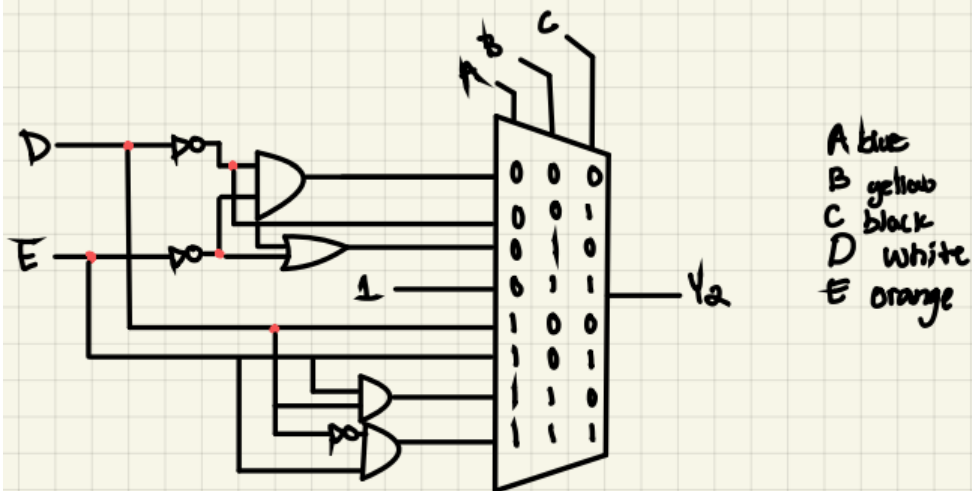
$$Y_2 \mid \begin{array}{l} 0 + 0 + 0 + 0 + D'E + DE + 0 + 0 \\ A=1B=0C=1 \end{array} \Rightarrow E$$

$$Y_2 \mid \begin{array}{l} D'E' + D'E' + D' + 0 + 0 + 0 + 0 \\ A=0B=1C=0 \end{array} \Rightarrow D' + E'$$

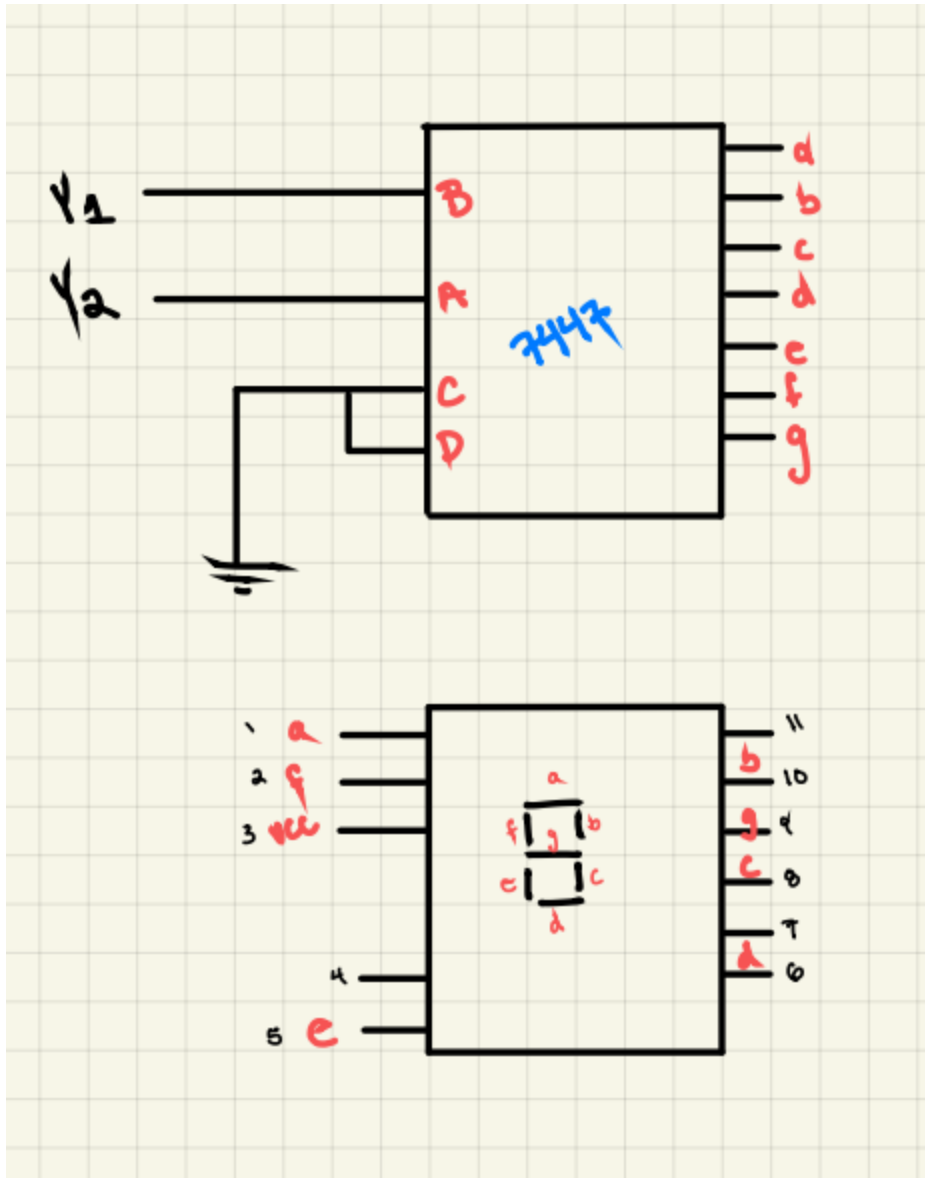
$$Y_2 \mid \begin{array}{l} 0 + 0 + 0 + 0 + 0 + 0 + 0 + DE \\ A=1B=1C=0 \end{array} \Rightarrow DE$$

$$Y_2 \mid \begin{array}{l} D'E' + 1 + E' + D' + D'E + 0 + 0 + 0 \\ A=0B=1C=1 \end{array} \Rightarrow 1$$

$$Y_2 \mid \begin{array}{l} 0 + 0 + 0 + 0 + D'E + 0 + 0 + 0 \\ A=1B=1C=1 \end{array} \Rightarrow D'E$$



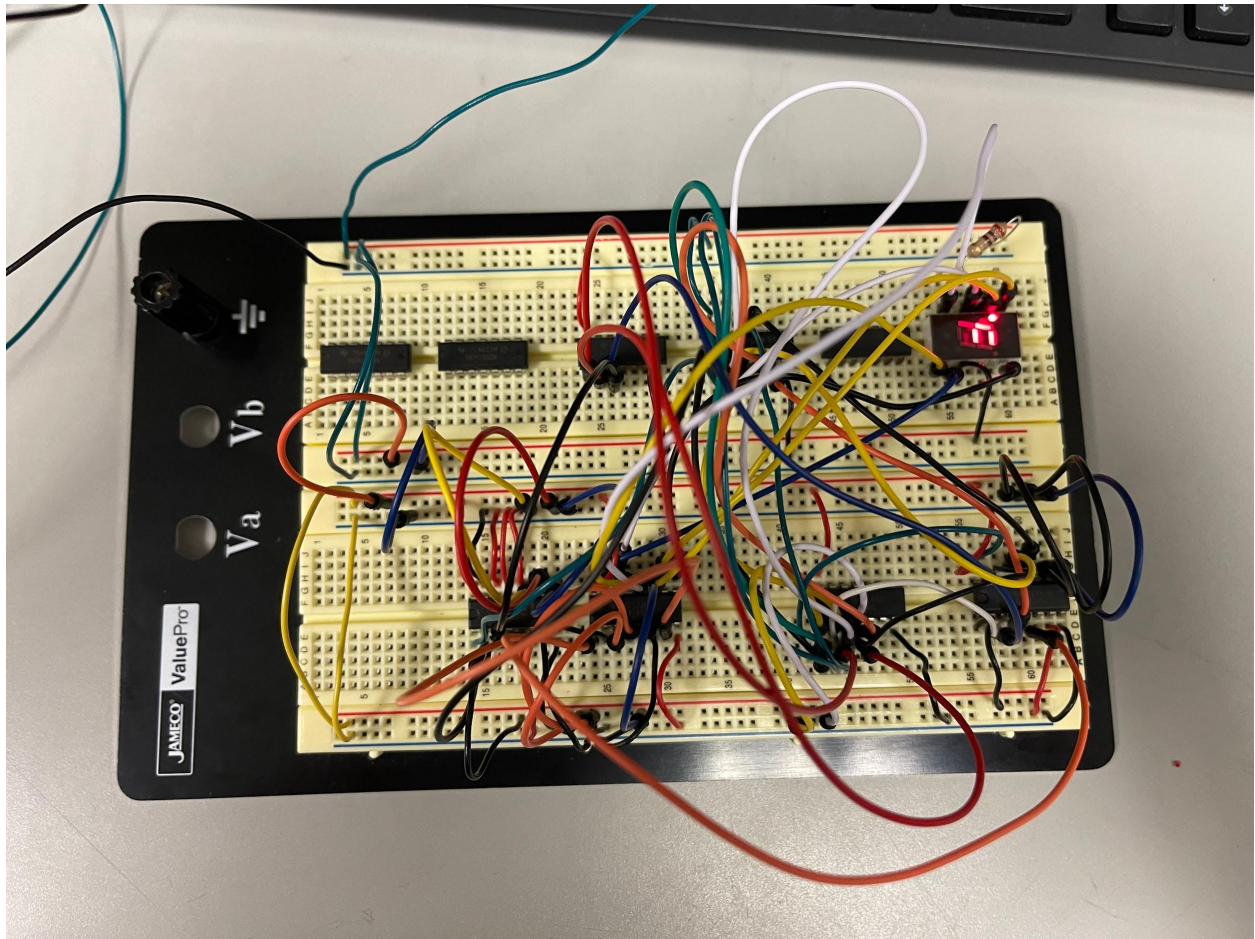
Y2 shannon's theorem and schematic (MUX)



7 segment decoder and 7 segment display schematic

Here is the completed breadboard. However, the breadboard was only partially working. Some inputs display the correct number, some inputs display the incorrect number. Faulty circuits may be the issue.

Samuel Lee - Problem 1 Breadboard



Conclusion:

Both teammates attempted breadboard construction. Samuel Lee was responsible for the truth table and half of this lab report, Carlos Alvizo was responsible for the rest of the prelab and half of this lab report. Unfortunately our circuits were only partially working and we ran out of time before being able to show the teaching assistant our partially working breadboard. The multiplexer gate was interesting, and had many different inputs/outputs to consider.