Lab 11: Memory Elements
EECE 2106.05

By: Samuel Lee & Carlos Alvizo

Abstract

In Experiment 11, we had to create an SR latch, a gated D latch, a master-slave latch. Circuits were constructed on a breadboard and we had to fill out multiple characteristic tables. One highlight was the multitude of circuits we had to build, ensuring that gates had the correct expected output.

Components:

The components utilized to complete the experiment include:

- Gate 7400 (NANDgate)
- Gate 7404 (NOT gate)
- Gate 7402 (NOR gate)
- 6 resistors
- 6 LED lights
- Breadboard
    - Cable wires
- Power supply (w/ 5v battery)
    - Multimeter

Experiment:

This experiment was divided into 12 problems.

1. Build the circuit on Figure 1 and test it by filling out and following the sequence on Table 1.

S	R	Q	Q'
0	1	0	1
0	0	0	1
1	0	1	0
0	0	1	0
0	1	0	1
1	0	1	0
1	1	0	0

Table 1 - SR Latch test

a.

2. What effect does setting both S and R to LOW have on the output Q?
    a. Setting S and R to low has Q and Q' set to the previous values (no change).
3. . With the information gathered from steps 1 and 2, fill out the characteristic table corresponding to an SR latch.

S	R	Q	Q'	
0	0	0/1	1/0	← No Change
0	1	0	1	
1	0	1	0	
1	1	0	0	← unstable

Table 2 - SR Latch Characteristic

a.

4. Alternate between S, R = 1 and S, R = 0, trying to change both inputs at exactly the same time. How do the outputs behave?
    a. S = R = 1 => Q and Q' = 0 (unstable output)
    b. S = R = 0 => Q and Q' = 0 (no change)
5. Build the circuit on Figure 2 and test it by filling out and following the sequence on Table 3.

Clk	S	R	Q	Q'
1	0	1	0	1
1	0	0	0	1
1	1	0	1	0
1	0	0	1	0
1	1	1	1	1
1	1	0	1	0
0	1	0	1	0
0	0	1	1	0
1	0	1	0	1
0	0	1	0	1
0	1	0	0	1

Table 3 - Gated SR Latch test

    a.
6. How does the input signal Clk affect the output Q?
    a. When Clk = 1 => changes are allowed, when Clk = 0 => no changes are allowed

7. With the information gathered from steps 4 and 5, fill out the characteristic table corresponding to a Gated SR latch.

Clk	S	R	Q(*t*+1)	
0	x	x	Q(t)	No change
1	0	0	Q(t)	No change
1	0	1	0	
1	1	0	1	
1	1	1	x	

Table 4 - Gated SR Latch Characteristic

a.

8. Build the circuit on Figure 4 and test it by filling out and following the sequence on Table 5

Clk	D	Q	
1	0	0	
1	1		
1	0	0	
1	1		
0	1	1	Q(t)
0	0	1	Q(t)
1	0	0	
0	0	0	Q(t)
0	1	0	Q(t)

Table 5 - Gated D Latch test

a.

9. How does the output Q on the Gated D latch behave in response to its inputs Clk and D?
    a. D = Q,
    b. Clk = 1 => changes are allowed,
    c. Clk = 0 => no changes
10. With the information gathered from steps 7 and 8, fill out the characteristic table corresponding to a Gated D latch.

Clk	D	Q(*t*+1)
0	x	Q(t)
1	0	0
1	1	1

Table 6 – Gated D Latch Characteristic

    a.
11. Build the circuit on Figure 6 and test it by filling out and following the sequence on Table 7. Demonstrate to lab instructor.

Clock	D	Q
0	0	0
0	1	0
1	1	0
0	1	1
0	0	1
1	0	1
0	0	0

Table 7 - Master-slave D flip-flop test

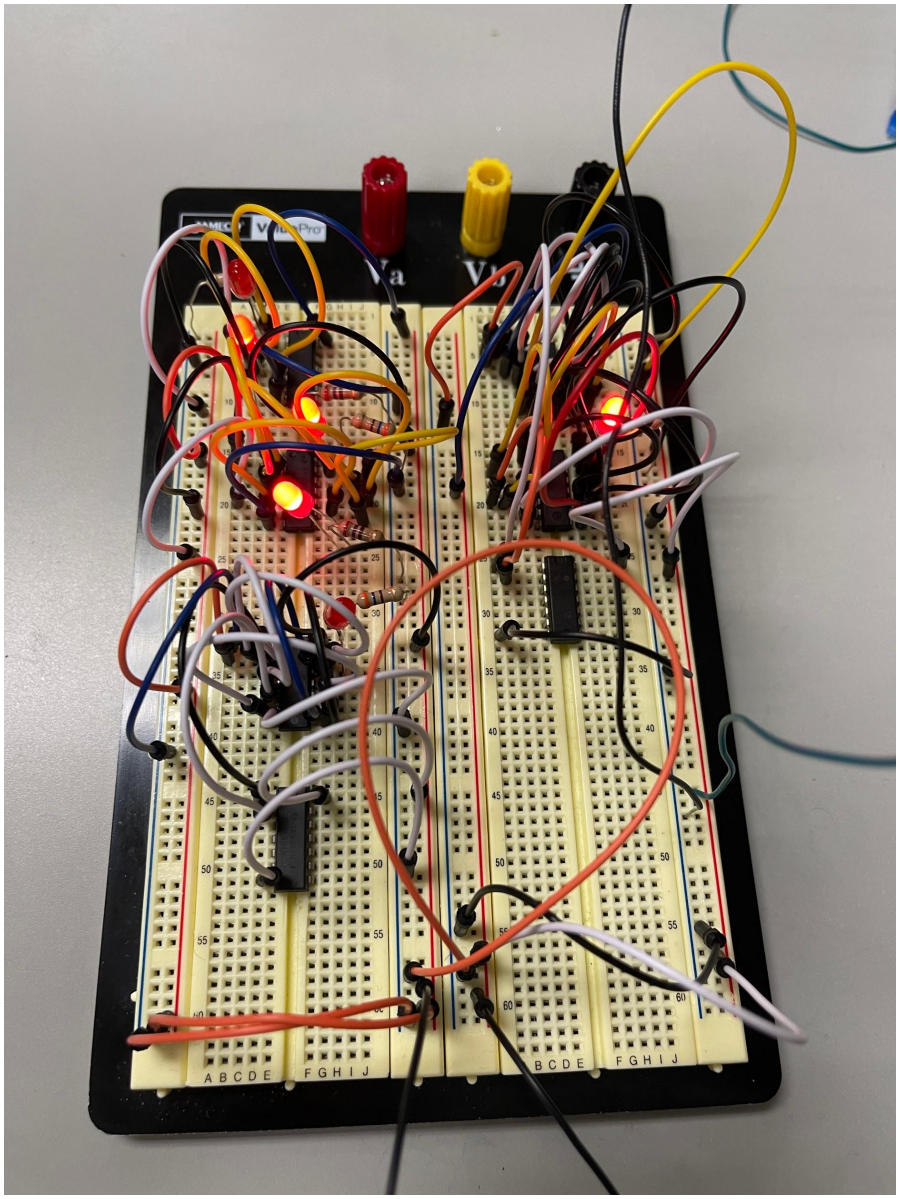
    a.

12. How does the behavior of the Master-slave D flip-flop differ from that of a Gated D latch?

    a. Master Slave D flip flop is negative-edge while Gated D latch is level.

Here is the completed breadboard for problems 1 - 12.

Carlos Alvizo - Breadboard



Conclusion:

Both teammates constructed a breadboard. Samuel Lee was responsible for the lab report, Carlos Alvizo was responsible for the prelab and the breadboard. Thankfully circuits seemed to be working, unlike last week. SR latch, master-slave, and gated D latch construction was successful. SR latch was interesting, had many different inputs/outputs to consider.