

D

The superscalar approach can be used on _____ architecture.

- A. RISC
- B. CISC
- C. neither RISC nor CISC
- D. both RISC and CISC

C

The essence of the _____ approach is the ability to execute instructions independently and concurrently in different pipelines.

- A. scalar
- B. branch
- C. superscalar
- D. flow dependency

D

Which of the following is a fundamental limitation to parallelism with which the system must cope? ★

- A. procedural dependency
- B. resource conflicts
- C. antidependency
- D. all of the above

A

The situation where the second instruction needs data produced by the first instruction to execute is referred to as _____. ★

- A. true data dependency
- B. output dependency
- C. procedural dependency
- D. antidependency

B

The instructions following a branch have a ____ on the branch and cannot be executed until the branch is executed. ★

- A. resource dependency
- B. procedural dependency
- C. output dependency
- D. true data dependency

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A

_____ refers to the process of initiating instruction execution in the processor's functional units.



- A. Instruction issue
- B. In-order issue
- C. Out-of-order issue
- D. Procedural issue

C

Instead of the first instruction producing a value that the second instruction uses, with _____ the second instruction destroys a value that the first instruction uses.



- A. in-order issue
- B. resource conflict
- C. antidependency
- D. out-of-order completion

A

_____ indicates whether this micro-op is scheduled for execution, has been dispatched for execution, or has completed execution and is ready for retirement.



- A. State
- B. Memory address
- C. Micro-op

Alias register

B

- _____ exists when instructions in a sequence are independent and thus can be executed in parallel by overlapping.
- A. Flow dependency
 - B. Instruction-level parallelism
 - C. Machine parallelism
 - D. Instruction issue

A

- _____ is determined by the number of instructions that can be fetched and executed at the same time and by the speed and sophistication of the mechanisms that the processor uses to find independent instructions.
- A. Machine parallelism
 - B. Instruction-level parallelism
 - C. Output dependency
 - D. Procedural dependency

D

- _____ is a protocol used to issue instructions.
- A. Micro-ops
 - B. Scalar
 - C. SIMD
 - D. Instruction issue policy

C

- _____ is used in scalar RISC processors to improve the performance of instructions that require multiple cycles.
- A. In-order completion
 - B. In-order issue
 - C. Out-of-order completion
 - D. Out-of-order issue



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D

- Which of the following is a hardware technique that can be used in a superscalar processor to enhance performance?
- A. duplication of resources
 - B. out-of-order issue
 - C. renaming
 - D. all of the above



B

The _____ introduced a full-blown superscalar design with out-of-order execution.

- A. Pentium
- B. Pentium Pro
- C. 386
- D. 486

C

Utilizing a branch target buffer (BTB), the _____ uses a dynamic branch prediction strategy based on the history of recent executions of branch instructions.

- A. 486
- B. Pentium
- C. Pentium 4
- D. Pentium Pro

QN=1 A taxonomy first introduced by ____ is still the most common way of categorizing systems with parallel processing capability.

- a. Randolph
- b. Flynn
- c. von Neuman
- d. Desai

Flynn

QN=2 Uniprocessors fall into the ____ category of computer systems.

- a. MIMD
- b. SIMD
- c. SISD
- d. MISD

SISD

QN=3 Vector and array processors fall into the _____ category of computer systems.

- a. SIMD
- b. SISD
- c. MISD
- d. MIMD

SIMD

QN=4 SMPs, clusters, and NUMA systems fit into the _____ category of computer systems.

- a. SISD
- b. MIMD
- c. SIMD
- d. MISD

MIMD

QN=5 A _____ problem arises when multiple copies of the same data can exist in different caches simultaneously, and if processors are allowed to update their own copies freely, an inconsistent view of memory can result.

- a. cache coherence
- b. cluster
- c. failover
- d. fallback

cache coherence

QN=6 Hardware-based solutions are generally referred to as cache coherence ____.

- a. clusters
- b. streams
- c. protocols
- d. vectors

protocols

QN=7 A _____ is an instance of a program running on a computer.

process

- a. process
- b. process switch
- c. thread
- d. thread switch

QN=8 A _____ is a dispatchable unit of work within a process that includes a processor context and its own data area for a stack.

thread

- a. process
- b. process switch
- c. thread
- d. thread switch

QN=9 Replicating the entire processor on a single chip with each processor handling separate threads is _____.

- a. interleaved multithreading
- b. blocked multithreading
- c. simultaneous multithreading
- d. chip multiprocessing

chip multiprocessing

QN=10 With no multithreading, _____ is the simple pipeline found in traditional RISC and CISC machines.

- a. superscalar
- b. single-threaded scalar
- c. blocked multithreaded scalar
- d. interleaved multithreaded scalar

single-threaded scalar

QN=11 _____ causes results issuing from one functional unit to be fed immediately into another functional unit and so on.

- a. Chaining
- b. Rollover
- c. Passive standby
- d. Pipelining

Chaining

QN=12 The _____ contains control fields, such as the vector count, that determine how many elements in the vector registers are to be processed.

- a. vector-mask register
- b. vector-activity count
- c. vector-status register
- d. vector-instruction register

vector-status register

QN=13 Which of the following is an approach to vector computation?

- a. pipelined ALU
- b. parallel ALU's
- c. parallel processors
- d. all of the above

all of the above

QN=14 An operation that switches the processor from one process to another by saving all the process control data, register, and other information for the first and replacing them with the process information for the second is:

- a. resource ownership switch
- b. process switch
- c. thread switch
- d. cluster switch

process switch

QN=15 With _____ instructions
are simultaneously issued from
multiple threads to the
execution units of a superscalar
processor.

SMT

- a. SMT
- b. single-threaded scalar
- c. coarse-grained
multithreading
- d. chip multiprocessing

A

With _____, register banks are replicated so that multiple threads can share the use of pipeline resources.

- A. SMT
- B. pipelining
- C. scalar
- D. superscalar

D

_____ is where individual instructions are executed through a pipeline of stages so that while one instruction is executing in one stage of the pipeline, another instruction is executing in another stage of the pipeline.

- A. Superscalar
- B. Scalar
- C. Pipelining
- D. Simultaneous multithreading

B

_____ is when multiple pipelines are constructed by replicating execution resources, enabling parallel execution of instructions in parallel pipelines so long as hazards are avoided.

- A. Vectoring
- B. Superscalar
- C. Hybrid multithreading
- D. Pipelining

B

One way to control power density is to use more of the chip area for _____.

- A. multicore
- B. cache memory
- C. silicon
- D. resistors

A

Lotus Domino or Siebel CRM are examples of _____ applications.

- A. threaded
- B. multi-process
- C. Java
- D. multi-instance

D Oracle database, SAP, and PeopleSoft are examples of _____ applications.

- A. Java
- B. multithreaded native
- C. multi-instance
- D. multi-process

C _____ applications that can benefit directly from multicore resources include application servers such as Sun's Java Application Server, BEA's Weblogic, IBM's Websphere, and the open-source Tomcat application server.

- A. Multi-instance
- B. Multi-process
- C. Java
- D. Threaded

A Putting rendering on one processor, AI on another, and physics on another is an example of _____ threading.

- A. coarse
- B. multi-instance
- C. fine-grained

B

A loop that iterates over an array of data can be split up into a number of smaller parallel loops in individual threads that can be scheduled in parallel when using _____ threading.



- A. multi-process
- B. fine-grained
- C. hybrid
- D. coarse

D

The _____ is an example of splitting off a separate, shared L3 cache, with dedicated L1 and L2 caches for each core processor.



- A. IBM 370
- B. ARM11 MPCore
- C. AMD Opteron
- D. Intel Core i7

C

The _____ connects to the external bus, known as the Front Side Bus, which connects to main memory, I/O controllers, and other processor chips.



- A. L2
- B. APIC
- C. bus interface
- D. all of the above

B

- The Intel Core i7-990X, introduced in 2008, implements ____ x86 SMT processors, each with a dedicated L2 cache, and with a shared L3 cache.
- A. 2
 - B. 4
 - C. 6
 - D. 8

AD



Stir up the season

Shop now

This is a Walmart advertisement for holiday mixers. It features the Walmart logo and the slogan "Stir up the season". Below the slogan is a photograph of several bottles of holiday-themed mixers, including "Merry & Bright" and "Cozy & Warm". A "Shop now" button is visible in the bottom right corner.

B

- Processors are called ____.
- A. dies
 - B. cores
 - C. QPI
 - D. interconnects

A

- The ____ feature enables moving dirty data from one CPU to another without writing to L2 and reading the data back in from external memory.
- A. migratory lines
 - B. DDI
 - C. VFP unit
 - D. IPIs

C

- The ____ is responsible for maintaining coherency among L1 data caches.
- A. VFP unit
 - B. distributed interrupt controller
 - C. snoop control unit (SCU)
 - D. watchdog

1. A single micro-operation generally involves which of the following?

D

- A. a transfer between registers
- B. a transfer between a register and an external bus
- C. a transfer between a register and the ALU
- D. all of the above

1. Each instruction executed during an instruction cycle is made up of shorter ____.

B

- A. executions
- B. subcycles
- C. steps
- D. none of the above

1. _____ are the functional, or atomic, operations of a processor.

- A. Micro-operations
- B. Interrupts
- C. Subcycles
- D. All of the above

A

1. The _____ cycle occurs at the beginning of each instruction cycle and causes an instruction to be fetched from memory.

- A. execute
- B. indirect
- C. fetch
- D. interrupt

C

1. The _____ is connected to the address lines of the system bus.

B

- A. MBR
- B. MAR
- C. PC
- D. IR

1. The _____ is connected to the data lines of the system bus.

C

- A. MAR
- B. PC
- C. MBR
- D. IR

1. The _____ holds the address of the next instruction to be fetched.

B

- A. IR
- B. PC
- C. MAR
- D. MBR

1. The _____ holds the last instruction fetched.

D

A. PC B. MBR

C. MAR D. IR

1. The groupings of micro-operations must follow which rule?

C

A. a sequence of events does not need to be followed

B. use read to and write from the same register in one time unit

C. conflicts must be avoided

D. all of the above

1. The _____ designates the state of the processor in terms of which portion of the cycle it is in.

A

A. ICC B. BSA

C. ALE D. ISC

1. Machine cycles are defined to be equivalent to _____ accesses.

B

A. flag B. bus

C. clock D. path

1. The _____ portion of the control unit issues a repetitive sequence of pulses.

D

- A. instruction register
- B. flag
- C. control bus signals
- D. clock

1. The _____ pulse signals the start of each machine cycle from the control unit and alerts external circuits.

C

- A. AC
- B. INSTR
- C. ALE
- D. OUT

1. Which of the following is an Intel 8085 external signal?

D

- A. CLK(OUT)
- B. read control
- C. HOLDA
- D. all of the above

1. The _____ module handles multiple levels of interrupt signals.

A

- A. interrupt control
- B. incrementer address latch
- C. serial I/O control
- D. decrementer address latch

QN=1 The term microprogram was first coined by _____ in the early 1950s.

- a. M.V. Wilkes
- b. D. Siewiorek
- c. M. Sebern
- d. S. Tucker

A

QN=2 The set of microinstructions is stored in the _____.

- a. control address register
- b. control buffer register
- c. control memory
- d. control word

C

QN=3 The _____ contains the address of the next microinstruction to be read.

- a. control memory
- b. control address register
- c. control word
- d. control buffer register

B

QN=4 When a microinstruction is read from the control memory it is transferred to a _____.
_____.

- a. control buffer register
- b. control memory
- c. control address register
- d. control unit

A

QN=5 Which of the following is a control unit input?

- a. IR
- b. ALU flags
- c. clock
- d. all of the above

D

QN=6 In executing a microprogram the address of the next microinstruction to be executed is in which of the following categories?

- a. determined by instruction register
- b. branch
- c. next sequential address
- d. all of the above

D

QN=7 The terms _____ relate to the relative width of microinstructions.

- a. packed/unpacked
- b. hard/soft
- c. horizontal/vertical
- d. direct/indirect

C

AD

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Exclusions apply.



QN=8 The terms _____ microprogramming are used to suggest the degree of closeness to the underlying control signals and hardware layout.

- a. hard/soft
- b. horizontal/vertical
- c. direct/indirect
- d. packed/unpacked

A

QN=9 With _____ encoding one field is used to determine the interpretation of another field.

B

- a. resource
- b. indirect
- c. direct
- d. functional

QN=10 Which of the following is a LSI-11 microinstruction?

D

- a. add word
- b. test word
- c. Jump
- d. all of the above

QN=11 The standard IBM 3033 control memory consists of _____ words.

C

- a. 2K
- b. 8K
- c. 4K
- d. 16K

QN=12 The _____ allows multiple levels of nested calls or interrupts and it can be used to support branching and looping.

- a. stack
- b. register
- c. counter
- d. firmware

A

QN=13 The _____ is a 32-bit ALU with 64 registers that can be configured to operate as four 8-bit ALUs, two 16-bit ALUs, or a single 32-bit ALU.

- a. PDP-11
- b. 8832
- c. 3033
- d. 8818

B

QN=14 _____ is a subfield that is used to indicate a conditional branch.

- a. ZERION
- b. S2-S0
- c. SELDR
- d. OSEL

A

QN=15 A _____ is a combinatorial circuit that generates an address based on the microinstruction, the machine instruction, the microinstruction program counter, and an interrupt register.

- a. microsequencer
- b. vertical microinstruction
- c. translation array
- d. control word

C

rapid

QN=16 Computer technology is changing at a _____ pace.



- a. slow
- b. slow to medium
- c. rapid
- d. non-existent

architecture

QN=17 Computer _____ refers to those attributes that have a direct impact on the logical execution of a program.



- a. organization
- b. specifics
- c. design
- d. architecture



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I/O mechanisms

QN=18 Architectural attributes include _____ .



- a. I/O mechanisms
- b. control signals
- c. interfaces

Organizational

QN=19 _____ attributes include hardware details transparent to the programmer.



- a. Interface
- b. Organizational
- c. Memory
- d. Architectural

architectural

QN=20 It is a(n) _____ design issue whether a computer will have a multiply instruction.



- a. architectural
- b. memory
- c. elementary
- d. organizational

organizational

QN=21 It is a(n) _____ issue whether the multiply instruction will be implemented by a special multiply unit or by a mechanism that makes repeated use of the add unit of the system.



- a. architectural
- b. memory
- c. mechanical
- d. organizational

hierarchical

QN=22 A _____ system is a set of interrelated subsystems.



- a. secondary
- b. hierarchical
- c. complex
- d. functional

peripheral

QN=23 An I/O device is referred to as a _____.



- a. CPU
- b. control device
- c. peripheral
- d. register

data communications

QN=24 When data are moved over longer distances, to or from a remote device, the process is known as _____.



- a. data communications
- b. registering
- c. structuring
- d. data transport

main memory

QN=25 The _____ stores data.

- a. system bus
- b. I/O
- c. main memory
- d. control unit

I/O

QN=26 The _____ moves data between the computer and its external environment.

- a. data transport
- b. I/O
- c. register
- d. CPU interconnection

system bus

QN=27 A common example of system interconnection is by means of a _____.

- a. register
- b. system bus
- c. data transport
- d. control device

system interconnection

QN=28 A _____ is a mechanism that provides for communication among CPU, main memory, and I/O.

- a. system interconnection
- b. CPU interconnection
- c. peripheral
- d. processor



Registers

QN=29 _____ provide storage internal to the CPU.

- a. Control units
- b. ALUs
- c. Main memory
- d. Registers



ALU

QN=30 The _____ performs the computer's data processing functions.

- a. Register
- b. CPU interconnection
- c. ALU
- d. system bus



Amdahlâ€™s

_____ law deals with the potential speedup of a program using multiple processors compared to a single processor.

Arithmetic

The _____ Mean used for a time-based variable, such as program execution time, has the important property that it is directly proportional to the total time.

Base

_____ metric are required for all reported results and have strict guidelines for compilation.

benchmark

A _____ suite is a collection of programs, defined in a high-level language, that together attempt to provide a representative test of a computer in a particular application or system programming area.

branch prediction	With _____ the processor looks ahead in the instruction code fetched from memory and predicts which branches, or groups of instructions, are likely to be processed next.
geometric	The three common formulas used for calculating a mean are arithmetic, harmonic, and _____ .
Geometric	The _____ Mean gives consistent results regardless of which system is used as a reference.
GPU (graphics processing units)	Traditionally found on a plug-in graphics card, a _____ is used to encode and render 2D and 3D graphics as well as process video.
Harmonic	The _____ Mean is preferred when calculating rates.
Hertz (Hz)	At the most fundamental level, the speed of a processor is dictated by the pulse frequency produced by the clock, measured in cycles per second, or _____.

Littleâ€™s

_____ Law applies to a queuing system.

Pipelining

_____ enables a processor to work simultaneously on multiple instructions by performing a different phase for each of the multiple instructions at the same time.

Speculative execution

_____ enables the processor to keep its execution engines as busy as possible by executing instructions that are likely to be needed.

Superscalar execution

_____ is the ability to issue more than one instruction in every processor clock cycle.

System Performance Evaluation Corporation (SPEC)

The best-known collection of benchmark suites is defined and maintained by an industry consortium known as _____.

John von Neumann

Virtually all contemporary computer designs are based on concepts developed by _____ at the Institute for Advanced Studies, Princeton.
a. John Maulchy
b. John von Neumann
c. Herman Hollerith
d. John Eckert

all of the above

The von Neumann architecture is based on which concept?
a. data and instructions are stored in a single read-write memory
b. the contents of this memory are addressable by location
c. execution occurs in a sequential fashion
d. all of the above

software

A sequence of codes or instructions is called _____.

- a. software
- b. memory
- c. an interconnect
- d. a register

instruction

The processing required for a single instruction is called a(n) _____ cycle.

- a. execute
- b. fetch
- c. instruction
- d. packet

hardware failure interrupt

A(n) _____ is generated by a failure such as power failure or memory parity error.

- a. I/O interrupt
- b. hardware failure interrupt
- c. timer interrupt
- d. program interrupt

program interrupt

A(n) _____ is generated by some condition that occurs as a result of an instruction execution.

- a. timer interrupt
- b. I/O interrupt
- c. program interrupt
- d. hardware failure interrupt

all of the above

The interconnection structure must support which transfer?

- a. memory to processor
- b. processor to memory
- c. I/O to or from memory
- d. all of the above

system bus

A bus that connects major computer components (processor, memory, I/O) is called a _____.

- a. system bus
- b. address bus
- c. data bus
- d. control bus

address lines

The _____ are used to designate the source or destination of the data on the data bus.

- a. system lines
- b. data lines
- c. control lines
- d. address lines

data bus

The data lines provide a path for moving data among system modules and are collectively called the _____.

- a. control bus
- b. address bus
- c. data bus
- d. system bus

protocol

A _____ is the high-level set of rules for exchanging packets of data between devices.

- a. bus
- b. protocol
- c. packet
- d. QPI

lane

Each data path consists of a pair of wires (referred to as a _____) that transmits data one bit at a time.

- a. lane
- b. path
- c. line
- d. bus



transaction layer

The _____ receives read and write requests from the software above the TL and creates request packets for transmission to a destination via the link layer.

- a. transaction layer
- b. root layer
- c. configuration layer
- d. transport layer

all of the above

The TL supports which of the following address spaces?

- a. memory
- b. I/O
- c. message
- d. all of the above

routing

The QPI _____ layer is used to determine the course that a packet will traverse across the available system interconnects.

- a. link
- b. protocol
- c. routing
- d. physical

Location

QN=1 _____ refers to whether memory is internal or external to the computer.

- a. Location
- b. Access
- c. Hierarchy
- d. Tag



bytes

QN=2 Internal memory capacity is typically expressed in terms of _____.

- a. hertz
- b. nanos
- c. bytes
- d. LOR



unit of transfer

QN=3 For internal memory, the _____ is equal to the number of electrical lines into and out of the memory module.

- a. access time
- b. unit of transfer
- c. capacity
- d. memory ratio

sequential access

QN=4 "Memory is organized into records and access must be made in a specific linear sequence" is a description of _____.
a. sequential access
b. direct access
c. random access
d. associative

direct access

QN=5 individual blocks or records have a unique address based on physical location with _____.
a. associative
b. physical access
c. direct access
d. sequential access

access time

QN=6 For random-access memory, _____ is the time from the instant that an address is presented to the memory to the instant that data have been stored or made available for use.

- a. memory cycle time
- b. direct access
- c. transfer rate
- d. access time



memory cycle time

QN=7 The _____ consists of the access time plus any additional time required before a second access can commence.

- a. latency
- b. memory cycle time
- c. direct access
- d. transfer rate



disk cache

QN=8 A portion of main memory used as a buffer to hold data temporarily that is to be read out to disk is referred to as a _____.

- a. disk cache
- b. latency
- c. virtual address
- d. alias



tag

QN=9 A line includes a _____ that identifies which particular block is currently being stored.

- a. cache
- b. hit
- c. tag
- d. locality

Direct mapping

QN=10 _____ is the simplest mapping technique and maps each block of main memory into only one possible cache line.

- a. Direct mapping
- b. Associative mapping
- c. Set associative mapping
- d. None of the above

write through

QN=11 When using the _____ technique all write operations made to main memory are made to the cache as well.

- a. write back
- b. LRU
- c. write through
- d. unified cache

split cache

QN=12 The key advantage of the _____ design is that it eliminates contention for the cache between the instruction fetch/decode unit and the execution unit.

- a. logical cache
- b. split cache
- c. unified cache
- d. physical cache



execution unit

QN=13 The Pentium 4 _____ component executes micro-operations, fetching the required data from the L1 data cache and temporarily storing results in registers.

- a. fetch/decode unit
- b. out-of-order execution logic
- c. execution unit
- d. memory subsystem



[k/click?imp=587b557c-f923-4a2c-b3d5-a8a7b4a8402d&aq=l6...](#)

miss

- QN=14 In reference to access time to a two-level memory, a _____ occurs if an accessed word is not found in the faster memory.
- a. miss
 - b. hit
 - c. line
 - d. tag

virtual addresses

- QN=15 A logical cache stores data using _____.
- a. physical addresses
 - b. virtual addresses
 - c. random addresses
 - d. none of the above

QN=1 Which properties do all semiconductor memory cells share?

- a. they exhibit two stable states which can be used to represent binary 1 and 0
- b. they are capable of being written into to set the state
- c. they are capable of being read to sense the state
- d. all of the above

all of the above

QN=2 One distinguishing characteristic of memory that is designated as _____ is that it is possible to both to read data from the memory and to write new data into the memory easily and rapidly.

- a. RAM
- b. ROM
- c. EPROM
- d. EEPROM

RAM

QN=3 Which of the following memory types are nonvolatile?

- a. erasable PROM
- b. programmable ROM
- c. flash memory
- d. all of the above

all of the above

QN=4 In a _____, binary values are stored using traditional flip-flop logic-gate configurations.

- a. ROM
- b. SRAM
- c. DRAM
- d. RAM

SRAM

QN=5 A _____ contains a permanent pattern of data that cannot be changed, is nonvolatile, and cannot have new data written into it.

ROM

RAM

QN=6 With _____ the microchip is organized so that a section of memory cells are erased in a single action.

- a. flash memory
- b. SDRAM
- c. DRAM
- d. EEPROM

flash memory

QN=7 _____ can be caused by harsh environmental abuse, manufacturing defects, and wear.

- a. SEC errors
- b. Hard errors
- c. Syndrome errors
- d. Soft errors

Hard errors

QN=8 _____ can be caused by power supply problems or alpha particles.

- a. Soft errors

Soft errors

QN=9 The _____ exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states.

- a. DDR-DRAM
- b. SDRAM
- c. CDRAM
- d. none of the above

SDRAM

QN=10 _____ can send data to the processor twice per clock cycle.

- a. CDRAM
- b. SDRAM
- c. DDR-DRAM
- d. RDRAM

DDR-DRAM

QN=11 _____ increases the data transfer rate by increasing the operational frequency of the RAM chip and by increasing the prefetch buffer from 2 bits to 4 bits per chip.

DDR2

- a. DDR2
- b. RDRAM
- c. CDRAM
- d. DDR3

QN=12 _____ increases the prefetch buffer size to 8 bits.

DDR3

QN=13 Theoretically, a DDR module can transfer data at a clock rate in the range of _____ MHz.

200 to 600

- a. 200 to 600
- b. 400 to 1066
- c. 600 to 1400
- d. 800 to 1600

QN=14 A DDR3 module transfers data at a clock rate of _____ MHz.

800 to 1600

- a. 600 to 1200
- b. 800 to 1600
- c. 1000 to 2000
- d. 1500 to 3000

QN=15 The _____ enables the RAM chip to preposition bits to be placed on the data bus as rapidly as possible.
a. flash memory

buffer

the glass substrate

Greater ability to withstand shock and damage, improvement in the uniformity of the magnet film surface to increase disk reliability, and a significant reduction in overall surface defects to help reduce read-write errors, are all benefits of _____.

- a. magnetic read and write mechanisms
- b. platters
- c. the glass substrate
- d. a solid state drive

gaps

Adjacent tracks are separated by _____.

- a. sectors
- b. gaps
- c. pits
- d. heads

sectors

Data are transferred to and from the disk in _____.  

- a. tracks
- b. gaps
- c. sectors
- d. pits

512

In most contemporary systems fixed-length sectors are used, with _____ bytes being the nearly universal sector size.  

- a. 64
- b. 128
- c. 256
- d. 512

constant angular velocity

Scanning information at the same rate by rotating the disk at a fixed speed is known as the _____.  

- a. constant angular velocity
- b. magnetoresistive
- c. rotational delay
- d. constant linear velocity

CAV

The disadvantage of _____ is that the amount of data that can be stored on the long outer tracks is only the same as what can be stored on the short inner tracks.

- a. SSD
- b. CAV
- c. ROM
- d. CLV

nonremovable

A _____ disk is permanently mounted in the disk drive, such as the hard disk in a personal computer.

- a. nonremovable
- b. movable-head
- c. double sided
- d. removable

double sided

When the magnetizable coating is applied to both sides of the platter the disk is then referred to as _____.

- a. multiple sided
- b. substrate
- c. double sided
- d. all of the above

cylinder

The set of all the tracks in the same relative position on the platter is referred to as a _____.
a. floppy disk
b. single-sided disk
c. sector
d. cylinder

access time

The sum of the seek time and the rotational delay equals the _____, which is the time it takes to get into position to read or write.
a. access time
b. gap time
c. transfer time
d. constant angular velocity

RAID

_____ is the standardized scheme for multiple-disk database design.
a. RAID
b. CAV
c. CLV
d. SSD

1

RAID level _____ has the highest disk overhead of all RAID types.



- a. 0
- b. 1
- c. 3
- d. 5



Blu-ray DVD

A _____ is a high-definition video disk that can store 25 Gbytes on a single layer on a single side.



- a. DVD
- b. DVD-R
- c. DVD-RW
- d. Blu-ray DVD

Constant linear velocity (CLV)

_____ is when the disk rotates more slowly for accesses near the outer edge than for those near the center.

- a. Constant angular velocity (CAV)
- b. Magnetoresistive
- c. Constant linear velocity (CLV)
- d. Seek time

lands

The areas between pits are called _____.

- a. lands
- b. sectors
- c. cylinders
- d. strips

Terms In this set (30)

Original

I/O module

QN=1 The _____ contains logic for performing a communication function between the peripheral and the bus.

- a. I/O channel
- b. I/O module
- c. I/O processor
- d. I/O command

keyboard/monitor

QN=2 The most common means of computer/user interaction is a _____.

- a. keyboard/monitor
- b. mouse/printer
- c. modem/printer
- d. monitor/printer

control and timing

QN=3 The I/O function includes a _____ requirement to coordinate the flow of traffic between internal resources and external devices.

- a. cycle
- b. status reporting
- c. control and timing
- d. data



I/O channel

QN=4 An I/O module that takes on most of the detailed processing burden, presenting a high-level interface to the processor, is usually referred to as an _____.

- a. I/O channel
- b. I/O command
- c. I/O controller
- d. device controller



I/O controller

QN=5 An I/O module that is quite primitive and requires detailed control is usually referred to as an _____.

- a. I/O command
- b. I/O controller



write

QN=6 The _____ command causes the I/O module to take an item of data from the data bus and subsequently transmit that data item to the peripheral.

- a. control
- b. test
- c. read
- d. write

control

QN=7 The _____ command is used to activate a peripheral and tell it what to do.

- a. control
- b. test
- c. read
- d. write

cycle stealing

QN=8 _____ is when the DMA module must force the processor to suspend operation temporarily.

- a. Interrupt
- b. Thunderbolt
- c. Cycle stealing
- d. Lock down

fly-by

QN=9 The 8237 DMA is known as a _____ DMA controller.



- a. command
- b. cycle stealing
- c. interrupt
- d. fly-by

DisplayPort

QN=10 _____ is a digital display interface standard now widely adopted for computer monitors, laptop displays, and other graphics and video interfaces.



- a. DisplayPort
- b. PCI Express
- c. Thunderbolt
- d. InfiniBand

common transport

QN=11 The _____ layer is the key to the operation of Thunderbolt and what makes it attractive as a high-speed peripheral I/O technology.



- a. cable
- b. application
- c. common transport

physical

QN=12 The Thunderbolt protocol _____ layer is responsible for link maintenance including hot-plug detection and data encoding to provide highly efficient data transfer.

- a. cable
- b. application
- c. common transport
- d. physical



application

QN=13 The _____ contains I/O protocols that are mapped on to the transport layer.

- a. cable
- b. application
- c. common transport
- d. physical

target channel adapter	QN=14 A _____ is used to connect storage systems, routers, and other peripheral devices to an InfiniBand switch. a. target channel adapter b. InfiniBand switch c. host channel adapter d. subnet
router	QN=15 A _____ connects InfiniBand subnets, or connects an InfiniBand switch to a network such as a local area network, wide area network, or storage area network. a. memory controller b. TCA c. HCA d. router
False	QN=15 A Thunderbolt compatible peripheral interface is no more complex than that of a simple USB device. a. True b. False

False	<p>QN=14 A multipoint external interface provides a dedicated line between the I/O module and the external device.</p> <p>a. True b. False</p>
True	<p>QN=13 An I/O channel has the ability to execute I/O instructions, which gives it complete control over I/O operations.</p> <p>a. True b. False</p>
True	<p>QN=12 When large volumes of data are to be moved, a more efficient technique is direct memory access (DMA).</p> <p>a. True b. False</p>
True	<p>QN=11 Because the 82C55A is programmable via the control register, it can be used to control a variety of simple peripheral devices.</p> <p>a. True</p>

False

QN=10 The rotating interrupt mode allows the processor to inhibit interrupts from certain devices.

- a. True
- b. False

True

QN=9 Bus arbitration makes use of vectored interrupts.

- a. True
- b. False

False

QN=8 With a daisy chain the processor just picks the interrupt line with the highest priority.

- a. True
- b. False

True

QN=7 The disadvantage of the software poll is that it is time consuming.

- a. True
- b. False

True	QN=6 A disadvantage of memory-mapped I/O is that valuable memory address space is used up. a. True b. False
False	QN=5 With isolated I/O there is a single address space for memory locations and I/O devices. a. True b. False
True	QN=4 It is the responsibility of the processor to periodically check the status of the I/O module until it finds that the operation is complete. a. True b. False
False	QN=3 I/O channels are commonly seen on microcomputers, whereas I/O controllers are used on mainframes. a. True

False

QN=3 I/O channels are commonly seen on microcomputers, whereas I/O controllers are used on mainframes.

- a. True
- b. False

True

QN=2 An I/O module must recognize one unique address for each peripheral it controls.

- a. True
- b. False

True

QN=1 A set of I/O modules is a key element of a computer system.

- a. True
- b. False

operating system

QN=1 The _____ is a program that controls the execution of application programs and acts as an interface between applications and the computer hardware.

- a. job control language
- b. operating system
- c. batch system
- d. nucleus

utility

QN=2 Facilities and services provided by the OS that assist the programmer in creating programs are in the form of _____ programs that are not actually part of the OS but are accessible through the OS.

- a. utility
- b. multitasking
- c. JCL
- d. logical address

ISA

QN=3 The _____ defines the repertoire of machine language instructions that a computer can follow.

- a. ABI
- b. API
- c. HLL
- d. ISA

ABI

QN=4 The _____ defines the system call interface to the operating system and the hardware resources and services available in a system through the user instruction set architecture.

- a. HLL
- b. API
- c. ABI
- d. ISA

API

QN=5 The _____ gives a program access to the hardware resources and services available in a system through the user instruction set architecture supplemented with high-level language library calls.

- a. ICI

uniprogramming QN=6 A _____ system works only one program at a time.

- a. batch
- b. uniprogramming
- c. kernel
- d. privileged instruction

job control language QN=7 A _____ is a special type of programming language used to provide instructions to the monitor.

- a. job control language
- b. multiprogram
- c. kernel
- d. utility

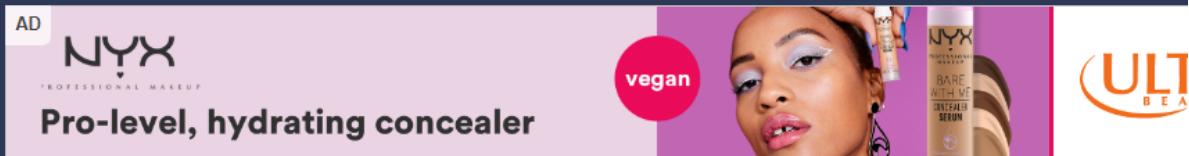
long-term QN=8 The _____ scheduler determines which programs are admitted to the system for processing.

- a. long-term

short-term	QN=9 The _____ scheduler is also known as the dispatcher. a. long-term b. medium-term c. short-term d. I/O
physical address	QN=10 A _____ is an actual location in main memory. a. logical address b. partition address c. base address d. physical address
thrashing	QN=11 _____ is when the processor spends most of its time swapping pages rather than executing instructions. a. Swapping

TLB

- QN=12 Virtual memory schemes make use of a _____ for page table entries.
- a. TLB
 - b. HLL
 - c. VMC
 - d. SPB



unsegmented unpaged
memory

- QN=13 With _____ the virtual address is the same as the physical address.
- a. unsegmented unpaged memory
 - b. unsegmented paged memory
 - c. segmented unpaged memory
 - d. segmented paged memory

domain

- QN=14 A _____ is a collection of memory regions.
- a. APX
 - b. nucleus

page table

- QN=15 The OS maintains a _____ for each process that shows the frame location for each page of the process.
- a. kernel
 - b. page table
 - c. TLB
 - d. logical address

opcode

QN=1 The _____ specifies the operation to be performed.

- a. source operand reference
- b. opcode
- c. next instruction reference
- d. processor register

high-level language

QN=2 A(n) _____ expresses operations in a concise algebraic form using variables.

- a. opcode
- b. high-level language
- c. machine language
- d. register

memory

QN=3 There must be _____ instructions for moving data between memory and the registers.

- a. branch
- b. logic
- c. memory
- d. I/O

logic

QN=4 _____ instructions operate on the bits of a word as bits rather than as numbers, providing capabilities for processing any other type of data the user may wish to employ.

- a. Logic
- b. Arithmetic
- c. Memory
- d. Test

arithmetic

QN=5 _____ instructions provide computational capabilities for processing number data.

- a. Boolean
- b. Logic
- c. Memory
- d. Arithmetic

I/O

QN=6 _____ instructions are needed to transfer programs and data into memory and the results of computations back out to the user.

- a. I/O
- b. Transfer
- c. Control
- d. Branch

integer

QN=7 The x86 data type that is a signed binary value contained in a byte, word, or doubleword, using two's complement representation is _____.

- a. general
- b. ordinal
- c. integer
- d. packed BCD

data transfer

QN=8 The most fundamental type of machine instruction is the _____ instruction.

- a. conversion
- b. data transfer
- c. arithmetic
- d. logical

skip

QN=9 The _____ instruction includes an implied address.

- a. skip
- b. rotate
- c. stack
- d. push

all of the above

QN=10 Which of the following is a true statement?

- a. a procedure can be called from more than one location
- b. a procedure call can appear in a procedure
- c. each procedure call is matched by a return in the called program
- d. all of the above

stack frame

QN=11 The entire set of parameters, including return address, which is stored for a procedure invocation is referred to as a _____.

- a. branch
- b. stack frame
- c. pop
- d. push

data-processing instructions

QN=12 Which ARM operation category includes logical instructions (AND, OR, XOR), add and subtract instructions, and test and compare instructions?

- a. data-processing instructions
- b. branch instructions
- c. load and store instructions
- d. extend instructions

load and store

QN=13 In the ARM architecture only _____ instructions access memory locations.

- a. data processing
- b. status register access
- c. load and store
- d. branch

all of the above

QN=14 Which data type is defined in MMX?

- a. packed byte
- b. packed word
- c. packed doubleword
- d. all of the above

unconditional branch

QN=15 A branch instruction in which the branch is always taken is _____.

- a. conditional branch
- b. unconditional branch
- c. jump
- d. bi-endian

immediate addressing

QN=1 The advantage of _____ is that no memory reference other than the instruction fetch is required to obtain the operand.

- a. direct addressing
- b. immediate addressing
- c. register addressing
- d. stack addressing



direct

QN=2 The principal advantage of _____ addressing is that it is a very simple form of addressing.

- a. displacement
- b. register
- c. stack
- d. direct



indirect addressing

QN=3 _____ has the advantage of large address space, however it has the disadvantage of multiple memory references.

- a. Indirect addressing
- b. Direct addressing
- c. Immediate addressing
- d. Stack addressing

register

QN=4 The advantages of _____ addressing are that only a small address field is needed in the instruction and no time-consuming memory references are required.

- a. direct
- b. indirect
- c. register
- d. displacement

displacement addressing

QN=5 _____ has the advantage of flexibility, but the disadvantage of complexity.



- a. Stack addressing
- b. Displacement addressing
- c. Direct addressing
- d. Register addressing

indexing

QN=6 For _____, the address field references a main memory address and the referenced register contains a positive displacement from that address.



- a. indexing
- b. base-register addressing
- c. relative addressing
- d. all of the above

postindexing

QN=7 Indexing performed after the indirection is _____.



- a. relative addressing
- b. autoindexing
- c. postindexing
- d. preindexing

immediate

QN=8 For the _____ mode, the operand is included in the instruction.

- a. immediate
- b. base
- c. register
- d. displacement

immediate

QN=9 The only form of addressing for branch instructions is _____ addressing.

- a. register
- b. relative
- c. base
- d. immediate

all of the above

QN=10 Which of the following interrelated factors go into determining the use of the addressing bits?

- a. number of operands
- b. number of register sets
- c. address range
- d. all of the above

orthogonality

QN=11 _____ is a principle by which two variables are independent of each other.

- a. Opcode
- b. Orthogonality
- c. Completeness
- d. Autoindexing

PDP-11

QN=12 The _____ was designed to provide a powerful and flexible instruction set within the constraints of a 16-bit minicomputer.

- a. PDP-1
- b. PDP-8
- c. PDP-11
- d. PDP-10

SIB

QN=13 The _____ byte consists of three fields: the Scale field, the Index field and the Base field.

- a. SIB
- b. VAX
- c. PDP-11
- d. ModR/M

32

QN=14 All instructions in the ARM architecture are _____ bits long and follow a regular format.

- a. 8
- b. 16
- c. 32
- d. 64

All of the above

QN=15 _____ is a design principle employed in designing the PDP-10 instruction set.

- a. Orthogonality
- b. Completeness
- c. Direct addressing
- d. All of the above

registers

QN=1 _____ are a set of storage locations.

- a. Processors
- b. PSWs
- c. Registers
- d. Control units

control unit

QN=2 The _____ controls the movement of data and instructions into and out of the processor.

- a. control unit
- b. ALU
- c. shifter
- d. branch

data

QN=3 _____ registers may be used only to hold data and cannot be employed in the calculation of an operand address.

- a. General purpose
- b. Data
- c. Address

condition codes

QN=4 _____ are bits set by the processor hardware as the result of operations.

- a. MIPS
- b. Condition codes
- c. Stacks
- d. PSWs

program counter

QN=5 The _____ contains the address of an instruction to be fetched.

- a. instruction register
- b. memory address register
- c. memory buffer register
- d. program counter

MBR

QN=6 The _____ contains a word of data to be written to memory or the word most recently read.

- a. MAR
- b. PC
- c. MBR
- d. IR

decode instruction

QN=7 The _____ determines the opcode and the operand specifiers.

- a. decode instruction
- b. fetch operands
- c. calculate operands
- d. execute instruction

all of the above

QN=8 _____ is a pipeline hazard.

- a. Control
- b. Resource
- c. Data
- d. All of the above

data

QN=9 A _____ hazard occurs when there is a conflict in the access of an operand location.

- a. resource
- b. data
- c. structural
- d. control

loop buffer

QN=10 A _____ is a small, very-high-speed memory maintained by the instruction fetch stage of the pipeline and containing the n most recently fetched instructions in sequence.

- a. loop buffer
- b. delayed branch
- c. multiple stream
- d. branch prediction

branch history table

QN=11 The _____ is a small cache memory associated with the instruction fetch stage of the pipeline.

- a. dynamic branch
- b. loop table
- c. branch history table
- d. flag

execute

QN=12 The _____ stage includes ALU operations, cache access, and register update.

- a. decode
- b. execute

trap flag

QN=13 _____ is used for debugging.

- a. Direction flag
- b. Alignment check
- c. Trap flag
- d. Identification flag

7

QN=14 The ARM architecture supports _____ execution modes.

- a. 2
- b. 8
- c. 11
- d. 7

supervisor mode

QN=15 The OS usually runs in _____.

- a. supervisor mode
- b. abort mode
- c. undefined mode
- d. fast interrupt mode

A

The Patterson study examined the dynamic behavior of _____ programs, independent of the underlying architecture.

- A. HLL
- B. RISC
- C. CISC
- D. all of the above

C

_____ is the fastest available storage device.

- A. Main memory
- B. Cache
- C. Register storage
- D. HLL

D

The first commercial RISC product was _____.

- A. SPARC
- B. CISC
- C. VAX
- D. the Pyramid

A

- _____ instructions are used to position quantities in registers temporarily for computational operations.
- A. Load-and-store
 - B. Window
 - C. Complex
 - D. Branch

D

- Which stage is required for load and store operations?
- A. I
 - B. E
 - C. D
 - D. all of the above

B

- A _____ instruction can be used to account for data and branch delays.
- A. SUB
 - B. NOOP
 - C. JUMP
 - D. all of the above

C

The instruction location immediately following the delayed branch is referred to as the ____.



- A. delay load
- B. delay file
- C. delay slot
- D. delay register

A

A tactic similar to the delayed branch is the ____, which can be used on LOAD instructions.



- A. delayed load
- B. delayed program
- C. delayed slot
- D. delayed register

C

The MIPS R4000 uses ____ bits for all internal and external data paths and for addresses, registers, and the ALU.



- A. 16
- B. 32
- C. 64
- D. 128

D

All MIPS R series processor instructions are encoded in a single _____ word format.



- A. 4-bit
- B. 8-bit
- C. 16-bit
- D. 32-bit

B

A _____ architecture is one that makes use of more, and more fine-grained pipeline stages.



- A. parallel
- B. superpipelined
- C. superscalar
- D. hybrid

A

The R4000 can have as many as _____ instructions in the pipeline at the same time.



- A. 8
- B. 10
- C. 5
- D. 3

C

SPARC refers to an architecture defined by _____.



- A. Microsoft
- B. Apple
- C. Sun Microsystems
- D. IBM

A

The R4000 pipeline stage where the instruction result is written back to the register file is the _____ stage.



- A. write back
- B. tag check
- C. data cache
- D. instruction execute