Engs 31 / CoSc 56

Exercise 21: VGA

To be completed in class on May 3, 2019

In this exercise you will implement the timing signals required for VGA interfacing. Specifically, you will generate the PCLK, H_sync, and V_sync signals.

Modify the starter code provided at: https://www.edaplayground.com/x/3DNM

Generating the PCLK signal

1) Add a STD_LOGIC signal named "PCLK". Initialize it to 0;
2) Write a process that will cause the PCLK signal to toggle every 20 ns (this means the overall period will be 40 ns and the frequency will be 25 MHz). Add any signals necessary to carry out this task. Assume the master clock (clk) has a frequency of 100 MHz.
3) Verify the correct timing of the PCLK via simulation.

Generating the H_Sync signal

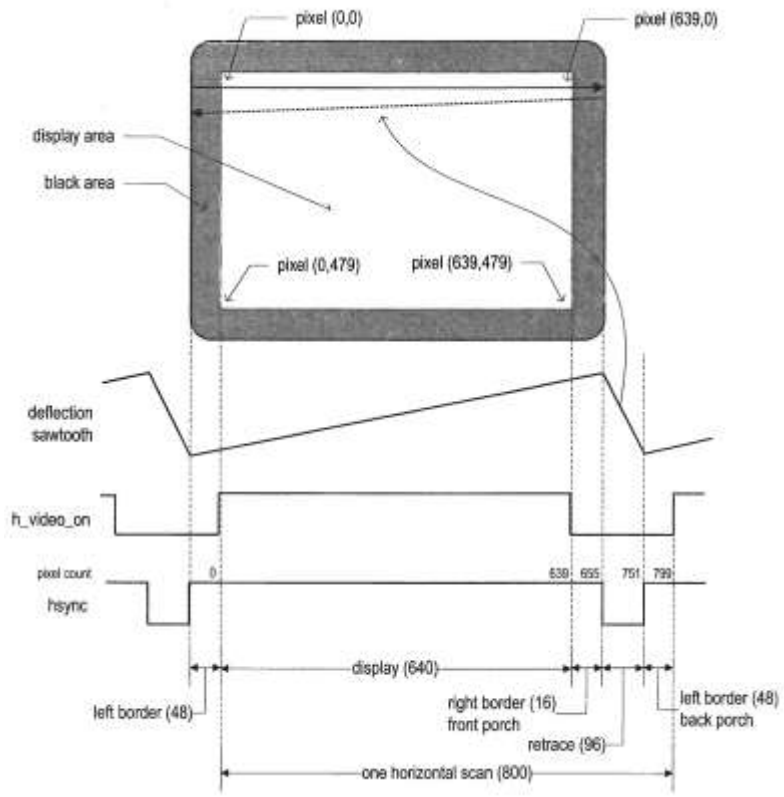
4) Make a counter that counts from 0 to HSCAN. This counter will count PCLK ticks.
5) Although the process runs off the 100 MHz clock, you need to add logic to detect the rising edge of the PCLK. You can't use the rising_edge keyword since PCLK is not a clock signal. The solution will be to add another signal that keeps track of the value of PCLK during the last clock tick. Then you can compare the current value of PCLK and the previous value of PCLK to detect a rising edge.
6) Add logic that uses the horizontal timing constants (left_border, h_display, right_border, and h_retrace) to set h_video_on and H_Sync high and low (see the timing diagram on the back).
7) Run the simulation to ensure correct timing of the H_sync and h_video_on signal. Calculate by hand how long you expect each high and low time to be. Compare this to the simulation.

Generating the V_Sync signal

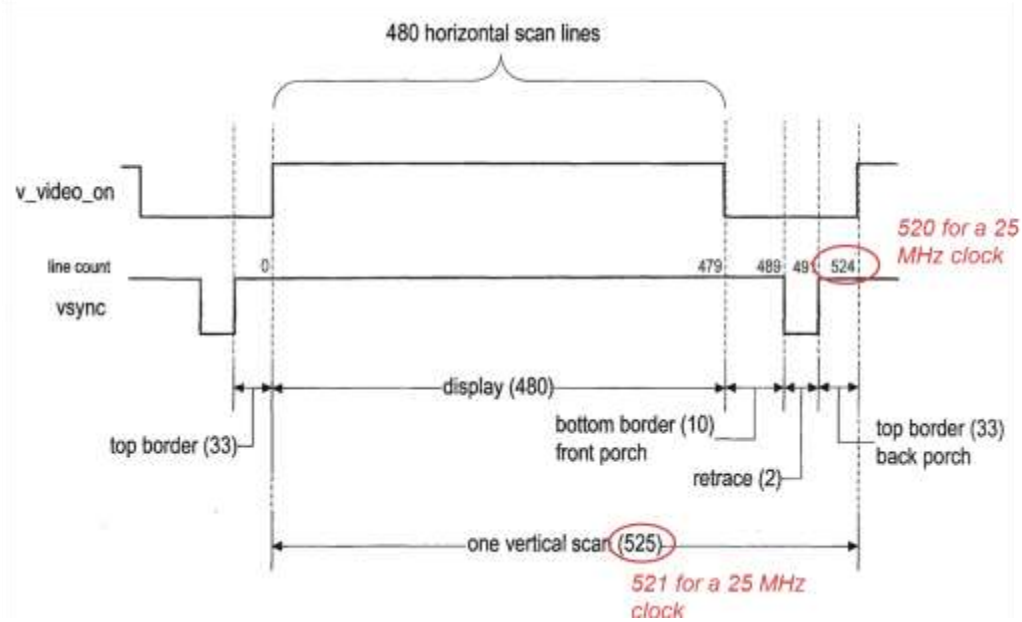
8) Repeat the procedure for generating the H_Sync signal. The two key differences are:
    a. Vertical timing constants (top_border, v_display, bottom_border, and v_retrace) are used instead of the horizontal constants
    b. The counter is incremented on H_Sync pulses instead of PCLK pulses
9) Simulating this with EDA playground is problematic since the V_Sync time is longer than we can simulate. Consider decreasing the value of the constants just to make sure the V_Sync signal is at least behaving properly.

Challenge: Generating pixel_x and pixel_y outputs

10) Add logic to generate the pixel_x and pixel_y outputs. These should range from 0-639 and 0-479, respectively. They should also only be valid when video_on is '1'.



H_sync timing



V_sync timing