Assignment - 2
4x4 Matrix Multiplier

The objective of this assignment is to get familiarised with the FPGA tools and the zybo board. I tried the 2018.3 version of the software tool, but it didn't seem to work. Downgraded it to **2017.4** and it worked like a charm.

Workflow:

The process starts with a simple HLS design that implements the 4x4 matrix multiplier as an IP. This IP is then added to the vivado repository, which is then integrated with the zynq PS and DMA. Automating the design using the tools gives the final block design. The bitstream for this design is then generated and exported. The SDK then runs a system debugger to verify the working of the designed IP on the FPGA board.

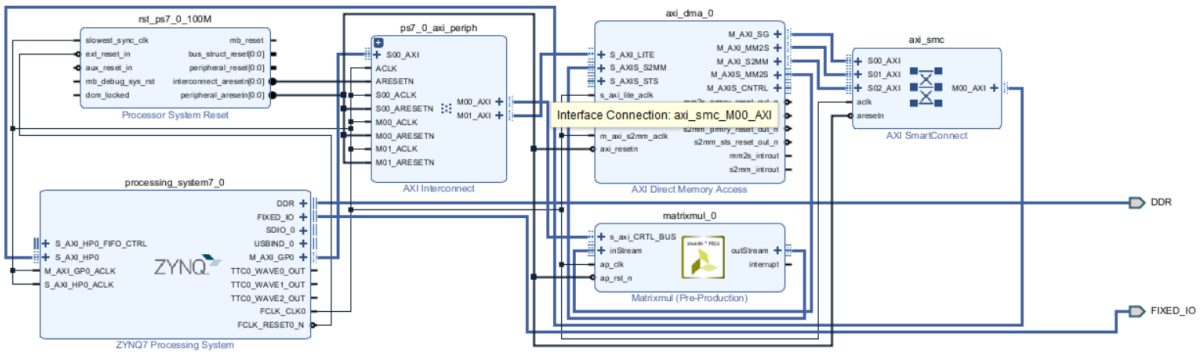
Screenshots:

Here's the acknowledgement of the work done.

HLS:-

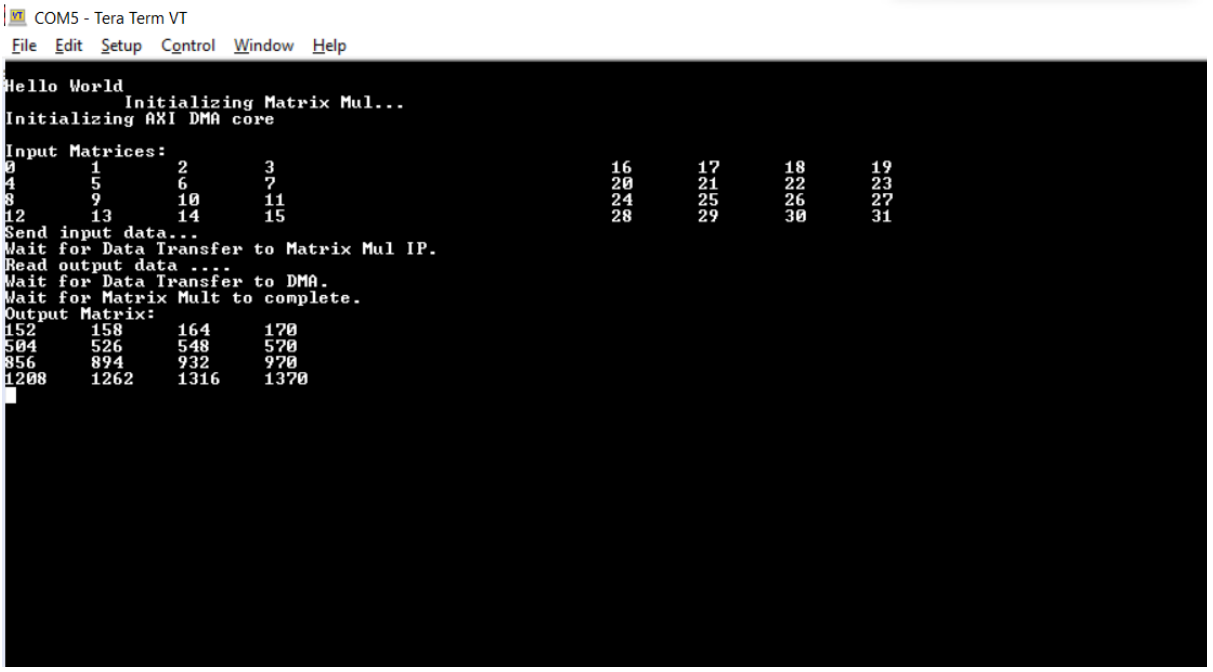
```
C:/Xilinx_2017/Vivado/2017.4/include/floating_point_v7_0_bitacc_cmodel.h:135:0: note: this is the location of the previous definition
 Matrix A
1 2 3 4
5 6 7 8
9 10 11 12
13 14 15 16
 Matrix B
17 18 19 20
21 22 23 24
25 26 27 28
29 30 31 32
 Matrix result
250 260 270 280
618 644 670 696
986 1028 1070 1112
```

Vivado:-



SDK:-

(used TeraTerm as the serial port monitor)



Result:

All the objectives of the assignment have been implemented.