November 30, 2025

Previously Published Statement

Dear Editors and Reviewers,

This statement accompanies the manuscript "RTL-to-Atoms Synthesis of a Machine Learning Accelerator on Atomic-Scale Computers", submitted for consideration as a Regular Paper in IEEE Transactions on Nanotechnology (TNANO), Special Section associated with the 25th IEEE International Conference on Nanotechnology (IEEE NANO 2025).

This manuscript is a substantially extended journal version of our IEEE NANO 2025 conference paper "Building a Machine Learning Accelerator with Silicon Dangling Bonds: From Verilog to Quantum Dot Layout", which received the Best Student Paper Award. The paper is properly mentioned and cited in the manuscript. A detailed comparison between the original and new contributions is provided in Table 1, highlighting substantial additions at every step of the end-to-end synthesis pipeline. In particular, the journal version introduces parameterizable bit-widths for systematic scaling studies, as well as silicon dangling bond (SiDB)-specific arithmetic logic unit (ALU) implementations and placement-and-routing cost functions tailored to SiDB logic. It also provides a significantly expanded experimental evaluation across multiple precision settings.

Thank you very much for considering this manuscript for publication in the IEEE Transactions on Nanotechnology Special Section associated with the 25th IEEE International Conference on Nanotechnology. The authors appreciate the time and effort of the editors and reviewers in evaluating this work.

Sincerely,

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Table 1: Summary of conference and journal contributions.

Topic	**Conference contributions**	**New contributions for journal extension**
RTL design of MXU	• Hierarchical RTL for the matrix-multiply unit with a processing-element core and clocked shell. • Each layer in the hierarchy verified with dedicated test benches. • Fixed weight and activation precision at W8A8.	• Parameterizable weight and activation bit-widths that enable scaling studies and benchmarking of state-of-the-art placement-and-routing algorithms when 8-bit layouts become intractable.
RTL-to-netlist	• Used *Yosys* for RTL-to-AIG conversion with its default ALU mapping geared toward CMOS libraries. • Optimized the AIG using ABC's *&deepsyn* strategy.	• Implemented SiDB-aligned ripple-carry adders and array multipliers as gate-level netlists and integrated them into *Yosys* for technology-aware mapping.
Netlist-to-atoms	• Applied figure-of-merit-aware technology mapping that favored robust SiDB gates despite the area overhead. • Extended the hexagonalization flow to align input and output pins with the fabric clocking scheme.	• Added SiDB-specific cost objectives to the *gold* placement-and-routing algorithm so that optimization targets the layout rules of SiDB fabrics rather than metrics tuned for other FCN platforms.
Experiment	• Compared synthesized MXU layouts against manually estimated blueprints from prior studies. • Evaluated uniform versus figure-of-merit-aware synthesis for the W8A8 configuration using the *ortho* placement-and-routing algorithm.	• Compared synthesis results across W8A8, W4A4, and W2A2. • Evaluated all bit-width configurations with figure-of-merit-aware technology mapping. • Reported *gold* placement-and-routing results for W4A4 and W2A2, which remain within *gold*'s tractable range. • Benchmarked new *gold* cost objectives to quantify SiDB-specific layout improvements.