Graphical user interface, application

Description automatically generated

Model Sim simulation shows that the full adder is adding A (0001) and B (0001) and outputs 0002 or 2.

Text, letter

Description automatically generated

Text

Description automatically generated

Diagram of 4-bit full adder with VHDL code representing it.

A picture containing electronics, circuit

Description automatically generated

Project uploaded to the FPGA board with A(1) and A(3) flipped on.