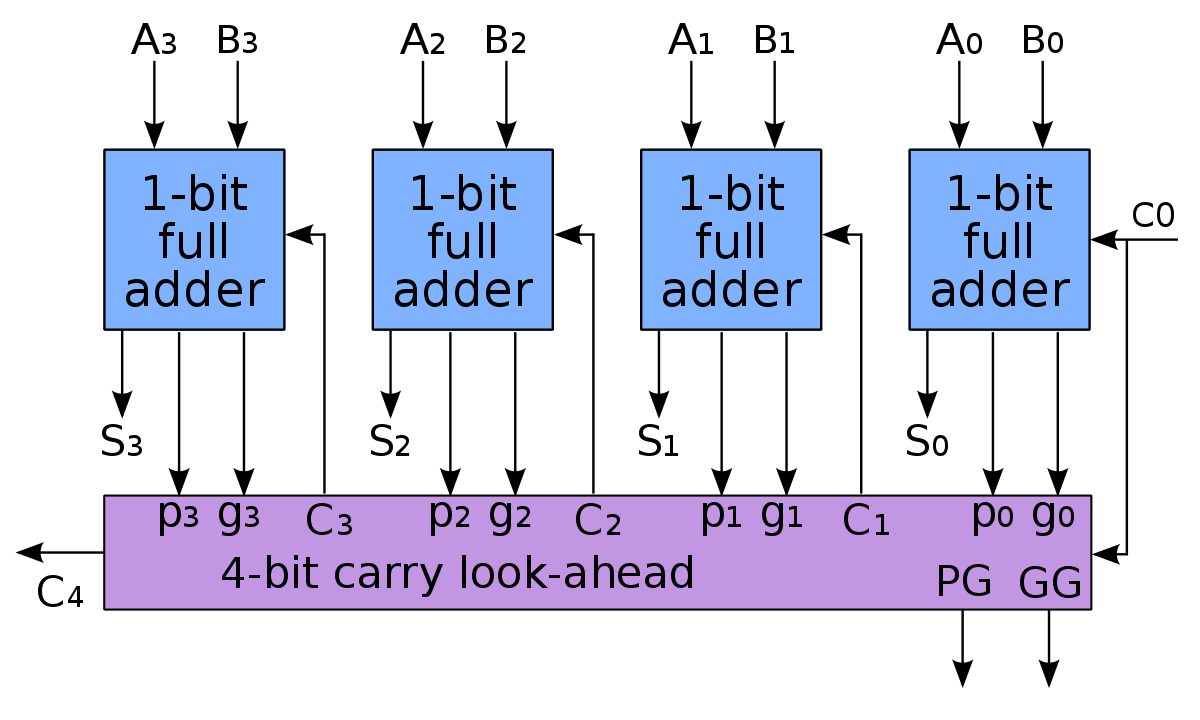


Model Sim simulation shows that the full adder is adding A (0001) and B (0001).

Text

Description automatically generated with low confidence

Diagram carry lookahead adder with VHDL code representing it.

A close-up of a computer chip

Description automatically generated with medium confidence

Project uploaded to the FPGA board with A(0)-A(3) and B(2) flipped on.