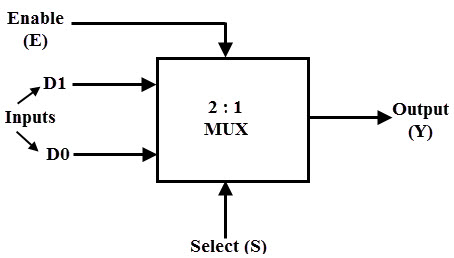


Model Sim simulation shows that the full adder is adding A (0001) and B (0001).



Text

Description automatically generatedText

Description automatically generated

Diagram of multiplexor with VHDL code representing it.

A close-up of a computer chip

Description automatically generated with medium confidence

Project uploaded to the FPGA board with B, E, and F flipped on.