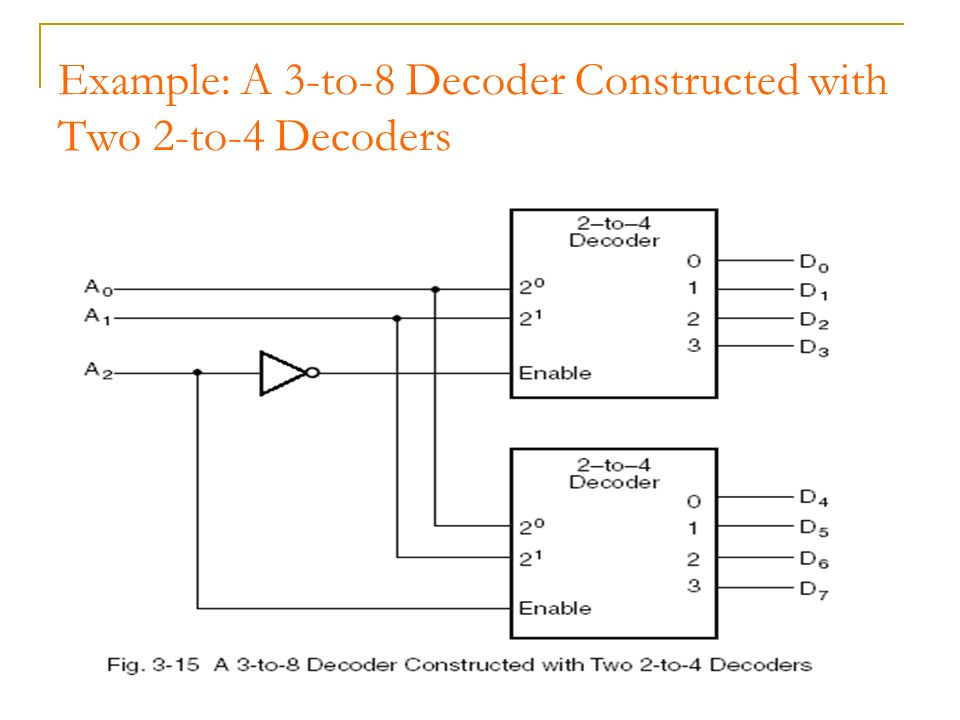
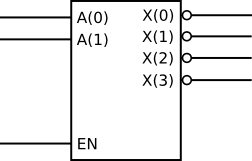


Model Sim simulation showing the waves of a 3:8 decoder using two 2:4 decoders.



Text

Description automatically generated

Diagram of a 2:4 decoder and a 3:8 decoder using two 2:4 decoders with VHDL code representing each. We couldn’t get the project uploaded to the FPGA board because we were having issues with Quartus and VHDL and eventually we ran out of time. I’m pretty sure you checked me and my partner off though.