

## 1. Description

### 1.1. Project

Project Name	_Lucky_Boar
Board Name	_Lucky_Boar
Generated with:	STM32CubeMX 4.25.0
Date	06/09/2018

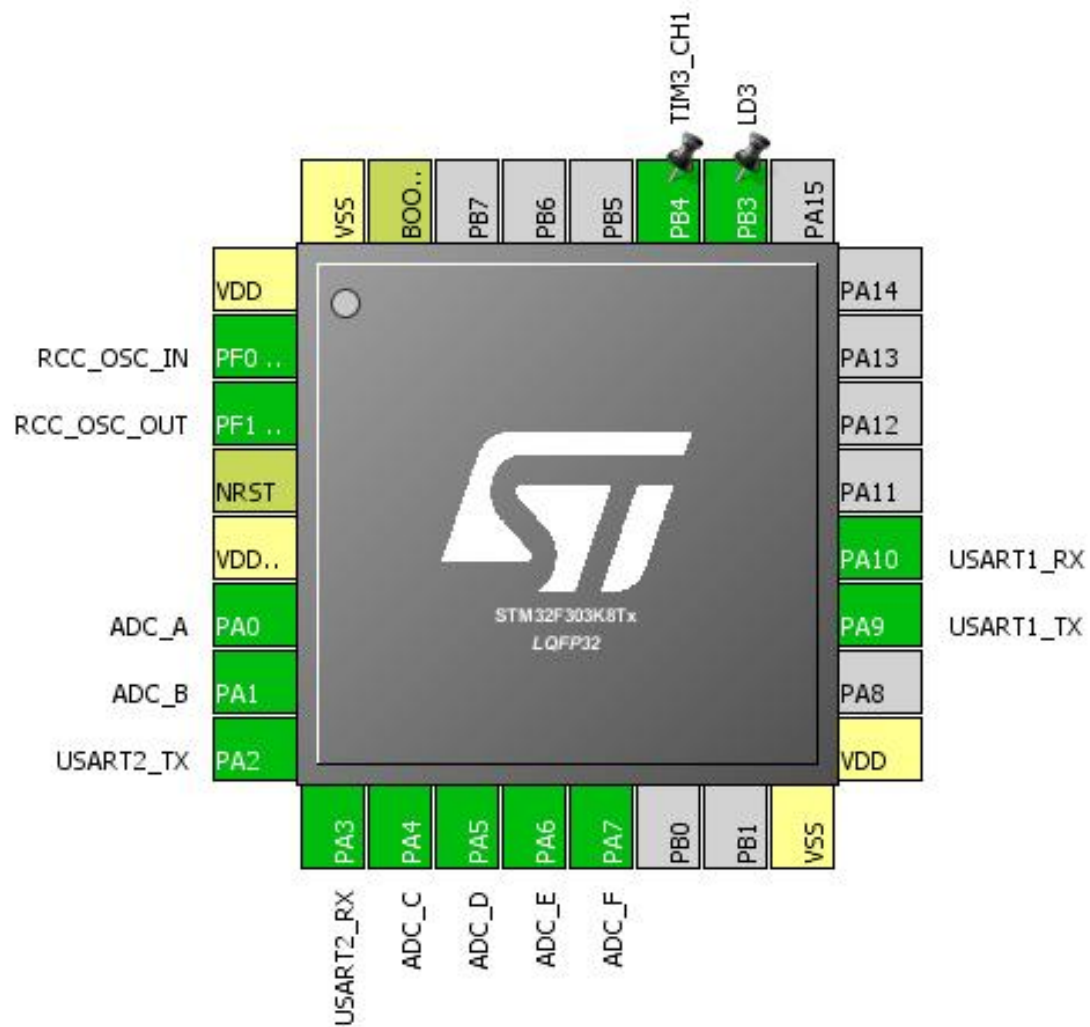
### 1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303K8Tx
MCU Package	LQFP32
MCU Pin number	32

### 1.3. Caution

The report was generated although the configuration was in a modified state. It may be not accurate

## 2. Pinout Configuration

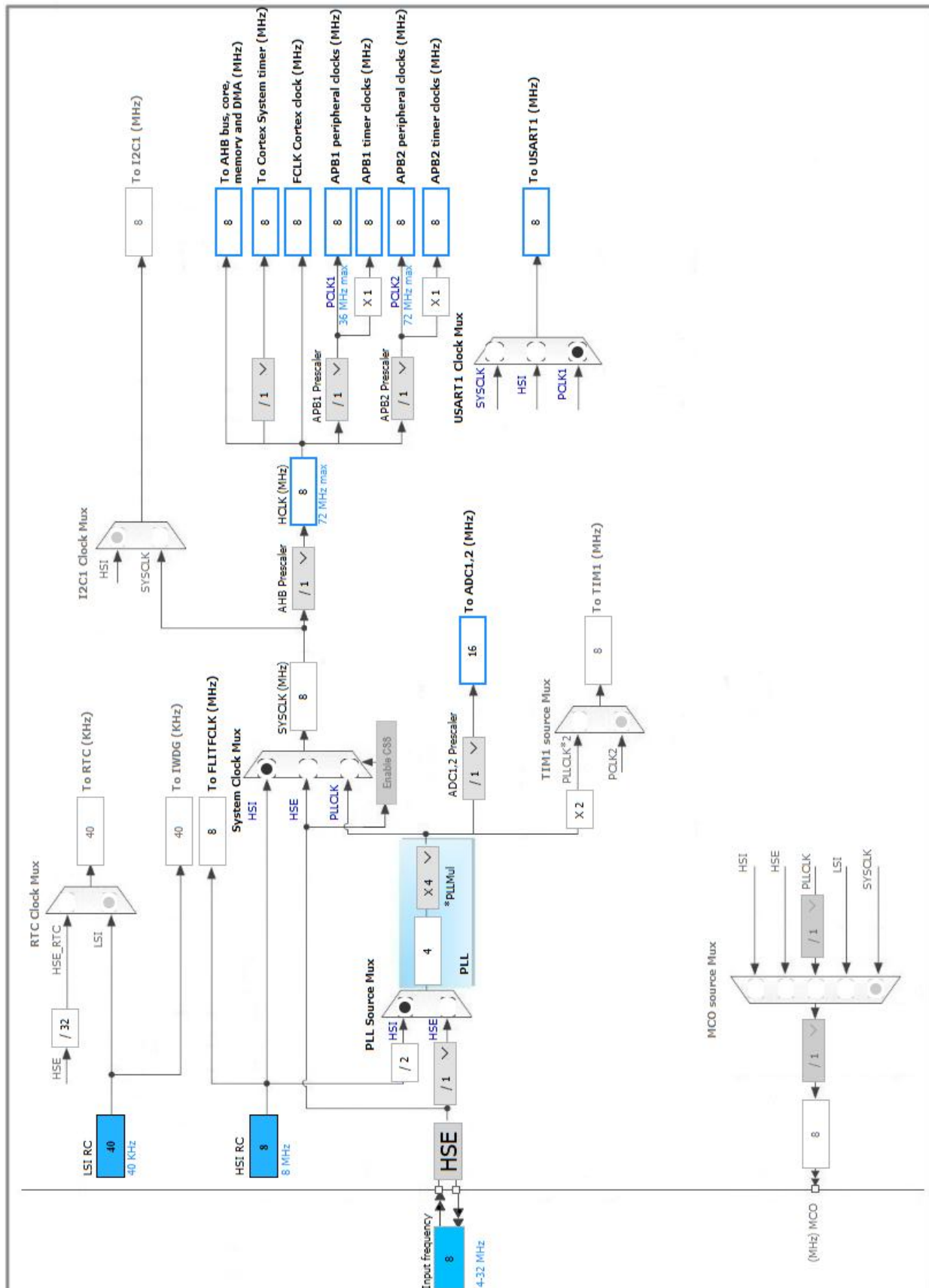


### 3. Pins Configuration

Pin Number LQFP32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PF0 / OSC_IN	I/O	RCC_OSC_IN	
3	PF1 / OSC_OUT	I/O	RCC_OSC_OUT	
4	NRST	Reset		
5	VDDA/VREF+	Power		
6	PA0	I/O	ADC1_IN1	ADC_A
7	PA1	I/O	ADC1_IN2	ADC_B
8	PA2	I/O	USART2_TX	
9	PA3	I/O	USART2_RX	
10	PA4	I/O	ADC2_IN1	ADC_C
11	PA5	I/O	ADC2_IN2	ADC_D
12	PA6	I/O	ADC2_IN3	ADC_E
13	PA7	I/O	ADC2_IN4	ADC_F
16	VSS	Power		
17	VDD	Power		
19	PA9	I/O	USART1_TX	
20	PA10	I/O	USART1_RX	
26	PB3 *	I/O	GPIO_Output	LD3
27	PB4	I/O	TIM3_CH1	
31	BOOT0	Boot		
32	VSS	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. IPs and Middleware Configuration

### 5.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

#### 5.1.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Clock Prescaler ADC Asynchronous clock mode

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data overwritten

Low Power Auto Wait Disabled

##### ADC\_Regular\_ConversionMode:

Enable Regular Conversions Enable

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel Channel 1

Sampling Time 1.5 Cycles

Offset Number No offset

Offset 0

##### ADC\_Injected\_ConversionMode:

Enable Injected Conversions Enable

Number Of Conversions 0

##### Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

##### Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

##### Analog Watchdog 3:

IN1: IN1 Single-ended  
IN2: IN2 Single-ended  
IN3: IN3 Single-ended  
mode: IN4

### ADCs\_Common\_Settings:

### ADC\_Settings:

**ADC\_Regular\_ConversionMode:**

**ADC\_Injected\_ConversionMode:**

### Analog Watchdog 1:

## Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

**Analog Watchdog 3:**

Enable Analog WatchDog3 Mode false

## 5.3. RCC

### High Speed Clock (HSE): Crystal/Ceramic Resonator

#### 5.3.1. Parameter Settings:

**System Parameters:**

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

**RCC Parameters:**

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

## 5.4. SYS

### Timebase Source: SysTick

## 5.5. TIM3

### Clock Source : Internal Clock Channel1: PWM Generation CH1

#### 5.5.1. Parameter Settings:

**Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>72 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>100 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

**Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
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Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
<b>Clear Input:</b>	
Clear Input Source	Disable
<b>PWM Generation Channel 1:</b>	
Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

## 5.6. USART1

**Mode: Asynchronous**

### 5.6.1. Parameter Settings:

**Basic Parameters:**

Baud Rate	9600 *
Word Length	8 Bits (including Parity) *
Parity	None
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

**Advanced Features:**

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

## 5.7. USART2

**Mode: Asynchronous**



### 5.7.1. Parameter Settings:

#### Basic Parameters:

Baud Rate	9600 *
Word Length	8 Bits (including Parity) *
Parity	None
Stop Bits	1

#### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

#### Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

\* User modified value

## 6. System Configuration

### 6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN1	Analog mode	No pull up pull down	n/a	ADC_A
	PA1	ADC1_IN2	Analog mode	No pull up pull down	n/a	ADC_B
ADC2	PA4	ADC2_IN1	Analog mode	No pull up pull down	n/a	ADC_C
	PA5	ADC2_IN2	Analog mode	No pull up pull down	n/a	ADC_D
	PA6	ADC2_IN3	Analog mode	No pull up pull down	n/a	ADC_E
	PA7	ADC2_IN4	Analog mode	No pull up pull down	n/a	ADC_F
RCC	PF0 / OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1 / OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull up pull down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull up pull down	High *	
	PA10	USART1_RX	Alternate Function Push Pull	No pull up pull down	High *	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull up pull down	High *	
	PA3	USART2_RX	Alternate Function Push Pull	No pull up pull down	High *	
GPIO	PB3	GPIO_Output	Output Push Pull	No pull up pull down	Low	LD3

## 6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Channel5	Peripheral To Memory	<b>Medium *</b>
USART1_TX	DMA1_Channel4	Memory To Peripheral	<b>Medium *</b>
USART2_RX	DMA1_Channel6	Peripheral To Memory	Low
USART2_TX	DMA1_Channel7	Memory To Peripheral	Low

### USART1\_RX: DMA1\_Channel5 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

### USART1\_TX: DMA1\_Channel4 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

### USART2\_RX: DMA1\_Channel6 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

### USART2\_TX: DMA1\_Channel7 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte

Memory Data Width:      Byte

### 6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel4 global interrupt	true	0	0
DMA1 channel5 global interrupt	true	0	0
DMA1 channel6 global interrupt	true	0	0
DMA1 channel7 global interrupt	true	0	0
ADC1 and ADC2 interrupts	true	0	0
TIM3 global interrupt	true	0	0
USART1 global interrupt / USART1 wake-up interrupt through EXT line 25	true	0	0
USART2 global interrupt / USART2 wake-up interrupt through EXT line 26	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
Floating point unit interrupt	unused		

\* User modified value

## ***7. Power Consumption Calculator report***

### 7.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303K8Tx
Datasheet	025083_Rev5

### 7.2. Parameter Selection

Temperature	25
Vdd	3.6

## 8. Software Project

### 8.1. Project Settings

Name	Value
Project Name	_Lucky_Boar
Project Folder	D:\Users\Samuel\workspace\METR4901\_Lucky_Boar
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_F3 V1.9.0

### 8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

## ***9. Software Pack Report***