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**March 5, 2018**

**CSC 34200 - Computer Organization**

Instructor: Prof. Zheng Peng

Lab **02**

1. The schematic diagram of the division circuit is:

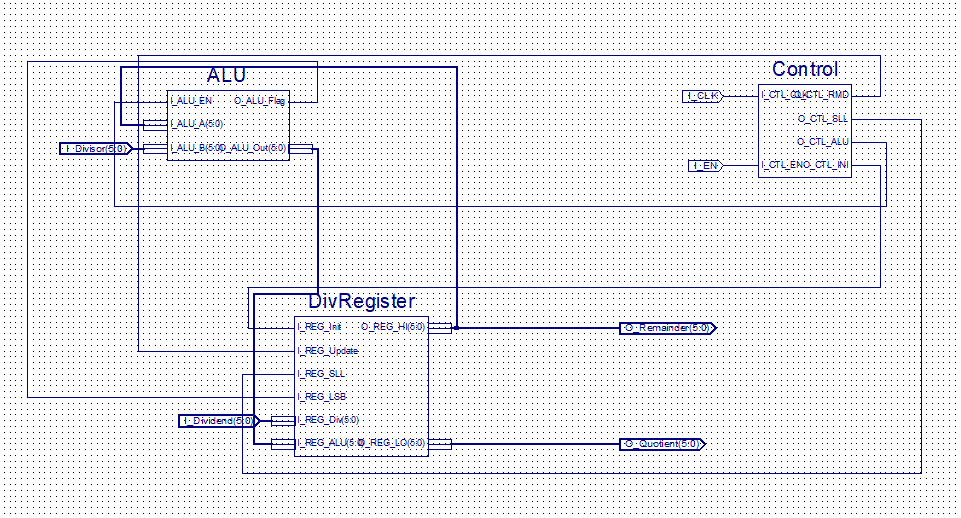


Figure 1: schematic diagram of constructed division circuit.

1. State diagram of the division circuit is:

if Control is disabled

else if control is enabled

If counter < 6

Counter++;

Else (counter = 6)

If control is disabled

If control is disabled

1. All Xilinx source files are uploaded to blackboard.
2. After running the simulation on given input values, the result is as following:

Remainder 🡪 000100 and Quotient 🡪 000011

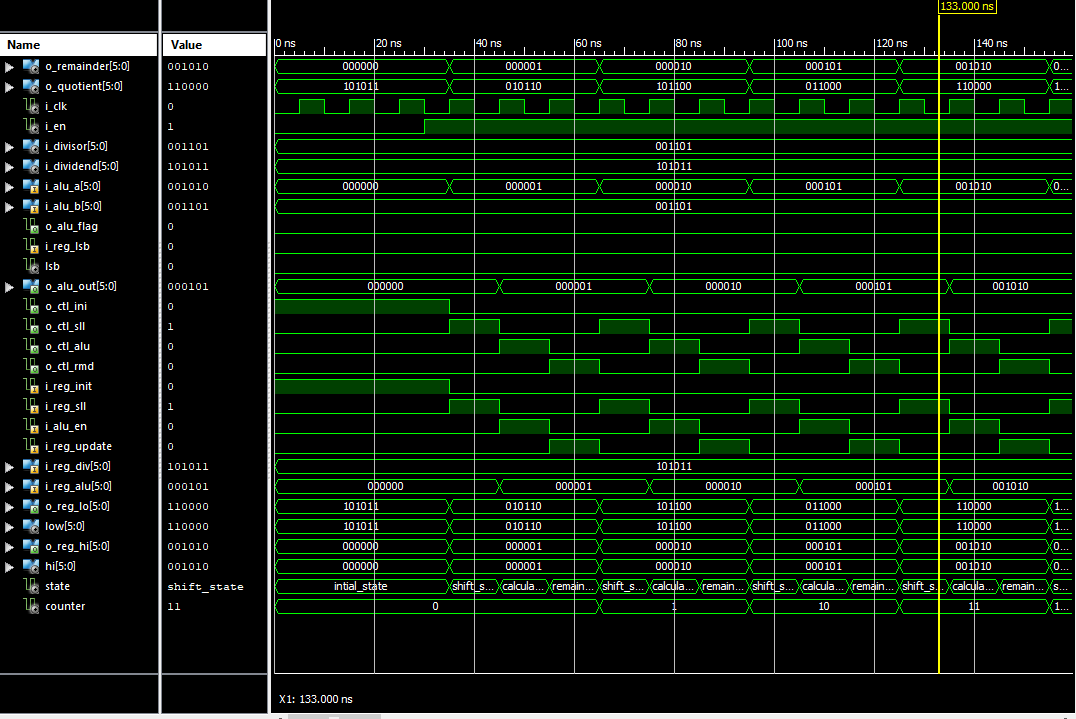


Figure 2: Running simulation on given input values to validate results.

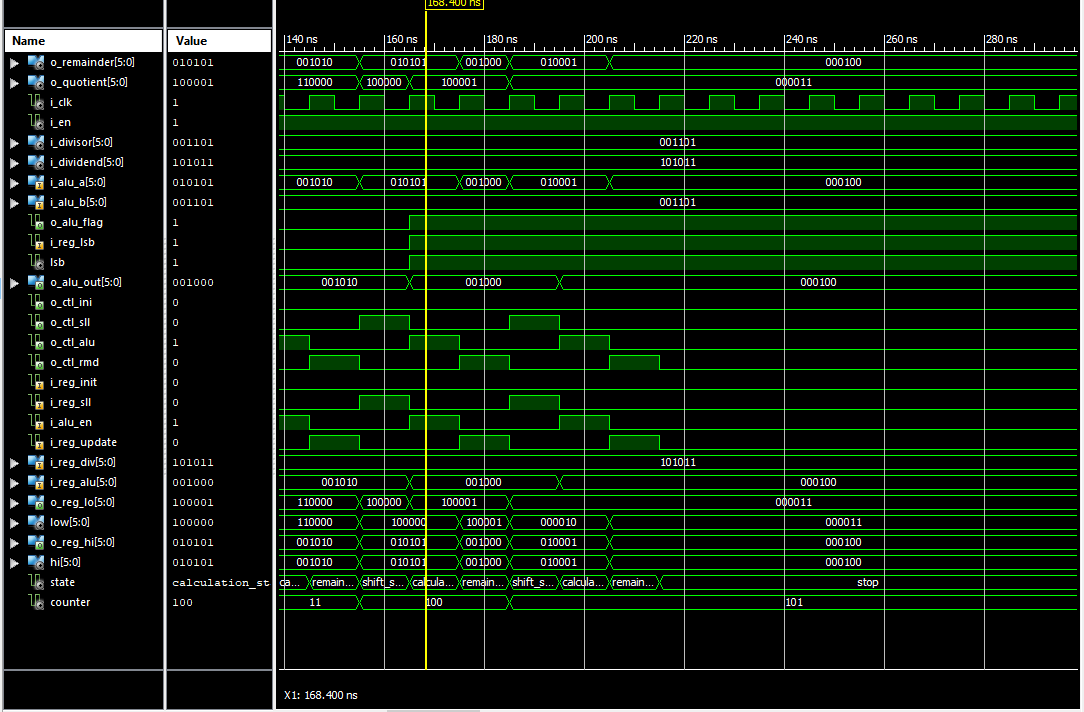


Figure 3: Running simulation on given input values to validate results.

1. According to the division algorithm, the table of the division process (101011 / 001101) is: ***(Note the following simulation performs 6 steps from step (0) to step (5))***

|  |  |  |  |
| --- | --- | --- | --- |
| Step | Divisor | After left shift | Remainder |
| Start | 001101 |  | 0000 0010 1011 |
| 1 | 001101 | 0000 0101 011? | 0000 0101 011**0** |
| 2 | 001101 | 0000 1010 110? | 0000 1010 11**00** |
| 3 | 001101 | 0001 0101 100? | 0001 0101 1**000** |
| 4 | 001101 | 0010 1011 000? | 0010 1011 **0000** |
| 5 | 001101 | 0101 0110 000? | 0010 001**0 0001** |
| 6 | 001101 | 0100 0100 001? | **0001 0000 0011** |

from the simulation we obtain the following waveform at step (0) in figure 4:

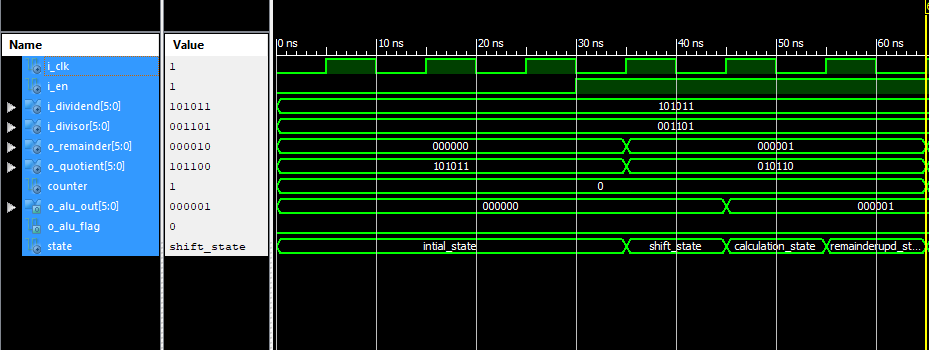


Figure 4: The simulation at step (0).

In the test bench program, the control unit is enabled after 30 ns. The full step (0) takes from 0 ns to 65 ns and the following occurs:

1. the remainder part of the register (higher 6 bits) is initialized to zero.
2. the quotient part of the register (lower 6 bits) is initialized to the value of the dividend which is (101011)
3. the first clock cycle at 35 ns performs shift operation. The value of the register after the shift becomes 000001 0101102.
4. The second clock cycle at 45 ns performs ALU operation. The output of the ALU is 0000012.
5. The third clock cycle at 55 ns updates the register value. The register value after update becomes 000001 0101102 and the operation ends at 65 ns.
6. The wave form is consistent with the value in the above table.

from the simulation we obtain the following waveform at step (1) in figure 5:

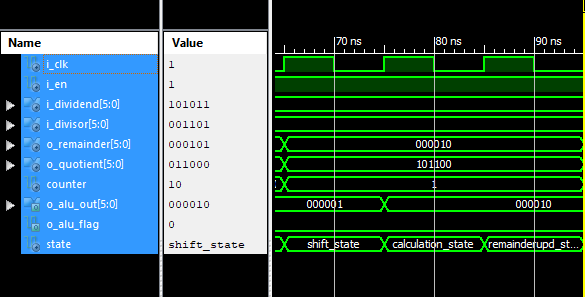


Figure 5: The simulation at step (1).

The full step 1 takes from 65 ns to 95 ns.

1. The previous register value is 000001 0101102.
2. the first clock cycle at 65 ns performs shift operation. The value of the register after the shift becomes 000010 1011002.
3. The second clock cycle at 75 ns performs ALU operation. The output of the ALU is 0000102.
4. The third clock cycle at 85 ns updates the register value. The register value after update becomes 000010 1011002 and the operation ends at 95 ns.
5. The wave form is consistent with the value in the above table.

From the simulation we obtain the following waveform at step (2) in figure 6:

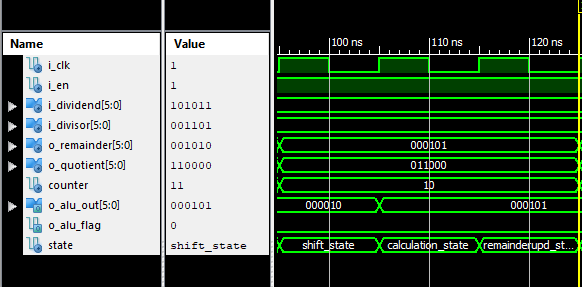


Figure 6: The simulation at step (2).

The full step 2 takes from 95 ns to 125 ns.

1. The previous register value is 000010 1011002.
2. the first clock cycle at 95 ns performs shift operation. The value of the register after the shift becomes 000101 0110002.
3. The second clock cycle at 105 ns performs ALU operation. The output of the ALU is 0001012.
4. The third clock cycle at 115 ns updates the register value. The register value after update becomes 000101 0110002 and the operation ends at 125 ns.
5. The wave form is consistent with the value in the above table.

from the simulation we obtain the following waveform at step (3) in figure 7:

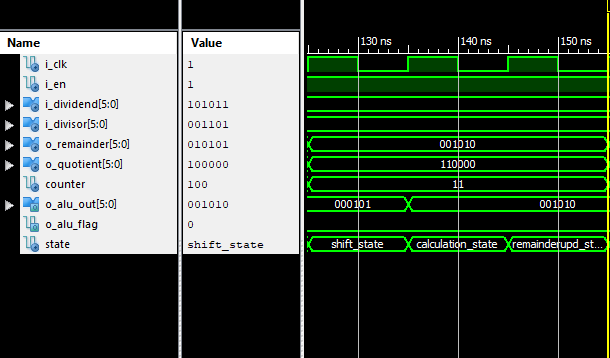


Figure 7: The simulation at step (3).

The full step 3 takes from 125 ns to 155 ns.

1. The previous register value is 000101 0110002.
2. the first clock cycle at 125 ns performs shift operation. The value of the register after the shift becomes 001010 1100002.
3. The second clock cycle at 135 ns performs ALU operation. The output of the ALU is 0010102.
4. The third clock cycle at 145 ns updates the register value. The register value after update becomes 001010 1100002 and the operation ends at 155 ns.
5. The wave form is consistent with the value in the above table.

from the simulation we obtain the following waveform at step (4) in figure 8:

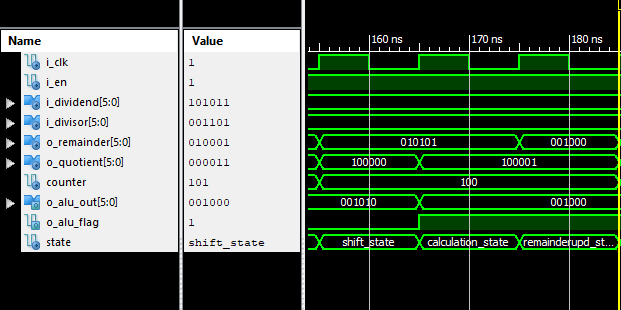


Figure 8: The simulation at step (4).

The full step 4 takes from 155 ns to 185 ns.

1. The previous register value is 001010 1100002.
2. the first clock cycle at 155 ns performs shift operation. The value of the register after the shift becomes 010101 1000002.
3. The second clock cycle at 165 ns performs ALU operation. The output of the ALU is 0010002.
4. The third clock cycle at 175 ns updates the register value. The register value after update becomes 001000 1000012 and the operation ends at 185 ns.
5. The wave form is consistent with the value in the above table.

from the simulation we obtain the following waveform at step (5) in figure 9:

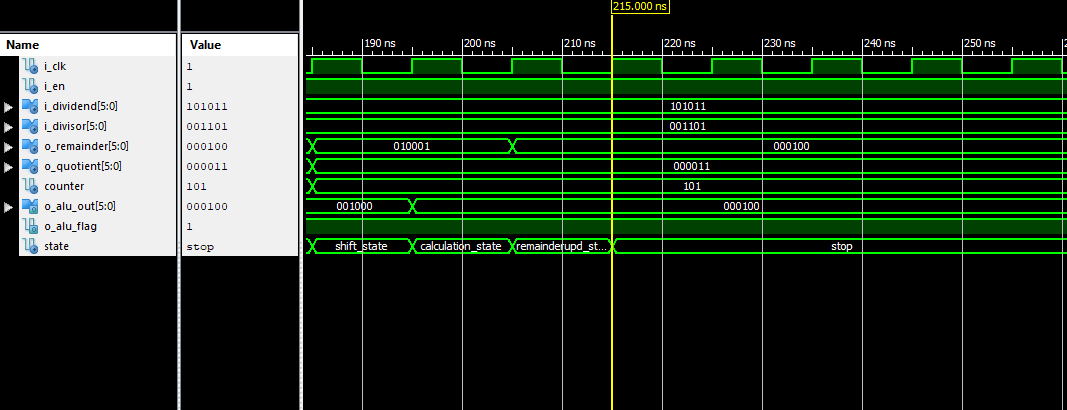


Figure 9: The simulation at the last step (step 5).

The full step 5 takes from 185 ns to 215 ns

1. The previous register value is 001000 1000012.
2. the first clock cycle at 185 ns performs shift operation. The value of the register after the shift becomes 010001 0000102.
3. The second clock cycle at 195 ns performs ALU operation. The output of the ALU is 0001002.
4. The third clock cycle at 205 ns updates the register value. The register value after update becomes 000100 0000112 and the operation ends at 215 ns.
5. The wave form is consistent with the value in the above table.
6. After that, STOP state becomes the present signal that stopes the whole division circuit as the division process ends. The result is:

Remainder 🡪 000100 and Quotient 🡪 000011