

# CSC34300

## Lecture 04: Xilinx ISE Design Suite

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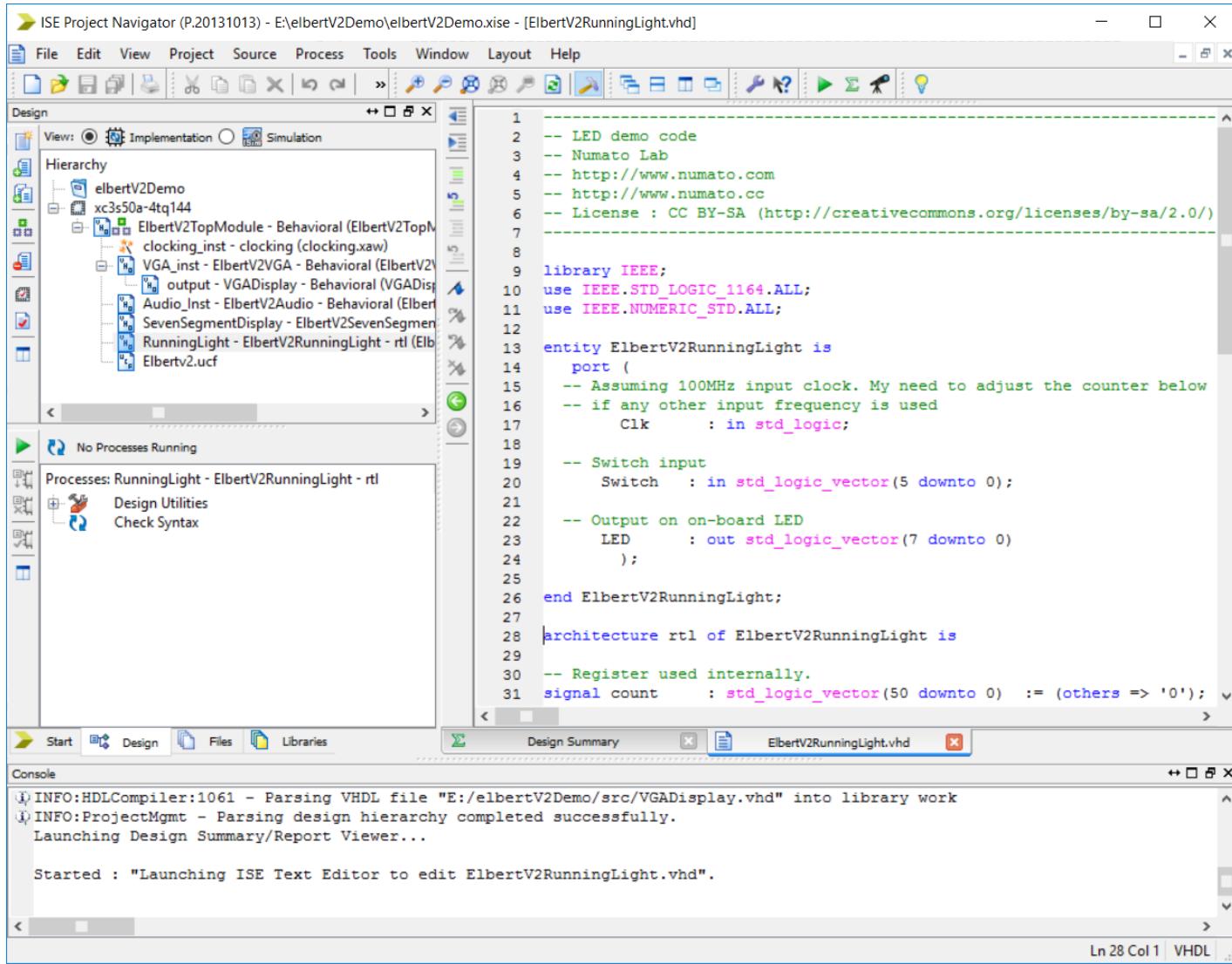
# Xilinx Design Suite

- An integrated development environment (IDE) for Xilinx lines of FPGA products
- Xilinx ISE Design Suite (discontinued since 2012)
  - Embedded Edition
  - System Edition
  - WebPACK edition
- Xilinx Vivado Design Suite
  - Successor of ISE

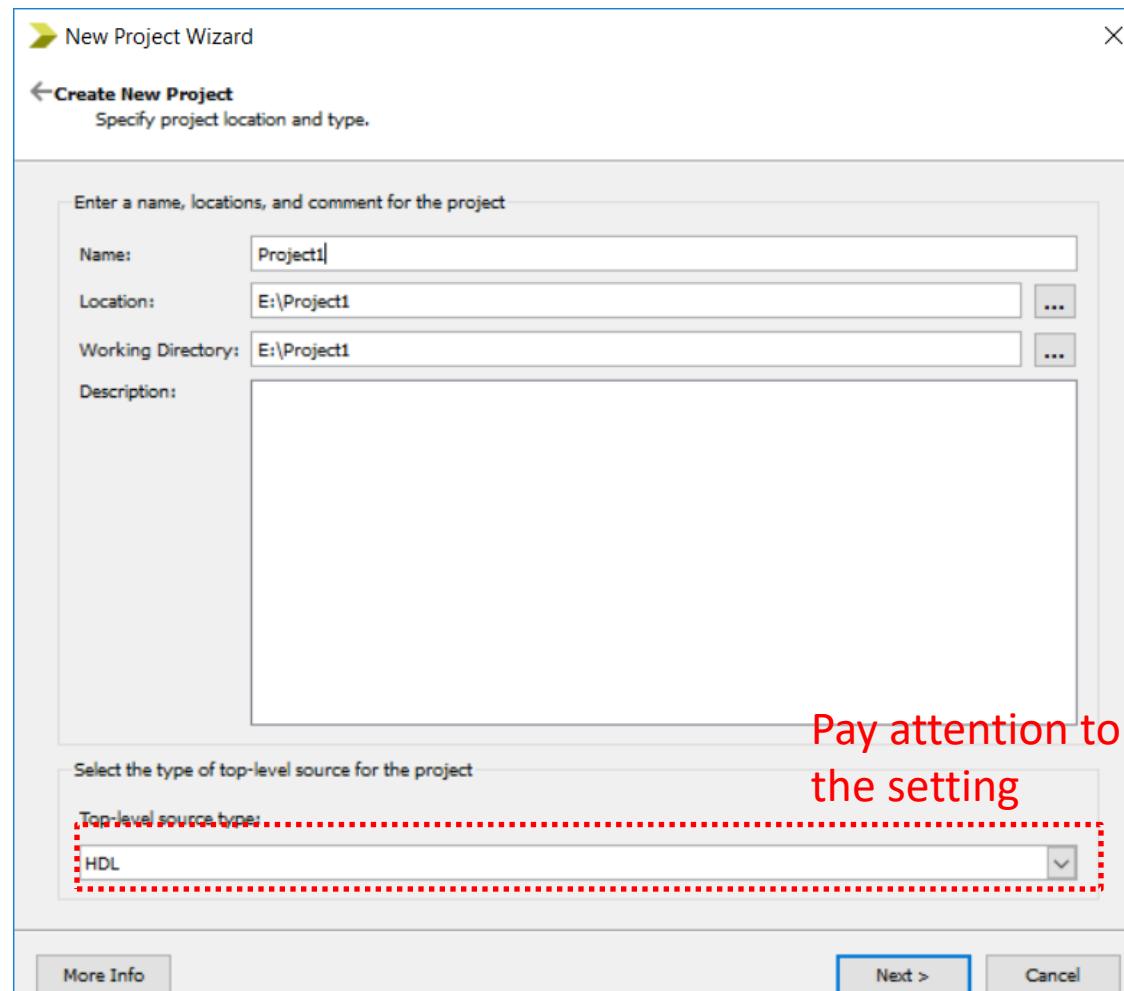
# Xilinx ISE Design Suite WebPACK 14.7

- WebPACK edition
  - Free to use
  - Available for both Windows and Linux
  - Support a large number of Xilinx FPGA products
  - Integrated HDL verification with the Lite version of the ISE Simulator (ISim)

# ISE Project Navigator



# Create a New Project (1)



# Create a New Project (2)

New Project Wizard

← Project Settings  
Specify device and project properties.

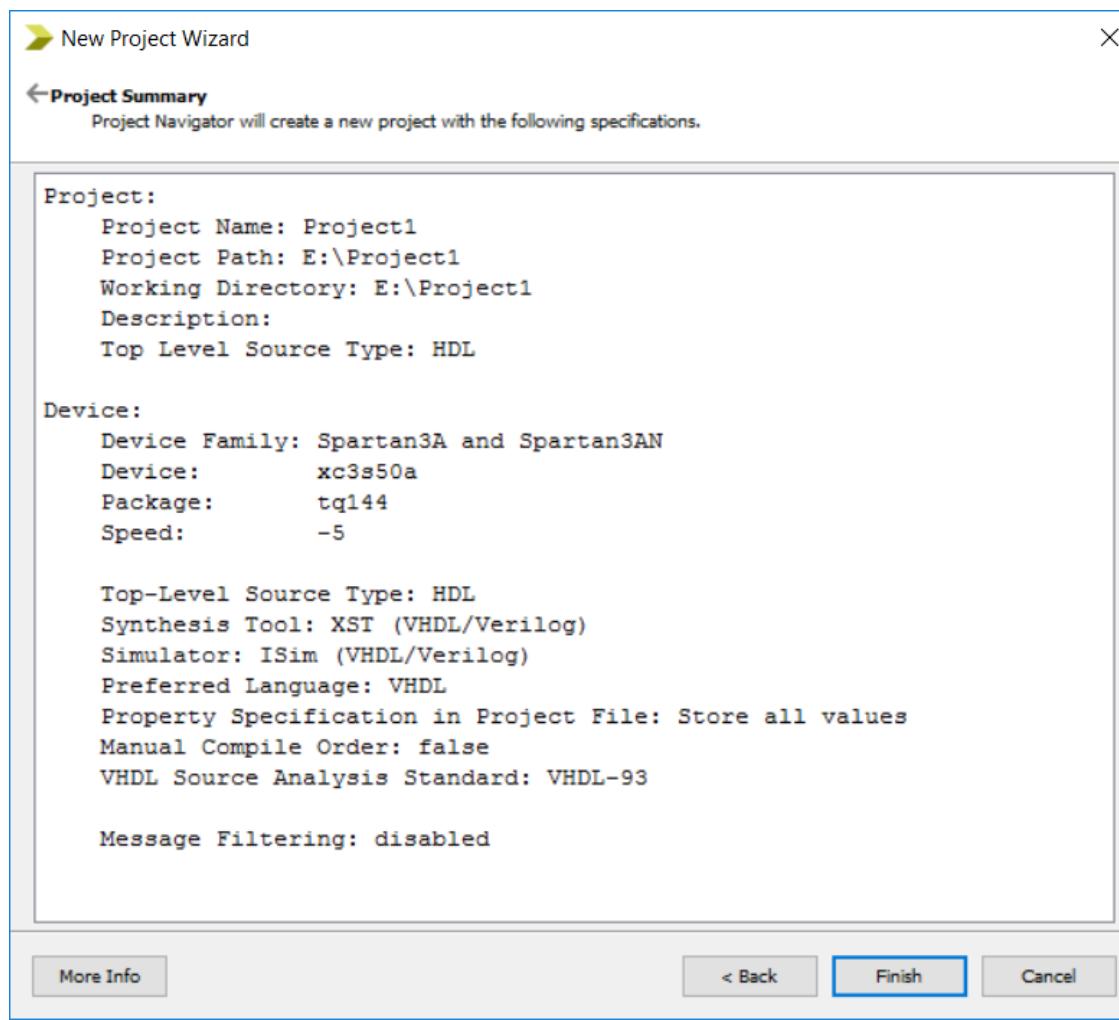
Select the device and design flow for the project

Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan3A and Spartan3AN
Device	XC3S50A
Package	TQ144
Speed	-5
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	I\$im (VHDL/Verilog)
Preferred Lanquage	VHDL
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

More Info      < Back      Next >      Cancel

Pay attention to these settings

# Create a New Project (3)



# Design a circuit using Xilinx

ISE Project Navigator (P.20131013) - E:\Project1\Project1.xise - [Design Summary]

File Edit View Project Source Process Tools Window Layout Help

Design Overview

- Summary
- IOB Properties
- Module Level Utilization
- Timing Constraints
- Pinout Report
- Clock Report
- Static Timing

Errors and Warnings

- Parser Messages
- Synthesis Messages
- Translation Messages
- Map Messages
- Place and Route Messages
- Timing Messages
- Bitgen Messages
- All Implementation Messages

Detailed Reports

- Synthesis Report
- Translation Report
- Map Report
- Place and Route Report
- Post-PAR Static Timing Report
- Power Report

Design Properties

- Enable Message Filtering
- Show Clock Report
- Show Failing Constraints
- Show Warnings
- Show Errors

Project File: Project1.xise      Parser Errors: No Errors

Module Name: eq2      Implementation State: New

Target Device: xc3s50a-5tq144      • Errors:

Product Version: ISE 14.7      • Warnings:

Design Goal: Balanced      • Routing Results:

Design Strategy: Xilinx Default (unlocked)      • Timing Constraints:

Environment:      • Final Timing Score:

No Processes Running

No single design module is selected

Design Utilities

New Source... Add Source... Add Copy of Source... Manual Compile Order Implement Top Module File/Path Display Expand All Collapse All Find... Design Properties... Ctrl+F

Design Summary

Console

```
Process "View HDL Instantiation Template" completed successfully
Started : "Launching Schematic Editor to edit sr_latch.sch".
Add a new source to the project
```

File Edit View Project Source Process Tools Window Layout Help

Design Overview

- Summary
- IOB Properties
- Module Level Utilization
- Timing Constraints
- Pinout Report
- Clock Report
- Static Timing

Errors and Warnings

- Parser Messages
- Synthesis Messages
- Translation Messages
- Map Messages
- Place and Route Messages

Project File: Project1.xise  
Module Name: eq2  
Target Device: xc3s50a-5tq144  
Product Version: ISE 14.7  
Design Goal: Balanced  
Design Strategy: Xilinx Default (unlocked)  
Environment:

eq2 Project Status

eq2 Project Status			
Project File:	Project1.xise	Parser Errors:	No Errors
Module Name:	eq2	Implementation State:	New
Target Device:	xc3s50a-5tq144	• Errors:	
Product Version:	ISE 14.7	• Warnings:	
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:		• Final Timing Score:	

New Source Wizard

Select Source Type

Select source type, file name and its location.

BMM File  
ChipScope Definition and Connection File  
Implementation Constraints File  
IP (CORE Generator & Architecture Wizard)  
MEM File  
Schematic  
**User Document**  
Verilog Module  
Verilog Test Fixture  
VHDL Module  
VHDL Library  
VHDL Package  
VHDL Test Bench  
Embedded Processor

File name: **DECODER\_4**  
Location: E:\Project1

Add to project

More Info Next > Cancel

No Processes Running

No single design module is selected.

Design Utilities

Start Design Files Libraries

Console

Process "Creating Schematic" completed successfully.

Started : "Launching Schematic Editor to edit decoder-4-2.sch".

Add a new source to the project



## Symbols

## Categories

- ... IO
- ... IO\_FlipFlop
- ... IO\_Latch
- LUT
- Latch
- Logic Logic
- Memory
- Mux
- Shift\_Register
- Shifter

## Symbols

- and12
- and16
- and2 and2
- and2b1
- and2b2
- and3
- and3b1
- and3b2
- and3b3
- and4
- and4b1

## Symbol Name Filter

## Orientation

Rotate 0

## Symbol Info



Design Summary



decoder-4-2.sch



## Console

Process "Creating Schematic" completed successfully

Started : "Launching Schematic Editor to edit decoder-4-2.sch".



Options

## Select Options

When you click on a branch:

- Select the entire branch
- Select the line segment

When you move an object:

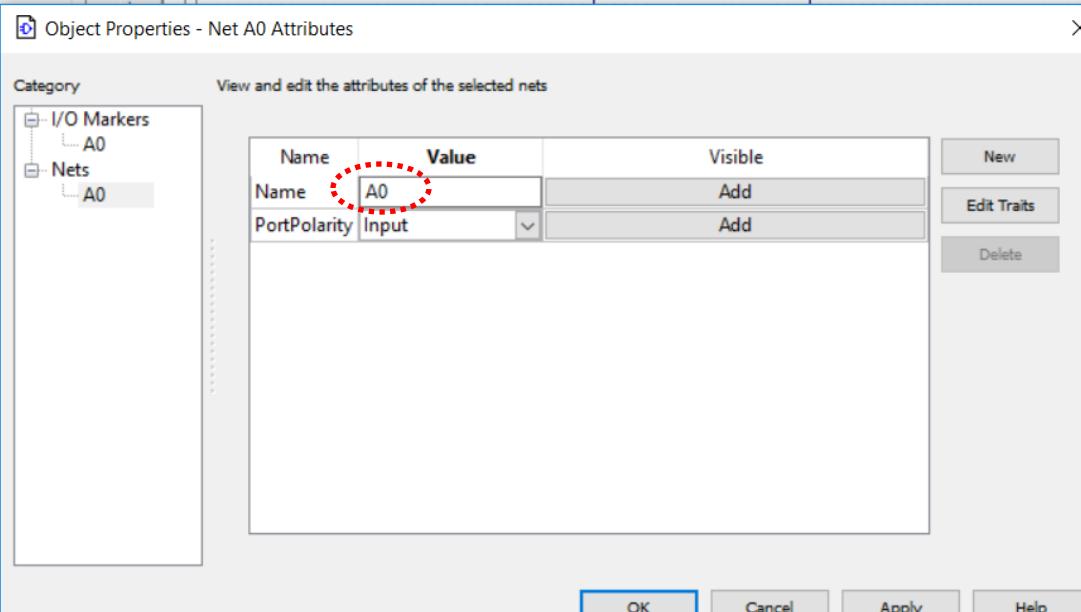
- Keep the connections to other objects
- Break the connections to other objects

When you use the area select tool, select the objects that:

- Are enclosed by the area
- Intersect the area

When you use the area select tool, select:

- Objects including attribute windows
- Objects excluding attribute windows
- Attribute windows only



Process "Creating Schematic" completed successfully

Started : "Launching Schematic Editor to edit decoder-4-2.sch".



## Options

## Select Options

When you click on a branch:

- Select the entire branch
- Select the line segment

When you move an object:

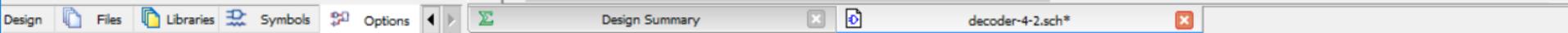
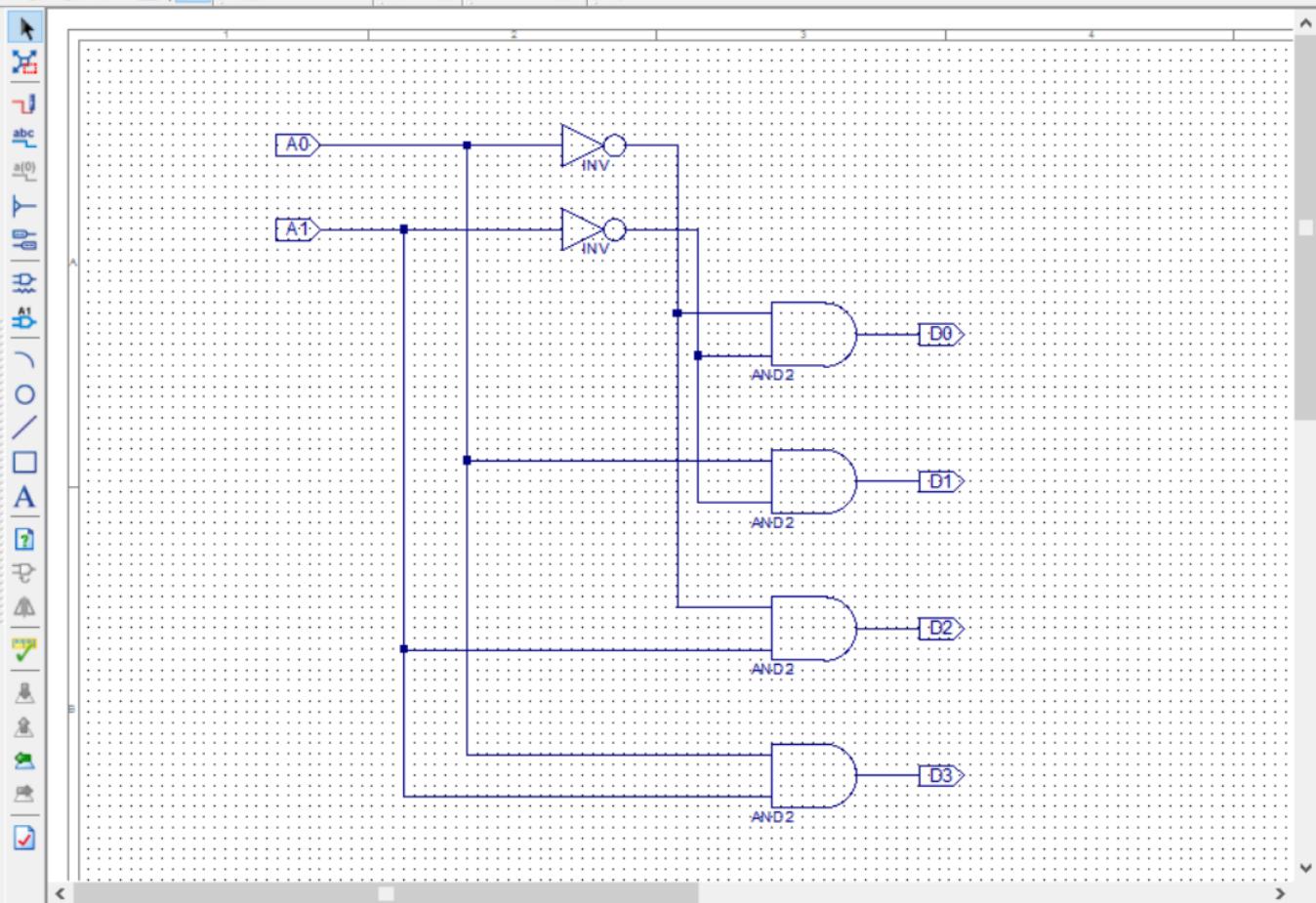
- Keep the connections to other objects
- Break the connections to other objects

When you use the area select tool, select the objects that:

- Are enclosed by the area
- Intersect the area

When you use the area select tool, select:

- Objects including attribute windows
- Objects excluding attribute windows
- Attributes windows only

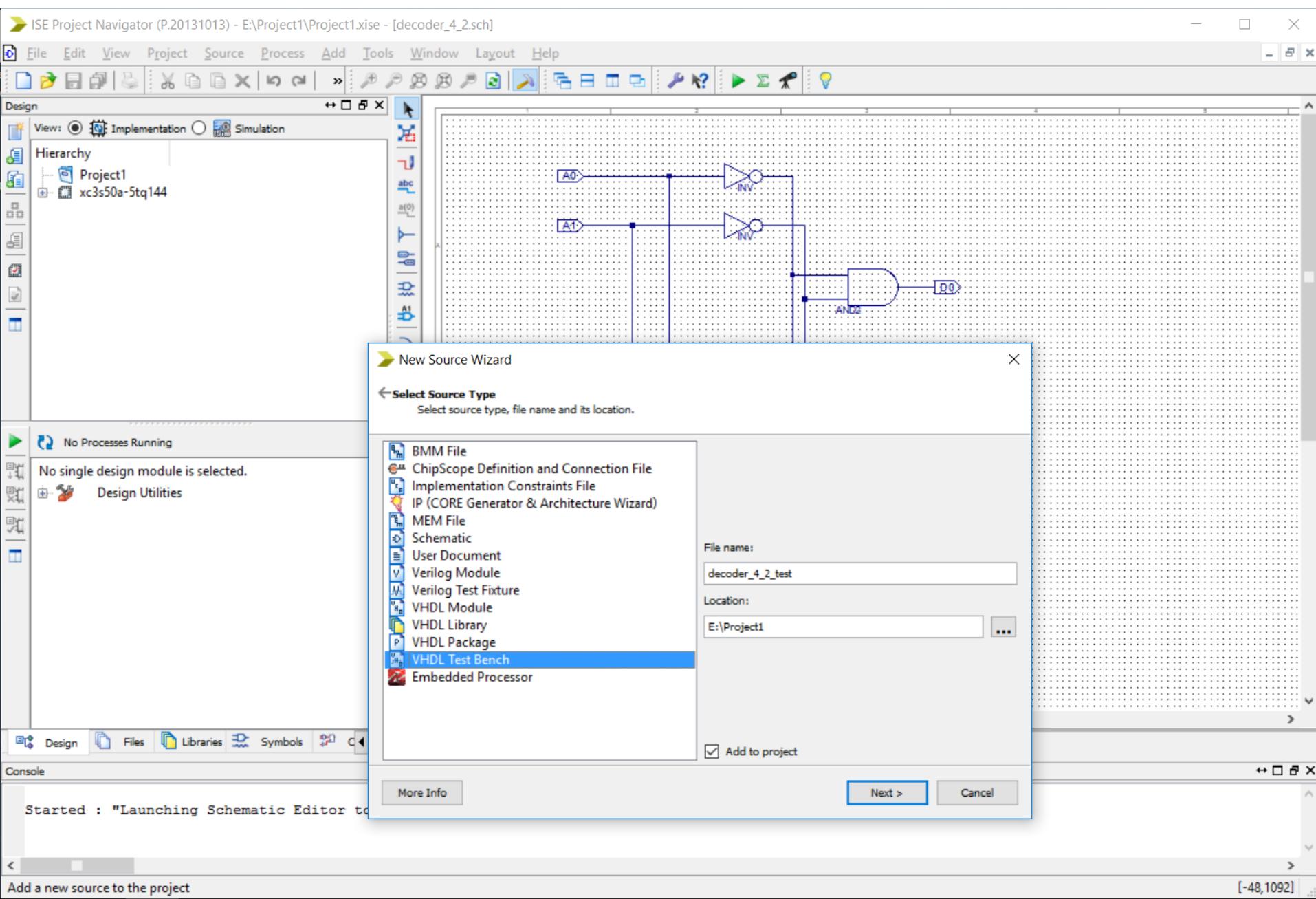


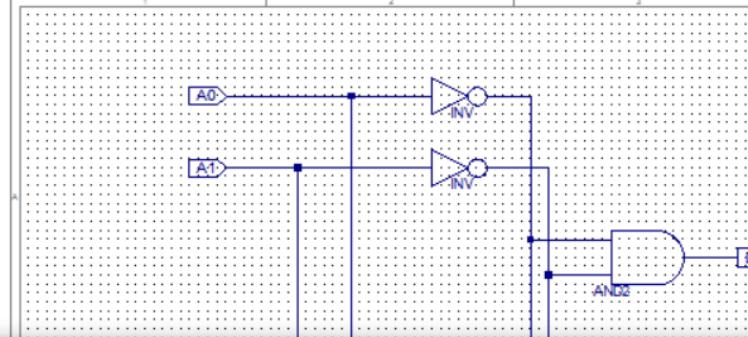
## Console

Process "Creating Schematic" completed successfully

Started : "Launching Schematic Editor to edit decoder-4-2.sch".

# Simulation





## New Source Wizard

## &lt; Associate Source

Select a source with which to associate the new source.

- eq2
- eq1
- comparator1
- decoder\_4\_2**
- sr\_latch

No Processes Running

No single design module is selected.

Design Utilities

Design

Files

Libraries

Symbols

C

More Info

&lt; Back

Next &gt;

Cancel

Started : "Launching Schematic Editor to

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

- Project1
  - xc3s50a-5tq144
    - eq2 - sop\_arch (eq2.vhd)
    - eq2 - struc\_arch (eq2.vhd)
    - comparator1 (comparator1.sch)
    - decoder\_4\_2 (decoder\_4\_2.sch)
    - sr\_latch (sr\_latch.sch)

No Processes Running

Processes: eq2 - struc\_arch

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
  - View RTL Schematic
  - View Technology Schematic
  - Check Syntax
  - Generate Post-Synthesis Simulation Model
- Implement Design
- Generate Programming File
- Configure Target Device
- Analyze Design Using ChipScope

```
15 LIBRARY ieee;
16 USE ieee.std_logic_1164.ALL;
17 USE ieee.numeric_std.ALL;
18 LIBRARY UNISIM;
19 USE UNISIM.Vcomponents.ALL;
20 ENTITY decoder_4_2_decoder_4_2_sch_tb IS
21 END decoder_4_2_decoder_4_2_sch_tb;
22 ARCHITECTURE behavioral OF decoder_4_2_decoder_4_2_sch_tb IS
23
24     COMPONENT decoder_4_2
25         PORT(
26             A0 : IN STD_LOGIC;
27             A1 : IN STD_LOGIC;
28             D0 : OUT STD_LOGIC;
29             D1 : OUT STD_LOGIC;
30             D2 : OUT STD_LOGIC;
31             D3 : OUT STD_LOGIC);
32
33     SIGNAL A0 : STD_LOGIC;
34     SIGNAL A1 : STD_LOGIC;
35     SIGNAL D0 : STD_LOGIC;
36     SIGNAL D1 : STD_LOGIC;
37     SIGNAL D2 : STD_LOGIC;
38     SIGNAL D3 : STD_LOGIC;
39
40 BEGIN
41
42     UUT: decoder_4_2 PORT MAP(
43         A0 => A0,
44         A1 => A1,
45         D0 => D0,
46         D1 => D1,
47         D2 => D2,
48         D3 => D3
49     );

```

Design Files: Design Summary, decoder\_4\_2.sch, decoder\_4\_2\_test.vhd

Console

INFO:ProjectMgmt - Parsing design hierarchy completed successfully.

Started : "Launching ISE Text Editor to edit decoder\_4\_2\_test.vhd".

Ln 1 Col 1 VHDL

File Edit View Project Source Process Tools Window Layout Help

Design

Hierarchy

- Project1
  - xc3s50a-5tq144
    - eq2 - sop\_arch (eq2.vhd)
    - eq2 - struc\_arch (eq2.vhd)
    - comparator1 (comparator1.sch)
    - decoder\_4\_2 (decoder\_4\_2.sch)
    - sr\_latch (sr\_latch.sch)

No Processes Running

Processes: decoder\_4\_2

- Design Utilities
  - Create Schematic Symbol
  - Check Design Rules
  - View HDL Functional Model
  - View HDL Instantiation Template**

```
35     SIGNAL D0 : STD_LOGIC;
36     SIGNAL D1 : STD_LOGIC;
37     SIGNAL D2 : STD_LOGIC;
38     SIGNAL D3 : STD_LOGIC;
39
40 BEGIN
41
42     UUT: decoder_4_2 PORT MAP(
43         A0 => A0,
44         A1 => A1,
45         D0 => D0,
46         D1 => D1,
47         D2 => D2,
48         D3 => D3
49     );
50
51 -- *** Test Bench - User Defined Section ***
52 tb : PROCESS
53 BEGIN
54
55     A1 <= '0'; A0 <= '0';
56     wait for 50 ns;
57     A1 <= '0'; A0 <= '1';
58     wait for 50 ns;
59     A1 <= '1'; A0 <= '0';
60     wait for 50 ns;
61     A1 <= '1'; A0 <= '1';
62     wait for 50 ns;
63
64     WAIT; -- will wait forever
65 END PROCESS;
66 -- *** End Test Bench - User Defined Section ***
67
68 END;
69
```

Design Files

Design Summary

decoder\_4\_2.sch

decoder\_4\_2\_test.vhd\*

## Console

ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully

File Edit View Project Source Process Tools Window Layout Help

Design View: Implementation Simulation

Hierarchy

- Project1
  - decoder\_4\_2\_decoder\_4\_2\_sch\_tb - behavioral (decoder\_4\_2.sch)
    - UUT - decoder\_4\_2 (decoder\_4\_2.sch)
  - eq2\_testbench - behavior (eq2\_testbench.vhd)
  - eq2 - sop\_arch (eq2.vhd)
  - sr\_latch\_sr\_latch\_sch\_tb - behavioral (sr\_latch\_test.vhd)
    - UUT - sr\_latch (sr\_latch.sch)
  - comparator1 (comparator1.sch)

No Processes Running

Processes: decoder\_4\_2\_decoder\_4\_2\_sch\_tb - behavioral

- ISim Simulator
  - Behavioral Check Syntax
  - Simulate Behavioral Model

```
35     SIGNAL D0 : STD_LOGIC;
36     SIGNAL D1 : STD_LOGIC;
37     SIGNAL D2 : STD_LOGIC;
38     SIGNAL D3 : STD_LOGIC;
39
40 BEGIN
41
42     UUT: decoder_4_2 PORT MAP(
43         A0 => A0,
44         A1 => A1,
45         D0 => D0,
46         D1 => D1,
47         D2 => D2,
48         D3 => D3
49     );
50
51 -- *** Test Bench - User Defined Section ***
52 tb : PROCESS
53 BEGIN
54
55     A1 <= '0'; A0 <= '0';
56     wait for 50 ns;
57     A1 <= '0'; A0 <= '1';
58     wait for 50 ns;
59     A1 <= '1'; A0 <= '0';
60     wait for 50 ns;
61     A1 <= '1'; A0 <= '1';
62     wait for 50 ns;
63
64     WAIT; -- will wait forever
65 END PROCESS;
66 -- *** End Test Bench - User Defined Section ***
67
68 END;
69
```

Design Files Libraries Symbols C ◀ ▶ Design Summary decoder\_4\_2.sch decoder\_4\_2\_test.vhd\* ◀ ▶

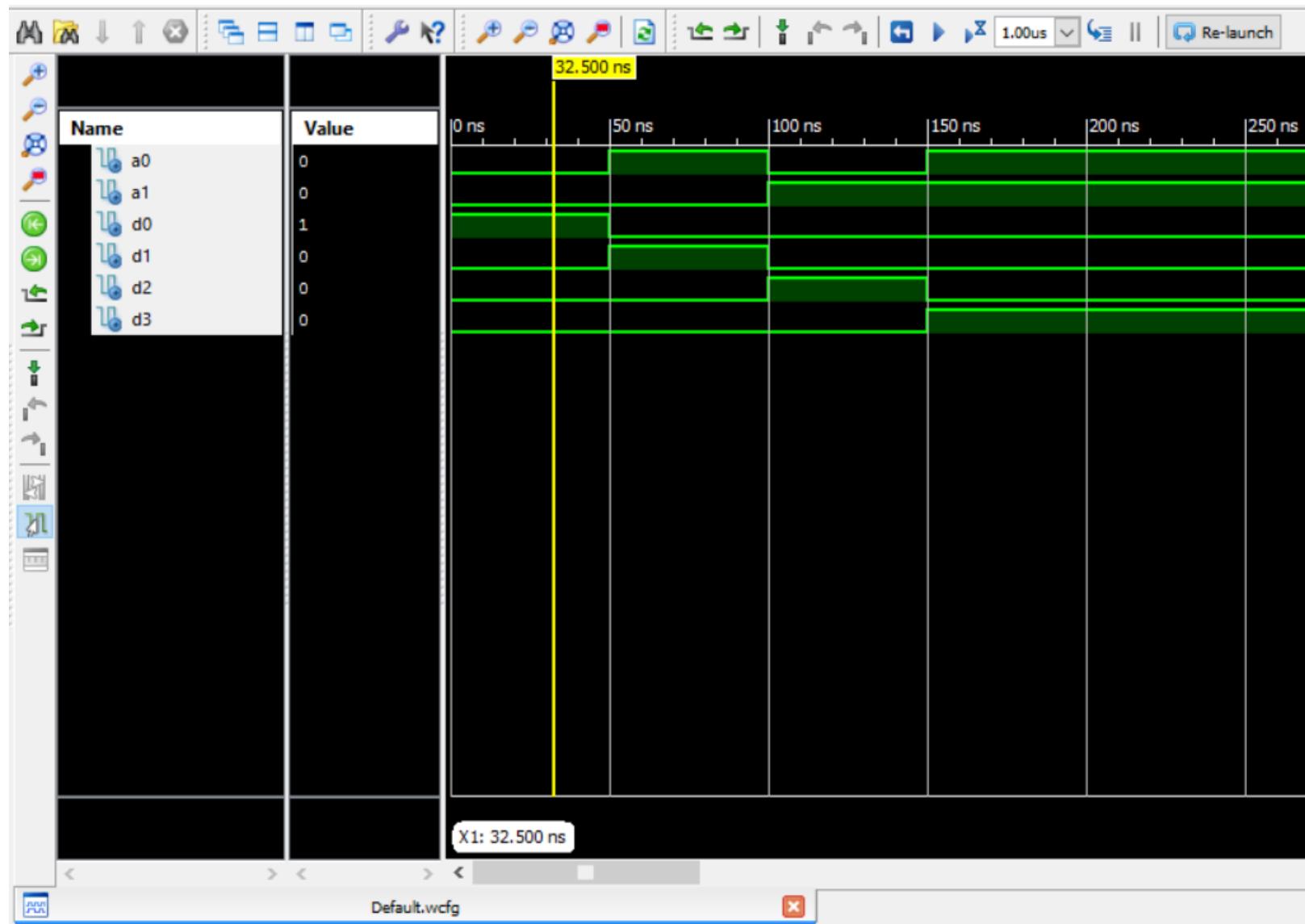
Console

ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully

Ln 57 Col 6 VHDL

# Wave Form



# Generate VHDL Code

ISE Project Navigator (P.20131013) - D:\Dropbox\My\_Documents\Teaching\CSC343\VHDL\_projects\Project1.xise - [decoder\_4\_2.sch]

File Edit View Project Source Process Add Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

- Project1
  - xc3s50a-5tq144
    - eq2 - sop\_arch (eq2.vhd)
    - eq2 - struc\_arch (eq2.vhd)
    - eq\_bit0\_unit - eq1 - sop\_arch (eq1.vhd)
    - eq\_bit1\_unit - eq1 - sop\_arch (eq1.vhd)
    - inhibit - Behavioral (inhibit.vhd)
    - ALU1 (ALU1.sch)
    - XLXI\_22 - mux4\_1 (mux4\_1.sch)
    - comparator1 (comparator1.sch)
    - decoder\_4\_2 (decoder\_4\_2.sch) (selected)
    - pet\_d\_ff (pet\_d\_ff.sch)
    - sr\_latch (sr\_latch.sch)
    - temp (temp.sch)

No Processes Running

Processes: decoder\_4\_2

- Design Utilities
  - Create Schematic Symbol
  - Check Design Rules
  - View HDL Functional Model** (selected)
  - View HDL Instantiation Template

decoder\_4\_2.sch

Console

Launching Design Summary/Report Viewer...

Started : "Launching Schematic Editor to edit decoder\_4\_2.sch".

```
graph LR; A((A)) --> Inv1(( )); A --> Inv2(( )); A --> Inv3(( )); A --> Inv4(( )); Inv1 --> Inv5(( )); Inv2 --> Inv6(( )); Inv3 --> Inv7(( )); Inv4 --> Inv8(( )); Inv5 --> And1(( )); Inv6 --> And1; Inv7 --> And2(( )); Inv8 --> And2; And1 --> Inv9(( )); And2 --> Inv9; Inv9 --> Z((Z))
```

File Edit View Project Source Process Tools Window Layout Help

Design

Hierarchy

- Project1
  - xc3s50a-5tq144
    - eq2 - sop\_arch (eq2.vhd)
    - eq2 - struc\_arch (eq2.vhd)
      - eq\_bit0\_unit - eq1 - sop\_arch (eq1.vhd)
      - eq\_bit1\_unit - eq1 - sop\_arch (eq1.vhd)
    - inhibit - Behavioral (inhibit.vhd)
    - ALU1 (ALU1.sch)
      - XLXI\_22 - mux4\_1 (mux4\_1.sch)
      - comparator1 (comparator1.sch)
    - decoder\_4\_2 (decoder\_4\_2.sch)
    - pet\_d\_ff (pet\_d\_ff.sch)
    - sr\_latch (sr\_latch.sch)
    - temp (temp.sch)

No Processes Running

Processes: decoder\_4\_2

  - Design Utilities
    - Create Schematic Symbol
    - Check Design Rules
    - View HDL Functional Model**
    - View HDL Instantiation Template

decoder\_4\_2.sch

```
22 library ieee;
23 use ieee.std_logic_1164.ALL;
24 use ieee.numeric_std.ALL;
25 library UNISIM;
26 use UNISIM.Vcomponents.ALL;
27
28 entity decoder_4_2 is
29     port ( A0 : in    std_logic;
30             A1 : in    std_logic;
31             D0 : out   std_logic;
32             D1 : out   std_logic;
33             D2 : out   std_logic;
34             D3 : out   std_logic);
35 end decoder_4_2;
36
37 architecture BEHAVIORAL of decoder_4_2 is
38     attribute BOX_TYPE : string ;
39     signal XLXN_1 : std_logic;
40     signal XLXN_5 : std_logic;
41     component AND2
42         port ( I0 : in    std_logic;
43                 I1 : in    std_logic;
44                 O : out   std_logic);
45     end component;
46     attribute BOX_TYPE of AND2 : component is "BLACK_BOX";
47
48     component INV
49         port ( I : in    std_logic;
50                 O : out   std_logic);
51     end component;
52     attribute BOX_TYPE of INV : component is "BLACK_BOX";
53
54 begin
55     XLXI_1 : AND2
56         port map (I0=>XLXN_5,
```

Ln 27 Col 1 VHDL

# Create Schematic Symbol

ISE Project Navigator (P.20131013) - D:\Dropbox\My\_Documents\Teaching\CSC343\VHDL\_projects\Project1.xise - [decoder\_4\_2.sch]

File Edit View Project Source Process Add Tools Window Layout Help

Design

Hierarchy

- Project1
  - xc3s50a-5tq144
    - eq2 - sop\_arch (eq2.vhd)
    - eq2 - struc\_arch (eq2.vhd)
    - eq\_bit0\_unit - eq1 - sop\_arch (eq1.vhd)
    - eq\_bit1\_unit - eq1 - sop\_arch (eq1.vhd)
    - inhibit - Behavioral (inhibit.vhd)
    - ALU1 (ALU1.sch)
      - XLXI\_22 - mux4\_1 (mux4\_1.sch)
    - comparator1 (comparator1.sch)
    - decoder\_4\_2 (decoder\_4\_2.sch)
    - pet\_d\_ff (pet\_d\_ff.sch)
    - sr\_latch (sr\_latch.sch)
    - temp (temp.sch)

View: Implementation Simulation

Toolbars: Various icons for design operations.

Schematic Editor Area:

Process Tree:

- No Processes Running
- Processes: decoder\_4\_2
  - Design Utilities
    - Create Schematic Symbol
    - Check Design Rules
    - View HDL Functional Model
    - View HDL Instantiation Template

Bottom Status Bar:

- Design
- Files
- Libraries
- Symbols
- C
- decoder\_4\_2.sch

Console Output:

```
Launching Design Summary/Report Viewer...
Started : "Launching Schematic Editor to edit decoder_4_2.sch".
```



## Symbols

## Categories

- <--All Symbols-->
- <D:\Dropbox\My\_Documents\Teaching\CSC343\...>
- Arithmetic
- Buffer
- Carry\_Logic
- Comparator
- Counter
- DDR Flip\_Flop
- Decoder
- Flip\_Flop
- General

## Symbols

- d\_latch
- decoder\_4\_2
- mux4\_1
- srl\_latch
- sr\_latch\_en

## Symbol Name Filter

## Orientation

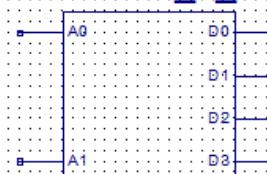
Rotate 0

## Symbol Info



UntitledSchematic1.sch\*

decoder\_4\_2



## Console

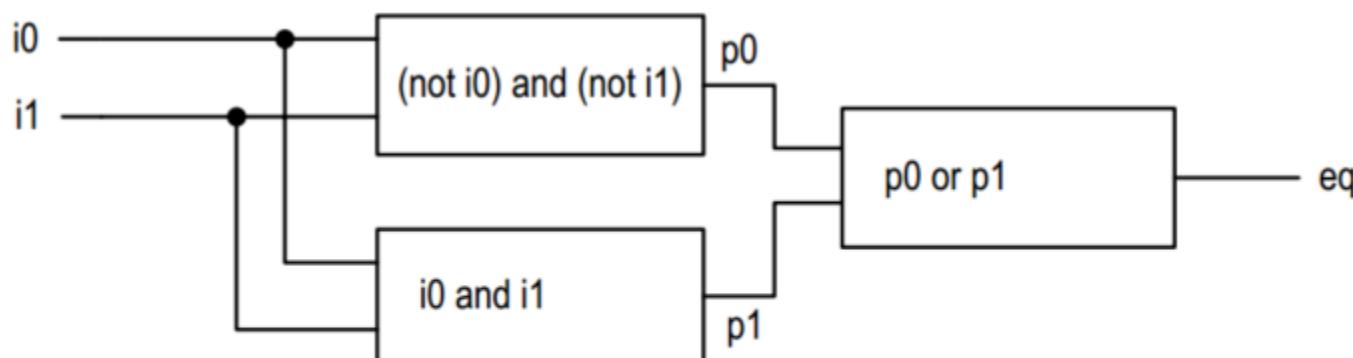
Started : "Launching ISE Text Editor to view decoder\_4\_2.vhf".

Process "View HDL Functional Model" completed successfully

# VHDL example: 1-bit Equality Comparator

**Table 1.1** Truth table of a 1-bit equality comparator

input		output
$i_0$	$i_1$	$eq$
0	0	1
0	1	0
1	0	0
1	1	1



**Figure 1.1** Graphical representation of a comparator program.

Design ↔ □ ✎View:  Implementation  Simulation

## Hierarchy

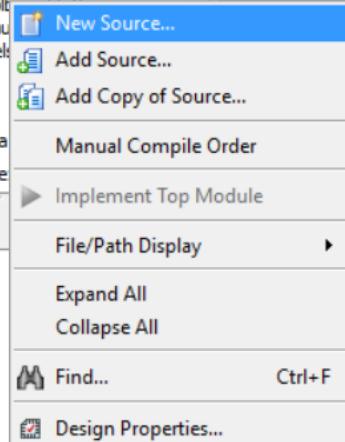
- Project1
  - xc3s50a-5tq144

## Empty View

The view currently contains no files. You can add files to the project using the toolbar commands from the Project menu, Design, Files, and Libraries panel.

## Use:

- New Source: To create a new source file.
- Add Source: To add an existing source file.



No Processes Running

No single design module is selected.

- Design Utilities

Start

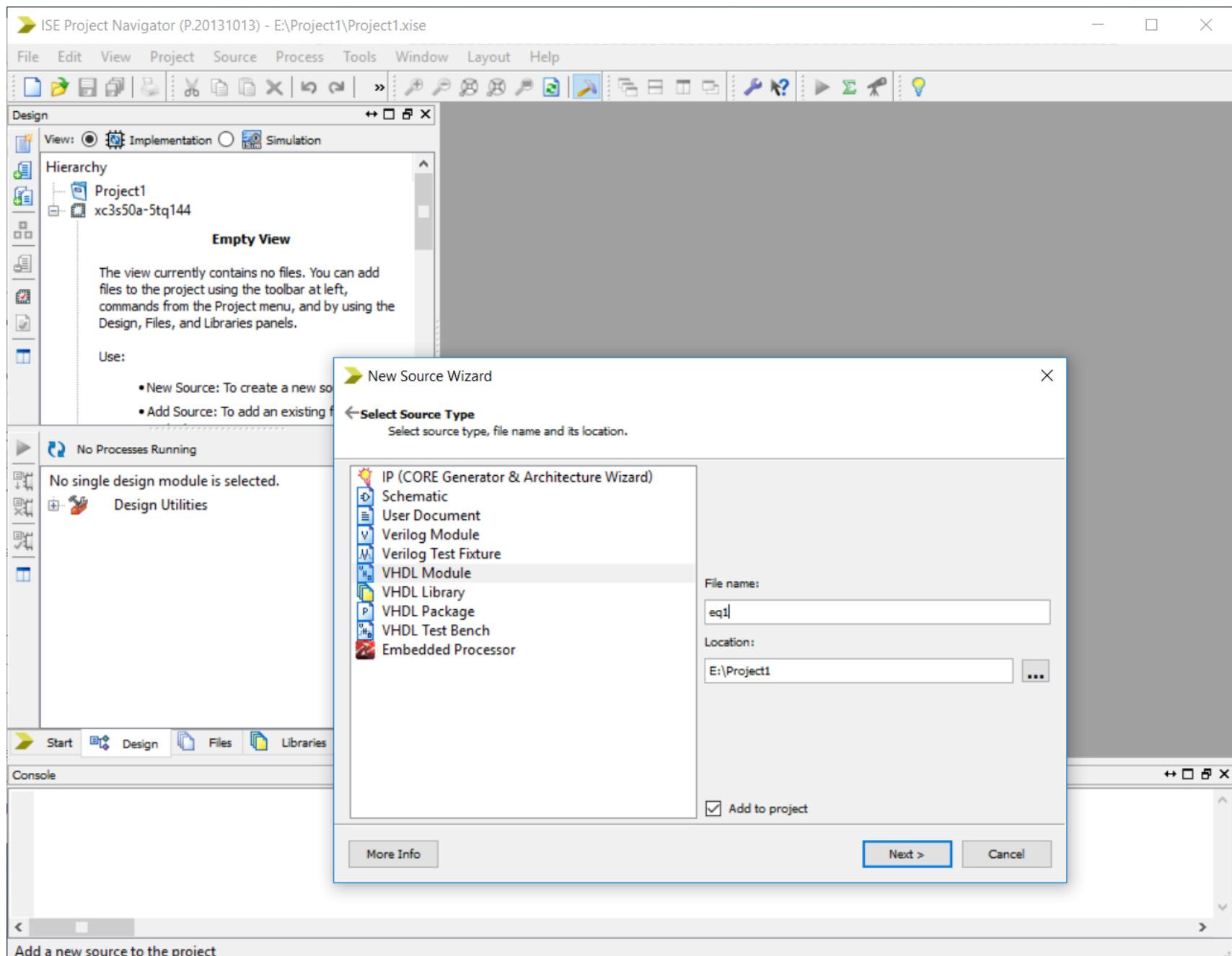
Design

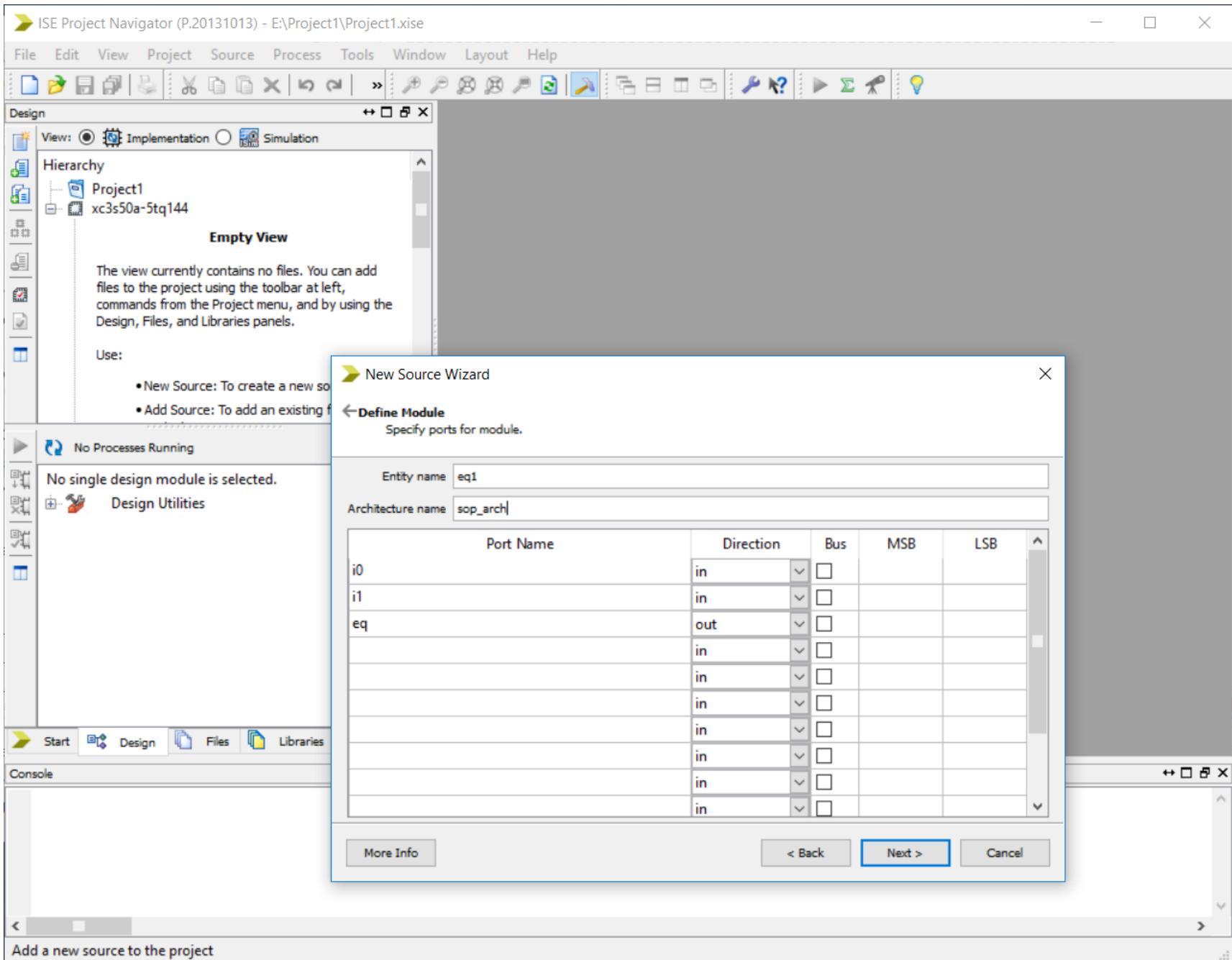
Files

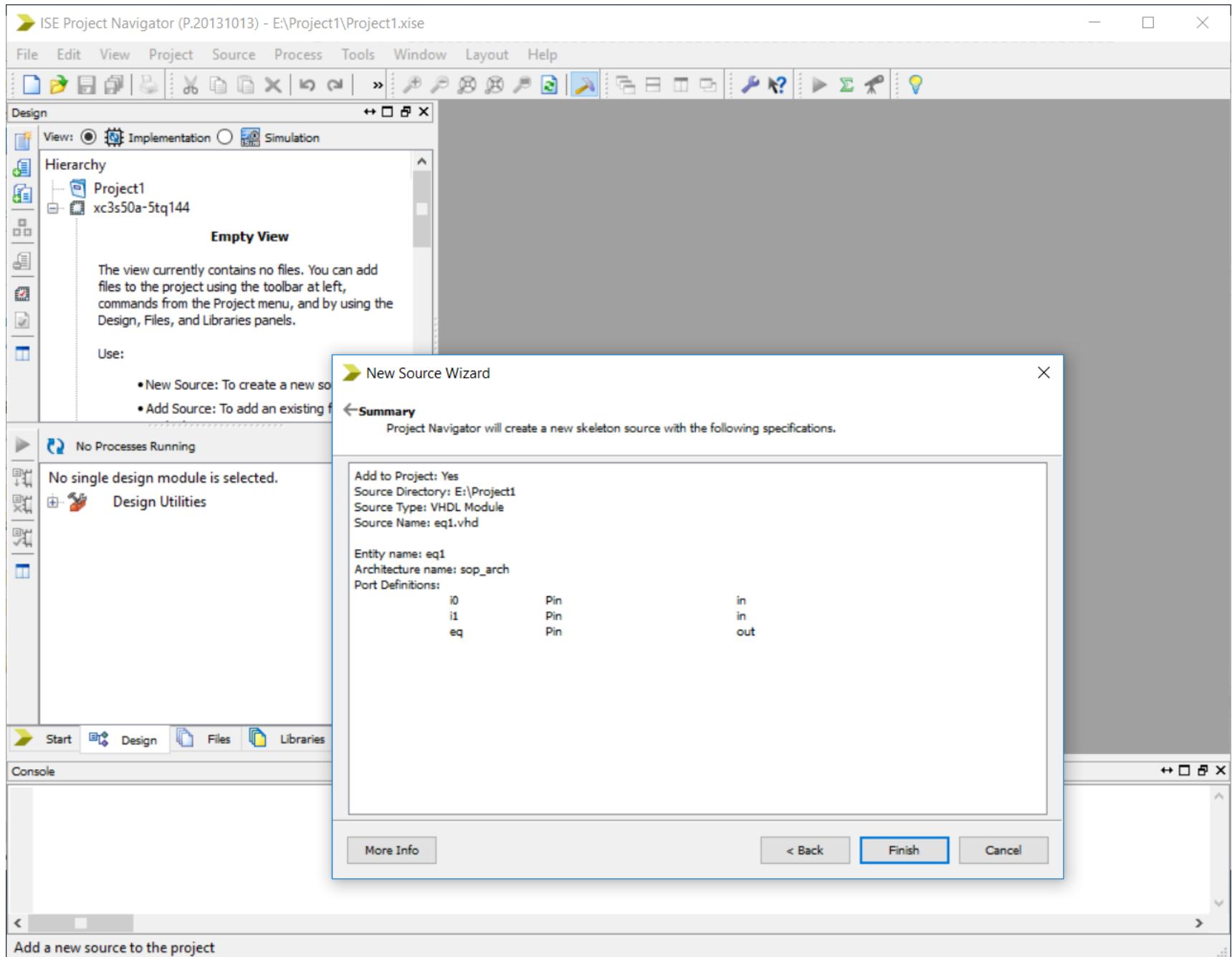
Libraries

## Console

Add a new source to the project







ISE Project Navigator (P.20131013) - E:\Project1\Project1.xise - [eq1.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

- Project1
  - xc3s50a-5tq144
    - eq1 - sop\_arch (eq1.vhd)

No Processes Running

Processes: eq1 - sop\_arch

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
- Implement Design
- Generate Programming File
- Configure Target Device
- Analyze Design Using ChipScope

```
18 --
19 --
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 --
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26 --
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31 
32 entity eq1 is
33     Port ( i0 : in STD_LOGIC;
34             i1 : in STD_LOGIC;
35             eq : out STD_LOGIC);
36 end eq1;
37 
38 architecture sop_arch of eq1 is
39     signal p0, p1: STD_LOGIC;
40 begin
41     -- sum of two product terms
42     eq <= p0 or p1;
43     -- product terms
44     p0 <= (not i0) and (not i1);
45     p1 <= i0 and i1;
46 end sop_arch;
47 
48
```

Start Design Files Libraries

eq1.vhd Design Summary

Console

INFO:HDLCompiler:1061 - Parsing VHDL file "E:/Project1/eq1.vhd" into library work  
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.

Ln 45 Col 20

ISE Project Navigator (P.20131013) - E:\Project1\Project1.xise - [eq1.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design View: Implementation Simulation

Hierarchy

- Project1
  - xc3s50a-5tq144
    - eq1 - sop\_arch (eq1.vhd)

No Processes Running

Processes: eq1 - sop\_arch

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
  - View RTL Schematic
  - View Technology Schematic
  - Check Syntax
- Generate Post-Synthesis Simulation Model
- Implement Design
- Generate Programming File
- Configure Target Device
- Analyze Design Using ChipScope

Start Design Files Libraries

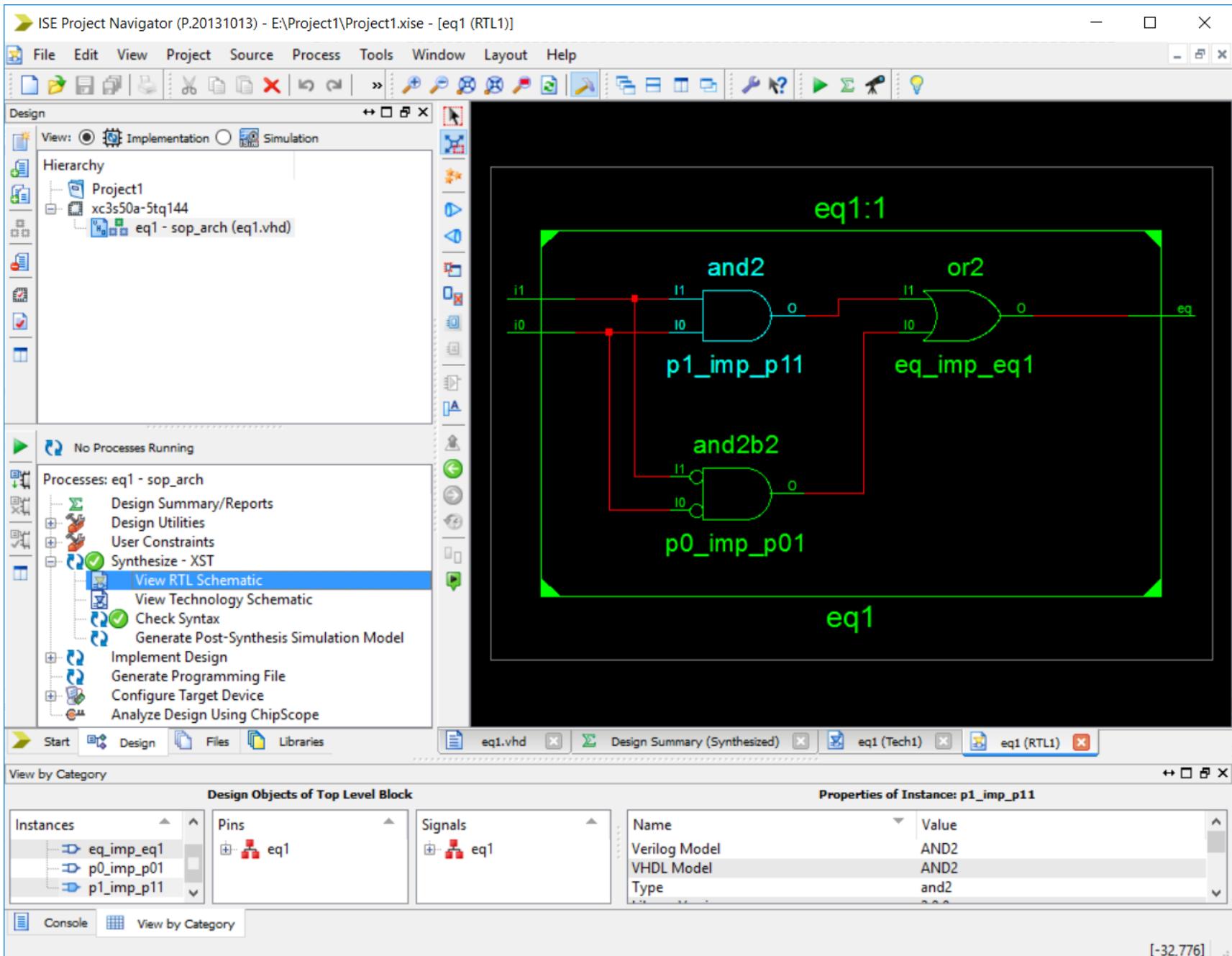
Console

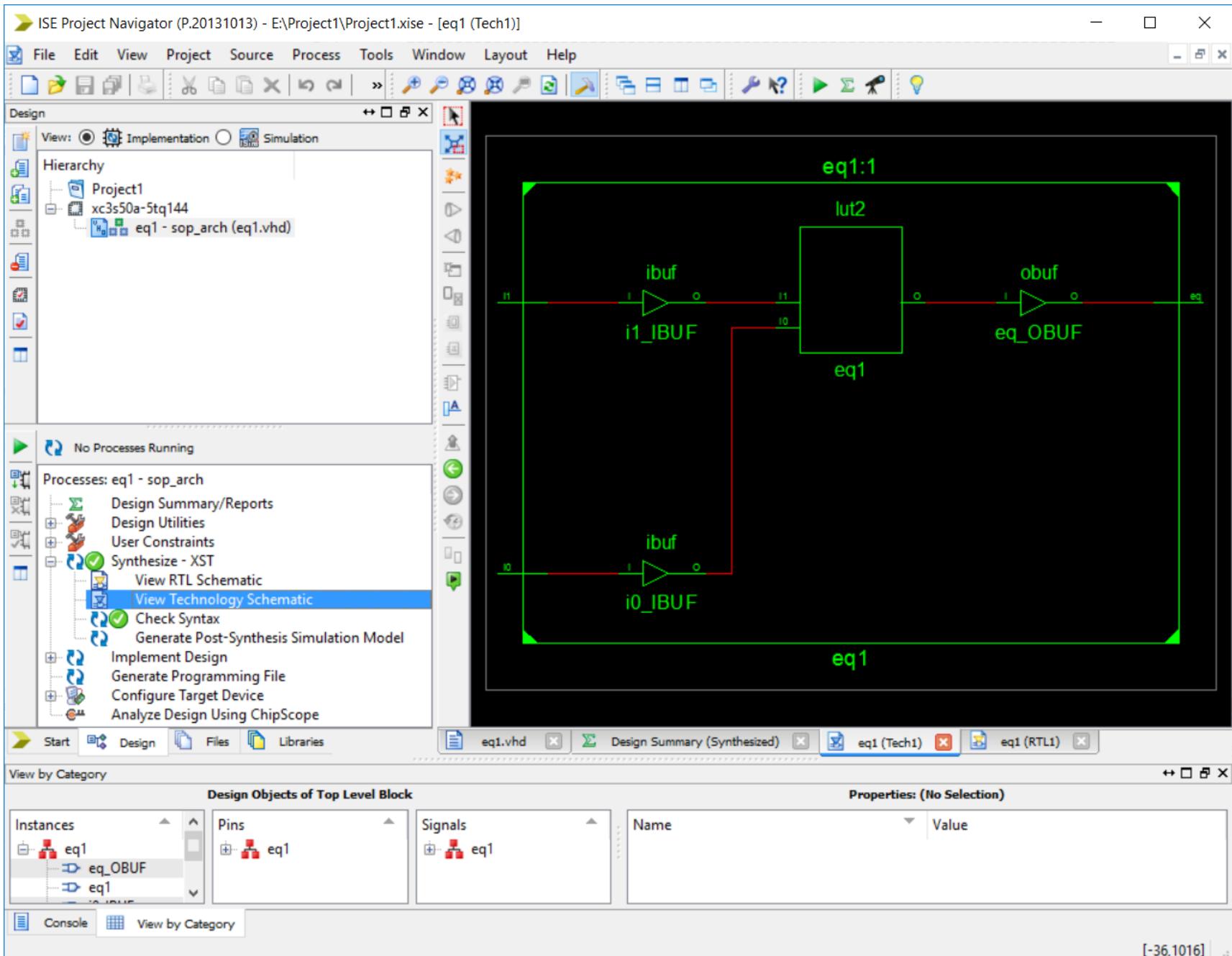
```
Compiling vhdl file "E:/Project1/eq1.vhd" in Library work.  
Entity <eq1> compiled.  
Entity <eq1> (Architecture <sop_arch>) compiled.  
  
Process "Check Syntax" completed successfully
```

eq1.vhd Design Summary

18 --  
19 --  
20 library IEEE;  
21 use IEEE.STD\_LOGIC\_1164.ALL;  
22  
23 -- Uncomment the following library declaration if using  
24 -- arithmetic functions with Signed or Unsigned values  
25 --use IEEE.NUMERIC\_STD.ALL;  
26  
27 -- Uncomment the following library declaration if instantiating  
28 -- any Xilinx primitives in this code.  
29 --library UNISIM;  
30 --use UNISIM.VComponents.all;  
31  
32 entity eq1 is  
33 Port ( i0 : in STD\_LOGIC;  
34 i1 : in STD\_LOGIC;  
35 eq : out STD\_LOGIC);  
36 end eq1;  
37  
38 architecture sop\_arch of eq1 is  
39 signal p0, p1: STD\_LOGIC;  
40 begin  
41 -- sum of two product terms  
42 eq <= p0 or p1;  
43 -- product terms  
44 p0 <= (not i0) and (not i1);  
45 p1 <= i0 and i1;  
46 end sop\_arch;

Ln 45 Col 20 VHDL





ISE Project Navigator (P.20131013) - E:\Project1\Project1.xise - [eq1 (Tech1)]

File Edit View Project Source Process Tools Window Layout Help

Design

Hierarchy

- Project1
- xc3s50a-5tq144
- eq1 - sop\_arch (eq1.vhd)

No Processes Running

Processes: eq1 - sop\_arch

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
  - View RTL Schematic
  - View Technology Schematic
  - Check Syntax
  - Generate Post-Synthesis
- Implement Design
- Generate Programming File
- Configure Target Device
- Analyze Design Using ChipScope

Start Design Files

View by Category

Design Objects

Instances

- eq1
  - eq\_OBUF
  - eq1
  - eq1\_value

Pins

- eq1

OK Help

LUT Dialog

LUT2\_9  
INIT = 9

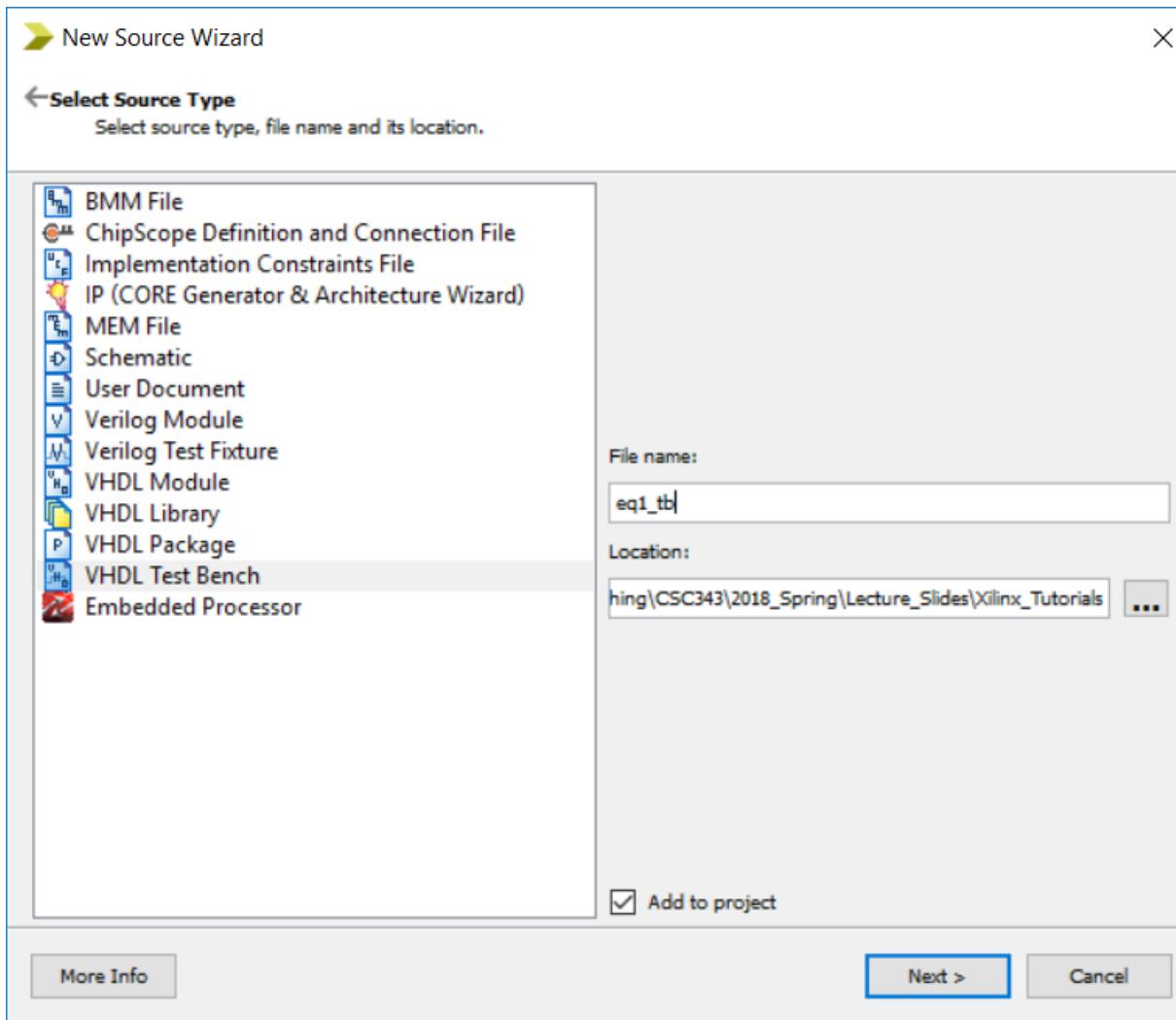
Schematic

TruthTable

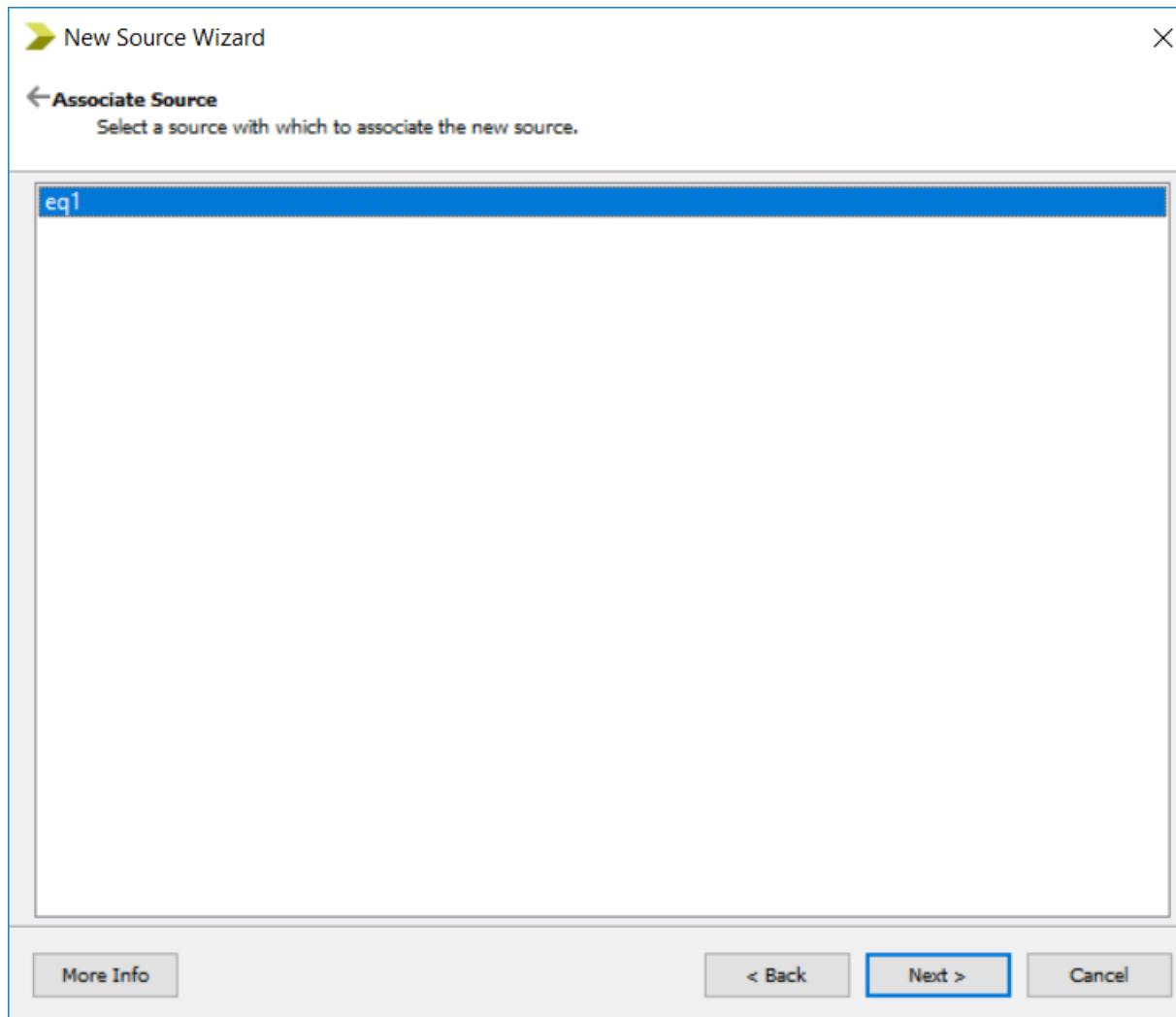
Karnaugh Map

[968,384]

# Create a testbench program (1)



# Create a testbench program (2)



# Create a testbench program (3)

The screenshot shows the Quartus II software interface with the following components:

- Menu Bar:** File, Edit, View, Project, Source, Process, Tools, Window, Layout, Help.
- Toolbar:** Includes icons for file operations, simulation, and design tools.
- Design View:**
  - View:** Implementation (radio button selected), Simulation.
  - Hierarchy:** Shows a project structure under "Xilinx\_Tutorials" and "xc3s50a-5tq144".
  - Processes:** Shows "No Processes Running".
- Process List:** Displays processes including "lSim Simulator", "Behavioral Check Syntax", and "Simulate Behavioral Model". The "Behavioral Check Syntax" item is highlighted with a red dashed border.
- Code Editor:** Displays the VHDL code for the testbench:

```
36 END eq1_tb;
37
38 ARCHITECTURE behavior OF eq1_tb IS
39   -- Component Declaration for the Unit Under Test (UUT)
40   COMPONENT eq1
41     PORT(
42       i0 : IN  std_logic;
43       il : IN  std_logic;
44       eq : OUT std_logic
45     );
46   END COMPONENT;
47   --Inputs
48   signal i0 : std_logic := '0';
49   signal il : std_logic := '0';
50   --Outputs
51   signal eq : std_logic;
52 BEGIN
53   -- Instantiate the Unit Under Test (UUT)
54   uut: eq1 PORT MAP (
55     i0 => i0,
56     il => il,
57     eq => eq
58   );
59   -- Stimulus process
60   stim_proc: process
61   begin
62     -- insert stimulus here
63     i0 <= '0'; il <= '0'; wait for 20 ns;
64     i0 <= '0'; il <= '1'; wait for 20 ns;
65     i0 <= '1'; il <= '0'; wait for 20 ns;
66     i0 <= '1'; il <= '1'; wait for 20 ns;
67     wait;
68   end process;
69 END;
```

**Run Check Syntax before simulation**

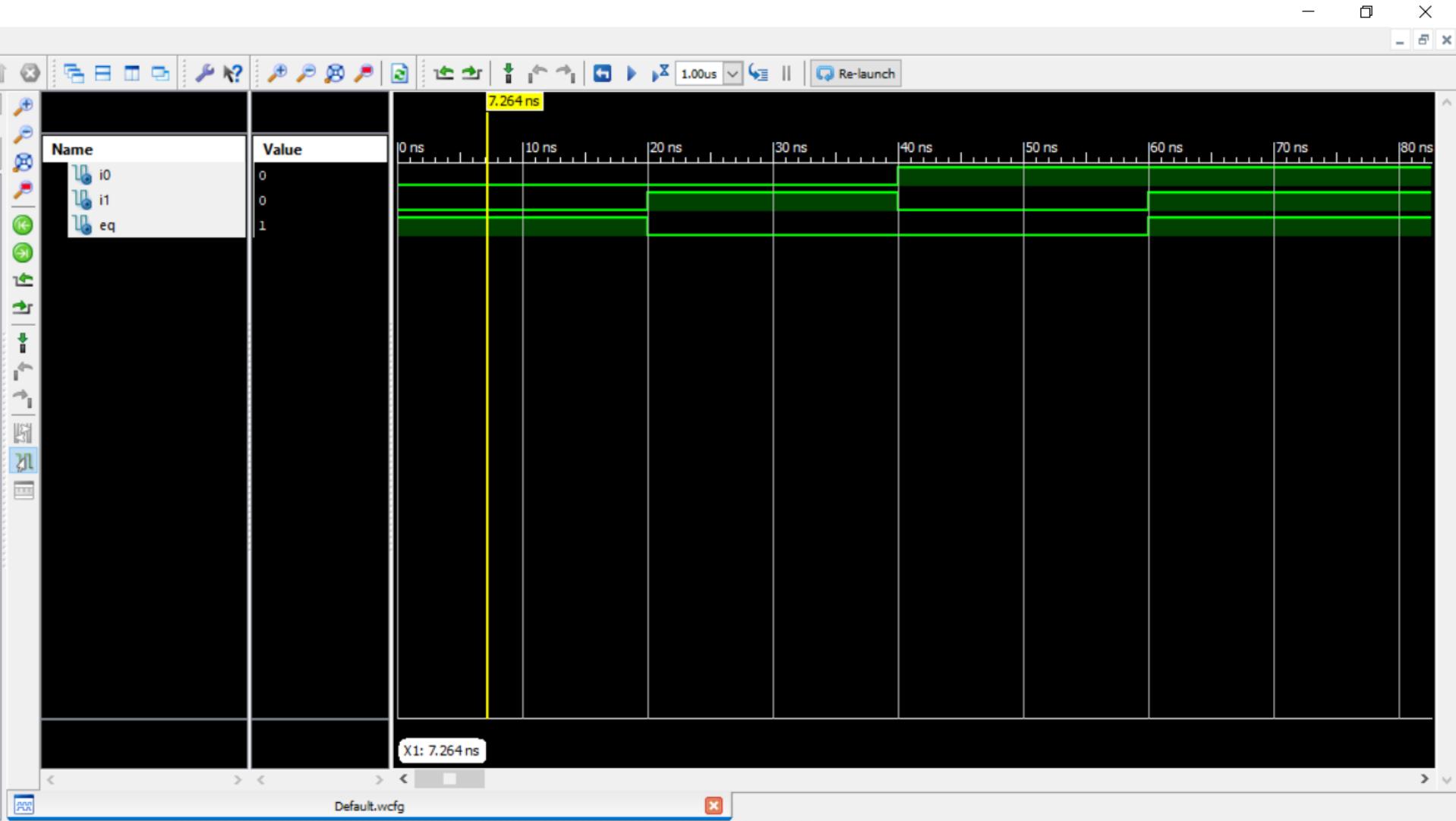
# Create a testbench program (4)

The screenshot shows the Quartus II software interface with the following components:

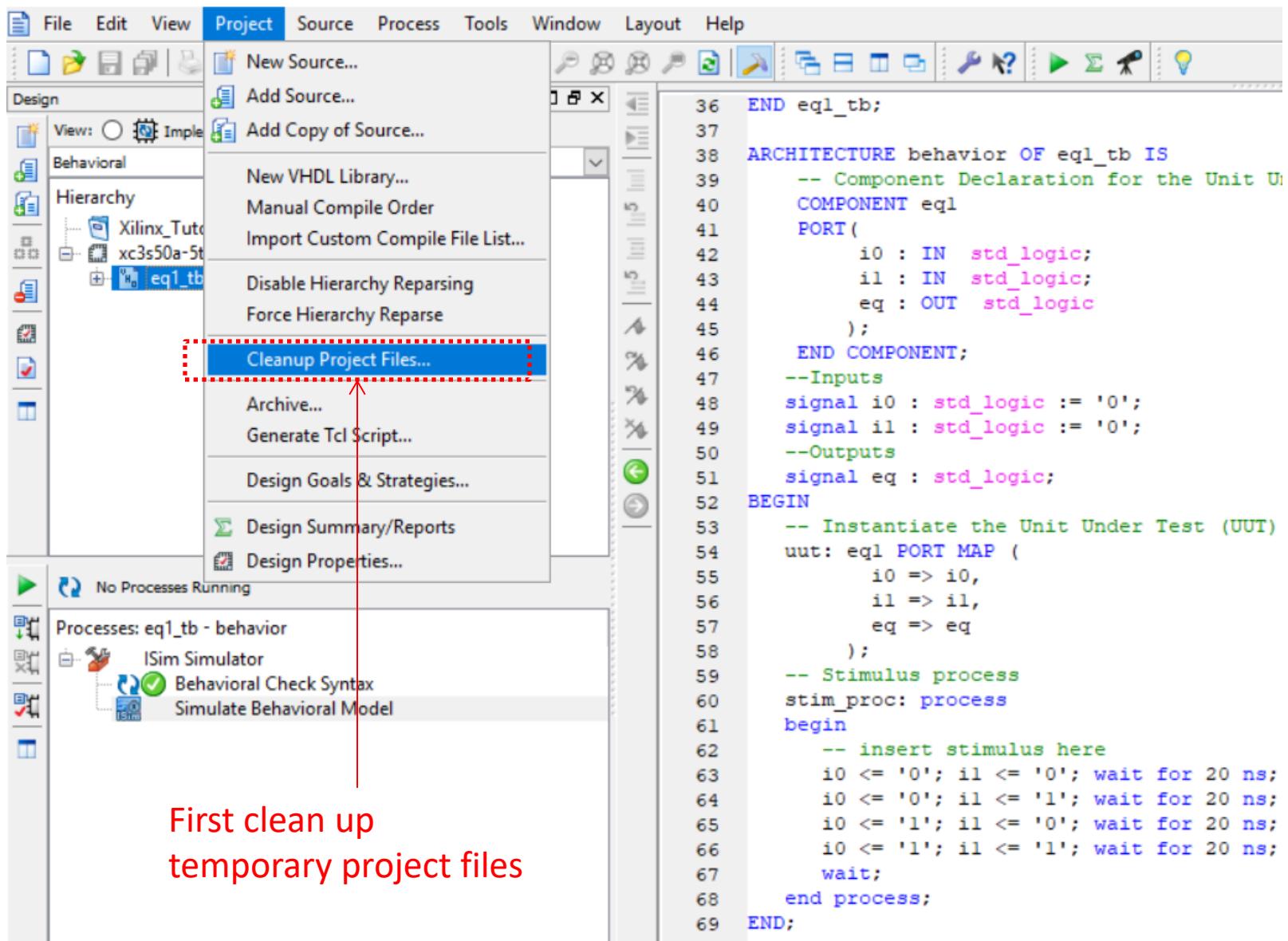
- Menu Bar:** File, Edit, View, Project, Source, Process, Tools, Window, Layout, Help.
- Toolbar:** Includes icons for file operations, search, and simulation.
- Design View:** Shows the project hierarchy under "Behavioral". The current view is set to "Implementation". The hierarchy includes "Xilinx\_Tutorials" and "xc3s50a-5tq144", with "eq1\_tb - behavior (eq1\_tb.vhd)" selected.
- Processes View:** Shows a list of processes. The "Processes: eq1\_tb - behavior" section contains "lSim Simulator", "Behavioral Check Syntax", and "Simulate Behavioral Model". The "Simulate Behavioral Model" item is highlighted with a red dashed border.
- Code Editor:** Displays the VHDL code for the testbench. The code defines an architecture for "eq1\_tb" with a component declaration for "eq", port mappings for inputs "io" and "il", and an output "eq". It also includes a stimulus process "stim\_proc" that waits for 20 ns at various points.
- Text at Bottom:** A red text overlay says "Run simulation" pointing to the highlighted process entry.

```
36 END eq1_tb;
37
38 ARCHITECTURE behavior OF eq1_tb IS
39   -- Component Declaration for the Unit Under Test
40   COMPONENT eq1
41     PORT(
42       io : IN std_logic;
43       il : IN std_logic;
44       eq : OUT std_logic
45     );
46   END COMPONENT;
47   --Inputs
48   signal io : std_logic := '0';
49   signal il : std_logic := '0';
50   --Outputs
51   signal eq : std_logic;
52 BEGIN
53   -- Instantiate the Unit Under Test (UUT)
54   uut: eq1 PORT MAP (
55     io => io,
56     il => il,
57     eq => eq
58   );
59   -- Stimulus process
60   stim_proc: process
61 begin
62   -- insert stimulus here
63   io <= '0'; il <= '0'; wait for 20 ns;
64   io <= '0'; il <= '1'; wait for 20 ns;
65   io <= '1'; il <= '0'; wait for 20 ns;
66   io <= '1'; il <= '1'; wait for 20 ns;
67   wait;
68 end process;
69 END;
```

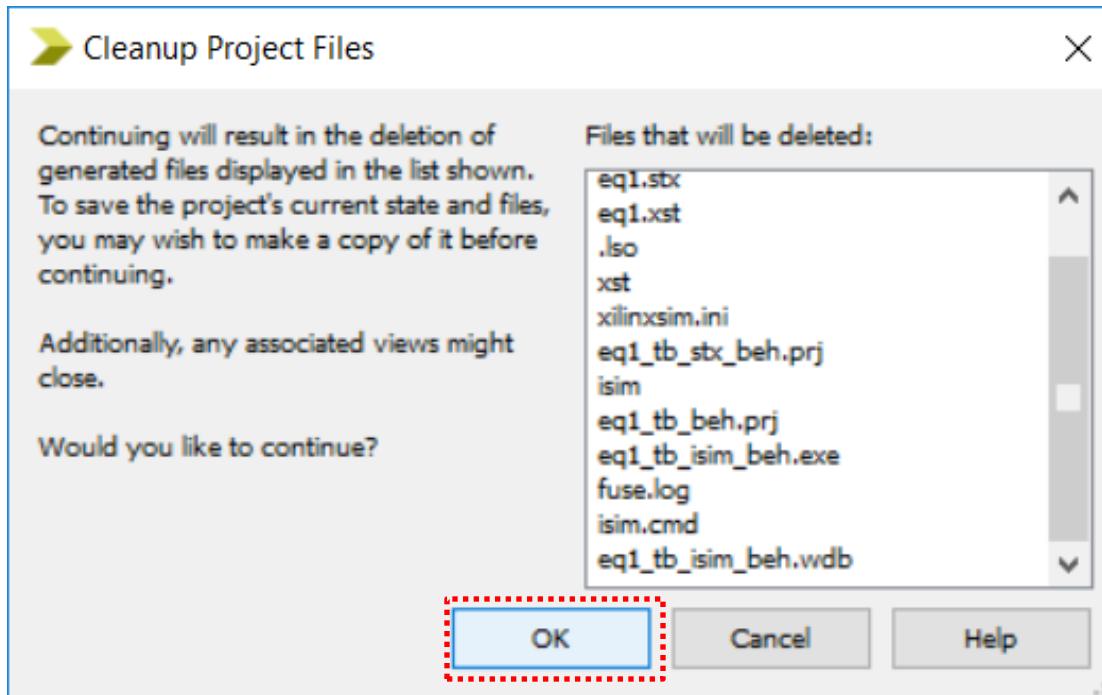
# Simulation results



# Export VHDL project (1)

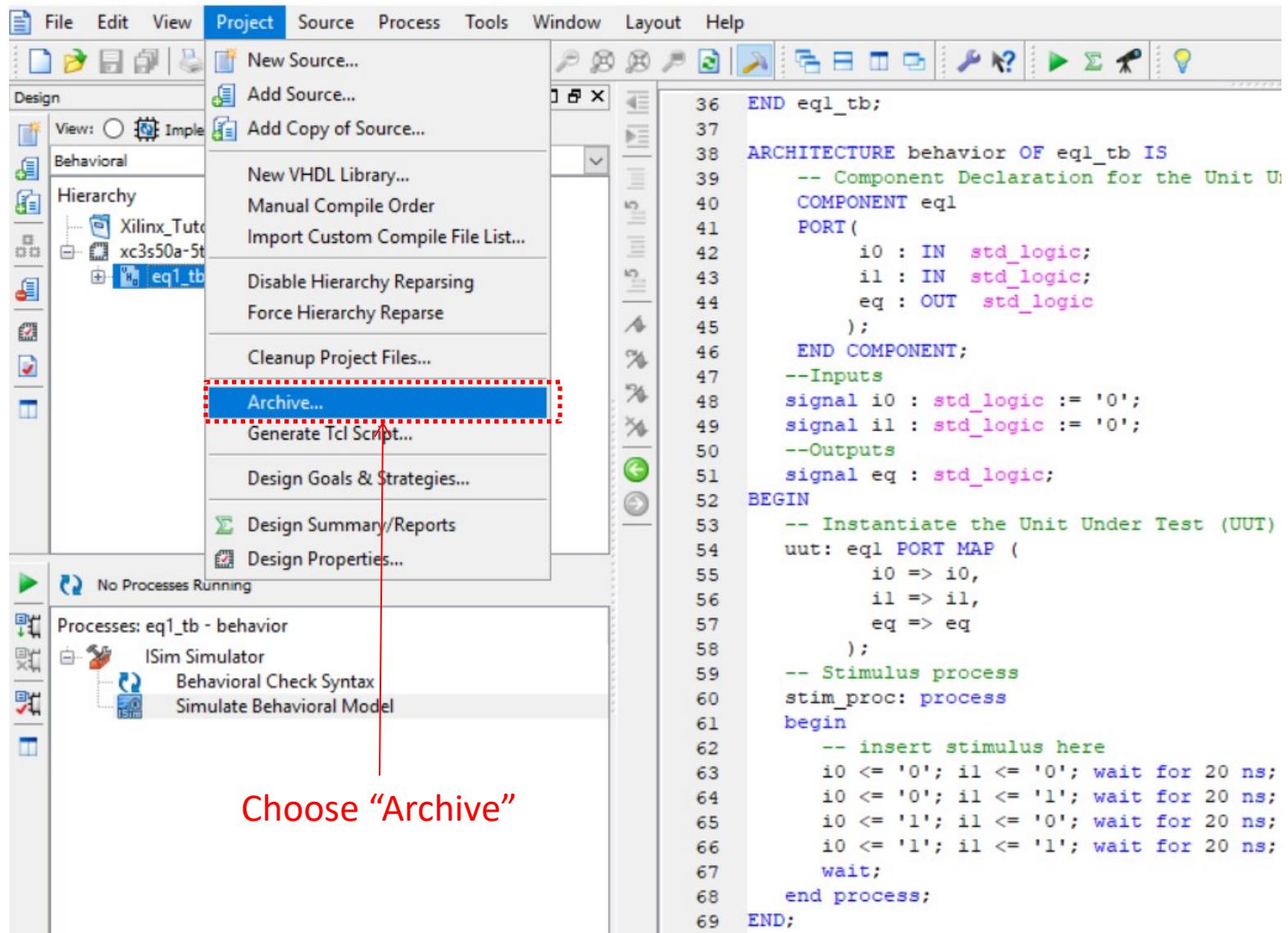


# Export VHDL project (2)



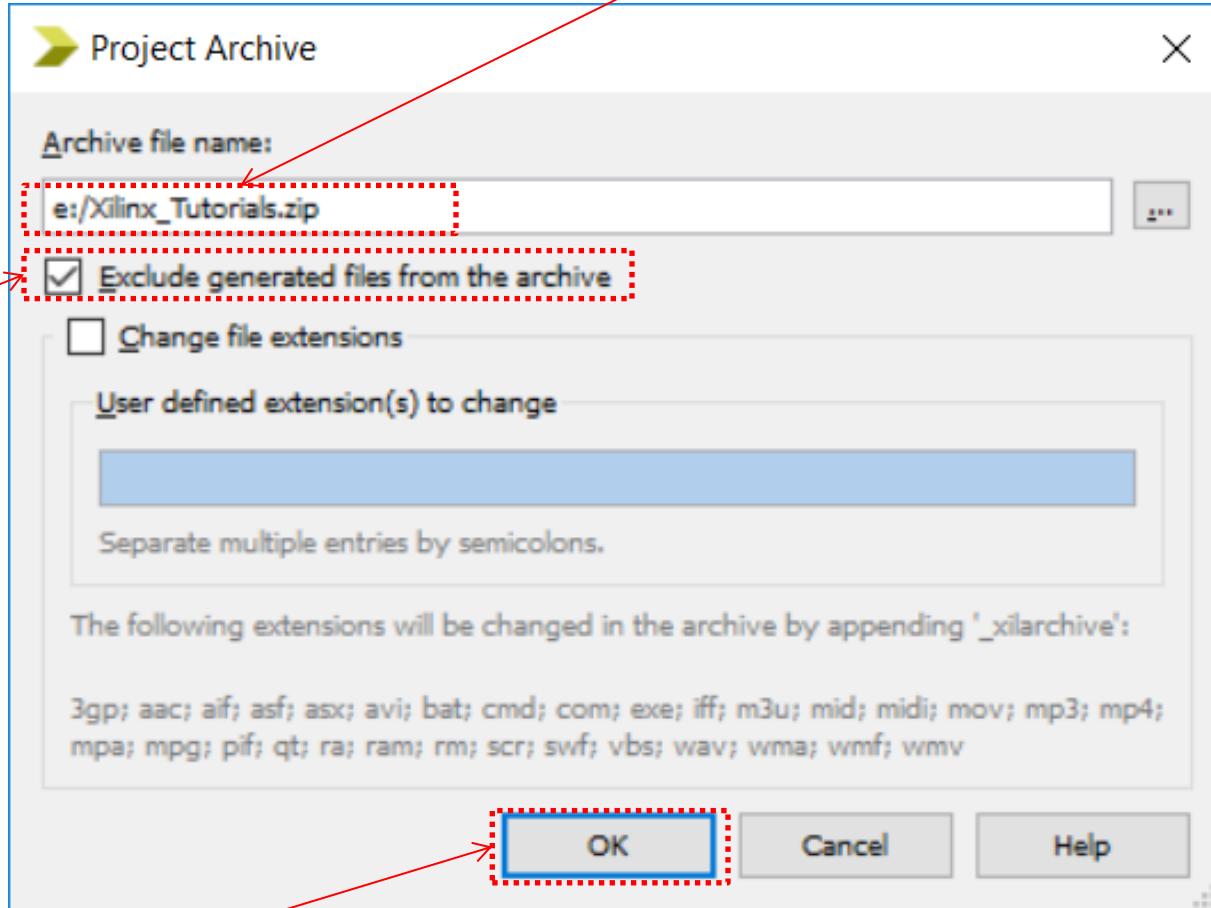
Confirm the cleanup

# Export VHDL project (3)



# Export VHDL project (4)

Choose the filename and where you want the file to be created



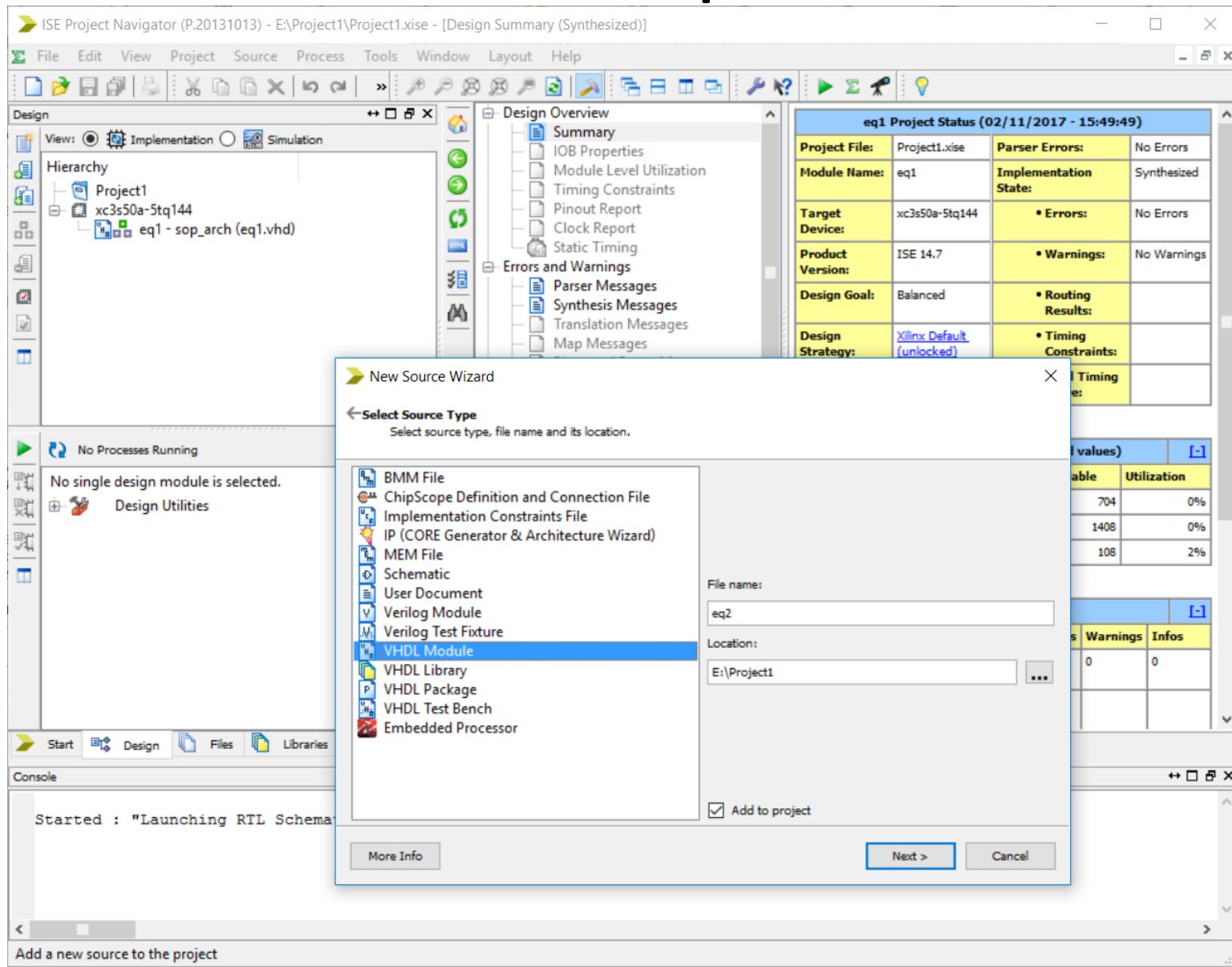
Check this box

Click OK to export your project

# Summary

- Xilinx GUI overview
- Project creation
- Xilinx for digital circuit design
- Xilinx for VHDL programming
- Xilinx simulation
- Xilinx project export

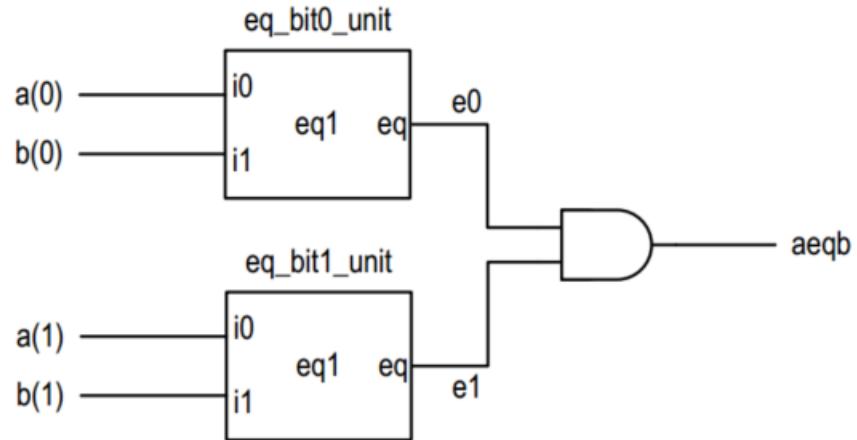
# 2-bit Comparator



# 2-bit Comparator

- Structural implementation

```
architecture struc_arch of eq2 is
    signal e0, e1: std_logic;
begin
    -- instantiate two 1-bit comparators
    eq_bit0_unit: entity work.eq1(sop_arch)
        port map(i0=>a(0), i1=>b(0), eq=>e0);
    eq_bit1_unit: entity work.eq1(sop_arch)
        port map(i0=>a(1), i1=>b(1), eq=>e1);
    -- a and b are equal if individual bits are equal
    eq <= e0 and e1;
end struc_arch;
```



# 2-bit Comparator

- Gate level implementation

- $F = a(1)'b(1)'a(0)'b(0)' + a(1)'b(1)'a(0)b(0) + a(1)b(1)a(0)'b(0)' + a(1)b(1)a(0)b(0)$

```
architecture sop_arch of eq2 is
    signal p0,p1,p2,p3: STD_LOGIC;
begin
    -- sum of product terms
    eq <= p0 or p1 or p2 or p3;
    -- product terms
    p0 <= ((not a(1)) and (not b(1))) and ((not a(0)) and (not b(0)));
    p1 <= ((not a(1)) and (not b(1))) and (a(0) and b(0));
    p2 <= (a(1) and b(1)) and ((not a(0)) and (not b(0)));
    p3 <= (a(1) and b(1)) and (a(0) and b(0));
end sop_arch;
```

ISE Project Navigator (P.20131013) - E:\Project1\Project1.xise - [Design Summary (Synthesized)]

File Edit View Project Source Process Tools Window Layout Help

Design Overview

- Summary
- IOB Properties
- Module Level Utilization
- Timing Constraints
- Pinout Report
- Clock Report
- Static Timing

Errors and Warnings

- Parser Messages
- Synthesis Messages
- Translation Messages
- Map Messages

Project Status (02/11/2017 - 15:49:49)

Project File:	Project1.xise	Parser Errors:	No Errors
Module Name:	eq1	Implementation State:	Synthesized
Target Device:	xc3s50a-5tq144	• Errors:	No Errors
Product Version:	ISE 14.7	• Warnings:	No Warnings
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	

New Source Wizard

Define Module

Specify ports for module.

Entity name: eq2

Architecture name: sop\_arch

Port Name	Direction	Bus	MSB	LSB
a	in	<input checked="" type="checkbox"/>	1	0
b	in	<input checked="" type="checkbox"/>	1	0
eq	out	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		

Values Utilization

704	0%
1408	0%
108	2%

Warnings Infos

0	0
---	---

Start Design Files Libraries

Console

Started : "Launching RTL Schema"

Add a new source to the project

More Info Back Next > Cancel

File Edit View Project Source Process Tools Window Layout Help

Design View: Implementation Simulation

Hierarchy

- Project1
  - xc3s50a-5tq144
    - eq2 - sop\_arch (eq2.vhd)
    - eq2 - struc\_arch (eq2.vhd)
      - eq\_bit0\_unit - eq1 - sop\_arch (eq1.vhd)
      - eq\_bit1\_unit - eq1 - sop\_arch (eq1.vhd)

No Processes Running

Processes: eq2 - struc\_arch

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
  - View RTL Schematic
  - View Technology Schematic
  - Check Syntax
  - Generate Post-Synthesis Simulation Model
- Implement Design
- Generate Programming File
- Configure Target Device
- Analyze Design Using ChipScope

```
32 entity eq2 is
33     Port ( a : in STD_LOGIC_VECTOR (1 downto 0);
34             b : in STD_LOGIC_VECTOR (1 downto 0);
35             eq : out STD_LOGIC);
36 end eq2;
37
38 -- gate level implementation
39 architecture sop_arch of eq2 is
40     signal p0,p1,p2,p3: STD_LOGIC;
41 begin
42     -- sum of product terms
43     eq <= p0 or p1 or p2 or p3;
44     -- product terms
45     p0 <= ((not a(1)) and (not b(1))) and
46             ((not a(0)) and (not b(0)));
47     p1 <= ((not a(1)) and (not b(1))) and (a(0) and b(0));
48     p2 <= (a(1) and b(1)) and ((not a(0)) and (not b(0)));
49     p3 <= (a(1) and b(1)) and (a(0) and b(0));
50 end sop_arch;
51
52 -- structural level implementation
53 architecture struc_arch of eq2 is
54     signal e0, e1: std_logic;
55 begin
56     -- instantiate two 1-bit comparators
57     eq_bit0_unit: entity work.eq1(sop_arch)
58         port map(i0=>a(0), i1=>b(0), eq=>e0);
59     eq_bit1_unit: entity work.eq1(sop_arch)
60         port map(i0=>a(1), i1=>b(1), eq=>e1);
61     -- a and b are equal if individual bits are equal
62     eq <= e0 and e1;
63 end struc_arch;
```

Start Design Files Libraries

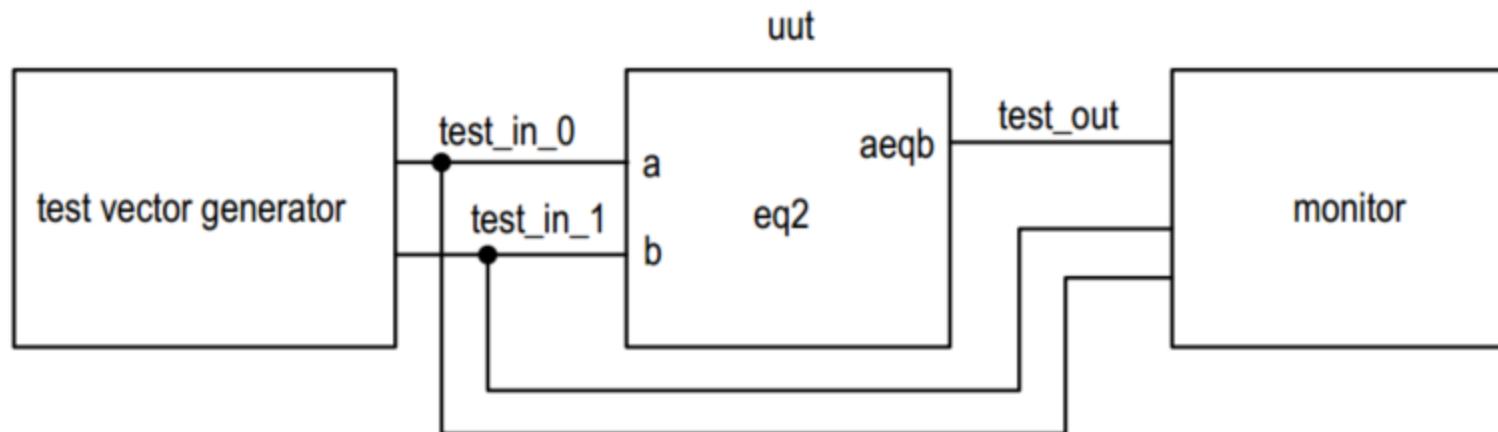
Console

INFO:HDLCompiler:1061 - Parsing VHDL file "E:/Project1/eq2.vhd" into library work  
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.

Ln 37 Col 1 VHDL

# Testbench

- A special program to mimic a physical lab bench



**Figure 1.3** Testbench for a 2-bit comparator.



Design

View: Implementation Simulation

Hierarchy

- Project1
  - xc3s50a-5tq144
    - eq2 - sop\_arch (eq2.vhd)
    - eq2 - struc\_arch (eq2.vhd)
    - eq\_bit0\_unit - eq1 - sop\_arch (eq1.vhd)
    - eq\_bit1\_unit - eq1 - sop\_arch (eq1.vhd)

```
32 entity eq2 is
33     Port ( a : in STD_LOGIC_VECTOR (1 downto 0);
34                     b : in STD_LOGIC_VECTOR (1 downto 0);
35                     eq : out STD_LOGIC);
36 end eq2;
37
38 -- gate level implementation
39 architecture sop_arch of eq2 is
40     signal p0,p1,p2,p3: STD_LOGIC;
41 begin
42     -- sum of product terms
43     eq <= p0 or p1 or p2 or p3;
44     -- product terms
45     p0 <= ((not a(1)) and (not b(1))) and
```

New Source Wizard

Select Source Type

Select source type, file name and its location.

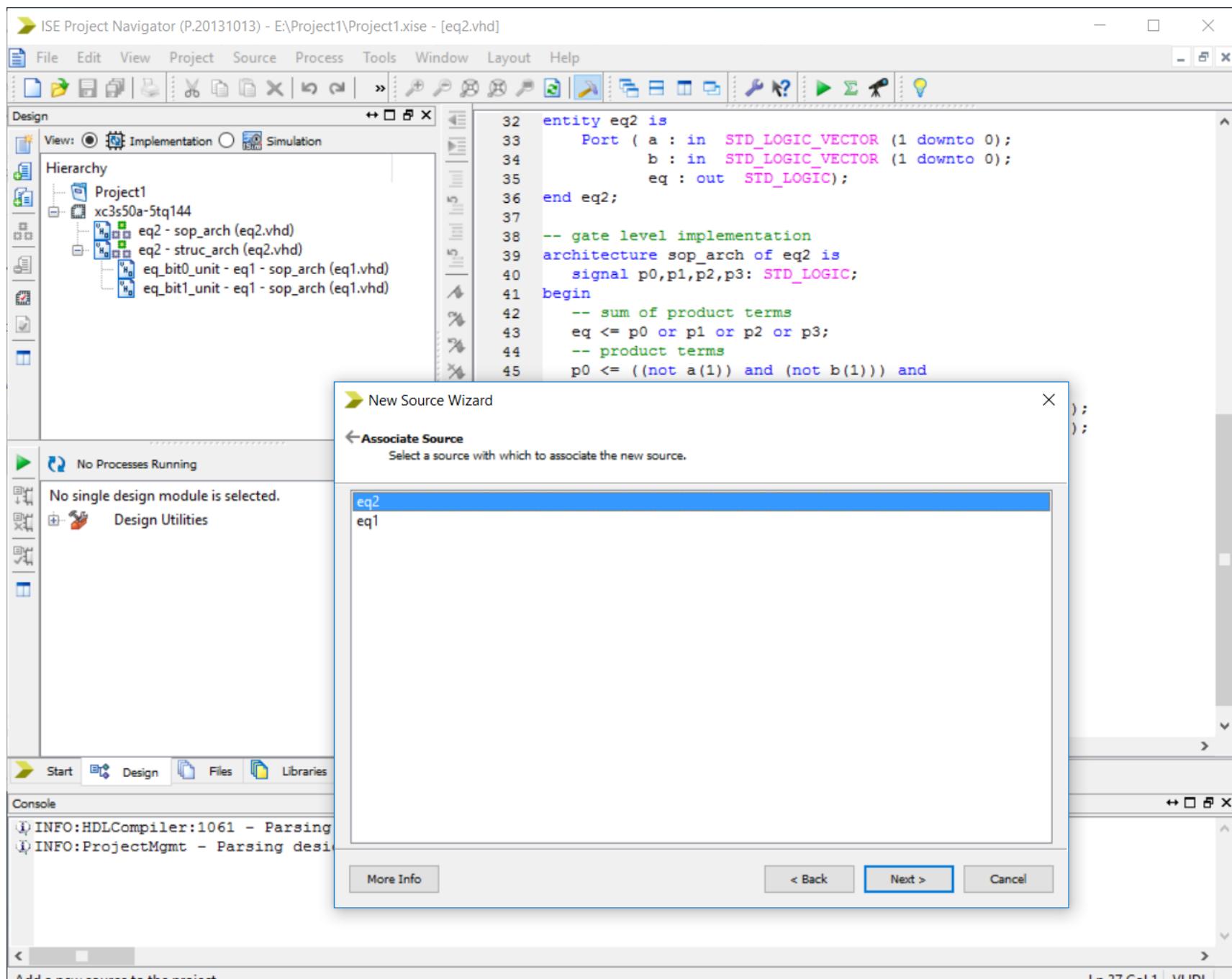
BMM File  
ChipScope Definition and Connection File  
Implementation Constraints File  
IP (CORE Generator & Architecture Wizard)  
MEM File  
Schematic  
User Document  
Verilog Module  
Verilog Test Fixture  
VHDL Module  
VHDL Library  
VHDL Package  
**VHDL Test Bench**  
Embedded Processor

File name: eq2\_testbench

Location: E:\Project1

Add to project

More Info Next > Cancel



File Edit View Project Source Process Tools Window Layout Help

Design View: Implementation Simulation

Hierarchy

- Project1
  - xc3s50a-5tq144
    - eq2\_testbench - behavior (eq2\_testbench.vhd)
    - eq2 - sop\_arch (eq2.vhd)

No Processes Running

Processes: eq2\_testbench - behavior

- ISim Simulator
  - Behavioral Check Syntax
  - Simulate Behavioral Model

```
32 -- arithmetic functions with Signed or Unsigned values
33 --USE ieee.numeric_std.ALL;
34
35 ENTITY eq2_testbench IS
36 END eq2_testbench;
37
38 ARCHITECTURE behavior OF eq2_testbench IS
39   --Inputs
40   signal test_a : std_logic_vector(1 downto 0) := (others => '0');
41   signal test_b : std_logic_vector(1 downto 0) := (others => '0');
42   --Outputs
43   signal test_eq : std_logic;
44
45 BEGIN
46   -- Instantiate the Unit Under Test (UUT)
47   uut: entity work.eq2(struc_arch) PORT MAP (a => test_a, b => test_b, eq => test_eq);
48   -- Stimulus process
49   stim_proc: process
50     begin
51       -- insert stimulus here
52       test_a <= "00"; test_b <= "00"; -- test vector 1
53       wait for 100 ns;
54       test_a <= "01"; test_b <= "00"; -- test vector 2
55       wait for 100 ns;
56       test_a <= "01"; test_b <= "11"; -- test vector 3
57       wait for 100 ns;
58       test_a <= "10"; test_b <= "10"; -- test vector 4
59       wait for 100 ns;
60       test_a <= "10"; test_b <= "00"; -- test vector 5
61       wait for 100 ns;
62       test_a <= "11"; test_b <= "11"; -- test vector 6
63       wait for 100 ns;
64       test_a <= "11"; test_b <= "01"; -- test vector 7
65       wait;
66   end process;
67 END;
```

Start Design Files Libraries eq1.vhd eq2.vhd eq2\_testbench.vhd

Console

```
Parsing VHDL file "E:/Project1/eq2_testbench.vhd" into library isim_temp
Process "Behavioral Check Syntax" completed successfully
```

Ln 66 Col 1 VHDL

# Simulation

ISE Project Navigator (P.20131013) - E:\Project1\Project1.xise - [eq2\_testbench.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design View: Implementation Simulation (selected)

Hierarchy

- Project1
  - xc3s50a-5tg144
  - eq2\_testbench - behavior (eq2\_testbench.vhd) (selected)
  - eq2 - sop\_arch (eq2.vhd)

No Processes Running

Processes: eq2\_testbench - behavior

- ISim Simulator
  - Behavioral Check Syntax (selected)
  - Simulate Behavioral Model

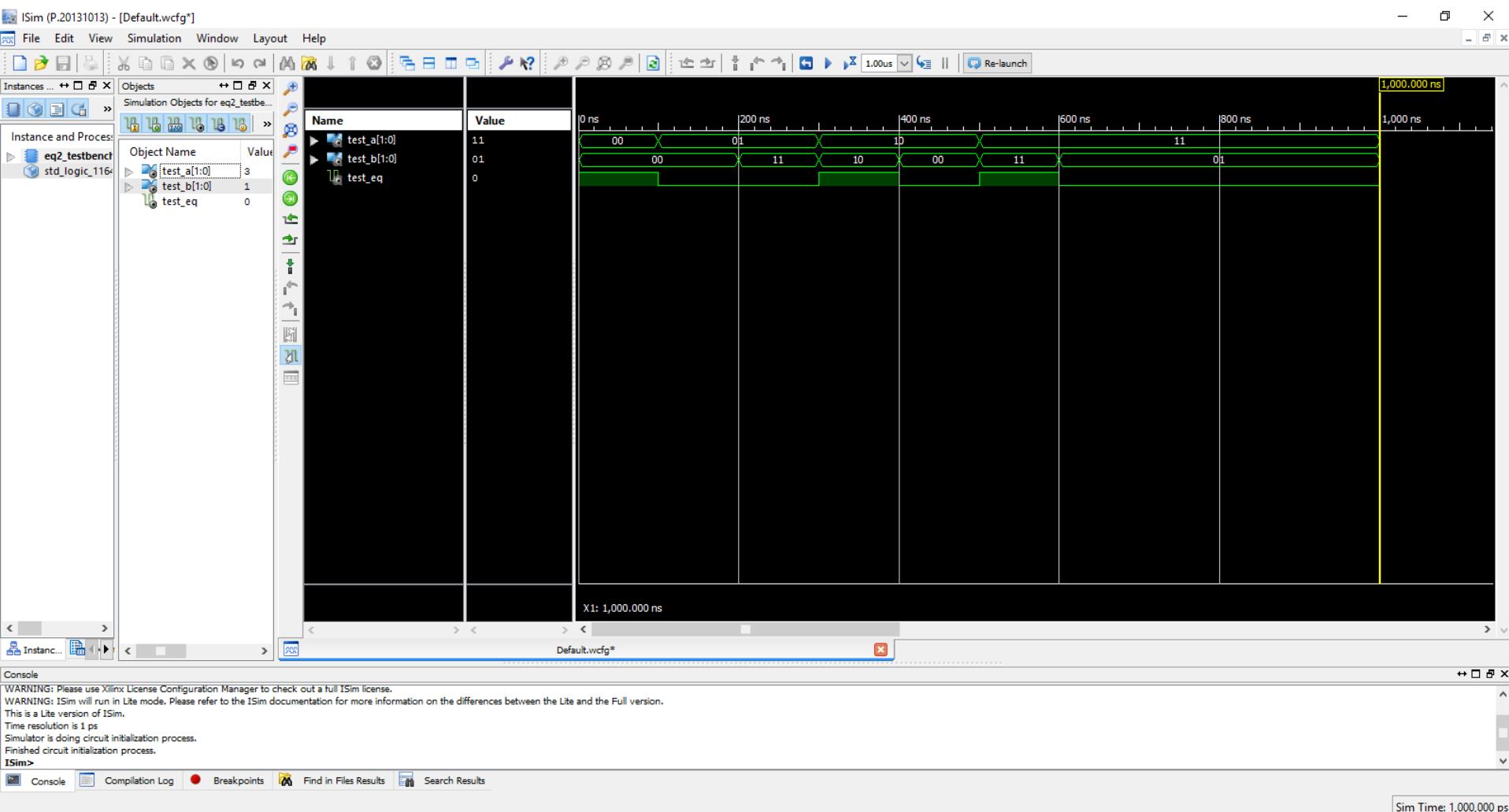
```
32 -- arithmetic functions with Signed or Unsigned values
33 --USE ieee.numeric_std.ALL;
34
35 ENTITY eq2_testbench IS
36 END eq2_testbench;
37
38 ARCHITECTURE behavior OF eq2_testbench IS
39   --Inputs
40   signal test_a : std_logic_vector(1 downto 0) := (others => '0');
41   signal test_b : std_logic_vector(1 downto 0) := (others => '0');
42   --Outputs
43   signal test_eq : std_logic;
44
45 BEGIN
46   -- Instantiate the Unit Under Test (UUT)
47   uut: entity work.eq2(struc_arch) PORT MAP (a => test_a, b => test_b, eq => test_eq);
48   -- Stimulus process
49   stim_proc: process
50     begin
51       -- insert stimulus here
52       test_a <= "00"; test_b <= "00";  -- test vector 1
53       wait for 100 ns;
54       test_a <= "01"; test_b <= "00";  -- test vector 2
55       wait for 100 ns;
56       test_a <= "01"; test_b <= "11";  -- test vector 3
57       wait for 100 ns;
58       test_a <= "10"; test_b <= "10";  -- test vector 4
59       wait for 100 ns;
60       test_a <= "10"; test_b <= "00";  -- test vector 5
61       wait for 100 ns;
62       test_a <= "11"; test_b <= "11";  -- test vector 6
63       wait for 100 ns;
64       test_a <= "11"; test_b <= "01";  -- test vector 7
65       wait;
66   end process;
67 END;
```

Start Design Files Libraries eq1.vhd Design Summary (out of date) eq2.vhd eq2\_testbench.vhd

Console

```
Parsing VHDL file "E:/Project1/eq2_testbench.vhd" into library isim_temp
Process "Behavioral Check Syntax" completed successfully
```

Ln 66 Col 1 VHDL



# Wave Form

