CSC 34300 Computer Systems Design Laboratory

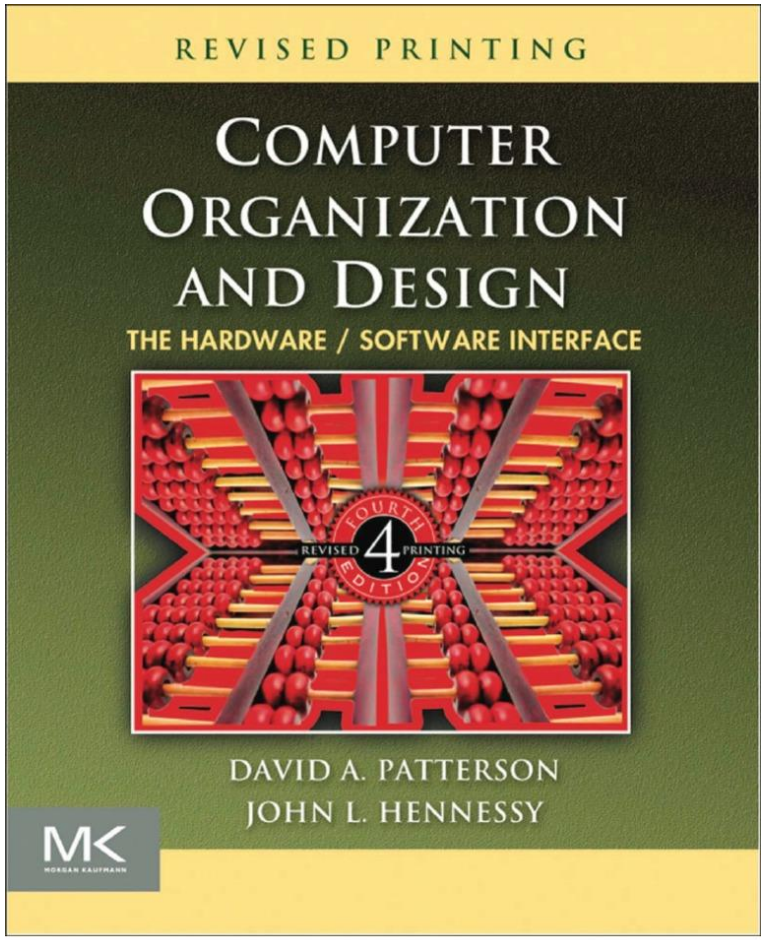
Instructor: Zheng Peng
Assistant Professor
Computer Science Department
City College of New York

Course Information

- CSC34300: Computer Systems Design Laboratory
  - Days and time:
    - Monday/Wednesday 2:00pm - 3:15pm*
  - Classroom:
    - NAC 7/118 (Windows Lab) on Wednesdays
    - NAC 7/106 (Linux Lab) on Mondays
  - Instructor: Zheng Peng
    - Email: zpeng@ccny.cuny.edu
    - Office: NAC 8/203
    - Office hour: Monday/Wednesday 10:00am-11:00am
  - Class website:
    - Hosted by CUNY Blackboard

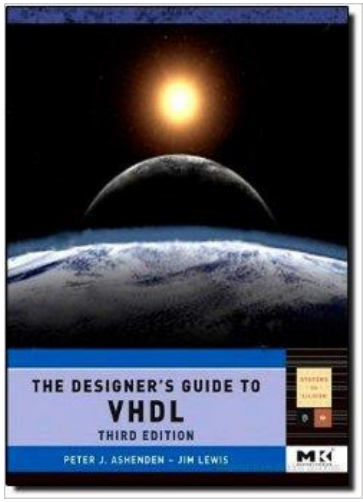
Textbook

- Computer Organization and Design
  - By David A. Patterson and John L. Hennessy
  - Morgan Kaufmann, 4th Edition, 2011.
  - ISBN-13: 978-0123747501
    ISBN-10: 0123747503

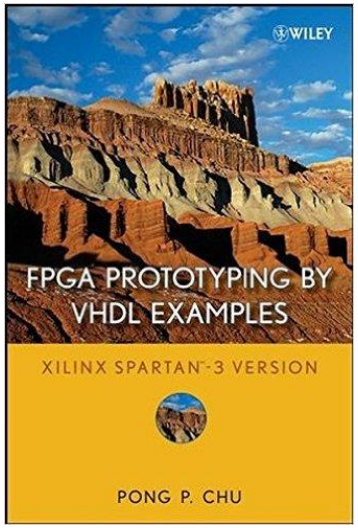


Reference Books

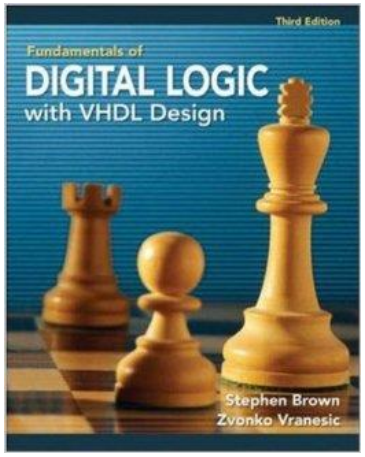
- The Designer's Guide to VHDL, 3rd Edition, by Peter J. Ashenden, Morgan Kaufmann.



- FPGA Prototyping by VHDL Examples: Xilinx Spartan-3 Version, 1st Edition, by Pong P. Chu, Wiley.



- Fundamentals of Digital Logic with VHDL Design, 3rd Edition, by Brown Vranesic, McGraw Hill



Grades and Grading (1)

- Workload:
  - 8 to 10 lab assignments
- Grade scale:
  - A 94-100%
  - A- 90-93%
  - B+ 87-89%
  - B 84-86%
  - B- 80-83%
  - C+ 77-79%
  - C 74-76%
  - C- 70-73%
  - D 60-69%
  - F Failure

Grades and Grading (2)

- Grade change
  - You have one week to request a grade change
  - Grade change will be allowed if
    - Your score is incorrectly added up, or
    - A mistake is made when grading a particular problem

Lab Submission Guidelines

- Students are expected to submit lab report and source files to Blackboard.
- Don’t share your source code or copy others’ source code.
- Lab report
  - The lab report is expected to be a single PDF file.
  - The name of the lab report is expected to be “FirstName_LastName_Lab_X_Report.pdf”
    - Replace “X” with the actual lab number.
- Source files
  - The source files are expected to be packed into a single ZIP file.
    - VHDL source files: please follow the instructions in my Xilinx Tutorial on how to properly export VHDL project files.
    - C/C++/Java source files: please include a README.txt file and give detailed instructions on how to compile and run your program.
  - The name of the zip file is expected to be “FirstName_LastName_Lab_X_Source.zip”
    - Replace “X” with the actual lab number.
- **Submissions that fail to follow the submission guidelines will be returned without any points.**

CSC 34300 Survival Tips

- Start early.
- Ask questions.
- Read the lab description carefully.
- Double check before submission.
  - Use the Virtual Machine to test your source files.
  - If the instructor is unable to run your code and generate the same results as shown in your report, the submission will be considered as incomplete.