Final Project Report

(Machine Learning Intelligent Chip Design)

學生 ： 燕新城　　學號 ：311591023

國 立 陽 明 交 通 大 學

國 際 半 導 體 產 業 學 院 碩 二

E-Mail : samuelyenyen@gmail.com　電話 ：0966071187

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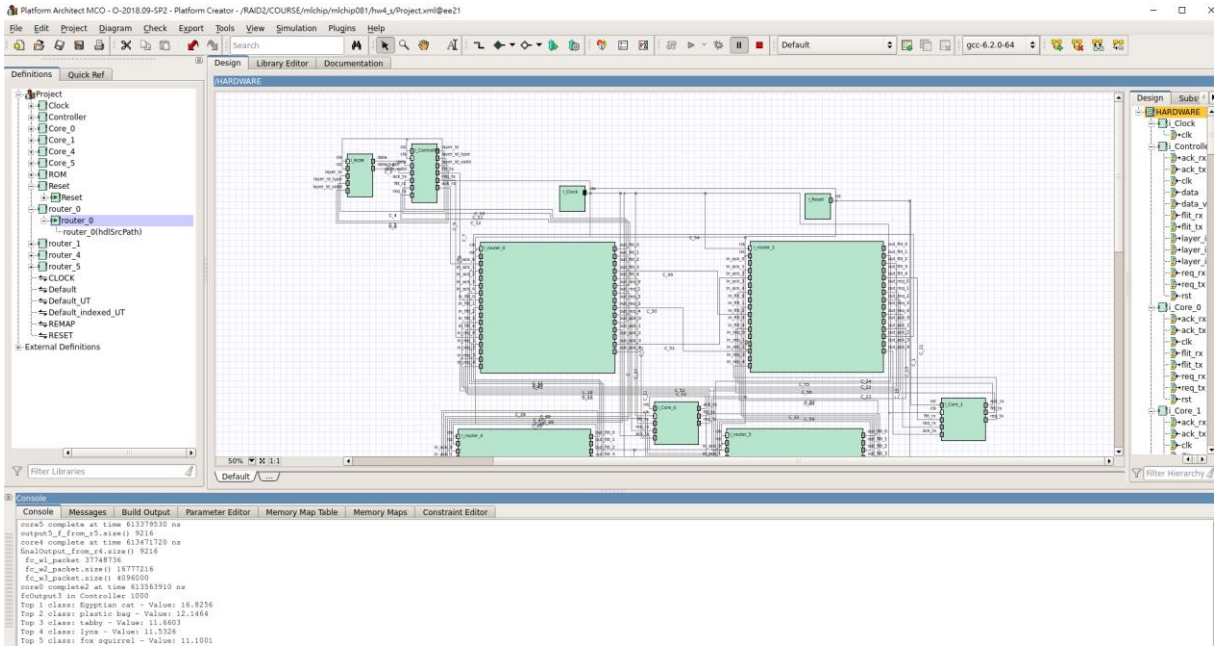
一、Simulation results

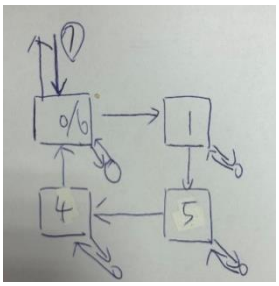
I successfully replaced the router design in Hw4 with Verilog and ran it on the PA.



二、Program Detail

1. Router and NI (I Design My own reset. Let the signal back to 1)

The core concept of the design is to keep the Router as simple and concise as possible. Therefore, it uses four Routers, and the direction of the data flow for each Router is fixed. There are two types of data flows: the first type is when the controller sends data to the Router, and the second type occurs after the transmission, where Router 0's out_flit[4] connects to data coming from different directions.



2. What is the depth of the buffer?

In both the Controller and the router, my buffer length is set to 1 for immediate receive and send, which helps save execution time. On the core, I store the data into different packets based on the length of various parameters.

3. Challenges faced

The biggest issue is the long execution time, especially when reading the FC parameters. Therefore, it's necessary to practice printing information more precisely, and accurately print the size of data passing through each path. The teaching assistant's reset starts at 1, waits for 15ns, and then is pulled to 0. For convenience, I added a piece of code to wait another 15ns before pulling it back to 1.

The teaching assistants have worked hard this semester. I learned a lot through the lab, and I appreciate the teaching assistants' dedication in proctoring our exams and answering our questions. Thank you for allowing us to extend the submission deadline, enabling us to complete the assignment thoroughly.