

Mlchip Fourth Report

(Machine Learning Intelligent Chip Design)

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- Simulation results

成功將資料送進 router 及 core 進行運算,並傳回 controller 進行結果打印。

```
ALL data Form CWB is received

CwS_packet.size() 663552

ALL data Form CWB is received

cbS_packet.size() 384

ALL data Form CWB is received

CwS_packet.size() 384736

ALL data Form CWB is received

CcS_packet.size() 589224

ALL data Form CWB is received

CwS_packet.size() 589224

ALL data Form CWB is received

CwS_packet.size() 589224

ALL data Form CWB is received

CwS_packet.size() 37748736

ALL data Form FCUB is received

fc_wI_packet.size() 37748736

ALL data Form FCUB is received

fc_wI_packet.size() 37748736

ALL data Form FCUB is received

fc_wI_packet.size() 37778736

ALL data Form FCUB is received

fc_wI_packet.size() 4096

ALL data Form FCUB is received

fc_wI_packet.size() 16777216

ALL data Form FCUB is received

fc_wI_packet.size() 4096

ALL data Form FCUB is received

fc_wI_packet.size() 40970

cwI_packet.size() 307700

cwI_packet.size() 663552

cwS_packet.size() 308924

coreD completed at time 612946860 ns

outputS_from_rO.size() 43264

coreD completed at time 612946800 ns

outputS_from_rO.size() 43264

coreS completed at time 613777216

fc_wI_packet.size() 4096000

Top 1 class: Epyptian cat - Value: 11.6003

Top 4 class: Ipynx - Value: 11.6003

Top 5 class: Topx Squirrel - Value: 11.1001

Suspended

22:59 mlchip081@ee21[-/hwd_s]$
```

二、程式細節

1. Router and NI

設計的核心理念為讓 Router 盡可能的簡單、簡潔,因此使用四個 Router,並且固定每個 Router 資料流的方向。資料流分為兩種,第一種為 controller 傳送資料到 Router 時,第二種為傳送完後,Router 0 的 out_flit[4]會分別接上來自不同方向的資料。

```
void run() {
    out_req[0].write(true);
    out_req[1].write(true);
    out_req[1].write(true);
    out_req[3].write(true);
    out_req[3].write(true);
    out_ack[0].write(true);
    out_ack[1].write(true);
    out_ack[2].write(true);
    out_ack[3].write(true);
    out_ack[3].write(true);
    out_ack[3].write(true);
    out_ack[3].write(true);
    out_ack[3].write(true);
    out_ack[3].write(true);
    out_ack[3].write(true);
    out_ack[3].write(true);
    out_ack[3].write(true);
    out_ack[4].write(irue);
    if (first_two bits = receive_data_range(33, 32);
    if (first_two bits = receive_data_ra
```



2. What is the depth of the buffer?

在 Controller 及 router 上,我的 buffer 長度皆為 1,為即收即送,能夠節省執行時間。在 core 上,我根據不同參數的長度,再將資料存入不同的 packet 當中。

3. Challenges faced

最大的問題為執行時間太長,尤其是在讀 FC 的參數時,因此需要練習更精準地打印資訊,將資料經過每個路徑的資料大小都準確地打印出來