Commands

Simulation command

- vcs +v2k –gui design_file.v tb.v
- ./simv –gui
- vcs +v2k –debug_all –gui –y /apps/toshiba/sjsu/verilog/tc240c +libext+.tsbvlibp tb.v design_netlist.v
- dc_shell –f synthesis.script | tee log.txt
- design_vision & DVE

RCA Synthesis Script

```
Set link_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
/apps/synopsys/SYNTH/libraries/syn/dw02.sldb
/apps/synopsys/SYNTH/libraries/syn/dw01.sldb}

Set_target_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}
read_verilog RCA64.v

current_design RCA64

check_design

create_clock clock -name clock -period 18.5600000

set_propagated_clock clock

set_clock_uncertainty 0.25 clock

set_propagated_clock clock

set_fix_hold [ get_clocks clock ]

compile -map_effort medium -incremental_mapping
```

update_timing

set_max_area 2500

report -cell

report_timing -max_paths 10

report_area

report_power

write -hierarchy -format verilog -output RCA64_1_nl.v

quit

CLA-2L Synthesis.script

set link_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
/apps/synopsys/SYNTH/libraries/syn/dw02.sldb
/apps/synopsys/SYNTH/libraries/syn/dw01.sldb}

set target_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}

read_verilog {CLA4.v,CLA4_2.v,CLA16.v CLA16_2.v,CLA_64.v}

current_design CLA_64

check_design

create_clock clock -name clock -period 4.9500000

set_propagated_clock clock

set_clock_uncertainty 0.25 clock

set_propagated_clock clock

```
set_fix_hold [ get_clocks clock ]

compile -map_effort medium -incremental_mapping

update_timing

set_max_area 2500

report -cell

report_timing -max_paths 5

report_area

report_power

write -hierarchy -format verilog -output CLA_64_1_nl.v

quit
```

CSAEQG Synthesis script

```
set link_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
/apps/synopsys/SYNTH/libraries/syn/dw02.sldb
/apps/synopsys/SYNTH/libraries/syn/dw01.sldb}

set target_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}

read_verilog {mux_carry.v,mux_sum.v,CSA64EQG.v}

current_design CSA64EQG

check_design

create_clock clock -name clock -period 5.200000

set_propagated_clock clock
```

```
set_clock_uncertainty 0.25 clock

set_propagated_clock clock

set_fix_hold [ get_clocks clock ]

compile -map_effort medium -incremental_mapping

update_timing

set_max_area 3100

report -cell

report_timing -max_paths 5

report_area

report_power

write -hierarchy -format verilog -output CSA64EQG_1_nl.v

quit
```

CSAUEQG Synthesis.script

```
set link_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
/apps/synopsys/SYNTH/libraries/syn/dw02.sldb
/apps/synopsys/SYNTH/libraries/syn/dw01.sldb}

set target_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}

read_verilog
{FA.v,CSA2.v,CSA3.v,CSA4.v,CSA5.v,CSA6.v,CSA7.v,CSA8.v,CSA9.v,CSA10
.v,CSA11.v,CSA64UEQG.v}

current_design CSA64UEQG
```

```
check_design

create_clock clock -name clock -period 8.00000

set_propagated_clock clock

set_clock_uncertainty 0.25 clock

set_propagated_clock clock

set_fix_hold [ get_clocks clock ]

compile -map_effort medium -incremental_mapping

update_timing

set_max_area 3200

report -cell

report_timing -max_paths 5

report_area

report_power

write -hierarchy -format verilog -output CSA64UEQG_nl.v

quit
```