

SAN JOSÉ STATE UNIVERSITY
Charles W. Davidson College of Engineering
DEPARTMENT OF ELECTRICAL ENGINEERING
EE 271 – Advanced Digital System Design and Synthesis

Fall 2015 Final Project Report
**Implement and Analyze Different Types of
64-bit Adders**

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Executive Summary

The **main aim** of the project is **to implement** different types of **64-bit Adders** and then **optimize and analyze its timing, area and power.**

Four Different types of 64 bit adders are being used:

1. Ripple Carry Adder (**RCA**)
2. Carry Look Ahead Adder with 4-bit group **2-Level P-G Generator (CLA-2L)**
3. Carry Select Adder with **Equal Groups** of 4-bits each (**CSAEQG**)
4. Carry Select Adder with **Unequal grouping.** (**CSAUEQG**)

- **Need to use 1 clock to complete the calculation**
- RTL level implementation **without** using arithmetic operators like +, -, *, and / for hardware implementation

I. General Project Information

Table I.1: List of EDA Tools Used

Name	Company	Used for	Free? (Y/N)	Software Documents
VCS	Synopsis	Simulation & test	No	VCS user guide
Design Vision	Synopsys	Synthesis	No	Design Vision user guide

Table I.2: List of Libraries Used

Library file name	Company	Used with (EDA tool)	The libraries are at (directories on eecad systems)
tc240c	synopsys	VCS	apps/toshiba/sjsu/synopsys/tc240c/tc240c
db_wccom25			db_wccom25
tc240c	synopsys	VCS	/apps/toshiba/sjsu/synopsys/tc240c/tc240c
db_bccom25			db_bccom25
tc240c.workview.sdb	synopsys	VCS	/apps/toshiba/sjsu/synopsys/tc240c/tc240c.workview.sdb

Table I.3: List of Verilog Modules (both design and test modules)

Module Name	Ports	Short Description
RCA64	op1,op2,sum,croout,clock,reset	2 operands to the adder are op1 & op2. Initial cin is not there, outputs are sum and croout. Clock and reset are controlling all the flipflops.
CLA_64	op1,op2,sum,croout,clock,reset	2 operands to the adder are op1 & op2. Initial cin is not there, outputs are sum and croout. Clock and reset are controlling all the flipflops.
CSA64EQG	op1,op2,sum,croout,clock,reset	2 operands to the adder are op1 & op2. Initial cin is not there, outputs are sum and croout. Clock and reset are controlling all the flipflops.
CSA64UEQG	op1,op2,sum,croout,clock,reset	2 operands to the adder are op1 & op2. Initial cin is not there, outputs are sum and croout. Clock and reset are controlling all the flipflops.
RCA64_tb		Test Benches for Ripple Carry adder
RCA64_tb_1		
RCA64_tb_2		
RCA64_tb_3		
RCA64_tb_4		

RCA64_tb_5		
CLA_64_tb CLA_64_tb_1 CLA_64_tb_2 CLA_64_tb_3 CLA_64_tb_4 CLA_64_tb_5		Test Benches for Carry Look Ahead adder
CSA64EQG_tb CSA64EQG_tb_1 CSA64EQG_tb_2 CSA64EQG_tb_3 CSA64EQG_tb_4 CSA64EQG_tb_5		Test Benches for Carry Select adder with Equal bits
CSA64UEQG_tb CSA64UEQG_tb_1 CSA64UEQG_tb_2 CSA64UEQG_tb_3 CSA64UEQG_tb_4 CSA64UEQG_tb_5		Test Benches for Carry Select Adder

II. The Implementation Overview

II. a BLOCK DIAGRAMS OF ADDERS

1. RCA: In this adder, a group of **4-bit full-adder including one 1-bit half-adder** is instantiated for 16 times in which carry of each previous full adder is **ripped** to the next full adder.

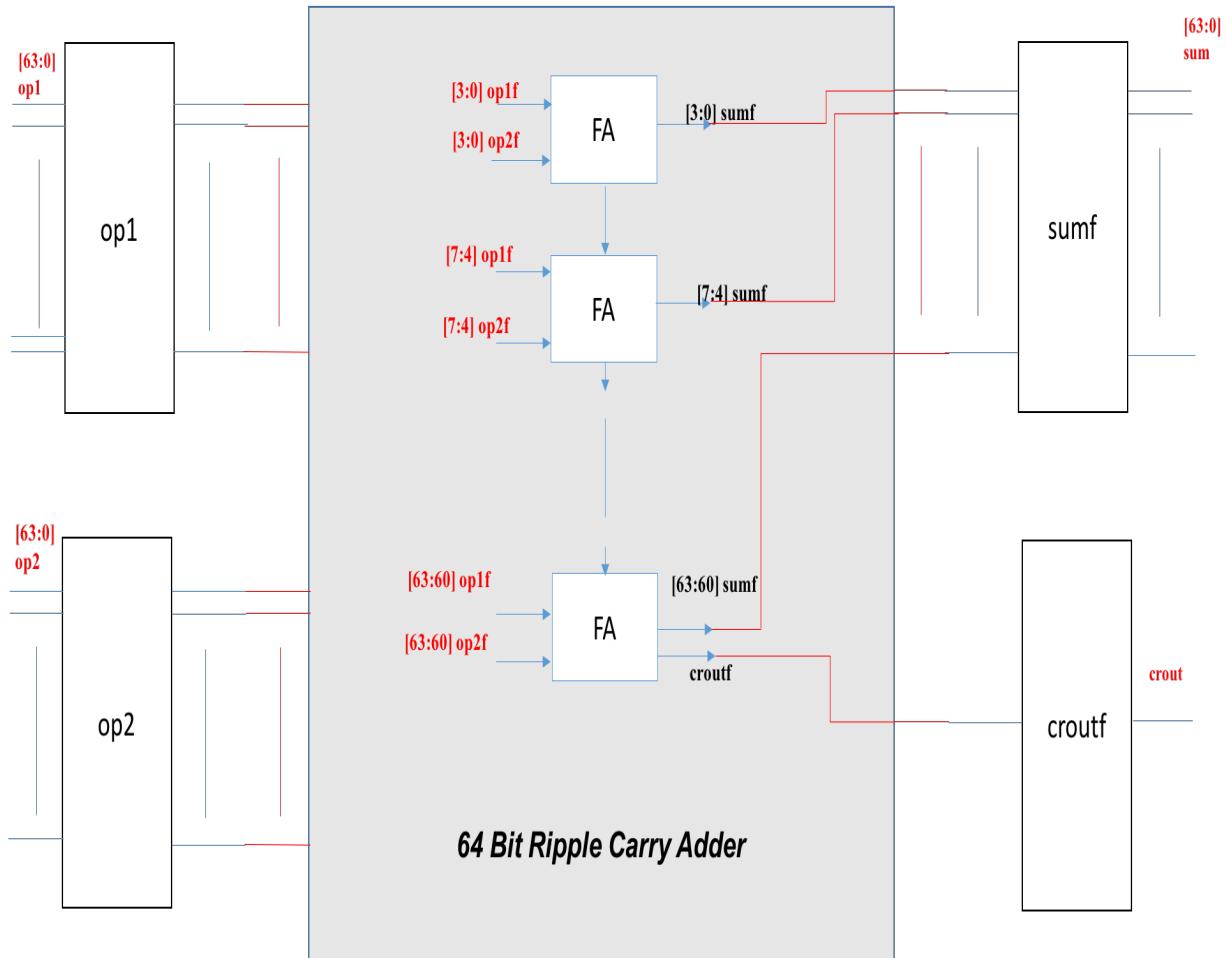


Figure II.1: Overall Block Diagram of the 64-bit RCA

2. CLA: In this adder, a **2-level PG generator** is used which contains a **Group-1: 4-bit full adder with level-1 PG generator and 16-bit adder containing level-2 PG generator containing 4 Group-1 circuits.**

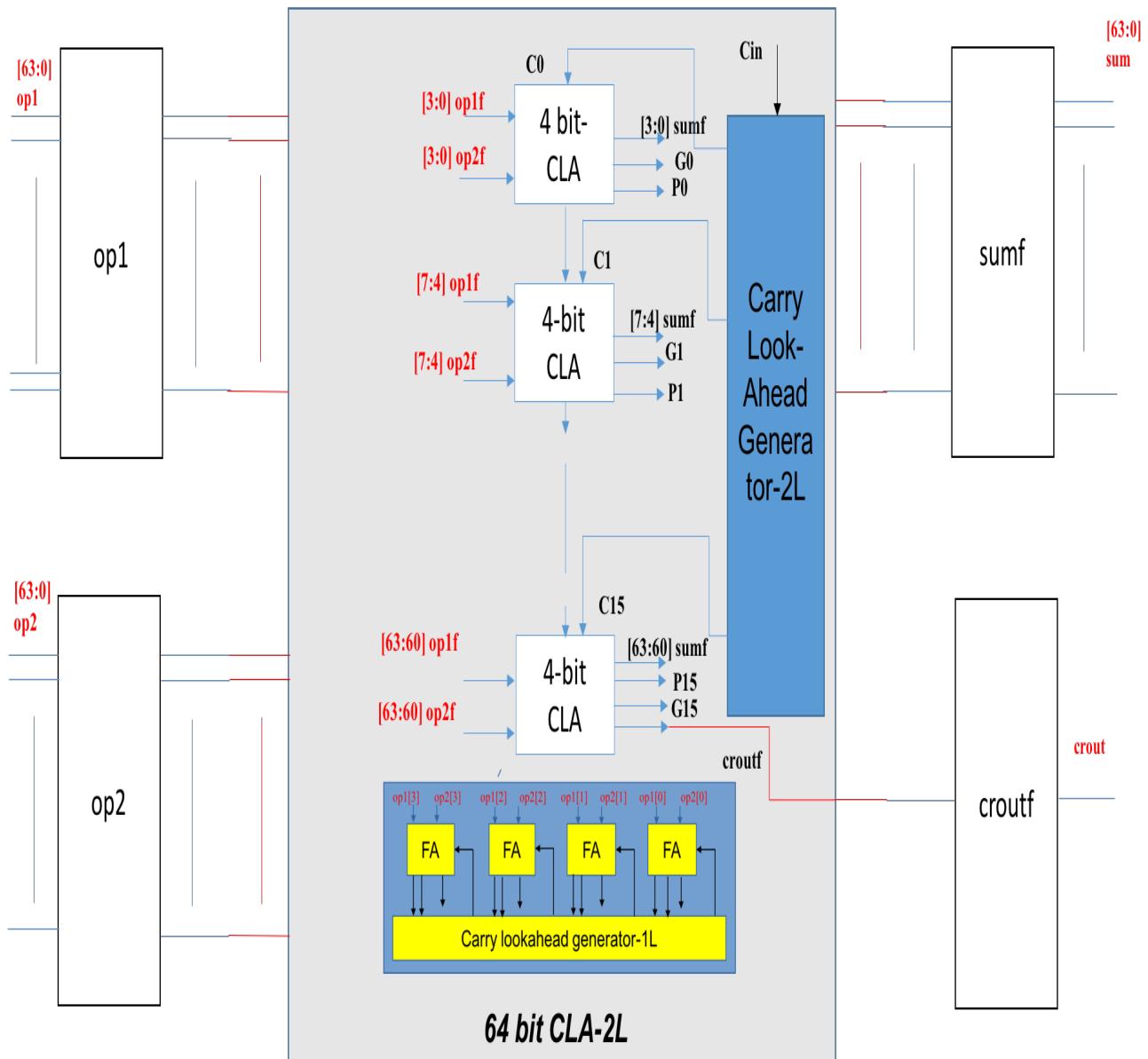


Figure II.2: Overall Block Diagram of the 64-bit CLA-2L

3. CSA-EQG: In this circuit, **equal group of two 4-bit full-adder with carry input 0 & 1** are being used in which other 3-bit receives carry input from 1st level PG generator and sum & carry output from these two adder group is selected by multiplexer based on carry input.

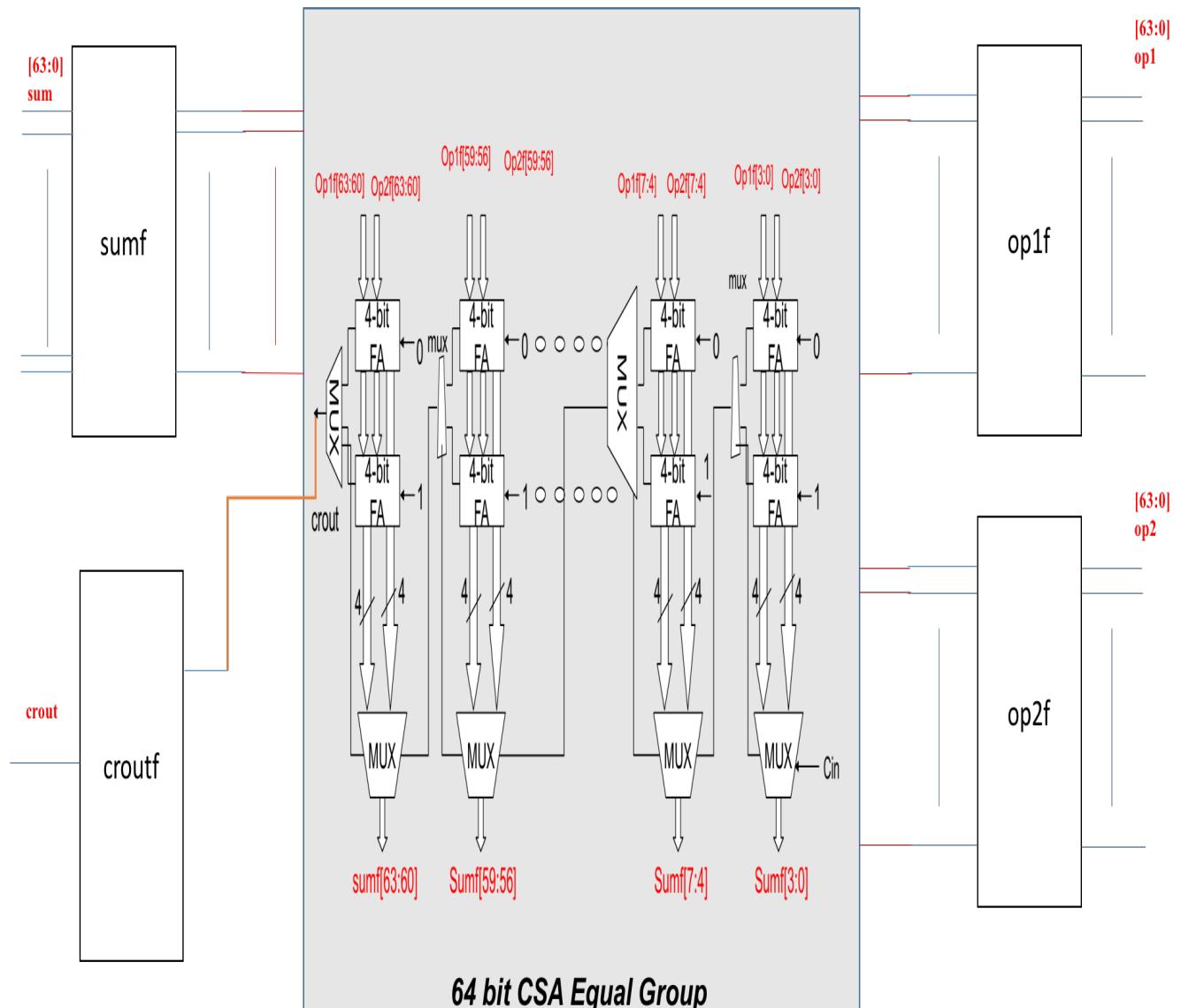


Figure II.3: Overall Block Diagram of the 64-bit CSA-EQG

4. CSA-UNEQG: In this circuit unequal group of two full adders having initial carry as **0 & 1** along with multiplexer for summation and carry out are being used. The un equal groups are as 1-bit full adder then followed by group of **4-bit, 4-bit, 5-bit, 6-bit, 7-bit, 8-bit, 9-bit, 10-bit, and 11-bit Carry Select Adder** for the best case.

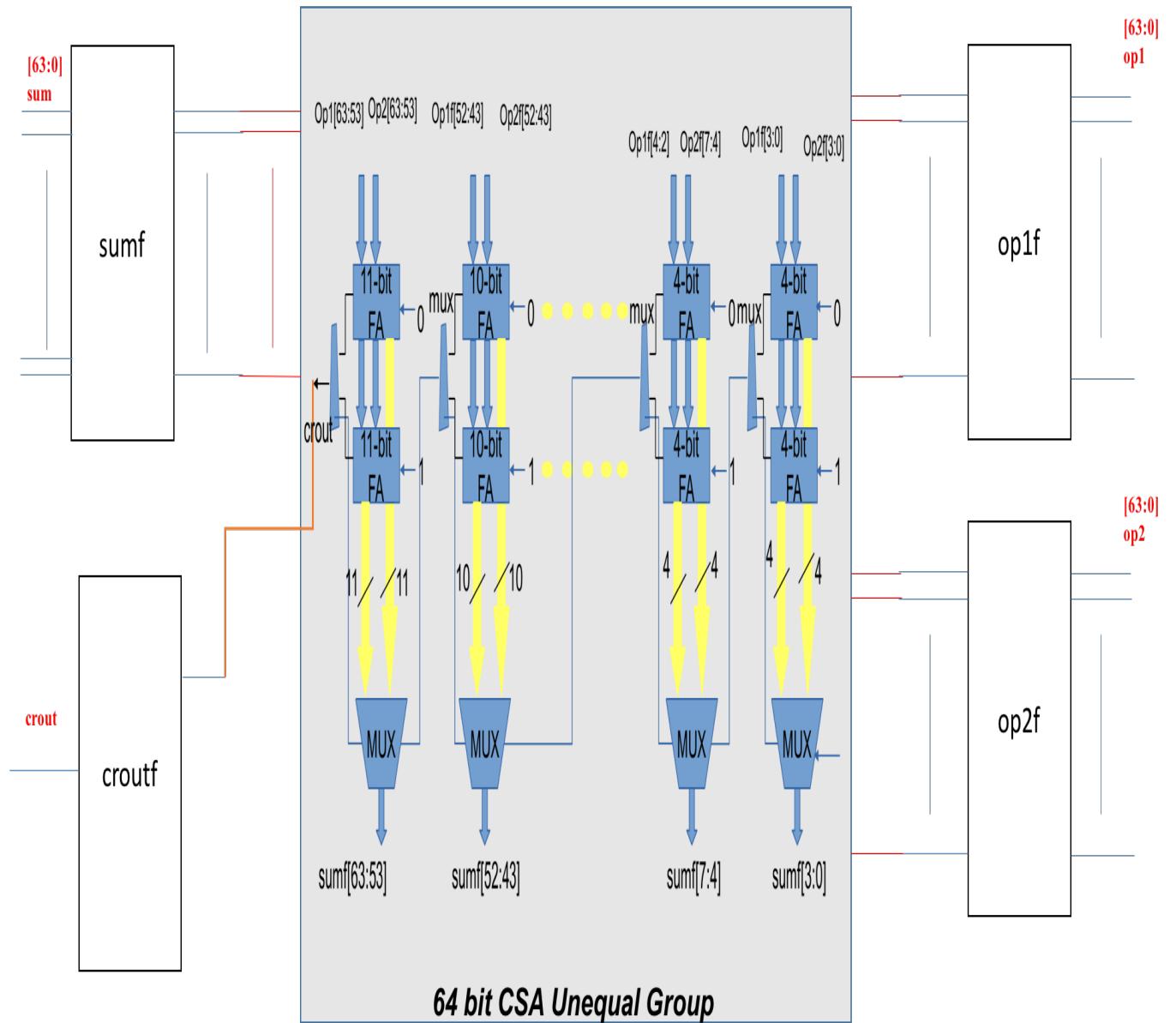


Figure II.4: Overall Block Diagram of the 64-bit CSA-UEQG

After Practical Implementation of the project there will be some difference comes in the time period of theoretical values and practical value because it depends upon maximum path taken by synthesis to find the data arrival time and slack.

Approximated delay based on theory and measured delays:

*****Ripple carry adder:*****

-Approximated delay

$$t_{add} = t_{setup} + (n-1) t_{carry} + t_{last_sum}$$

$$t_{add} = 0.34 + (64 - 1)(0.2 + 0.07) + (0.9 + 0.11 + 0.25)$$

$$t_{add} = \mathbf{18.61 \text{ ns}}$$

-Measured delay from synthesis

$$t_{add} = \mathbf{20.78 \text{ ns}}$$

*****Carry look ahead adder: *****

-Approximated delay

$$t_{add} = 8 * T_g$$

$$t_{add} = 8 * (0.28 + 0.28 + 0.26)$$

$$t_{add} = \mathbf{6.56 \text{ ns}}$$

Using another Formula-

$$t_{add} = \mathbf{6 \text{ ns}}$$

-Measured delay from synthesis

$$t_{add} = \mathbf{6.97 \text{ ns}}$$

*****Carry Select EQG adder: *****

-Approximated delay

$$t_{add} = t_{setup} + 4t_{carry} + (n/4)t_{mux} + t_{extra_for_last_sum}$$

$$t_{add} = 0.37 + 4(0.14 + 0.15 + 0.1) + 16(0.27) + 0.35$$

$$t_{add} = \mathbf{6.60 \text{ ns}}$$

-Measured delay from synthesis

$$t_{add} = \mathbf{6.7 \text{ ns}}$$

*****Carry Select UNEQG adder: *****

-Approximated delay

$$t_{add} = t_{setup} + t_{carry} + 16 * t_{mux} + t_{extra_for_last_sum}$$

$$t_{add} = 0.34 + 0.18 + 16(0.27) + 0.33$$

$$t_{add} = \mathbf{5.17 \text{ ns}}$$

-Measured delay from synthesis

$$t_{add} = \mathbf{6.10 \text{ ns}}$$

III. RTL-Level (Pre-synthesis) Simulations/Tests

In this project **six different cases and their test-benches** are being used each of them having different pairs of **input operands** to verify the design. To set initial conditions to “0” an active high reset signal is used. **To test timing and delay, appropriate clock frequency is set to observe the accurate operation of adders without any errors.** These six different values of inputs are selected in such a way that the complete functionality of these adders is achieved. These values help in verifying and observing gate level functionality, delay, glitches, behavior of circuit.

Table III.1 – Six Selected Test Data

Test Case	op1 (hex)	op2 (hex)	sum (hex)			
			RCA	CLA-2L	CSA-EQG	CSA-UEQG
1	f20f_ffff_f fff_ffff	ffff_ffff_fff f_ff50	f20f_ffff_fff f_ff4f	f20f_ffff_ffff ff4f	f20f_ffff_ffff ff4f	f20f_ffff_ffff ff4f
2	1010_101 0_1199_ff ff	abcd_1100 _1100_ddd d	Bbdd_2110_229a_dddc	Bbdd_2110_229a_dddc	Bbdd_2110_229a_dddc	Bbdd_2110_229a_dddc
3	ffff_ffff_ff ff_ffff	eeee_dddd _cccc_ffff	Eeee_dddd_c ccc_fffe	Eeee_dddd_c ccc_fffe	Eeee_dddd_c ccc_fffe	Eeee_dddd_c ccc_fffe
4	bbbb_cdc d_aaaa_11 11	ffff_ffff_fff f_dddd	Bbbb_cdcd_aaa9_eeee	Bbbb_cdcd_aaa9_eeee	Bbbb_cdcd_aaa9_eeee	Bbbb_cdcd_aaa9_eeee
5	1234_ffff_dfff_eeee	dddd_dddd _ddd_dddd d	f012_dddd_b ddd_cccb	f012_dddd_b ddd_cccb	f012_dddd_b ddd_cccb	f012_dddd_b ddd_cccb
6	1234_567 8_90ab_c def	5555_5555 _5555_ddd d	6789_abcd_e 601_abcc	6789_abcd_e 601_abcc	6789_abcd_e 601_abcc	6789_abcd_e 601_abcc

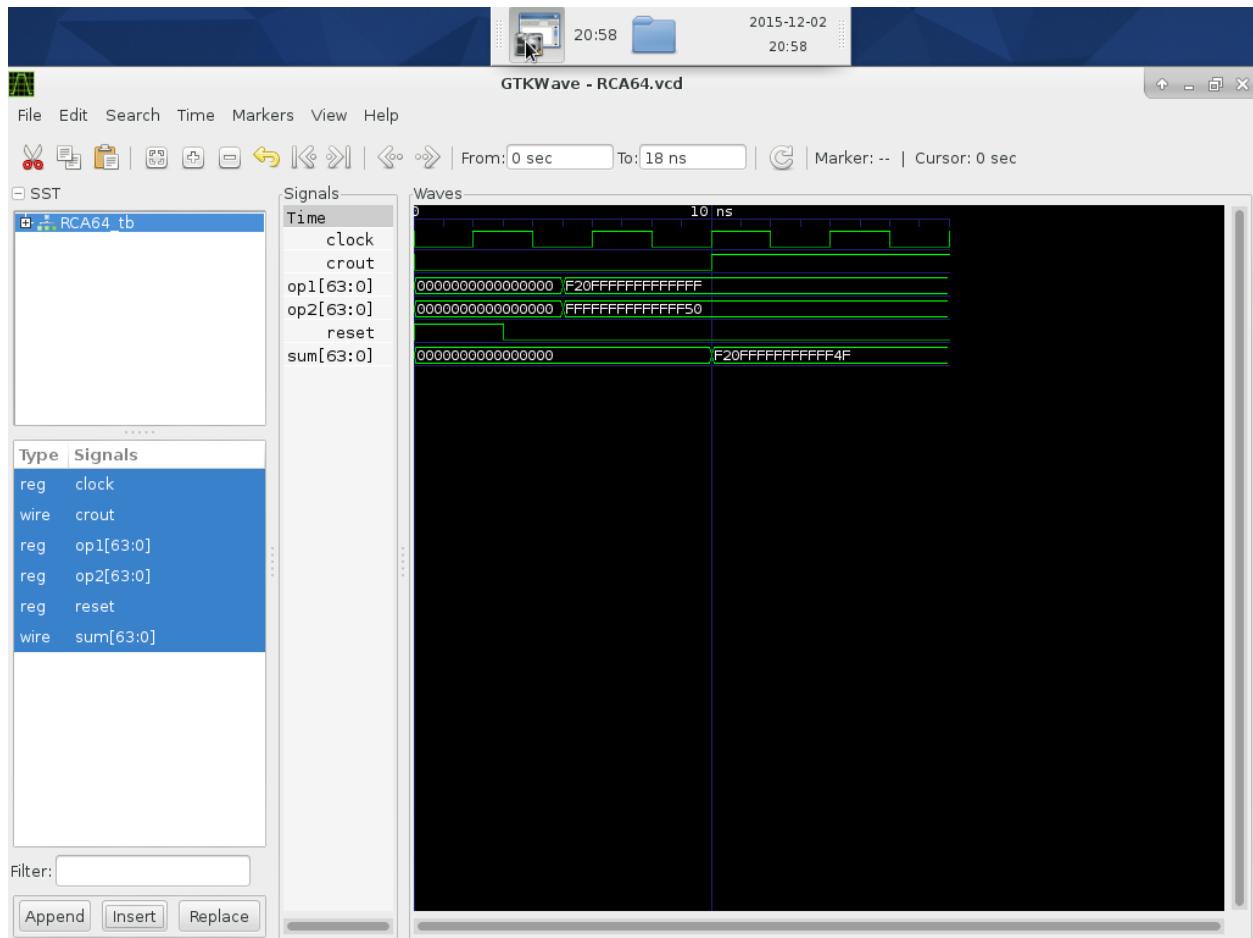


Figure III.1a: RTL simulation waveform that contains test case #1 for RCA

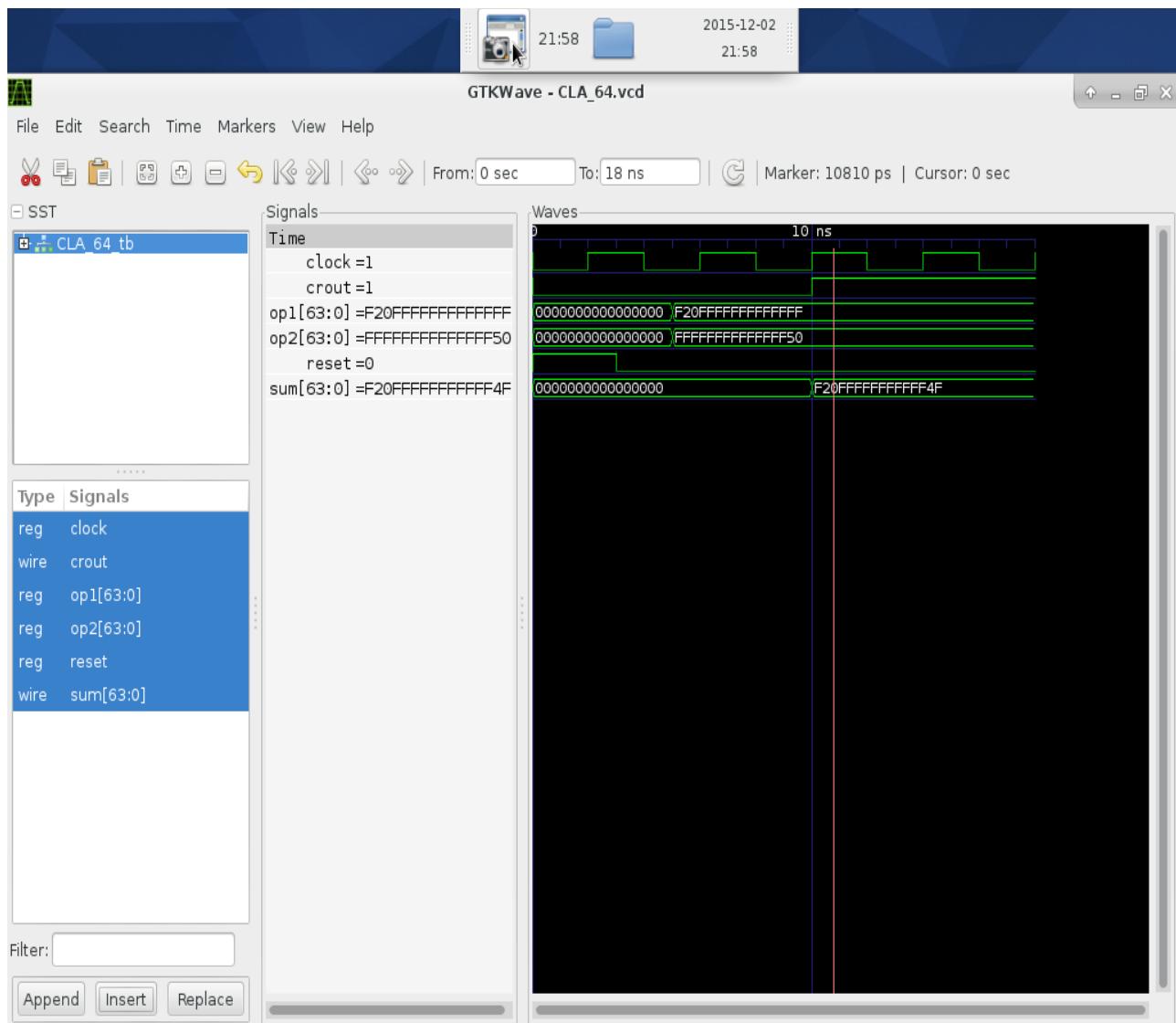


Figure III.1b: RTL simulation waveform that contains test case #1 for CLA-2L

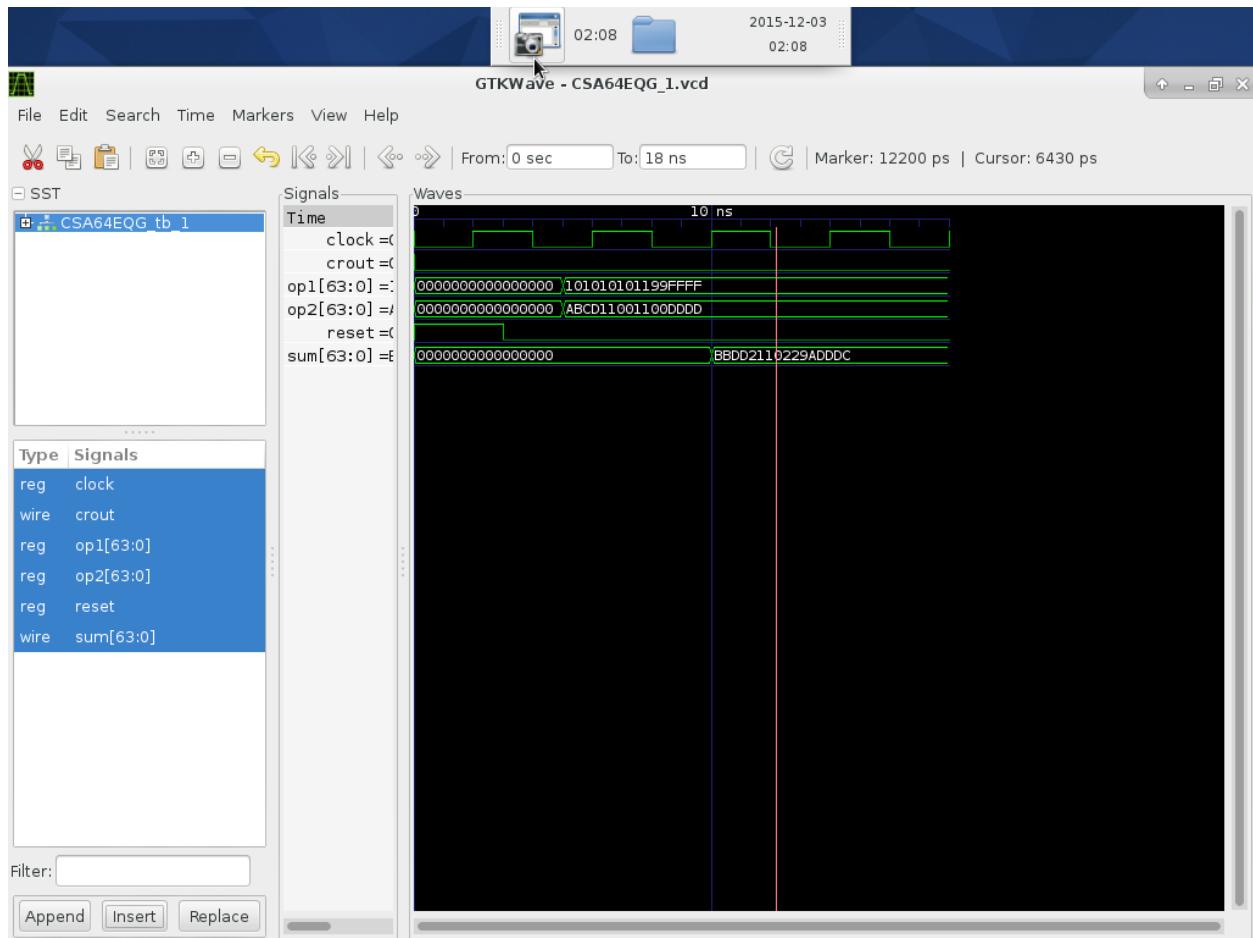


Figure III.1c: RTL simulation waveform that contains test case #1 for CSA-EQG

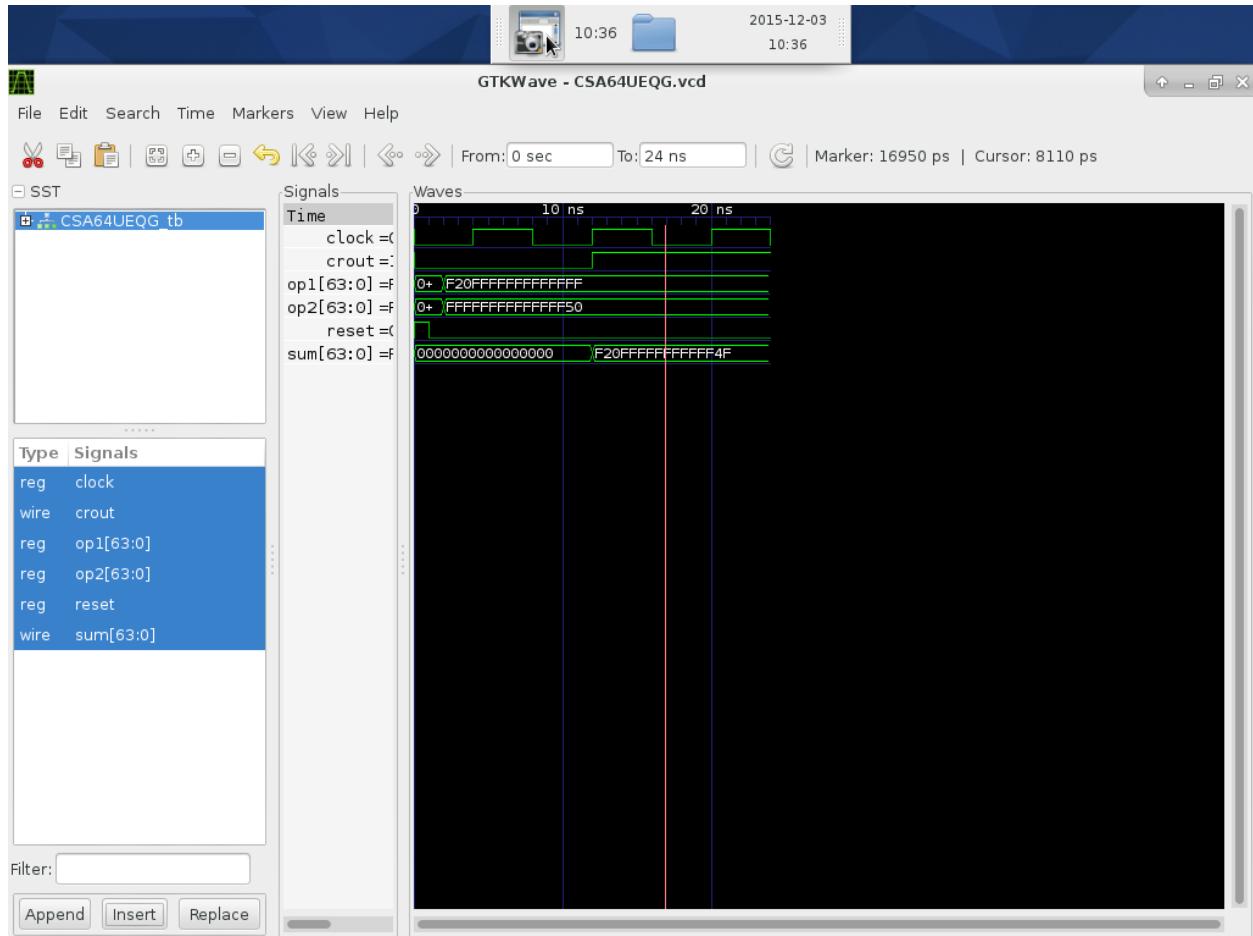


Figure III.1d: RTL simulation waveform that contains test case #1 for CSA-UEQG

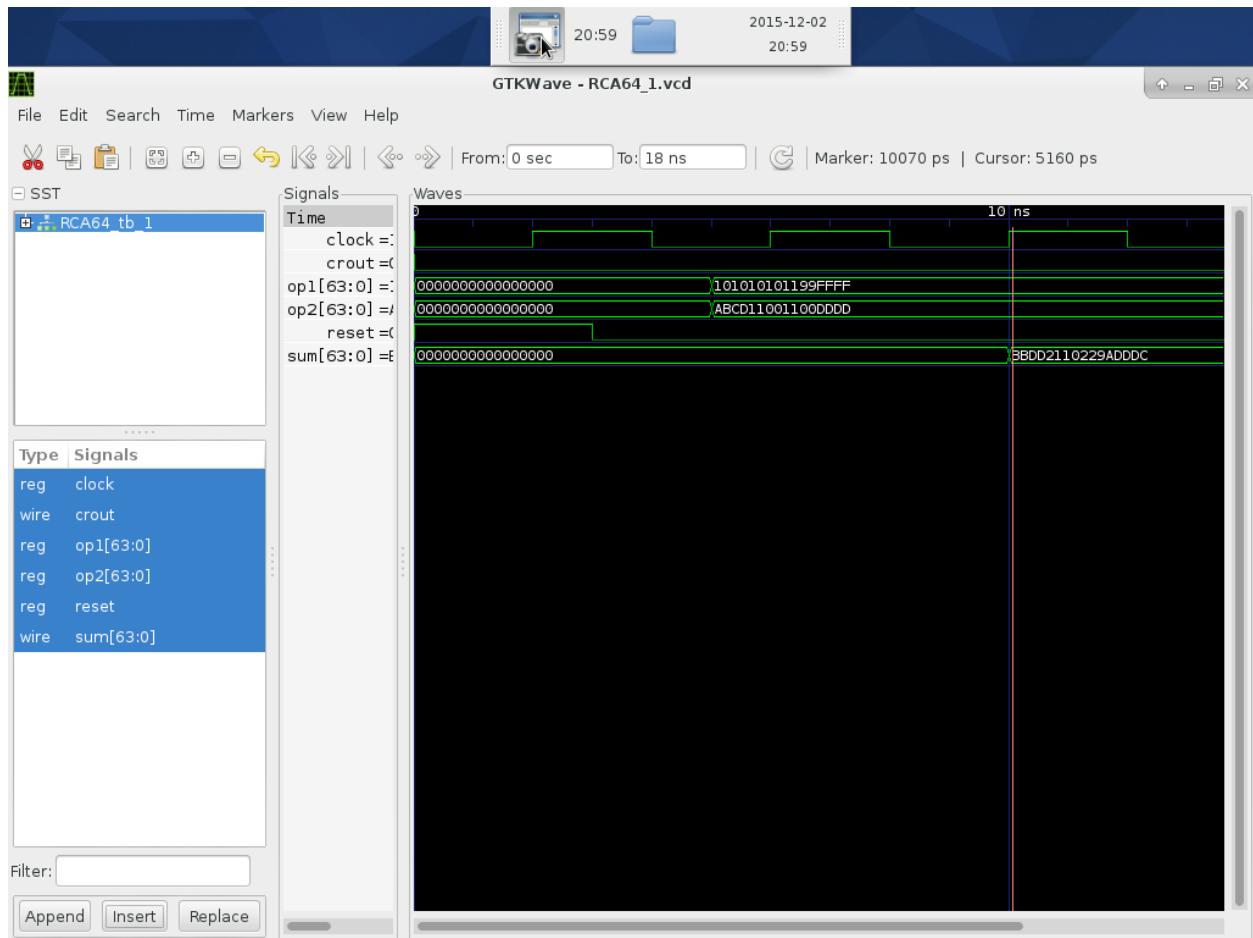


Figure III.2a: RTL simulation waveform that contains test case #2 for RCA

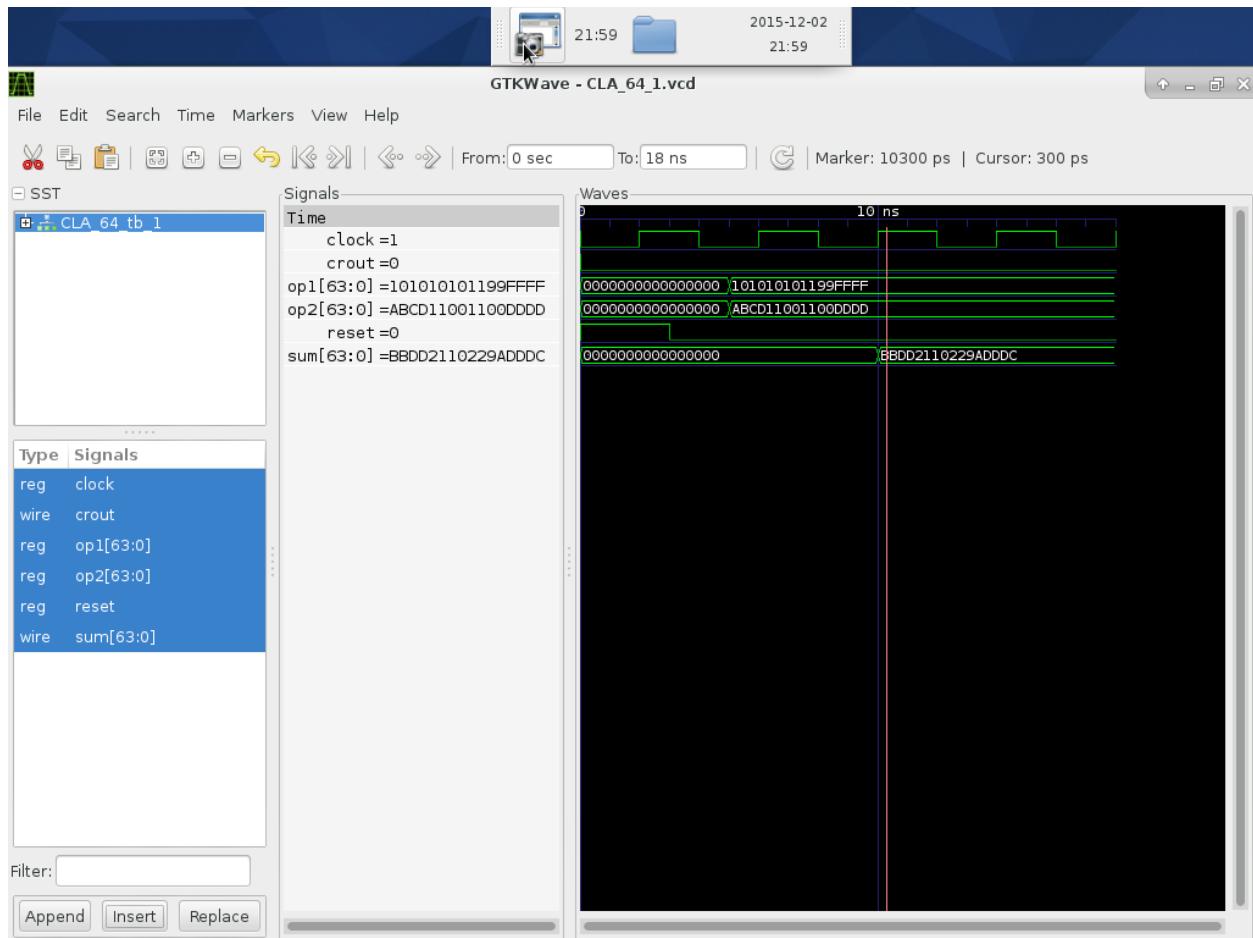


Figure III.2b: RTL simulation waveform that contains test case #2 for CLA-2L

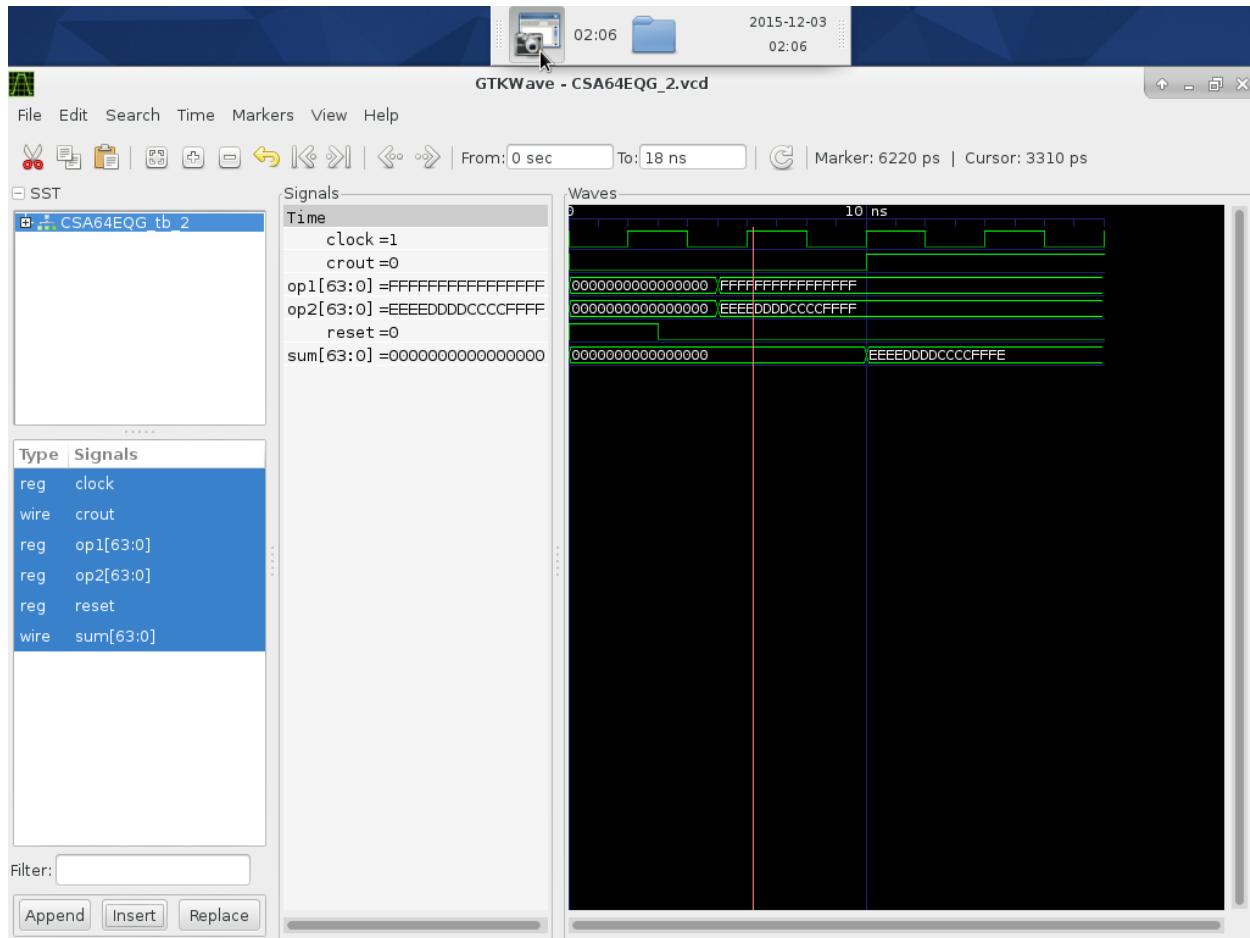


Figure III.2c: RTL simulation waveform that contains test case #2 for CSA-EQG

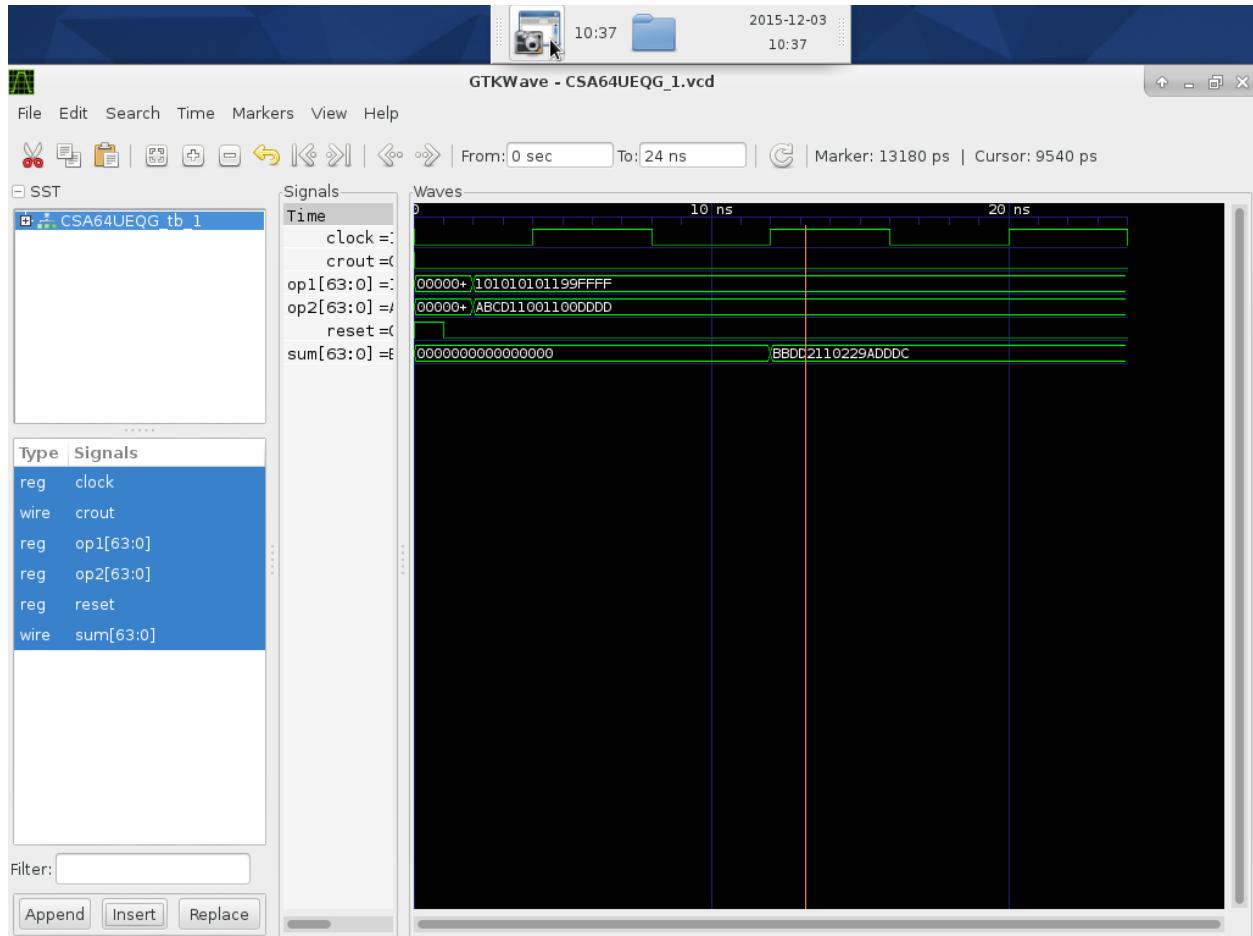


Figure III.2d: RTL simulation waveform that contains test case #2 for CSA-UEQG

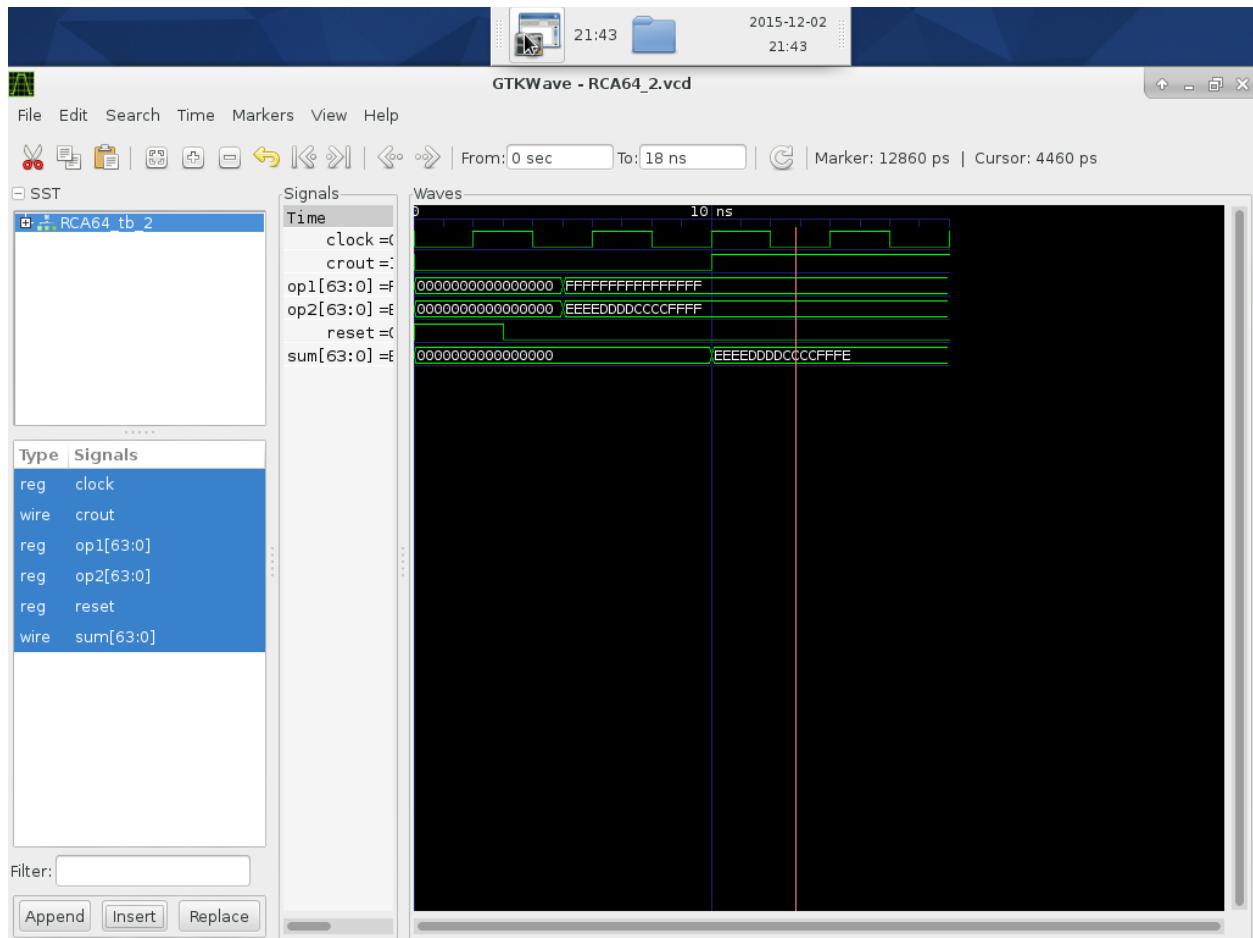


Figure III.3a: RTL simulation waveform that contains test case #3 for RCA

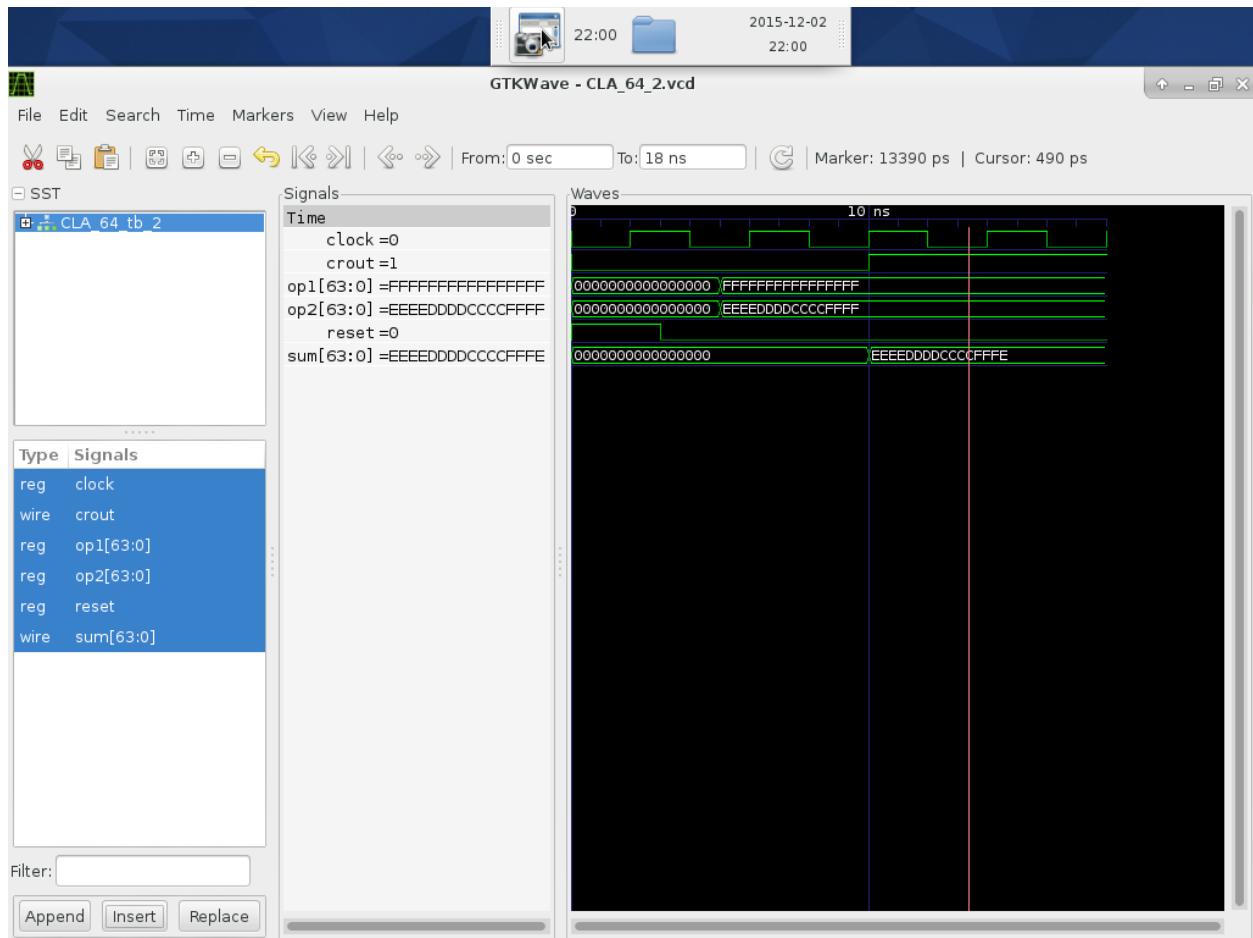


Figure III.3b: RTL simulation waveform that contains test case #3 for CLA-2L

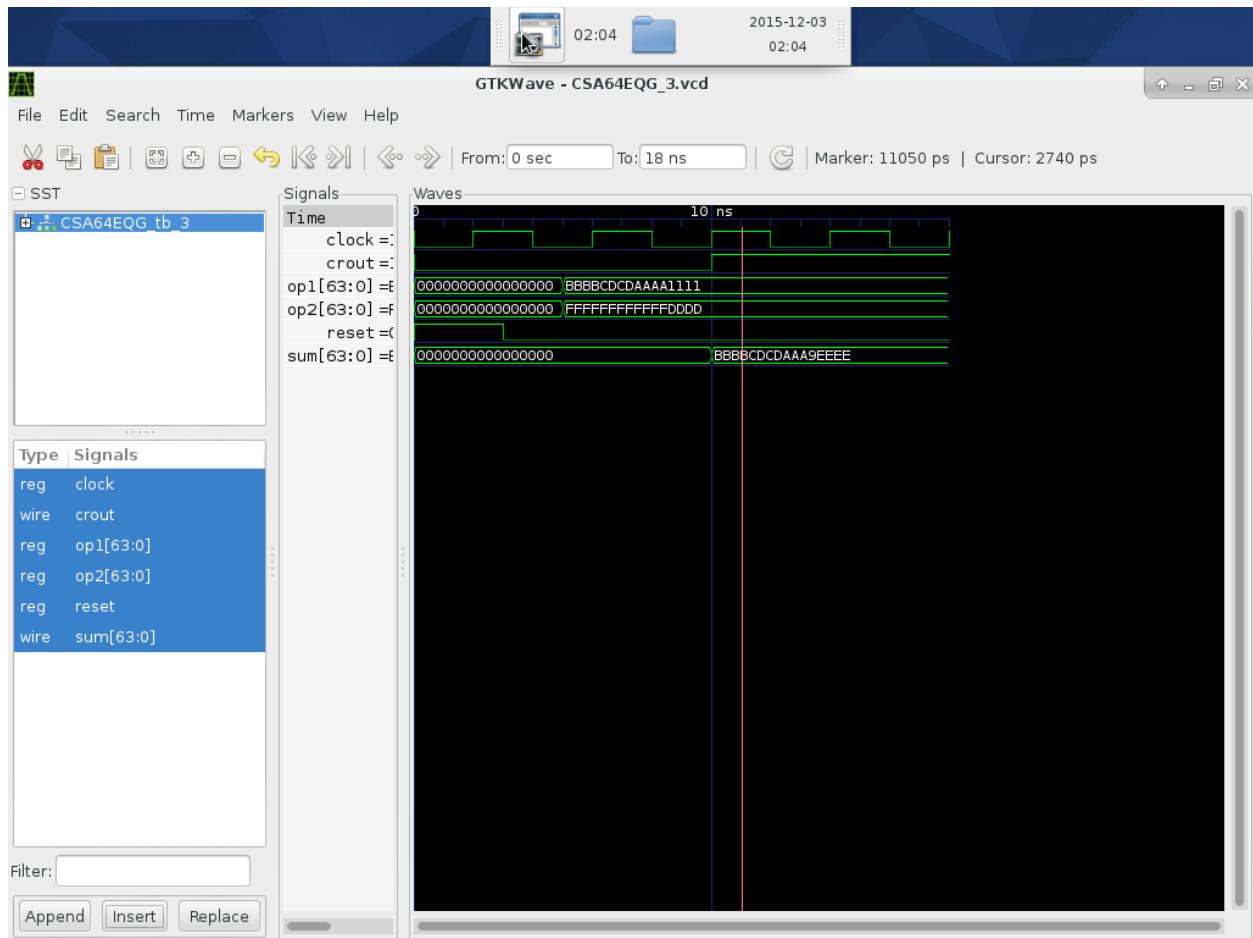


Figure III.3c: RTL simulation waveform that contains test case #3 for CSA-EQG

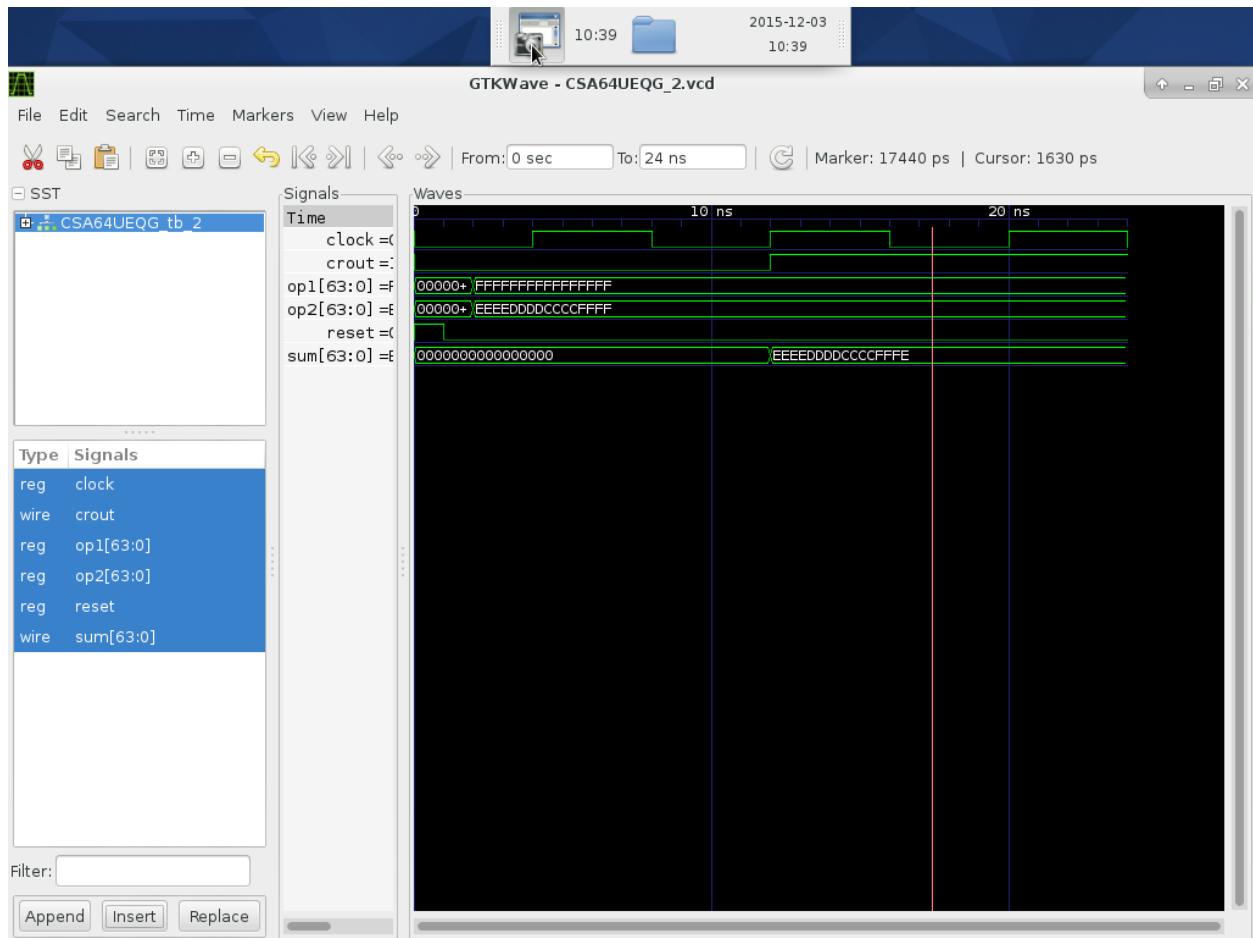


Figure III.3d: RTL simulation waveform that contains test case #3 for CSA-UEQG

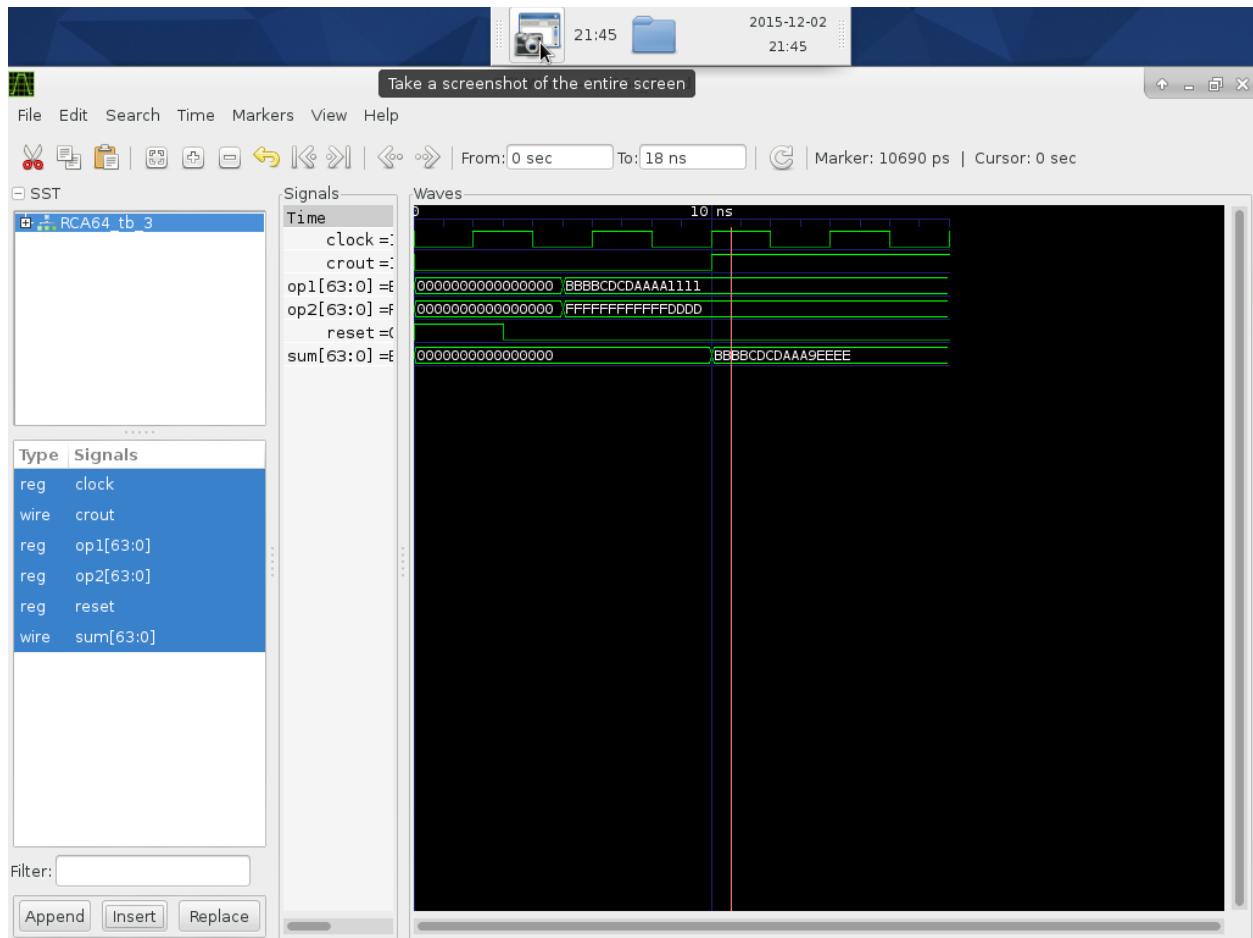


Figure III.4a: RTL simulation waveform that contains test case #4 for RCA

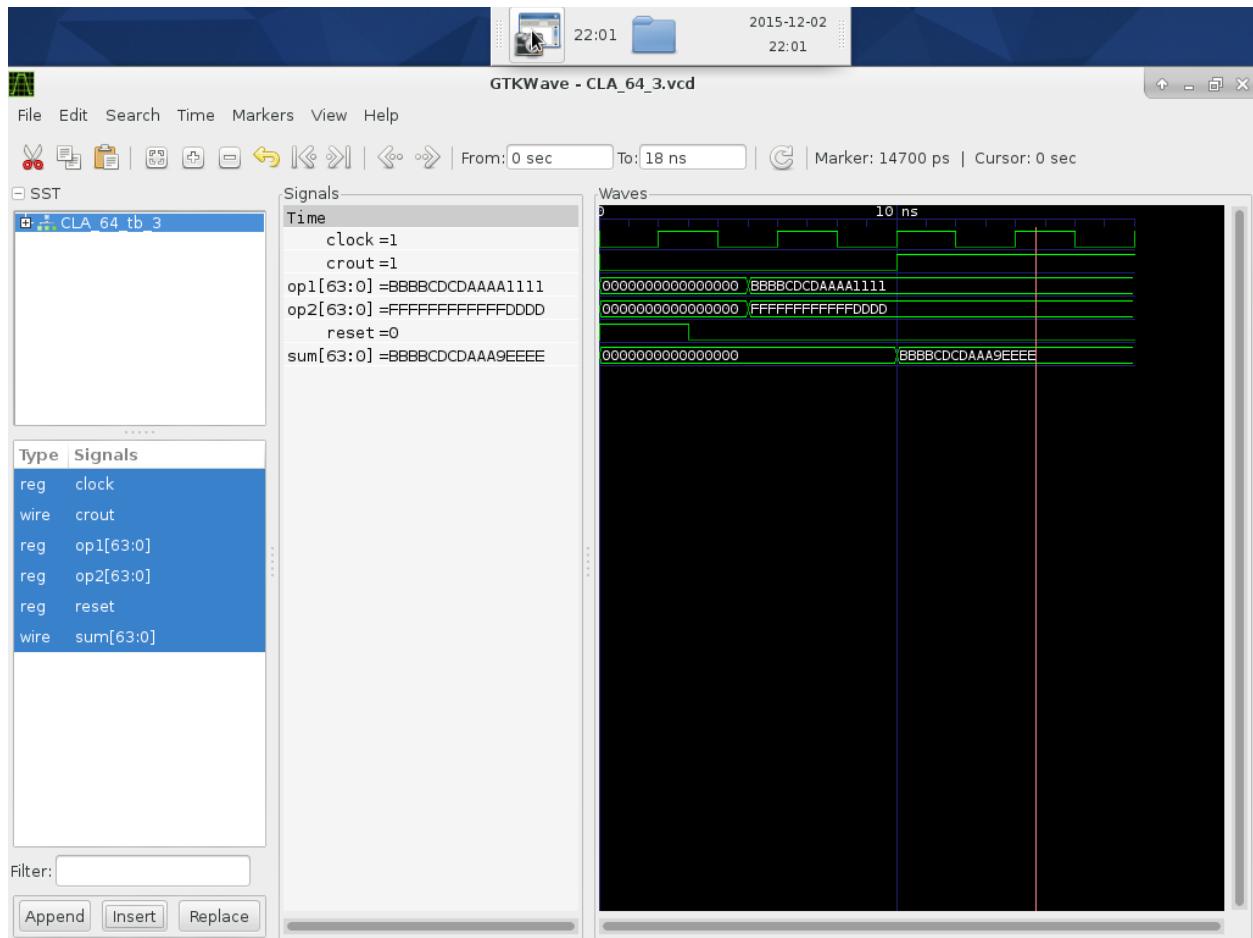


Figure III.4b: RTL simulation waveform that contains test case #4 for CLA-2L

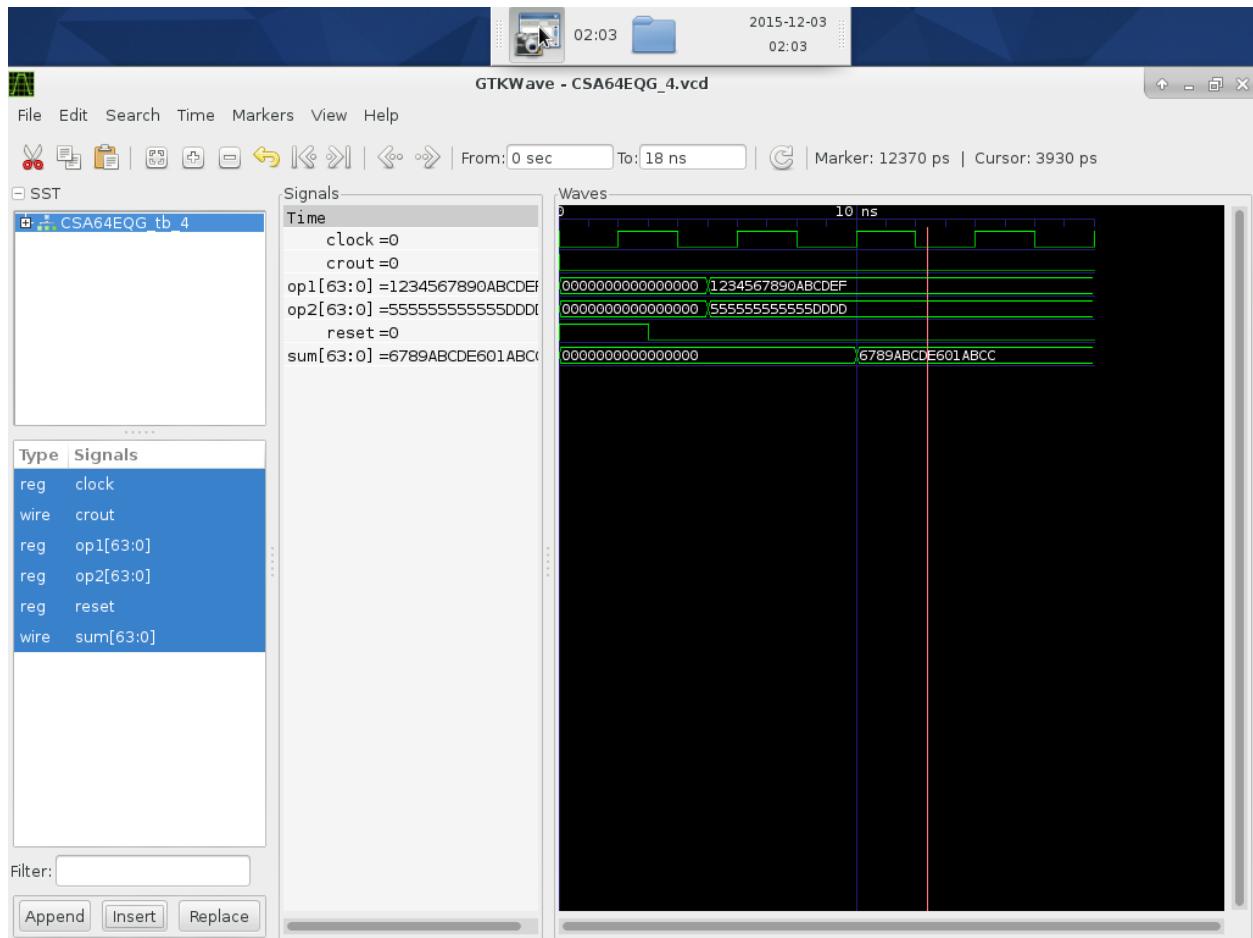


Figure III.4c: RTL simulation waveform that contains test case #4 for CSA-EQG

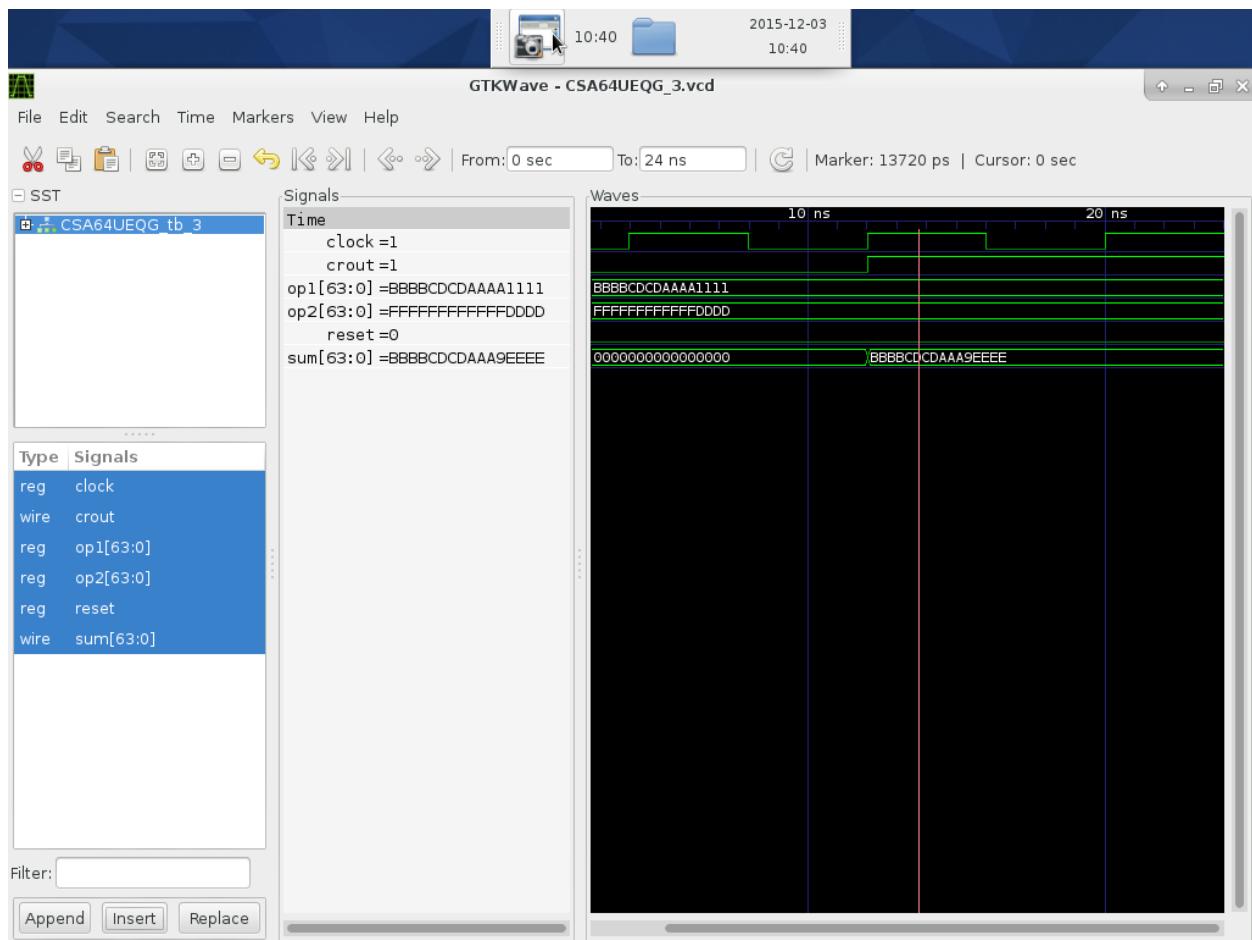


Figure III.4d: RTL simulation waveform that contains test case #4 for CSA-UEQG

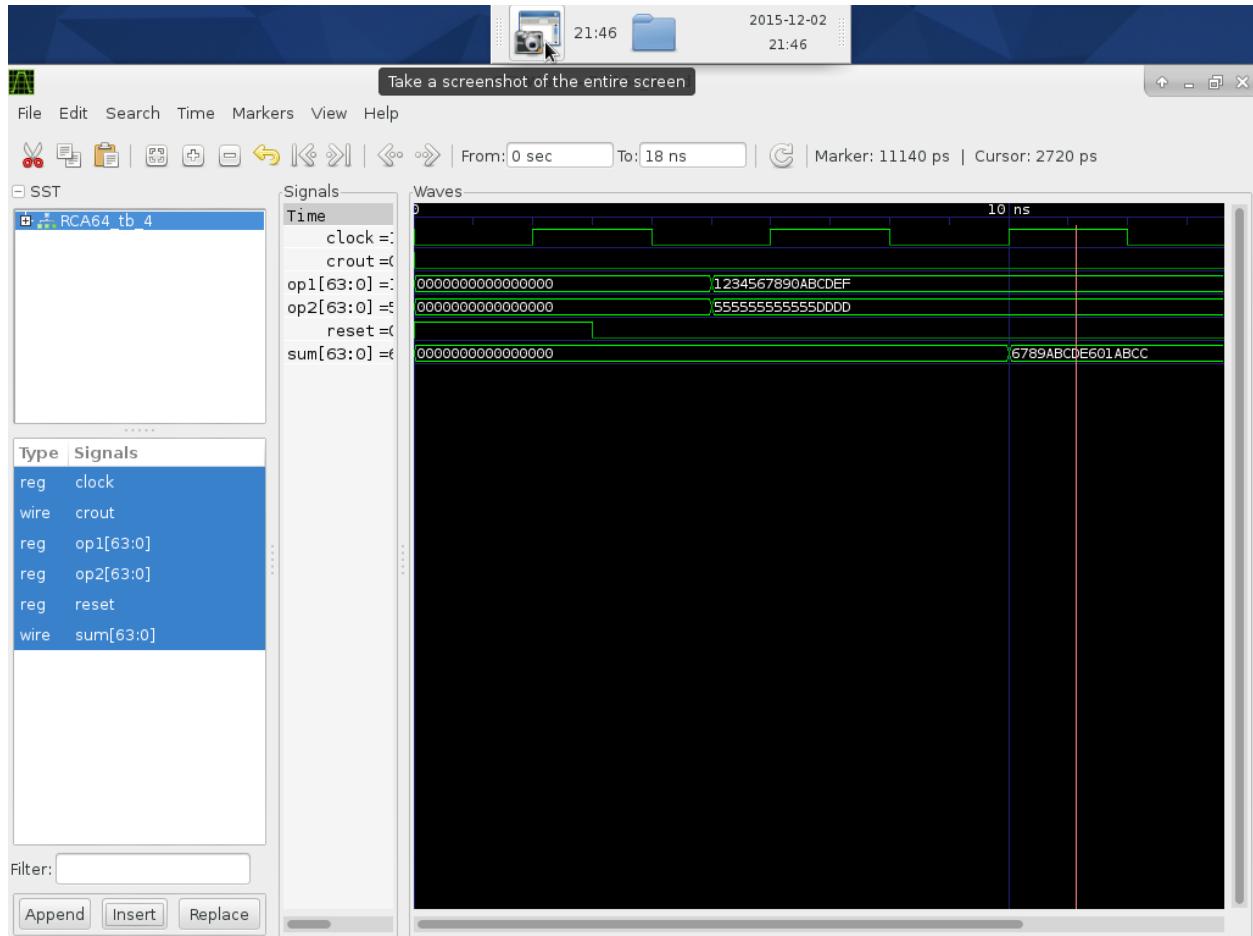


Figure III.5a: RTL simulation waveform that contains test case #5 for RCA

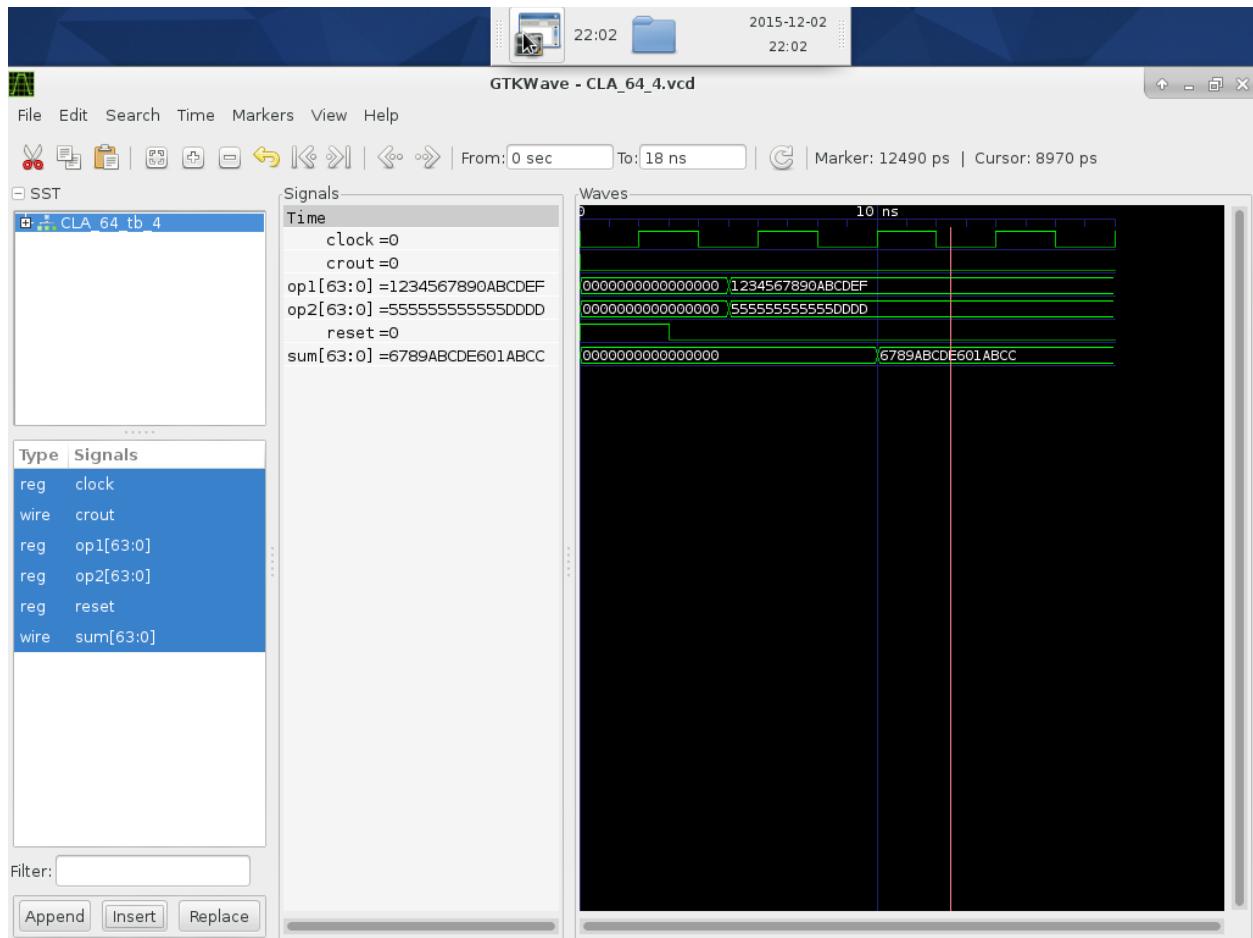


Figure III.5b: RTL simulation waveform that contains test case #5 for CLA-2L

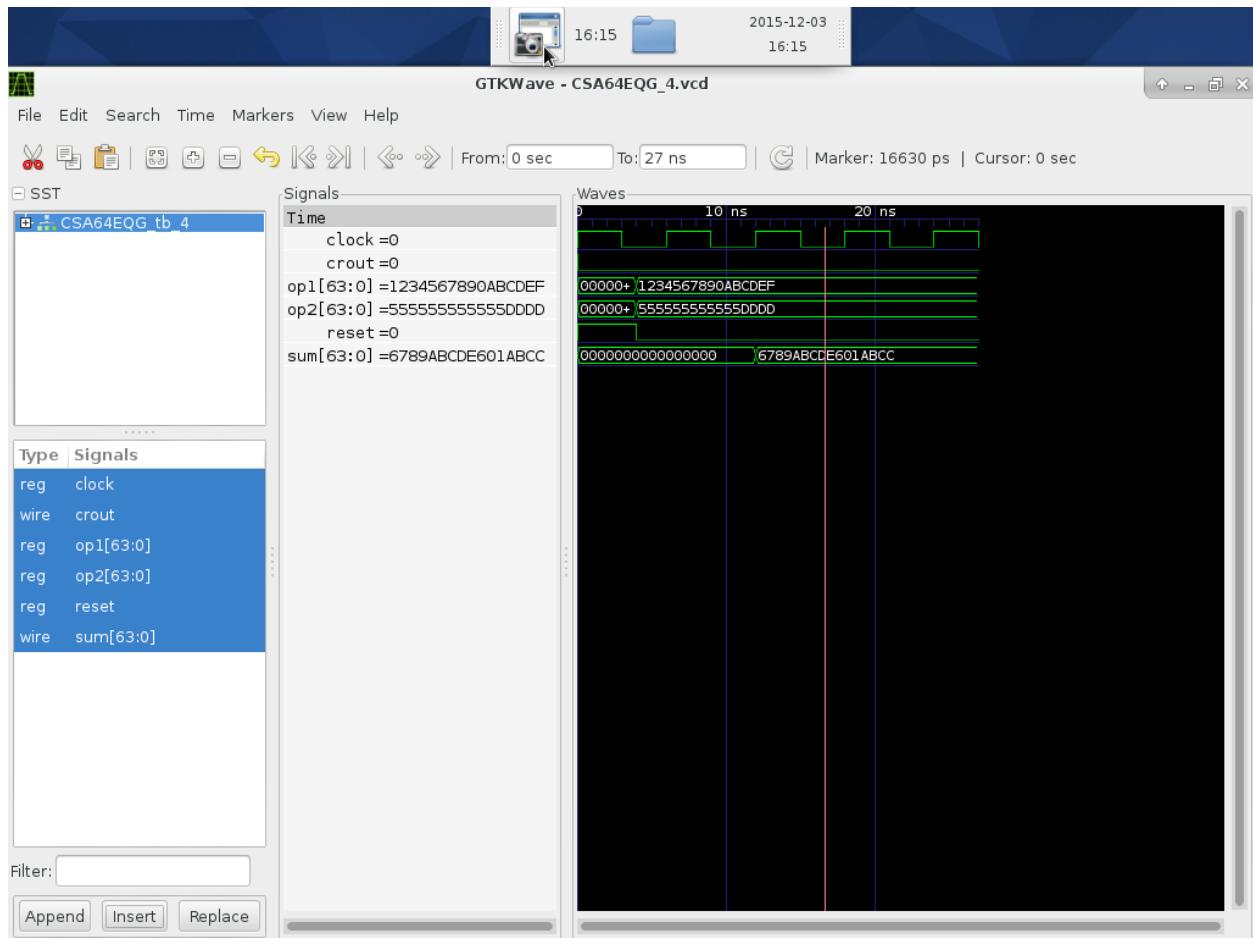


Figure III.5c: RTL simulation waveform that contains test case #5 for CSA-EQG

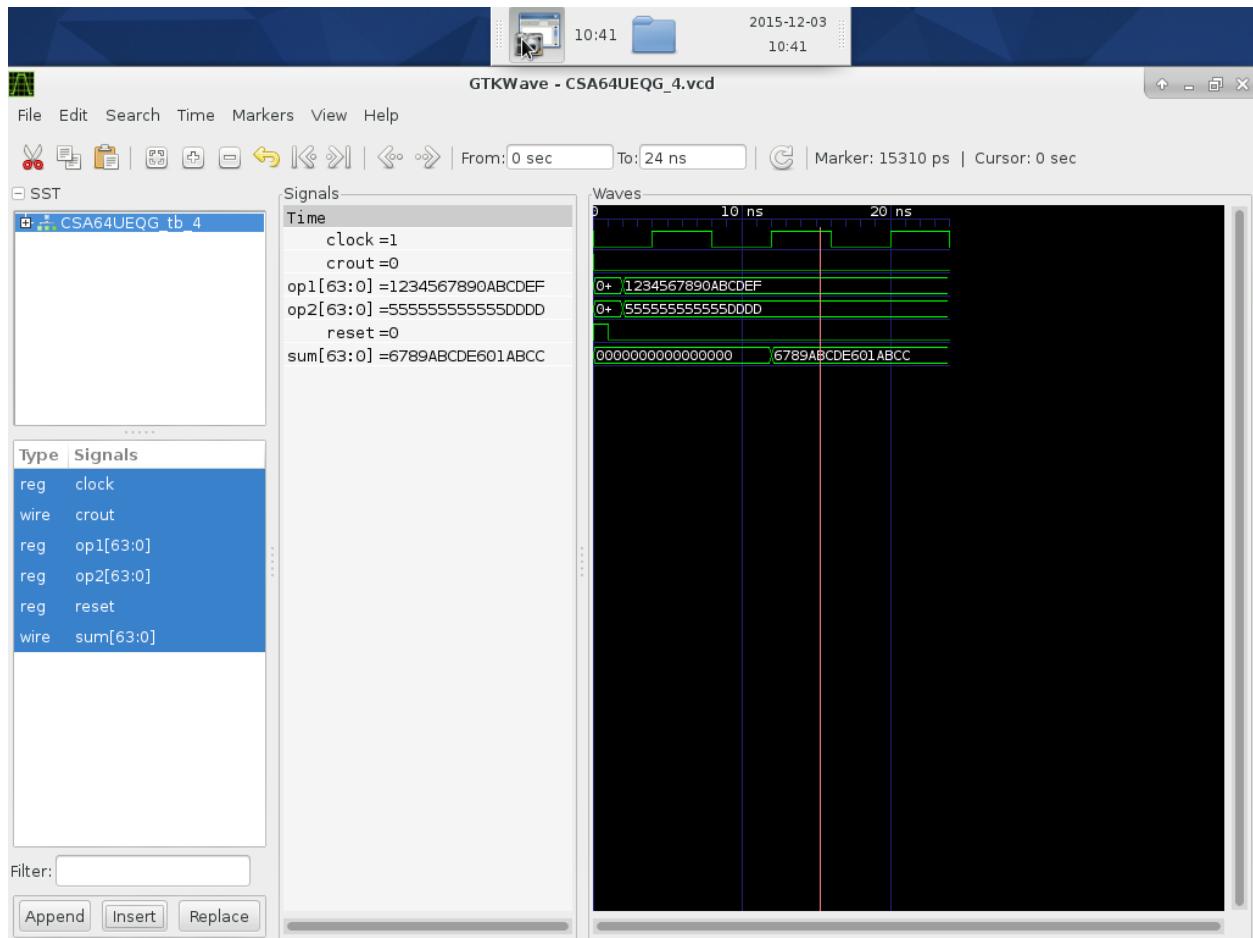


Figure III.5d: RTL simulation waveform that contains test case #5 for CSA-UEQG

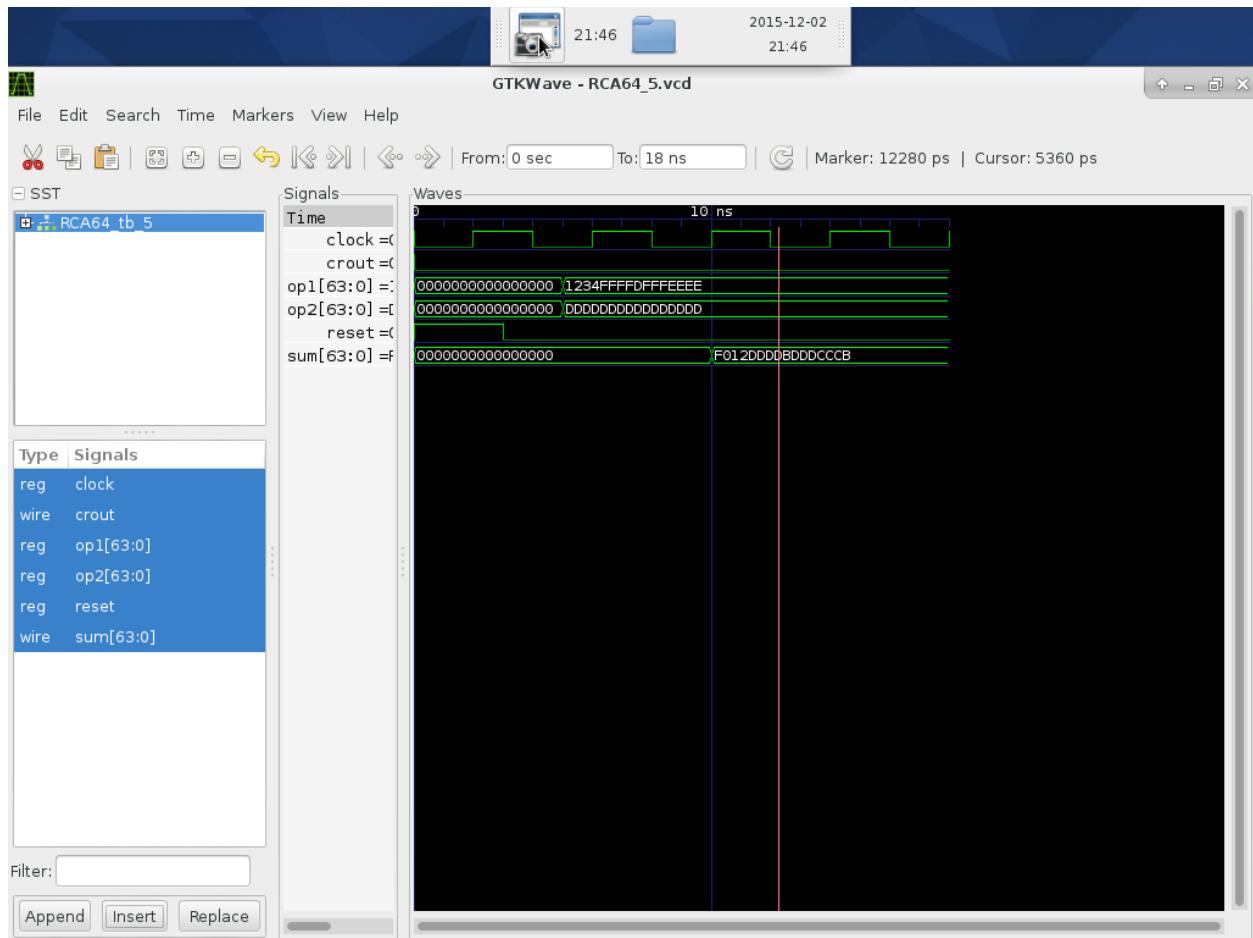


Figure III.6a: RTL simulation waveform that contains test case #6 for RCA

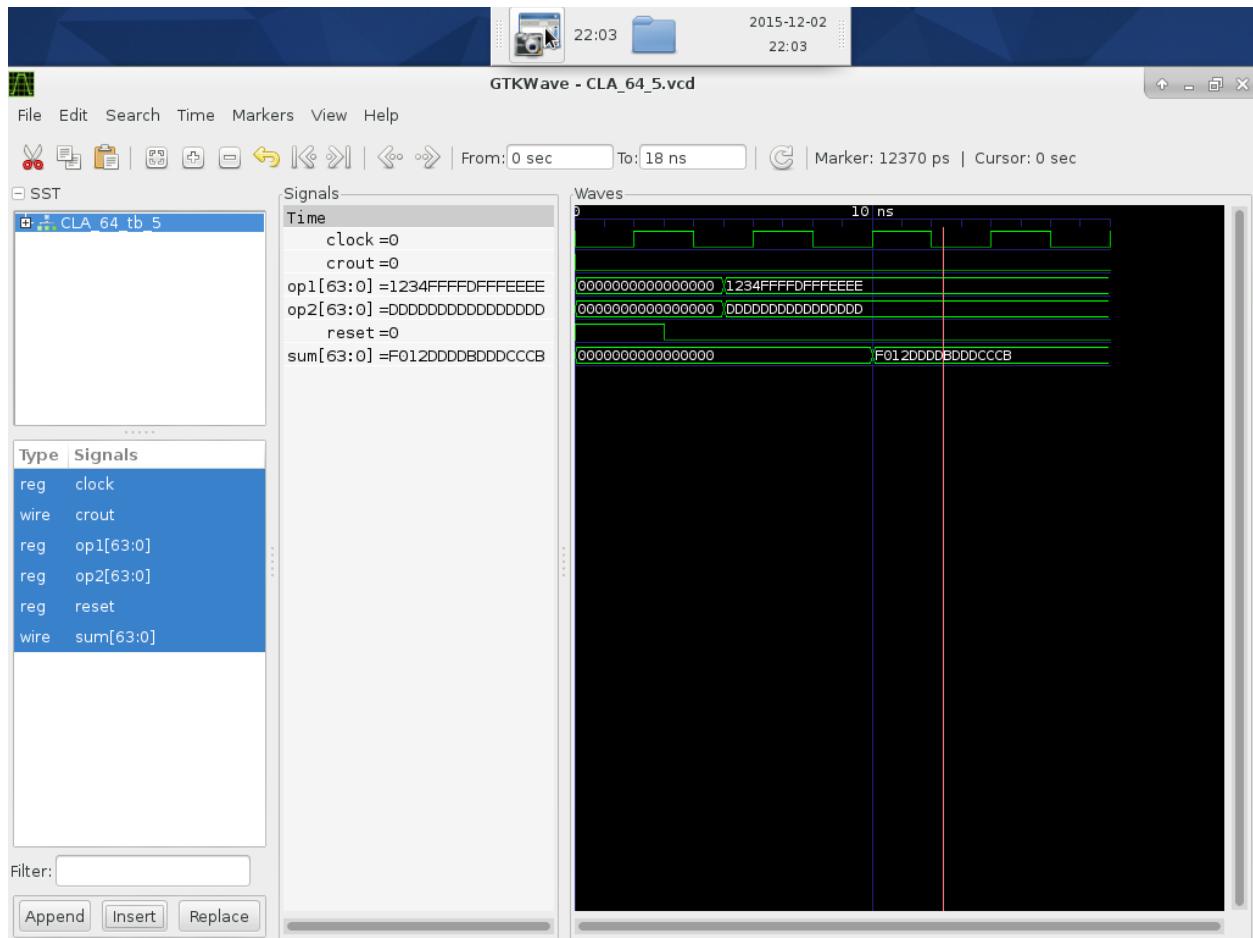


Figure III.6b: RTL simulation waveform that contains test case #6 for CLA-2L

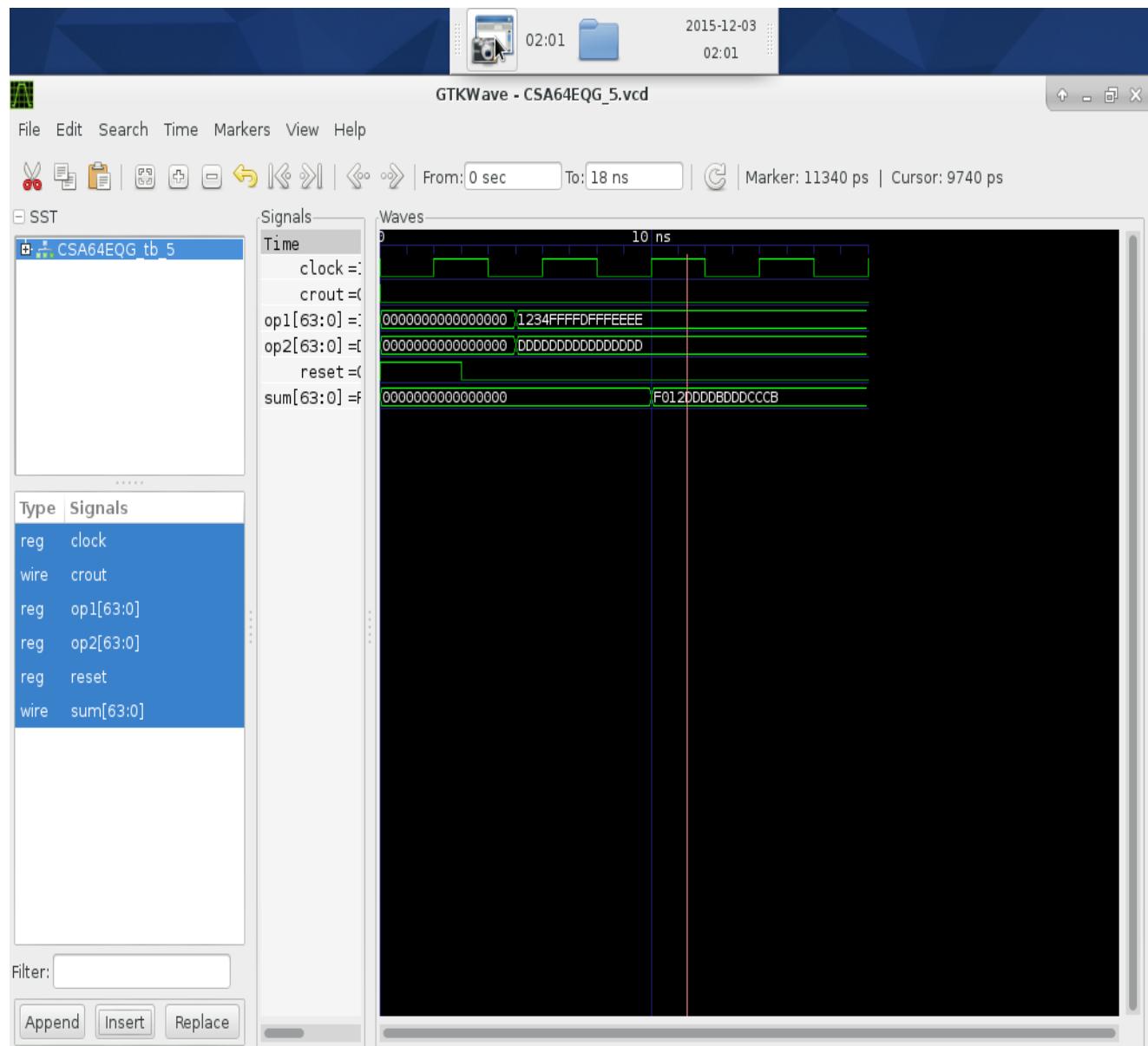


Figure III.6c: RTL simulation waveform that contains test case #6 for CSA-EQG

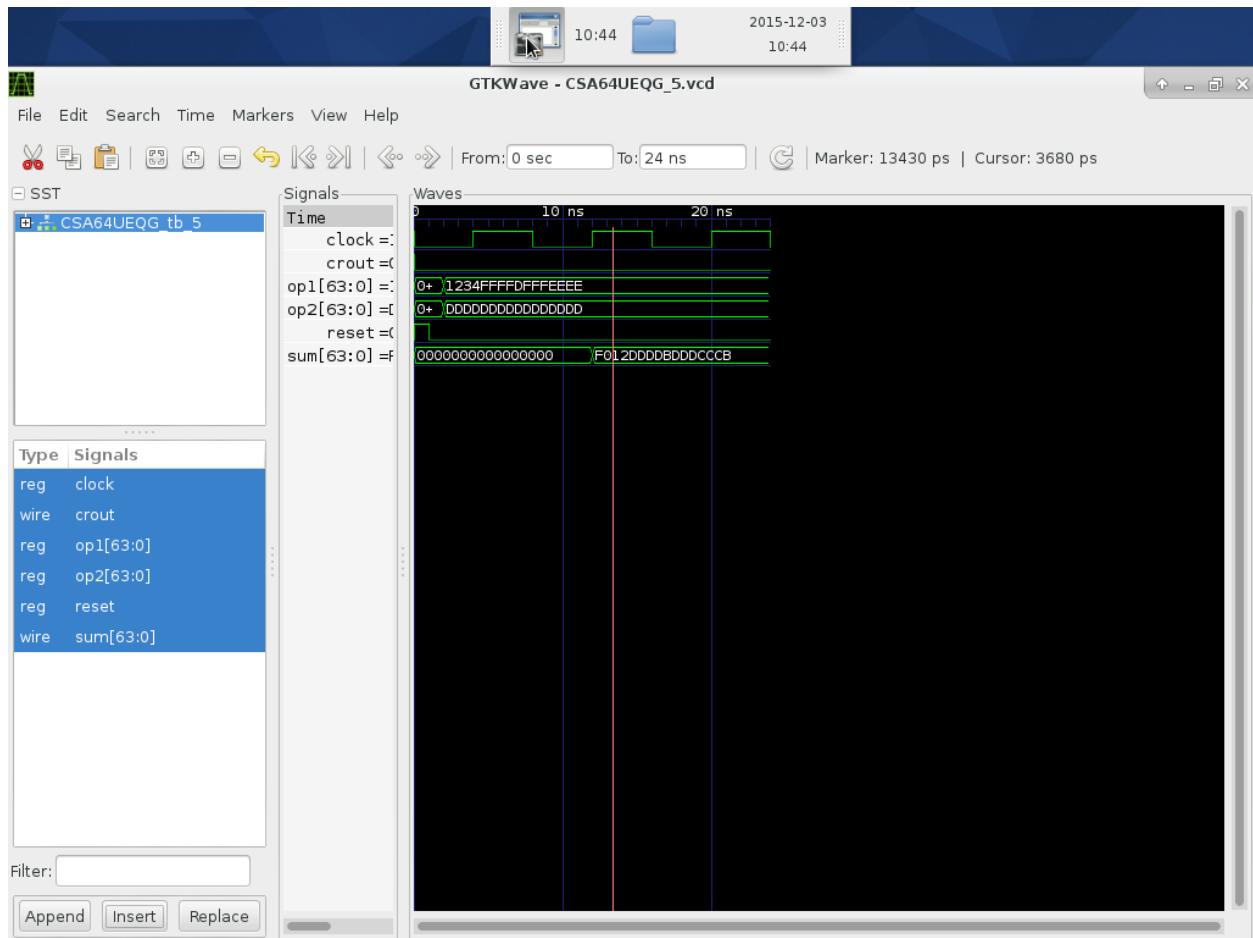


Figure III.6d: RTL simulation waveform that contains test case #6 for CSA-UEQG

IV. Synthesis and Optimizations

Table IV.1: Synthesis Constraints and Results for RCA

Trial #	Design Constraint Settings Clock(ns), Area	Results after Synthesis Slack, Area, Power(mw)
1	Clock=17 ns, Area= 1500	Slack= -3.77, Area=3765.00, Power=4.71 mW
2	Clock=19 ns, Area = 2700	Slack= -1.79, Area=3693.00, Power=4.73 mW
3	Clock=23 ns, Area= 3500	Slack= 2.21, Area=2900.00, Power=4.58 mW
4	Clock= 20 ns, Area= 3000	Slack= -0.78, Area=3200.00, Power=4.70 mW
5	Clock= 20.80 ns, Area= 3000	Slack= 0.01, Area=3039.20, Power=4.67 mW
6	Clock =21 ns, Area= 3100	Slack= 0.21, Area=2995.500, Power=4.60 mW

Table IV.2: Synthesis Constraints and Results for CLA-2L

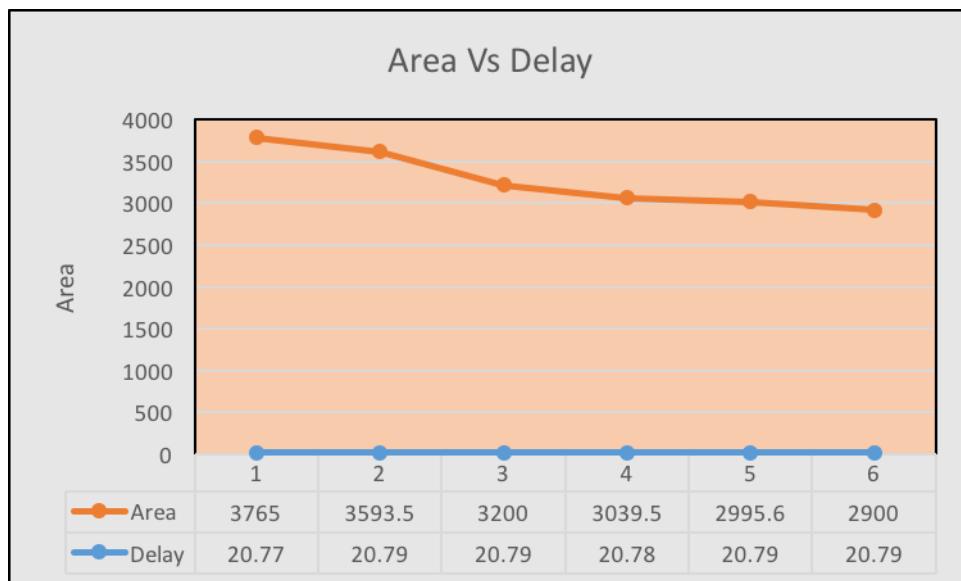
Trial #	Design Constraint Settings Clock(ns), Area	Results after Synthesis Slack, Area, Power(mw)
1	Clock=5 ns, Area=2700	Slack= -2, Area=2855.50, Power=17.16mW
2	Clock=6 ns, Area = 2800	Slack= -1, Area=2820.00, Power=16.89 mW
3	Clock=6.5 ns, Area=3000	Slack= -0.5, Area=2811.50, Power=16.50 mW
4	Clock=7.3 ns, Area=3100	Slack= 0.01, Area=2776.00, Power=15.11 mW
5	Clock=7.5 ns, Area=2900	Slack= 0.51, Area=2730.50, Power=14.260 mW
6	Clock=8 ns, Area=2600	Slack= 1.01, Area=2696.5.00, Power=13.31 mW

Table IV.3: Synthesis Constraints and Results for CSA-EQG

Trial #	Design Constraint Settings Clock(ns), Area	Results after Synthesis Slack, Area, Power(mw)
1	Clock=6 ns, Area=3100	Slack= -0.93, Area=3653.00, Power=13.79 mW
2	Clock=6.5 ns, Area=3400	Slack= -.43, Area=3576.00, Power=16.35 mW
3	Clock=7 ns, Area=3450	Slack= -0.05, Area=3479.50, Power=14.79 mW
4	Clock=7.5 ns, Area= 3500	Slack= 0.47, Area=3409.00, Power=15.28 mW
5	Clock=8 ns, Area=3300	Slack= 0.93, Area=3351.50, Power=13.56 mW
6	Clock=7.1 ns, Area=3400	Slack= 0.03, Area=3424.00, Power=16.23 mW

Table IV.4: Synthesis Constraints and Results for CSA-UEQG

Trial #	Design Constraint Settings Clock(ns), Area	Results after Synthesis Slack, Area, Power(mw)
1	Clock=6 ns	Slack= -1.75, Area=3782.00, Power=14.46 mW
2	Clock=6.5 ns	Slack= -1.24, Area=3759.00, Power=13.95 mW
3	Clock=7 ns	Slack= -0.73, Area=3714.500, Power=11.50 mW
4	Clock=7.2 ns	Slack= -0.56, Area=3685.00, Power=13.379 mW
5	Clock=7.7 ns	Slack= -0.05, Area=3567.500, Power=13.99 mW
6	Clock=7.8 ns	Slack= 0.05, Area=3538.00, Power=14.09 mW

**Figure IV.1: Area versus Delay of RCA**

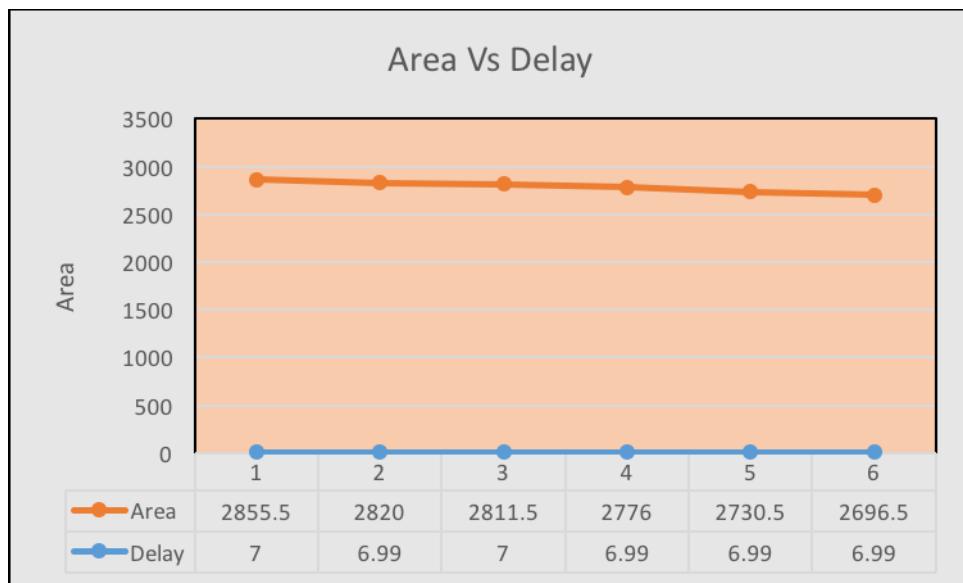


Figure IV.2: Area versus Delay of CLA-2L

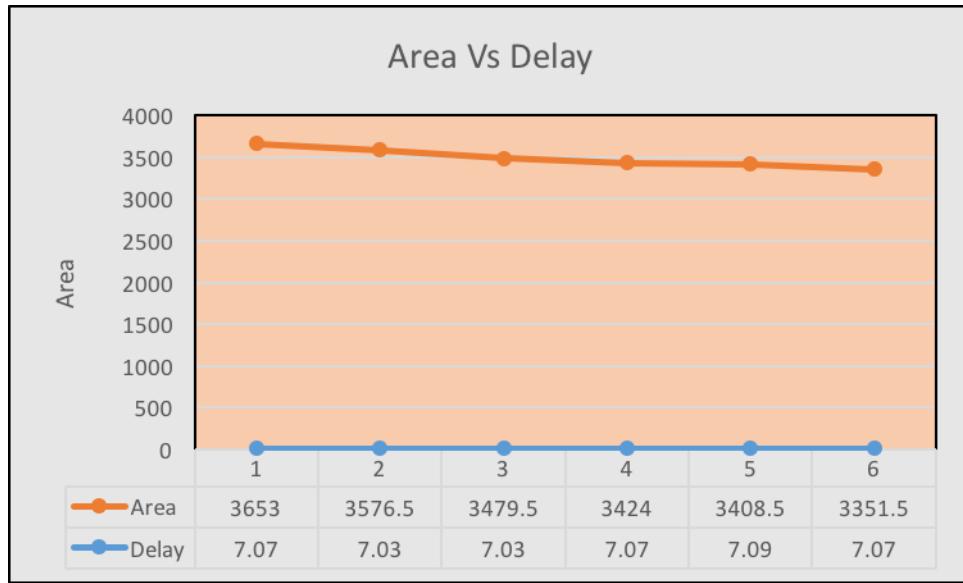


Figure IV.3: Area versus Delay of CSA-EQG

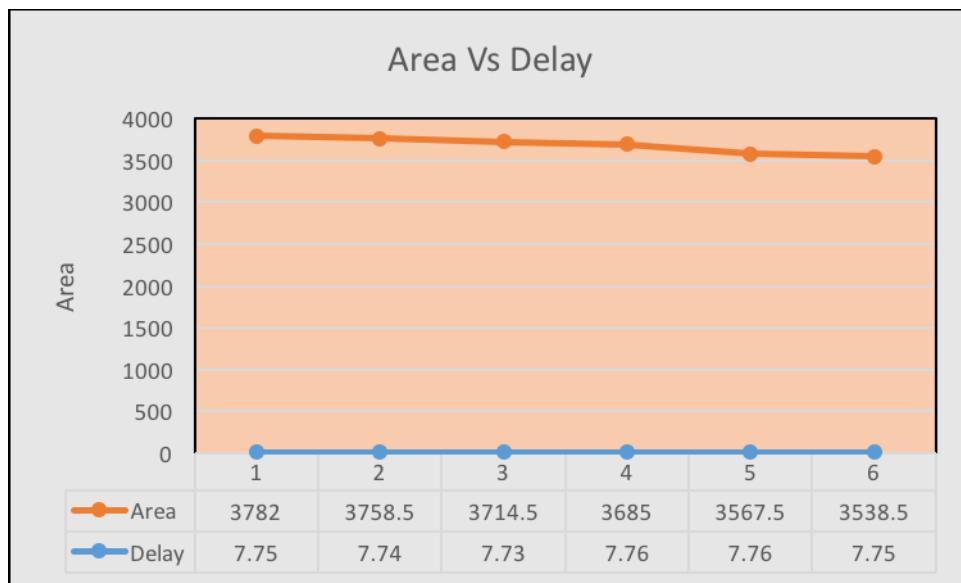


Figure IV.4: Area versus Delay of CSA-UEQG

From the graphs of Area Vs Delay, The area of the adder changes with change in time period. If clock period increases, then area will decrease. The area is inversely proportional to the clock period.

V. Gate-Level (Post-synthesis) Dynamic Simulations/Tests

Table V.1 – Performance of Six Selected Test Cases

Test Case	op1 (hex)	op2 (hex)	Timings (Delays) ns			
			RCA	CLA-2L	CSA-EQG	CSA-UEQG
1	f20f_ffff_f fff ffff	ffff_ffff_fff f ff50	2.89	1.54	2.2	1.95
2	1010_101 0_1199_ff ff	abcd_1100 _1100_ddd d	2.95	0.95	1.9	2.2
3	ffff_ffff_ff ff ffff	eeee_dddd cccc ffff	2.05	1.05	1.64	2.38
4	bbbb_cdc d_aaaa_1 111	ffff_ffff_fff f_dddd	2.22	0.89	1.68	2.08
5	1234_ffff dff_eeee	dddd_ddd d_dddd_d ddd	2.55	2.23	2.11	2.50
6	1234_567 8_90ab_c def	5555_5555 _5555_ddd d	2.85	2.13	2.350	2.7

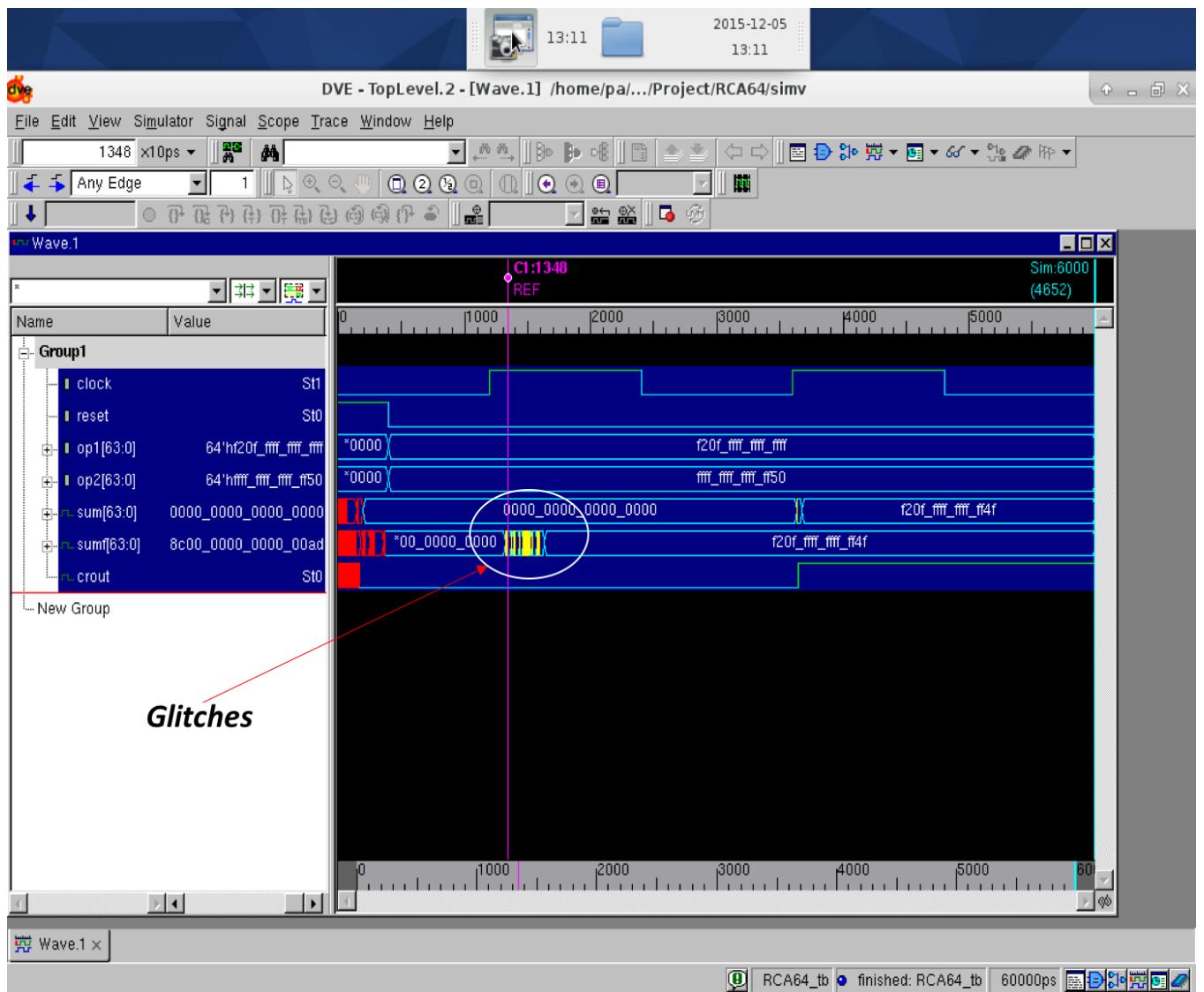


Figure V.1a: Post-synthesis (dynamic) simulation waveform that contains test case #1 for RCA

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.89 ns

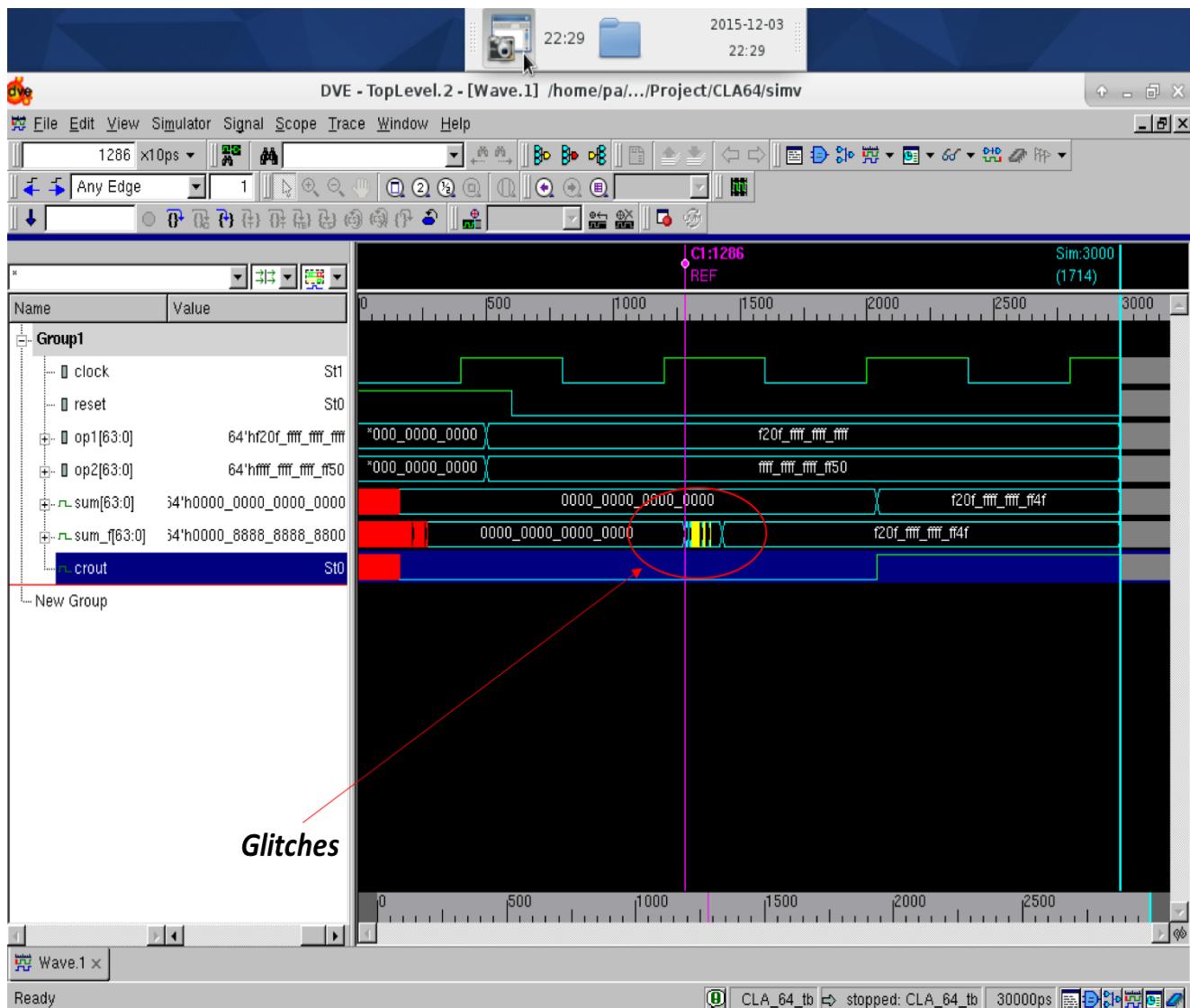


Figure V.1b: Post-synthesis (dynamic) simulation waveform that contains test case #1 for CLA-2L

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 1.54 ns

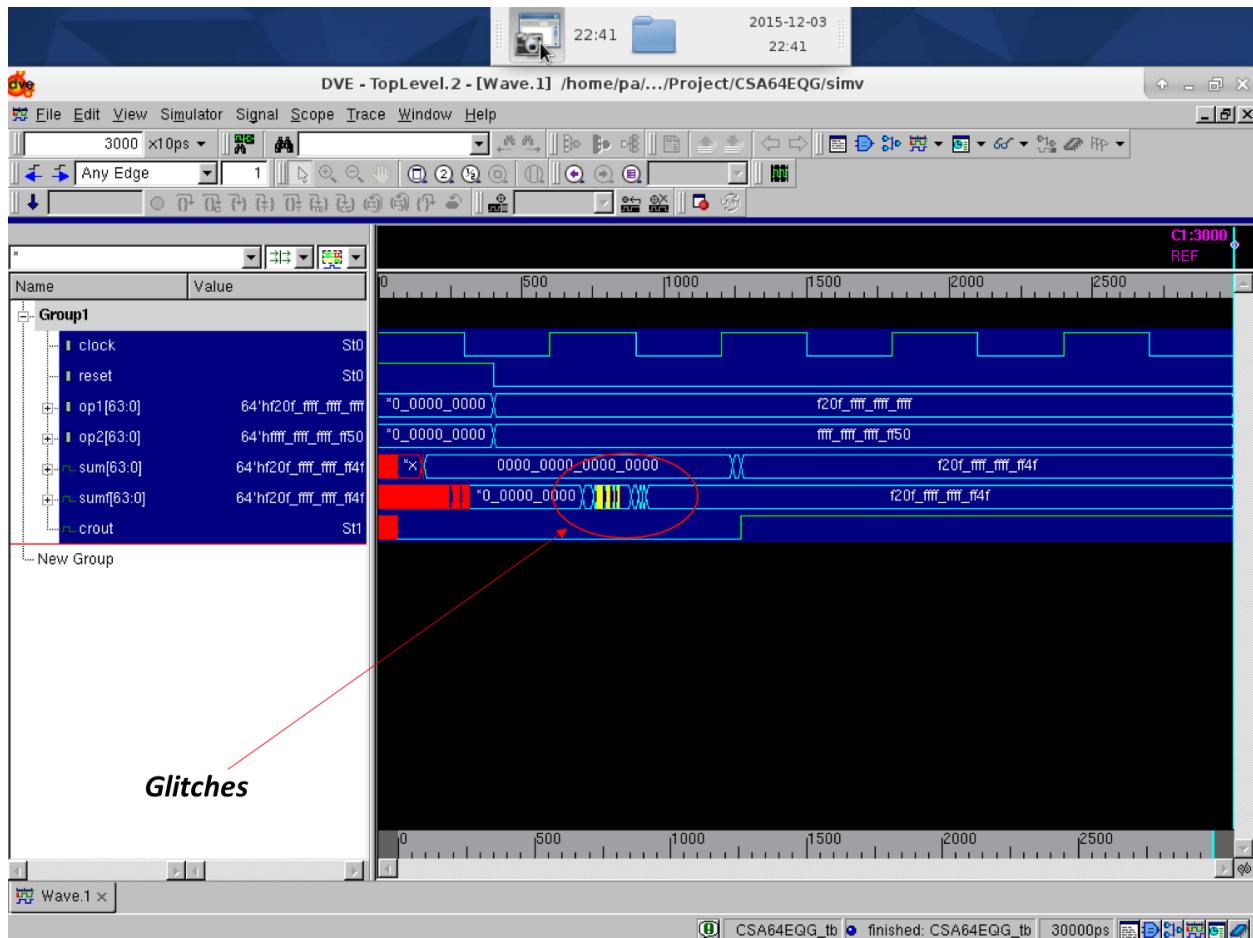


Figure V.1c: Post-synthesis (dynamic) simulation waveform that contains test case #1 for CSA-EQG

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.2 ns

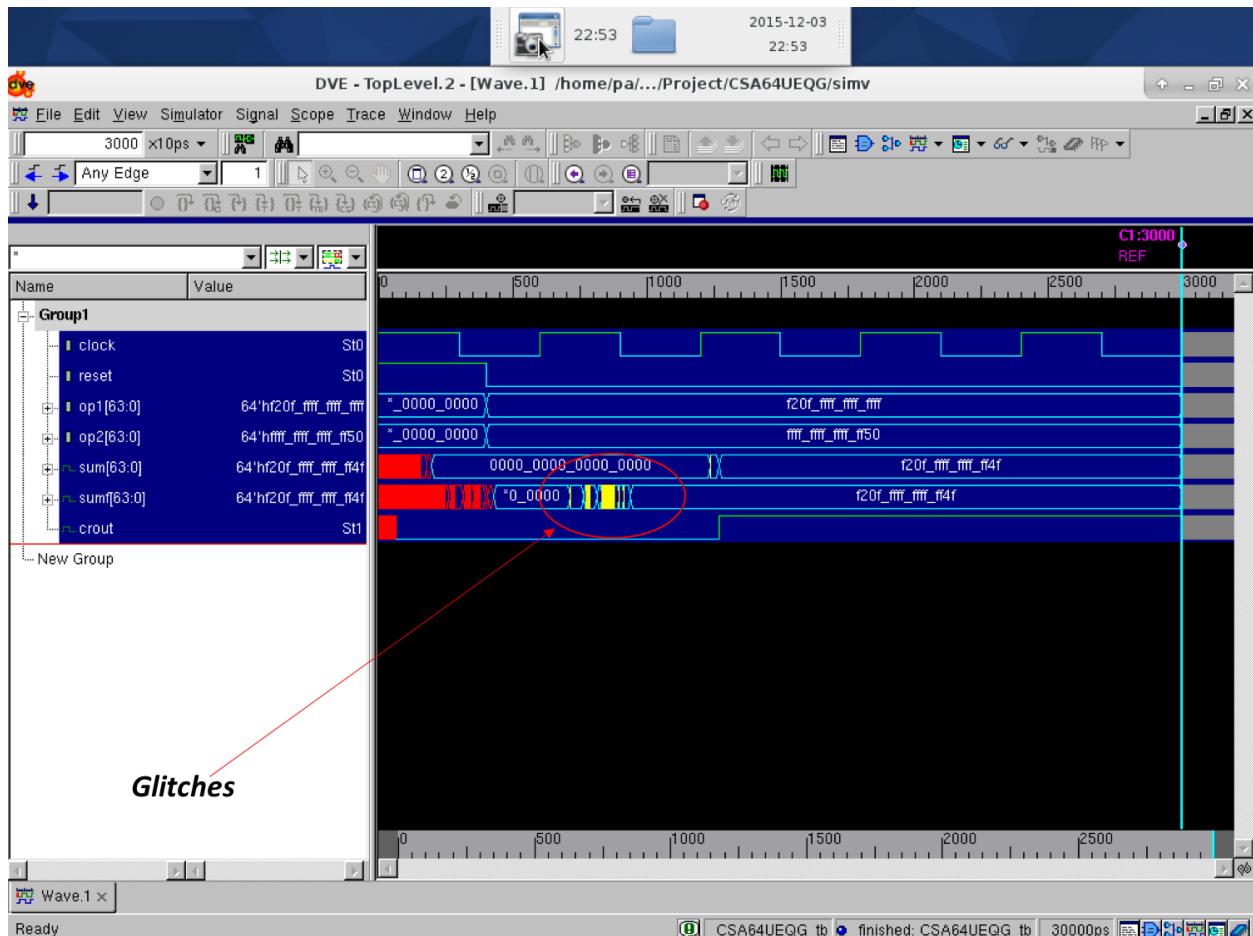


Figure V.1d: Post-synthesis (dynamic) simulation waveform that contains test case #1 for CSA-UEQG

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 1.95 ns

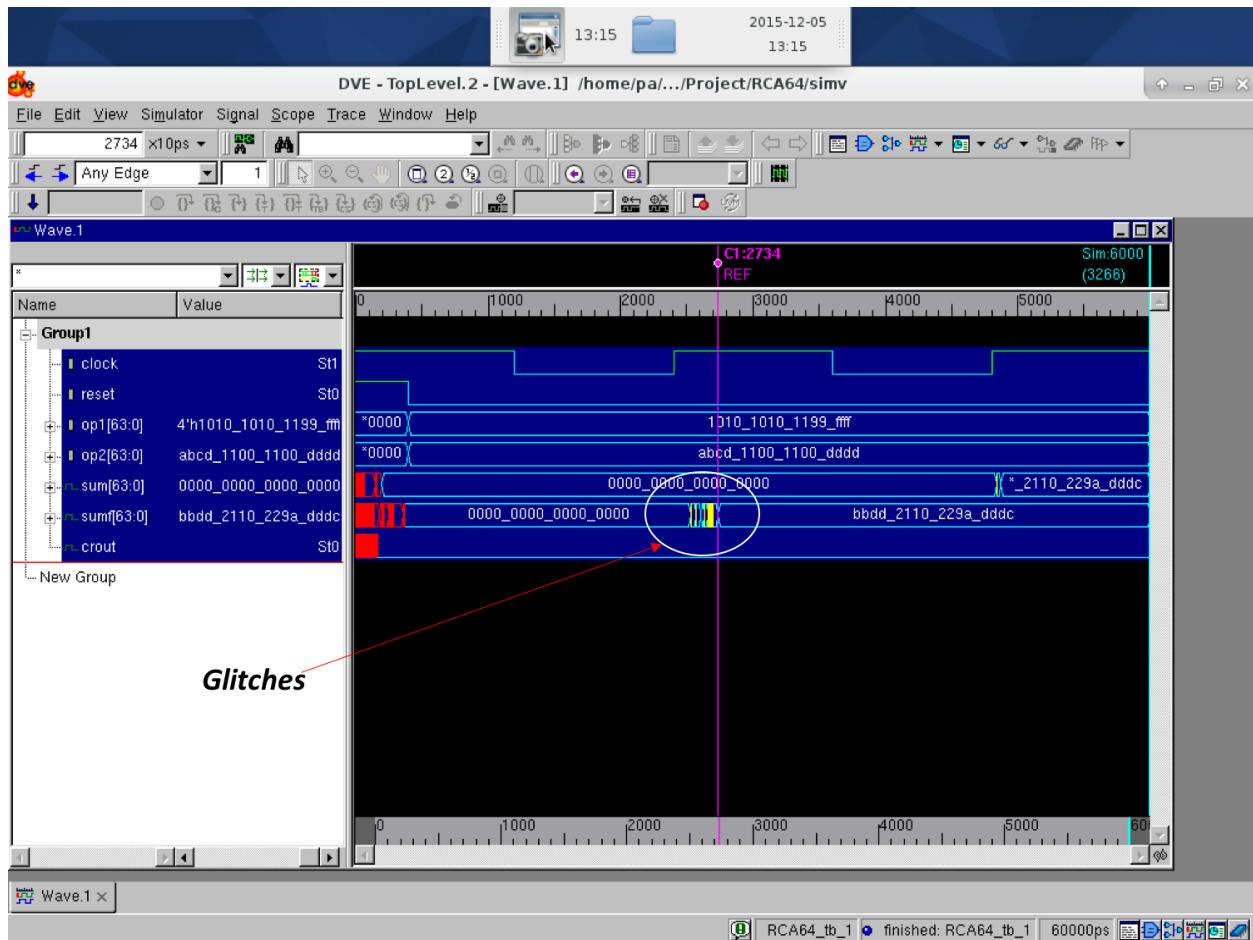


Figure V.2a: Post-synthesis (dynamic) simulation waveform that contains test case #2 for RCA

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.95 ns

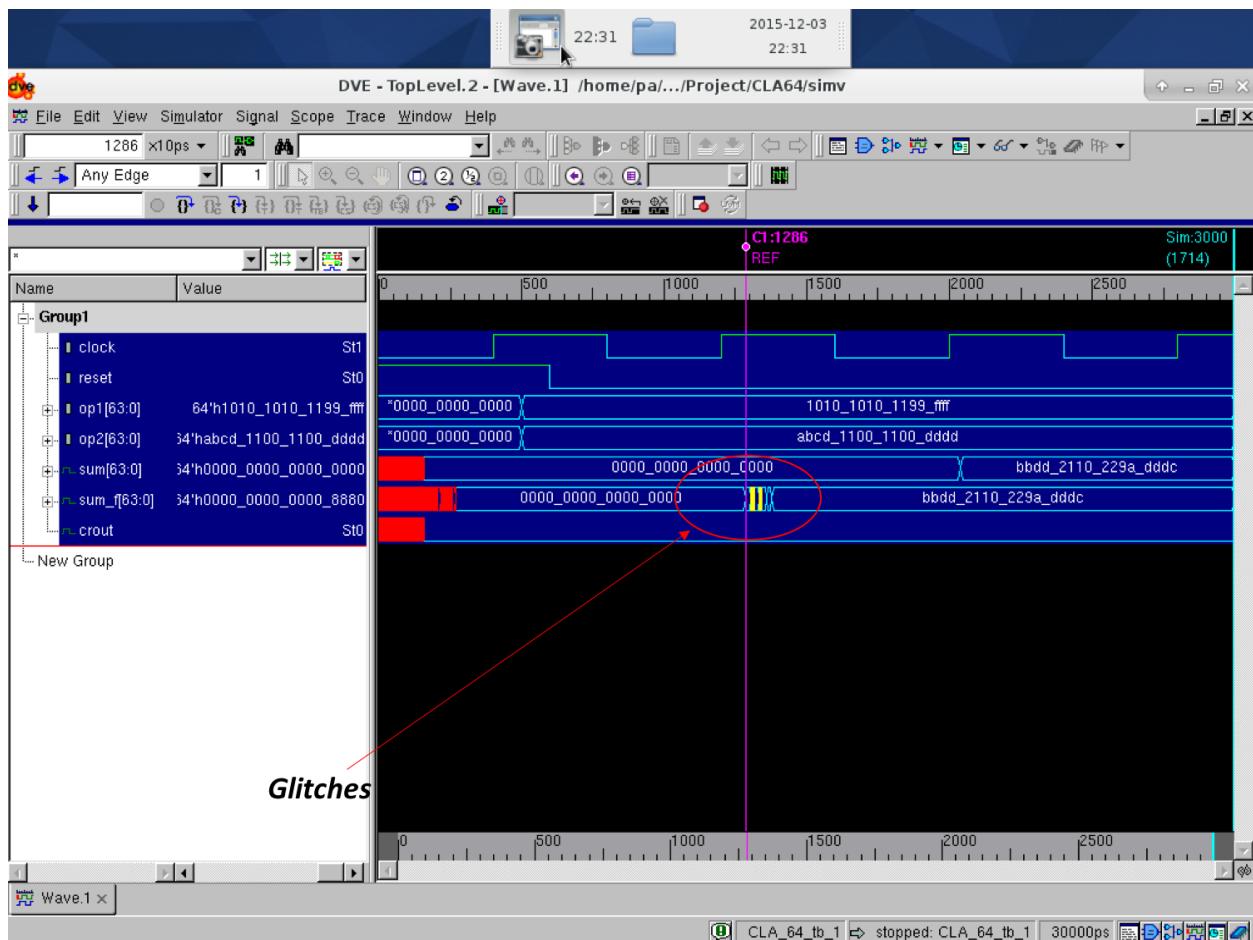


Figure V.2b: Post-synthesis (dynamic) simulation waveform that contains test case #2 for CLA-2L

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 0.95 ns

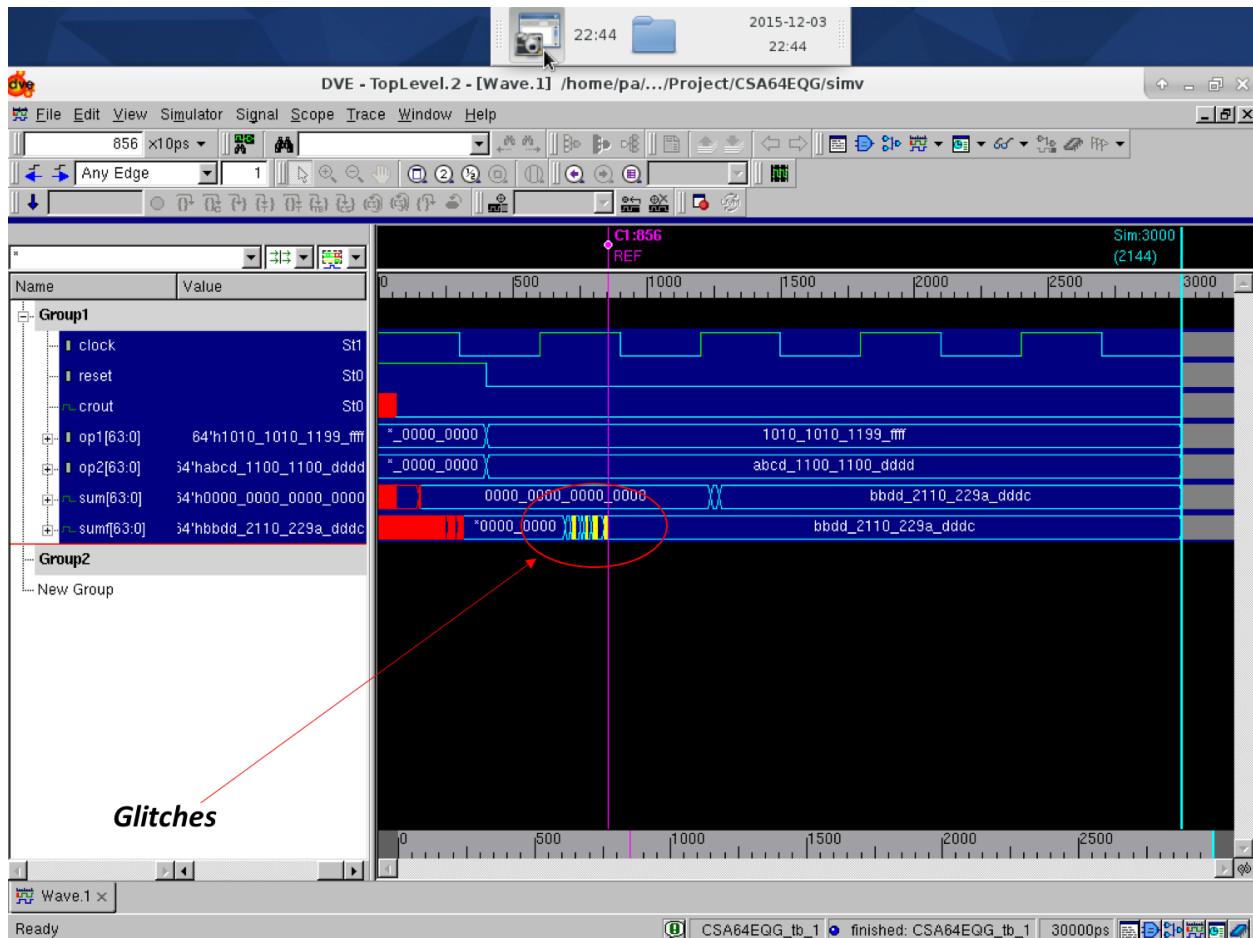


Figure V.2c: Post-synthesis (dynamic) simulation waveform that contains test case #2 for CSA-EQG

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 1.90 ns

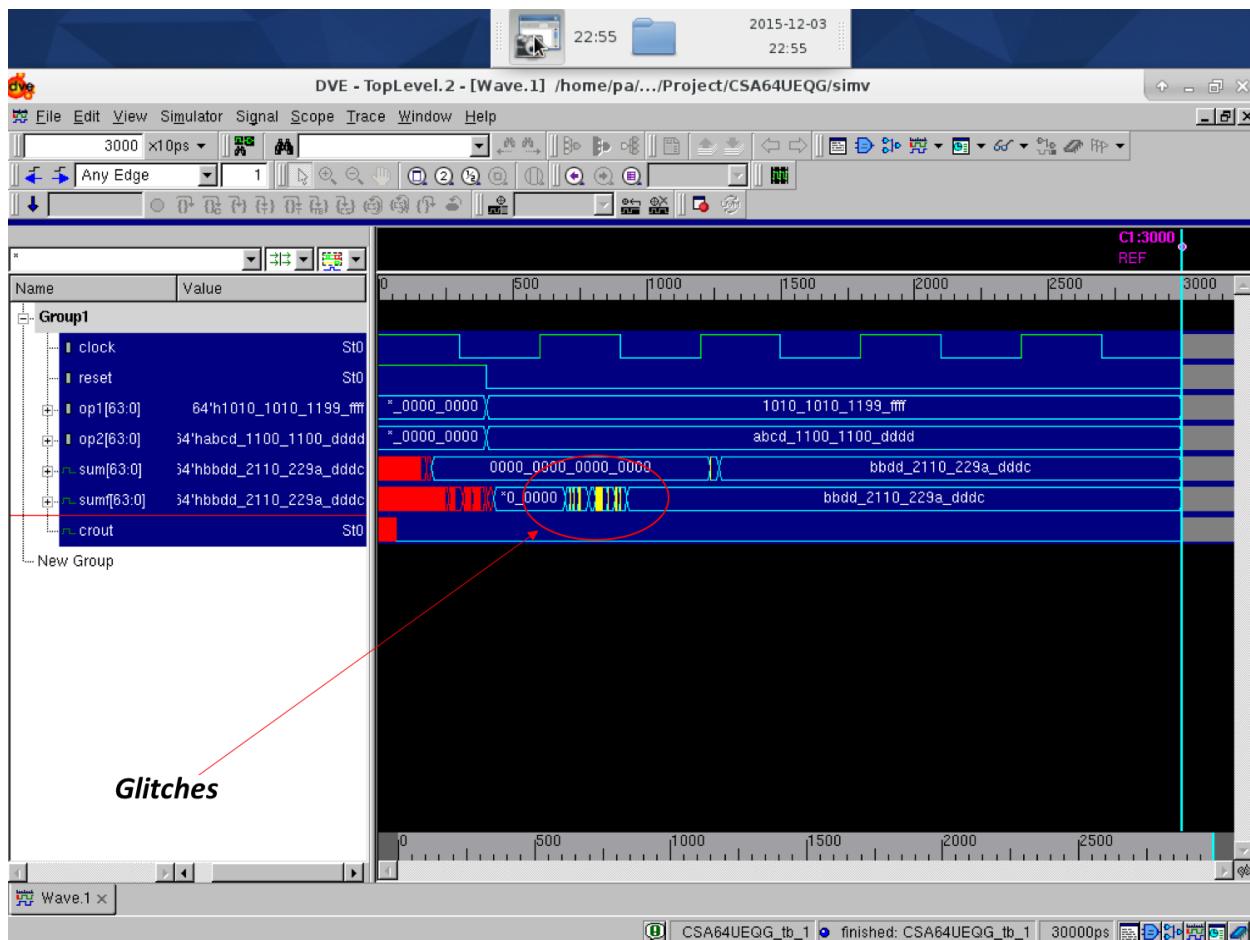


Figure V.2d: Post-synthesis (dynamic) simulation waveform that contains test case #2 for CSA-UEQG

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.2 ns

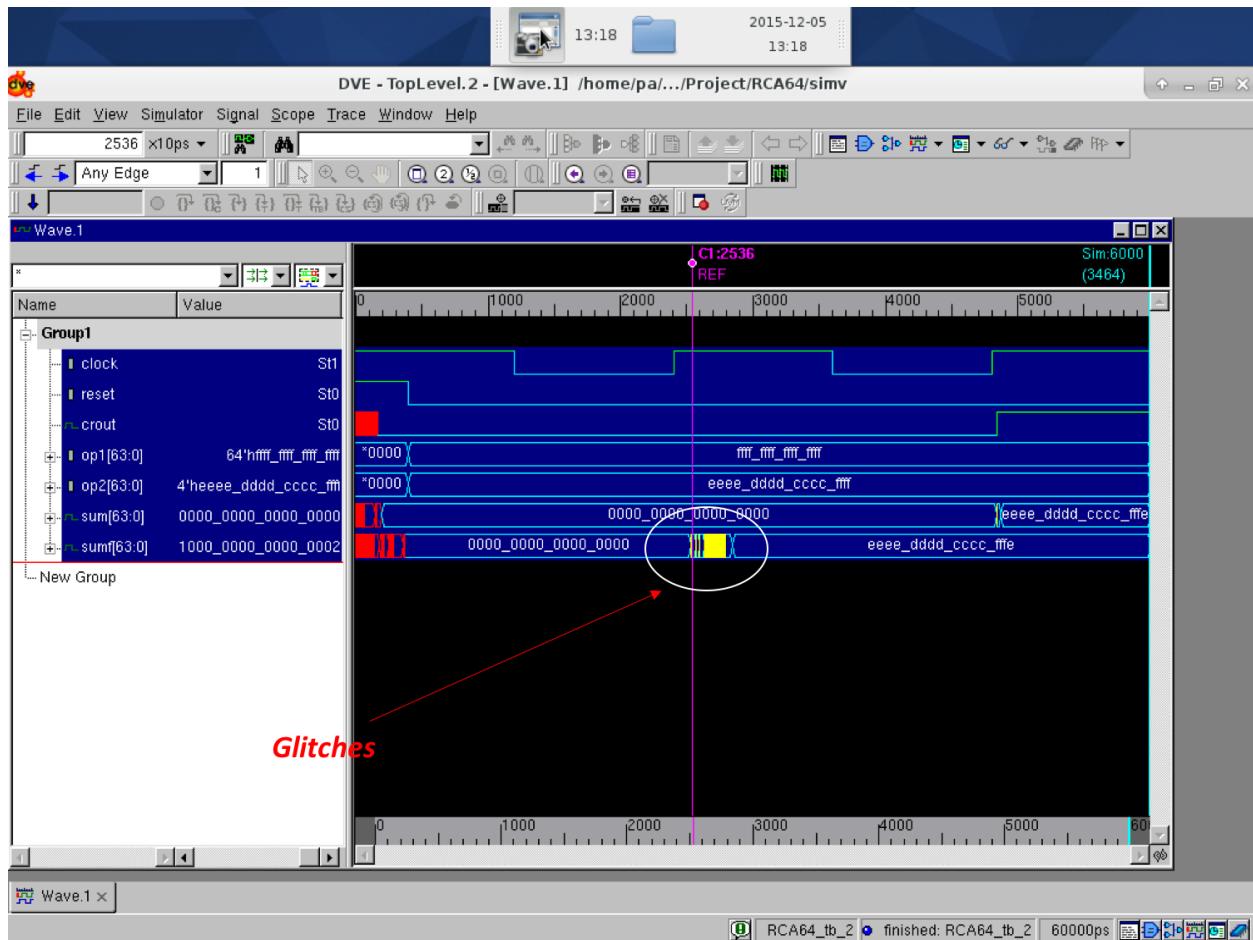


Figure V.3a: Post-synthesis (dynamic) simulation waveform that contains test case #3 for RCA

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.05 ns

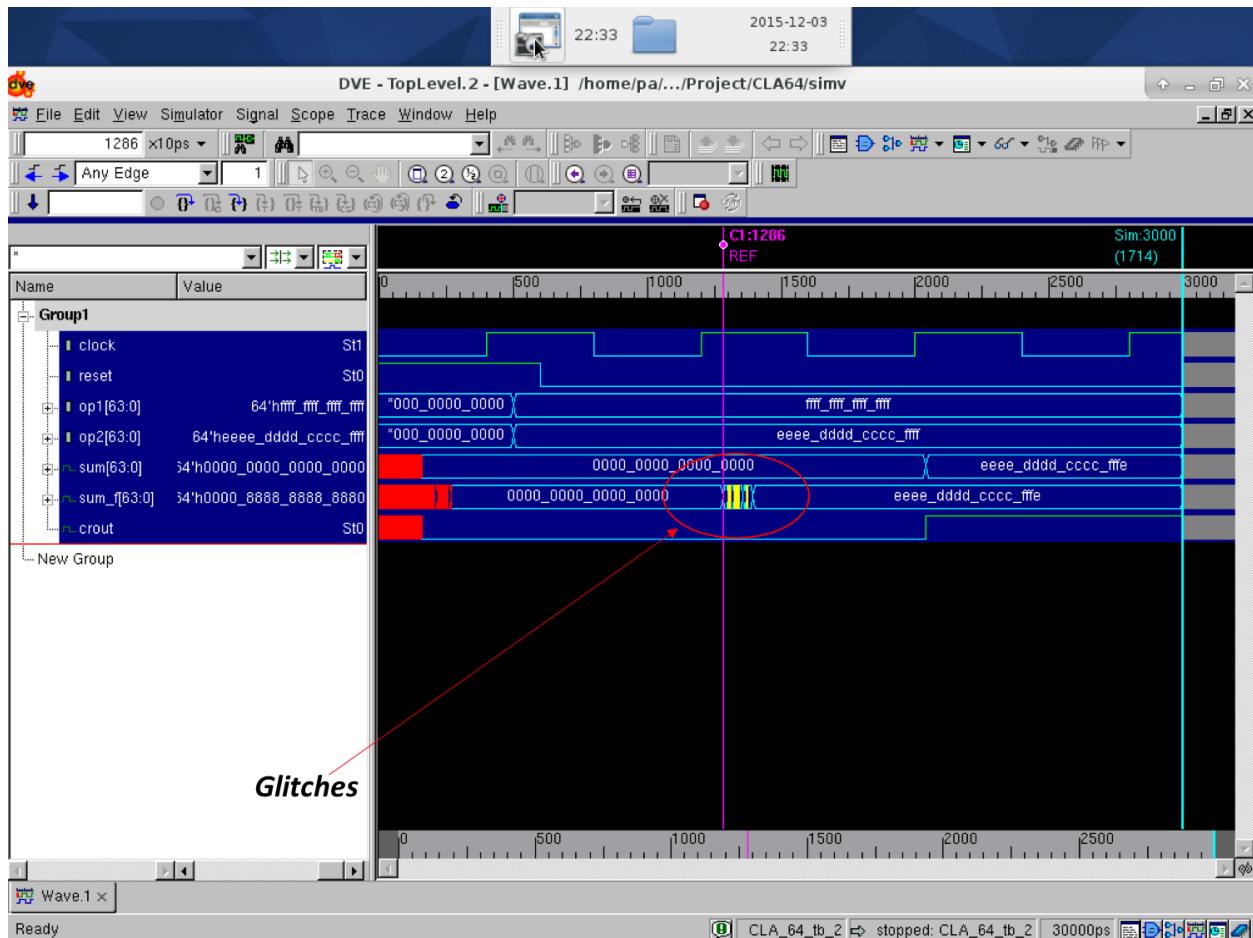


Figure V.3b: Post-synthesis (dynamic) simulation waveform that contains test case #3 for CLA-2L

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 1.05 ns

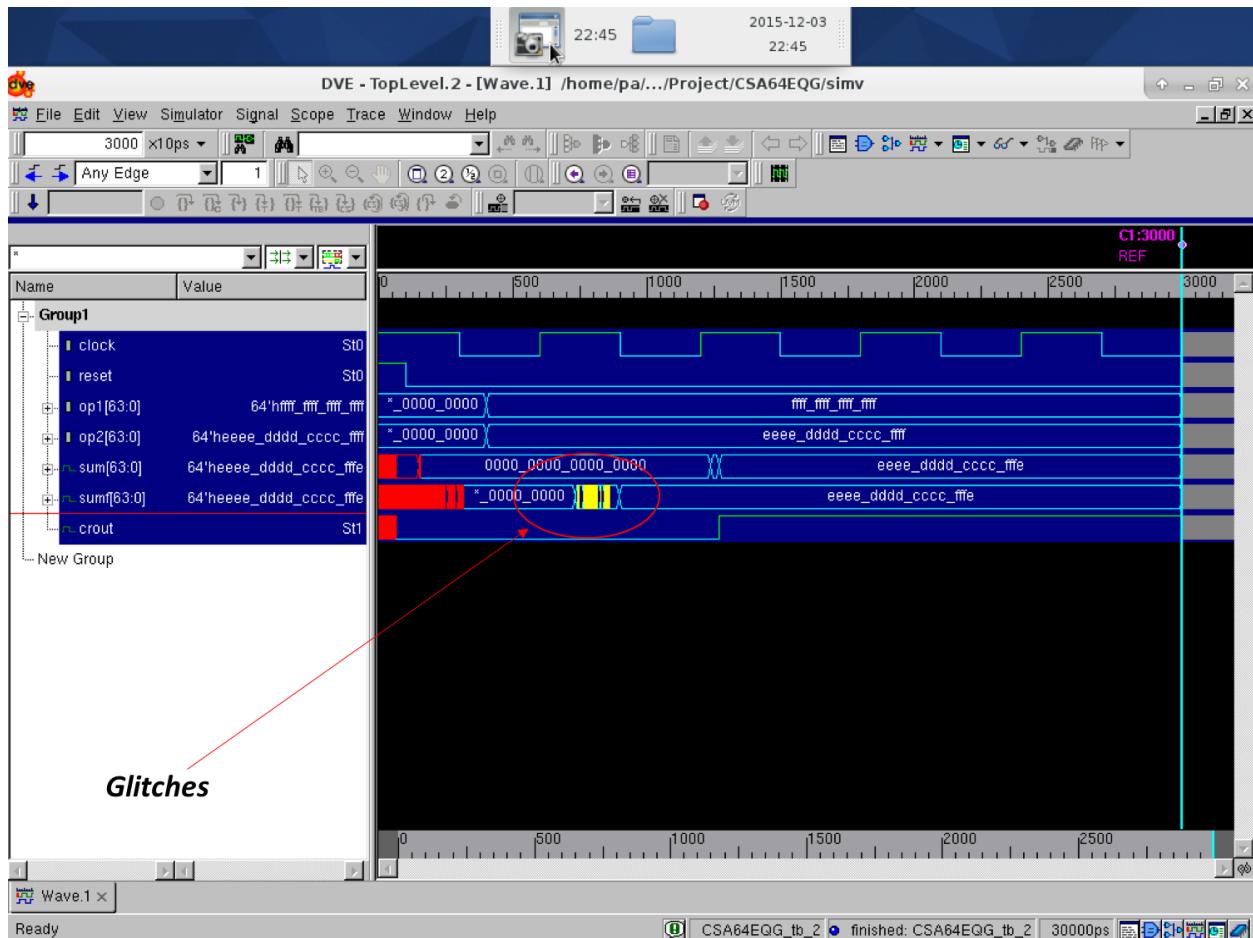


Figure V.3c: Post-synthesis (dynamic) simulation waveform that contains test case #3 for CSA-EQG

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 1.64 ns

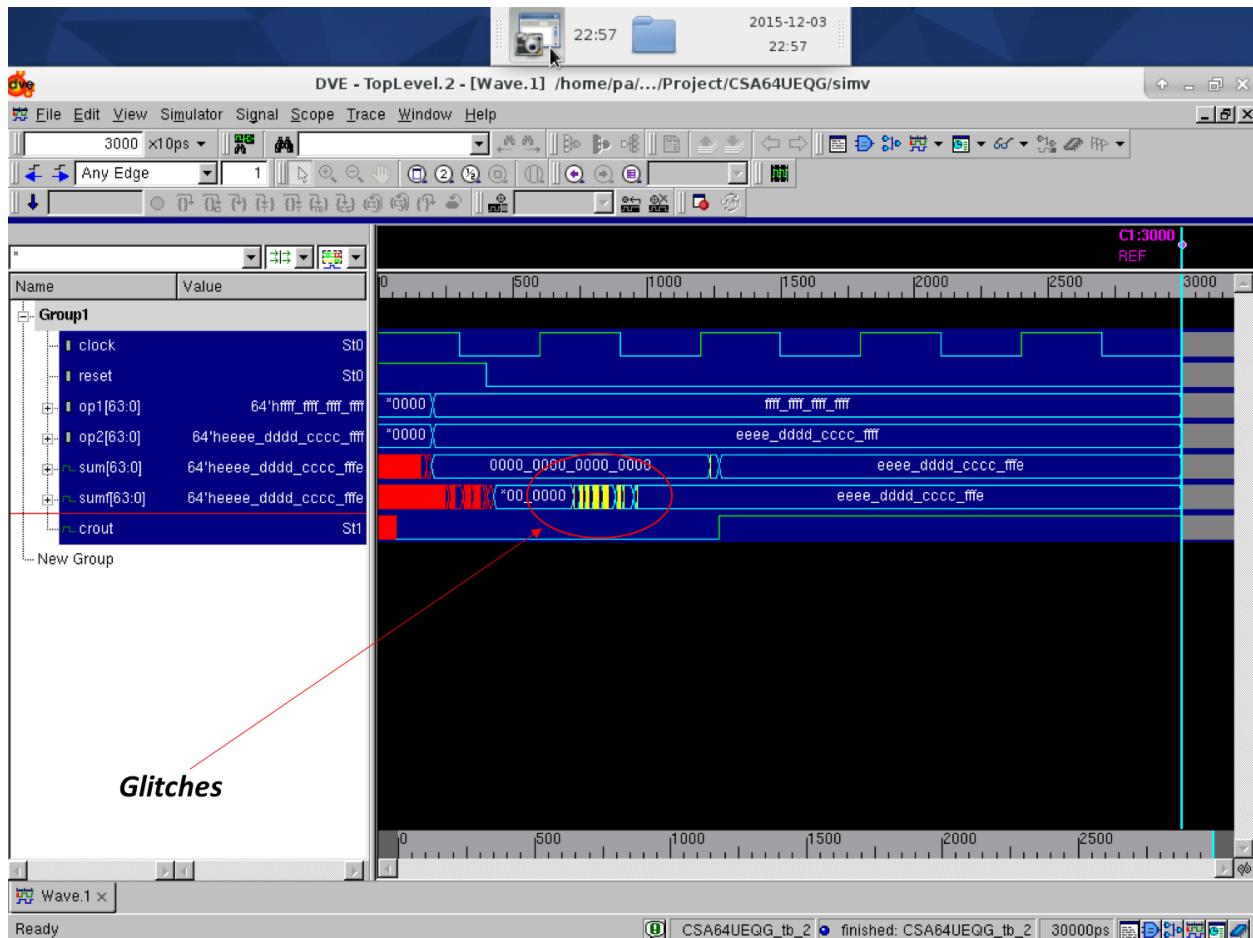


Figure V.3d: Post-synthesis (dynamic) simulation waveform that contains test case #3 for CSA-UEQG

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.38 ns

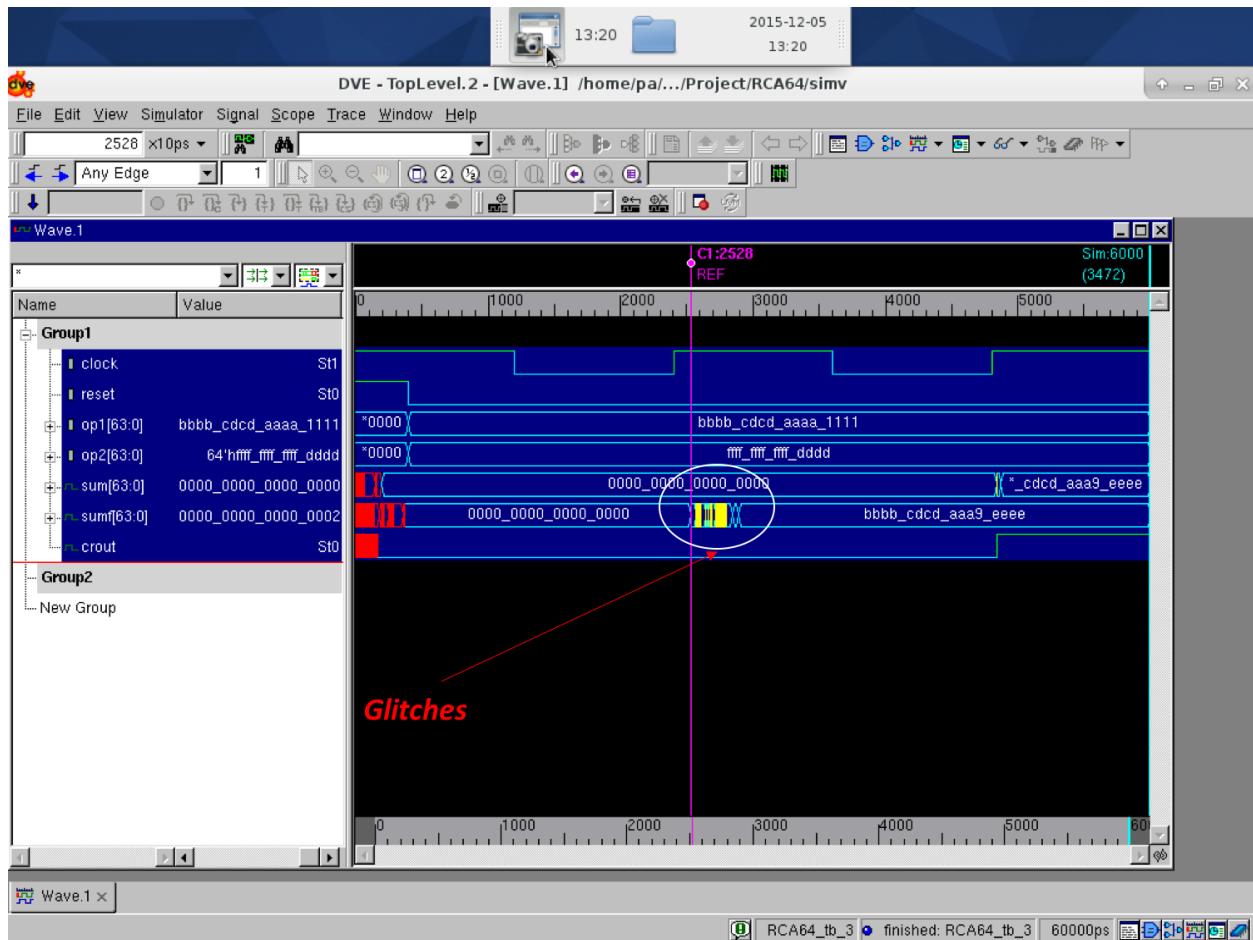


Figure V.4a: Post-synthesis (dynamic) simulation waveform that contains test case #4 for RCA

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.22 ns

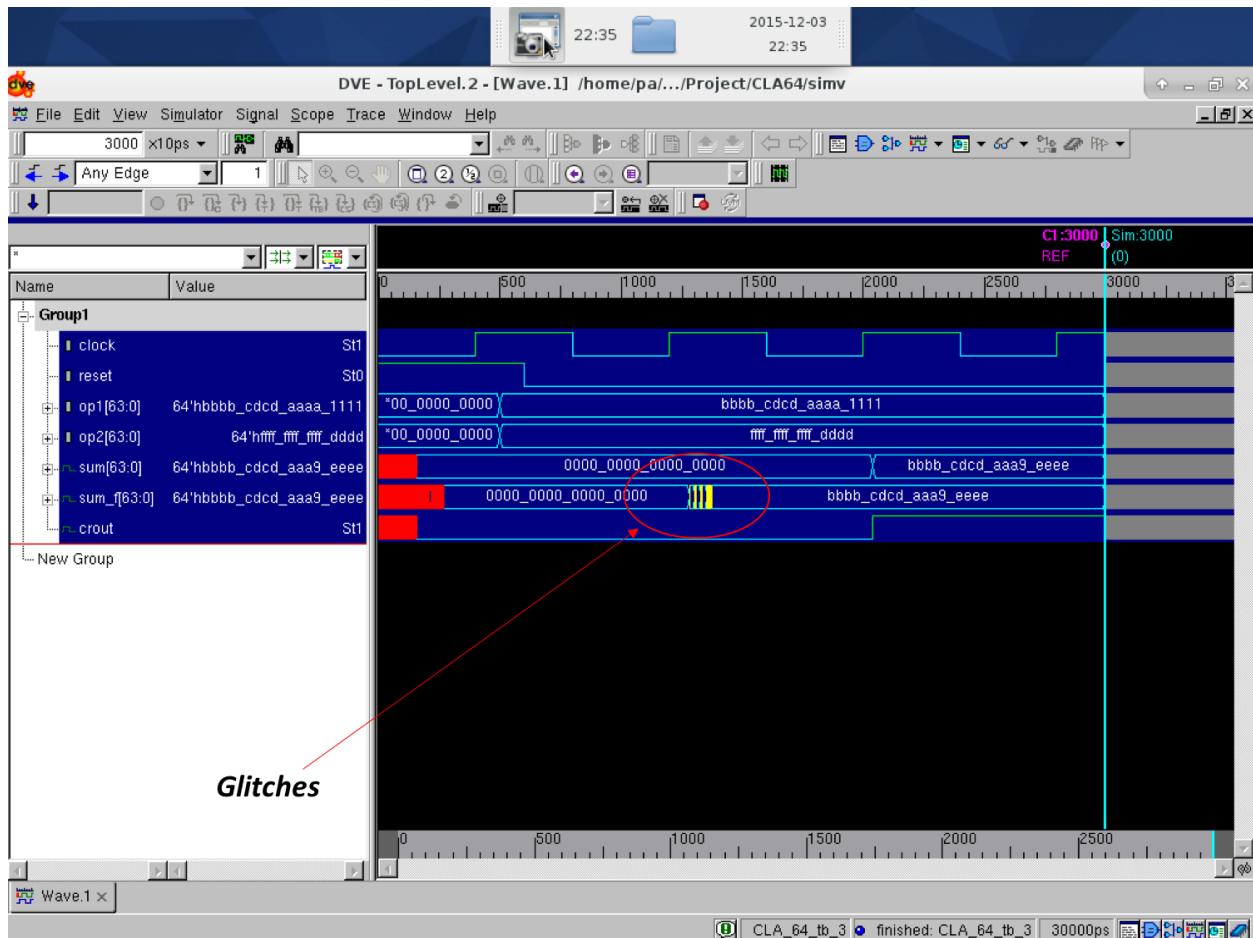


Figure V.4b: Post-synthesis (dynamic) simulation waveform that contains test case #4 for CLA-2L

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 0.89 ns

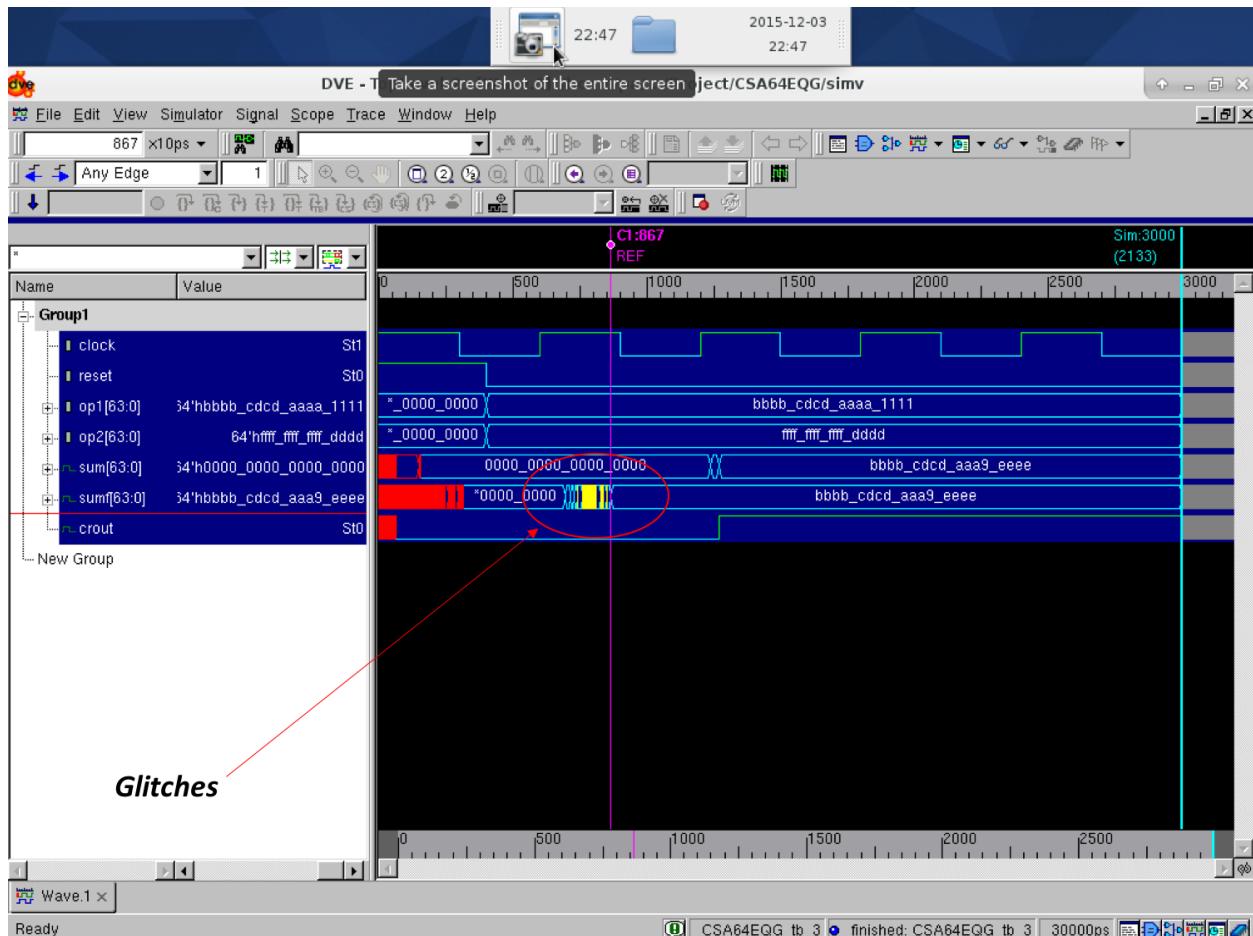


Figure V.4c: Post-synthesis (dynamic) simulation waveform that contains test case #4 for CSA-EQG

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 1.68 ns

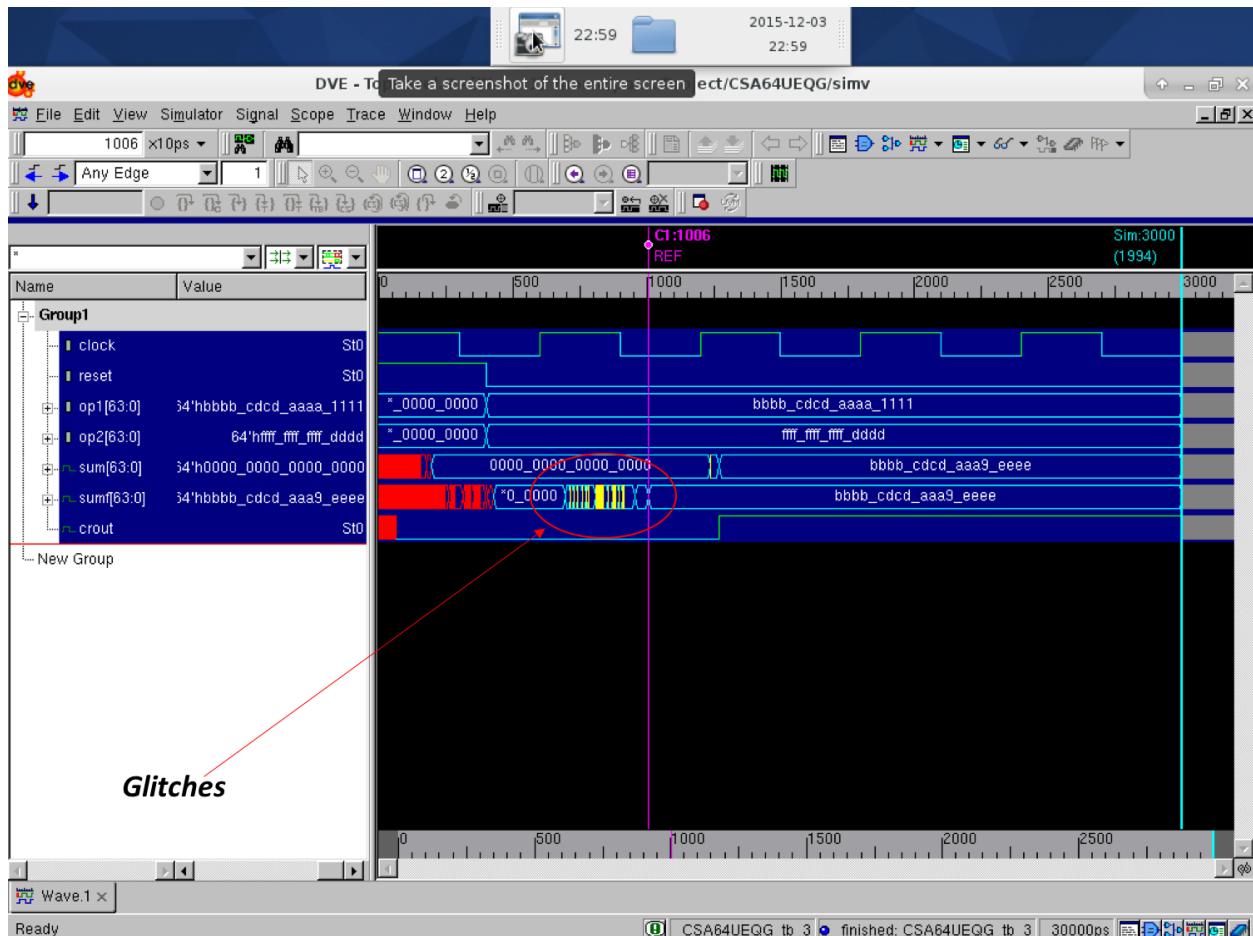


Figure V.4d: Post-synthesis (dynamic) simulation waveform that contains test case #4 for CSA-UEQG

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.08 ns

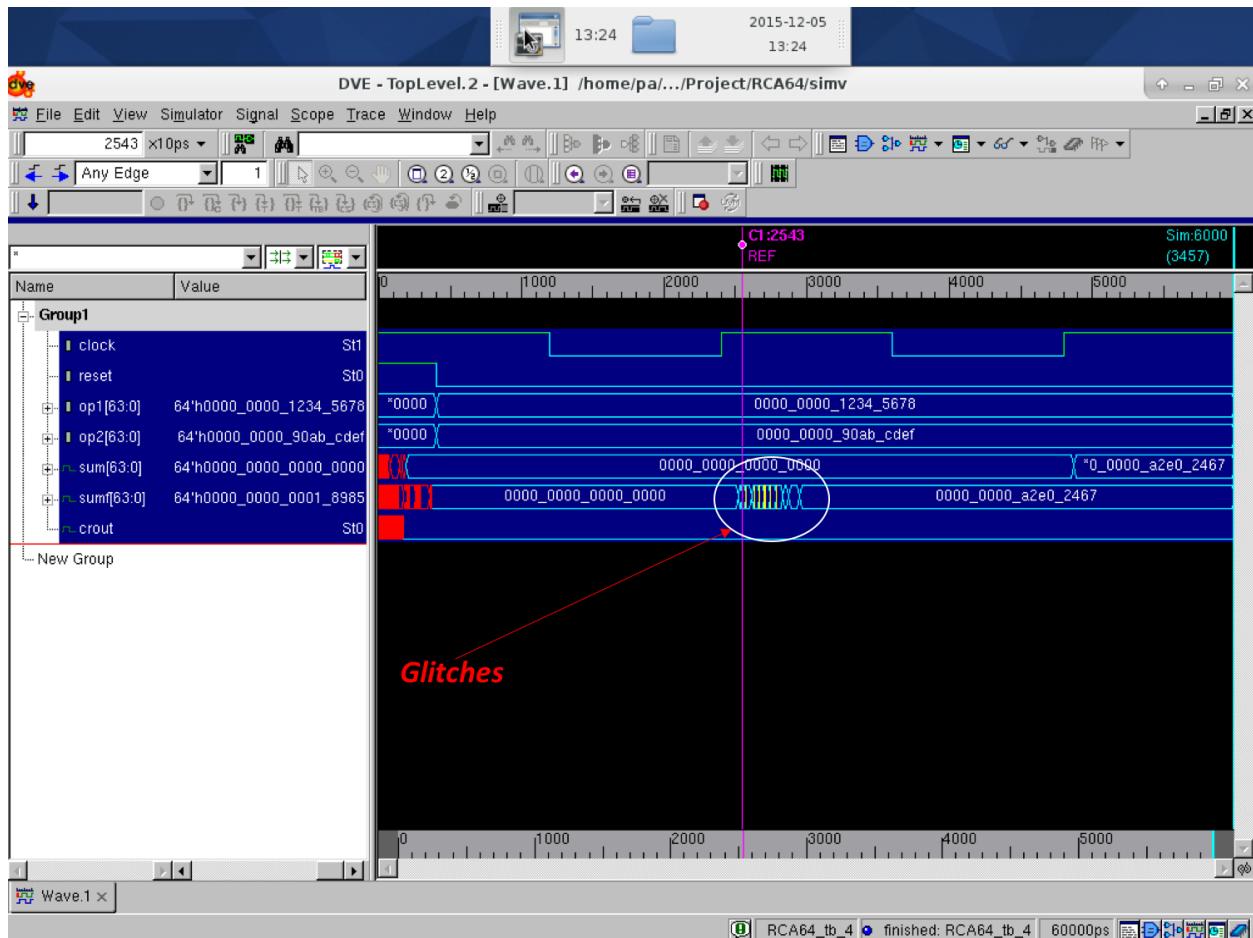


Figure V.5a: Post-synthesis (dynamic) simulation waveform that contains test case #5 for RCA

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.55 ns

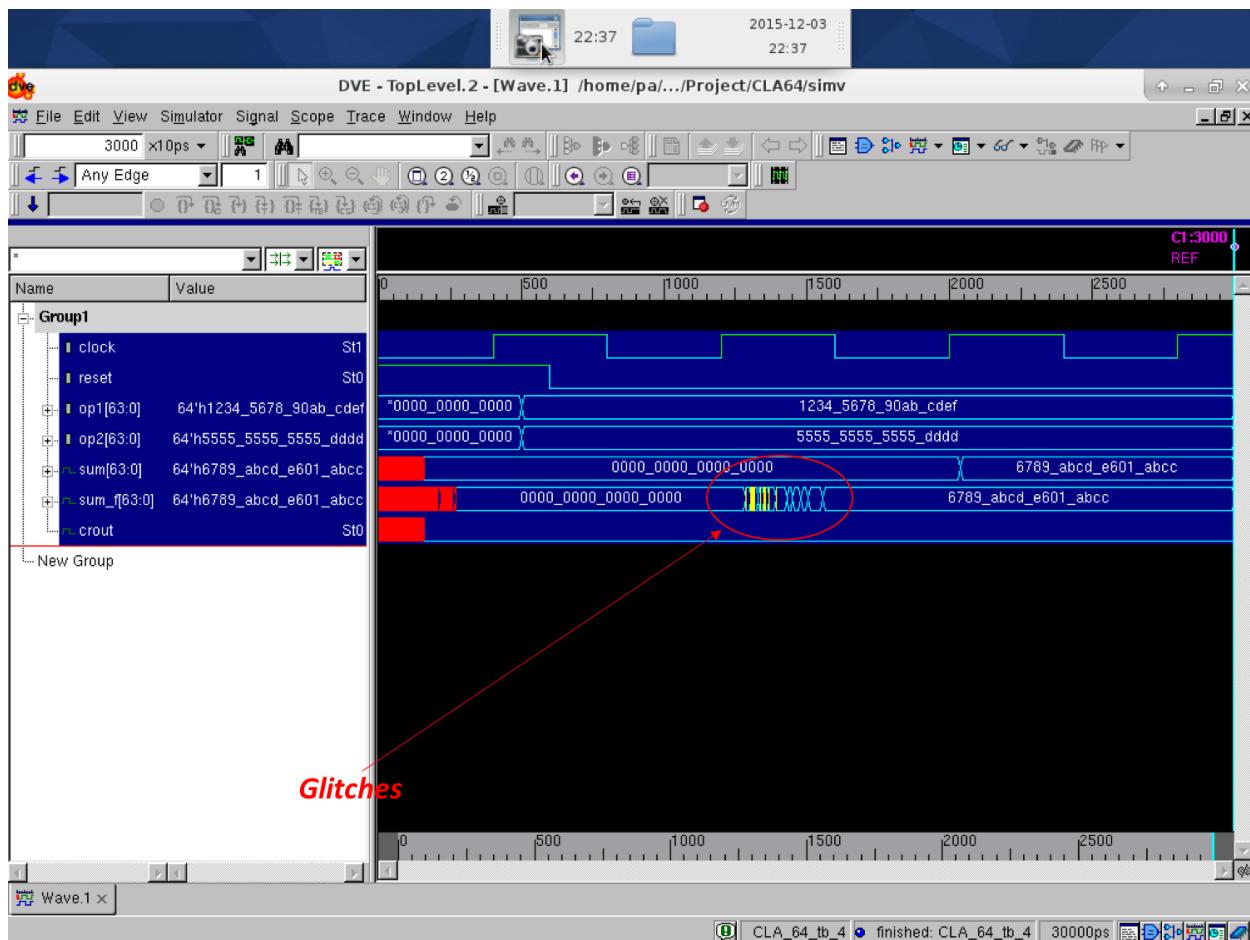


Figure V.5b: Post-synthesis (dynamic) simulation waveform that contains test case #5 for CLA-2L

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.23 ns

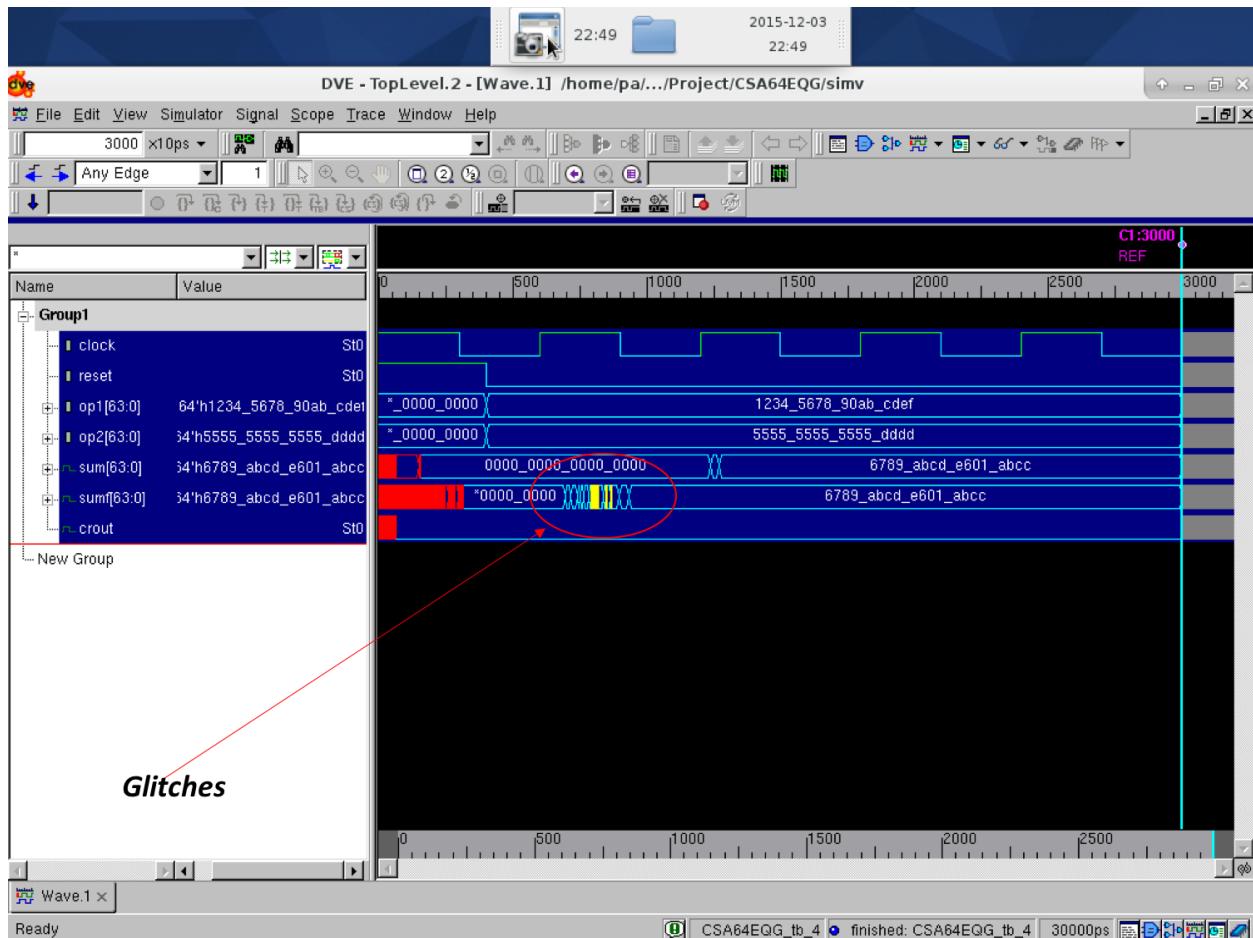


Figure V.5c: Post-synthesis (dynamic) simulation waveform that contains test case #5 for CSA-EQG

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.11 ns

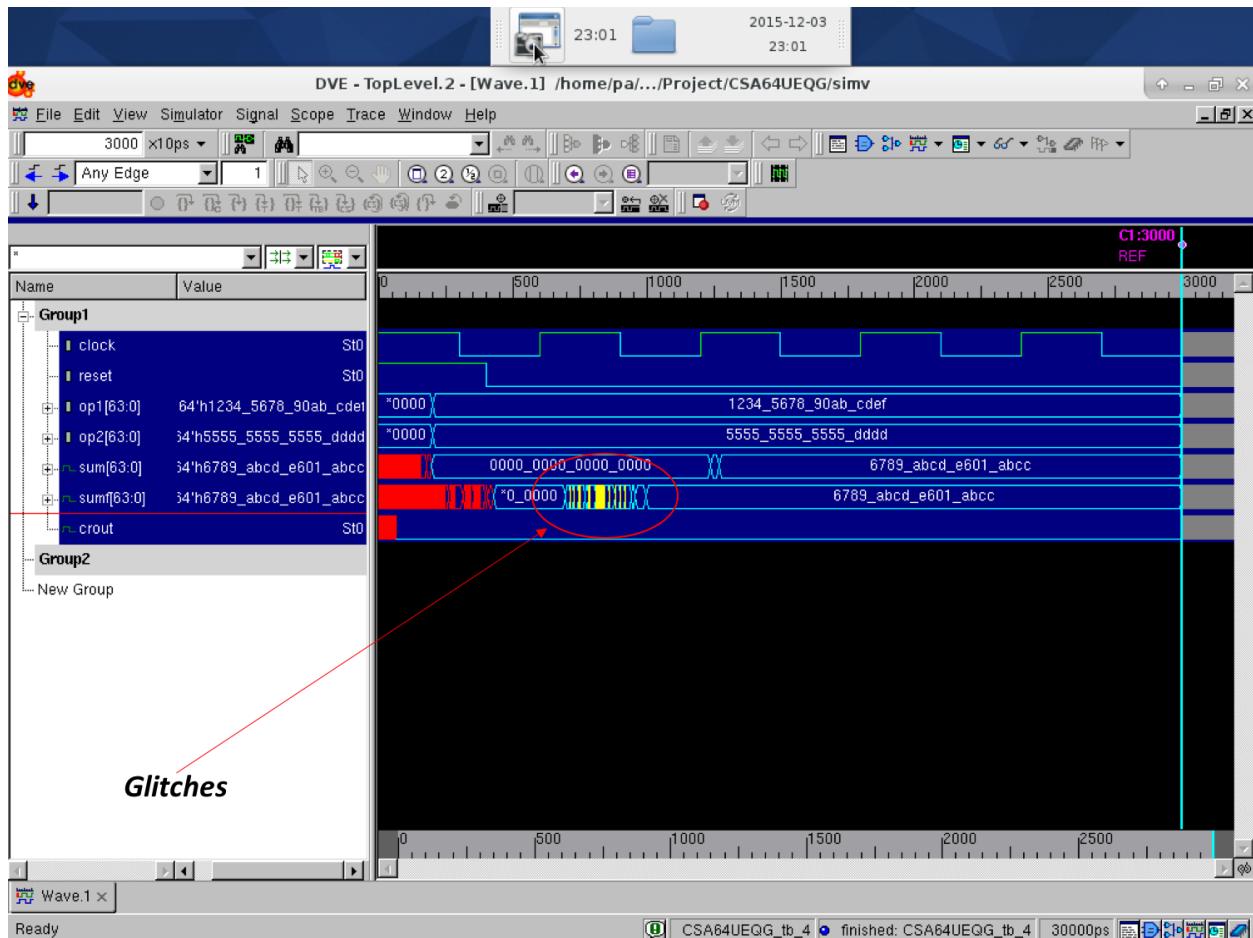


Figure V.5d: Post-synthesis (dynamic) simulation waveform that contains test case #5 for CSA-UEQG

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.5 ns

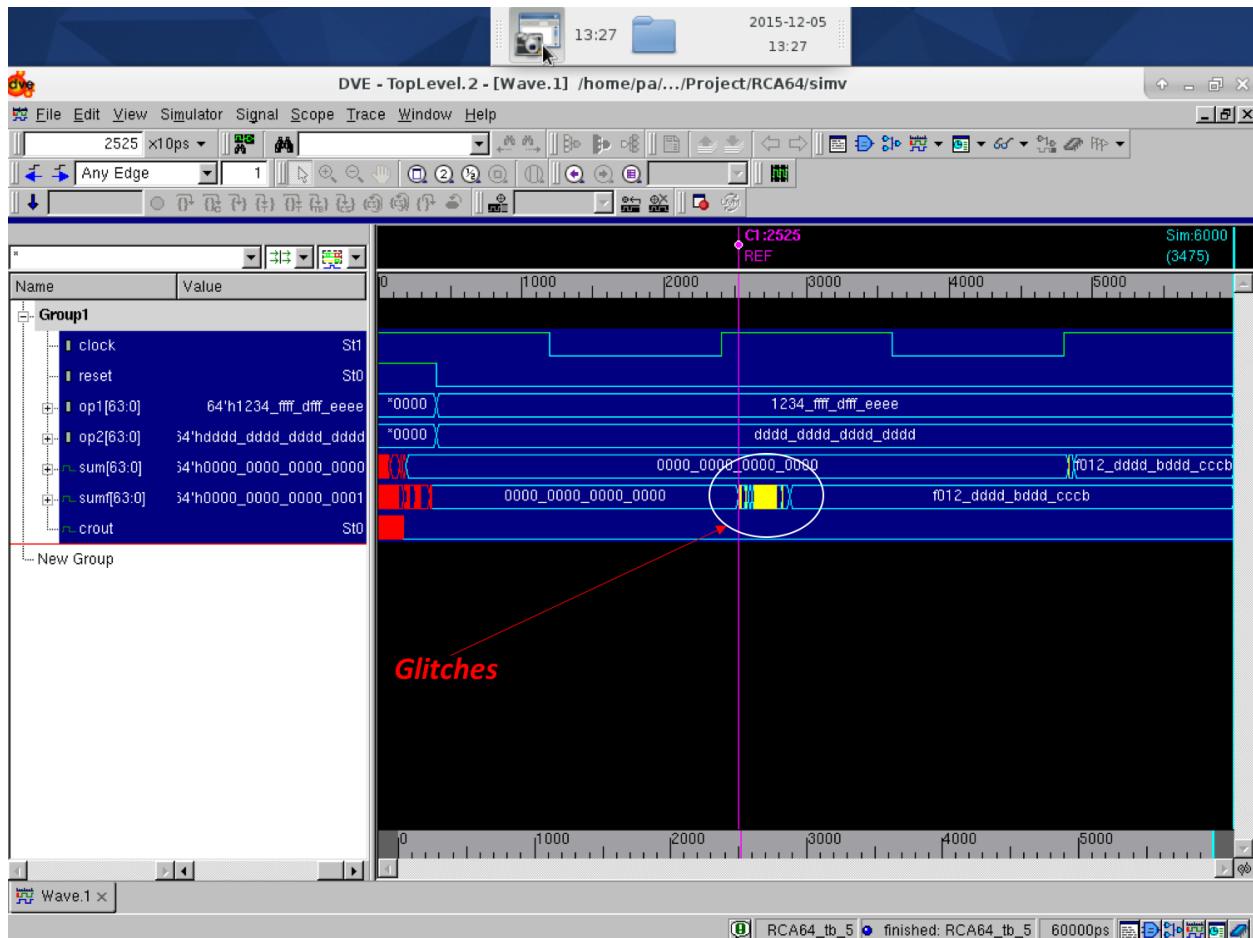


Figure V.6a: Post-synthesis (dynamic) simulation waveform that contains test case #6 for RCA

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.85 ns

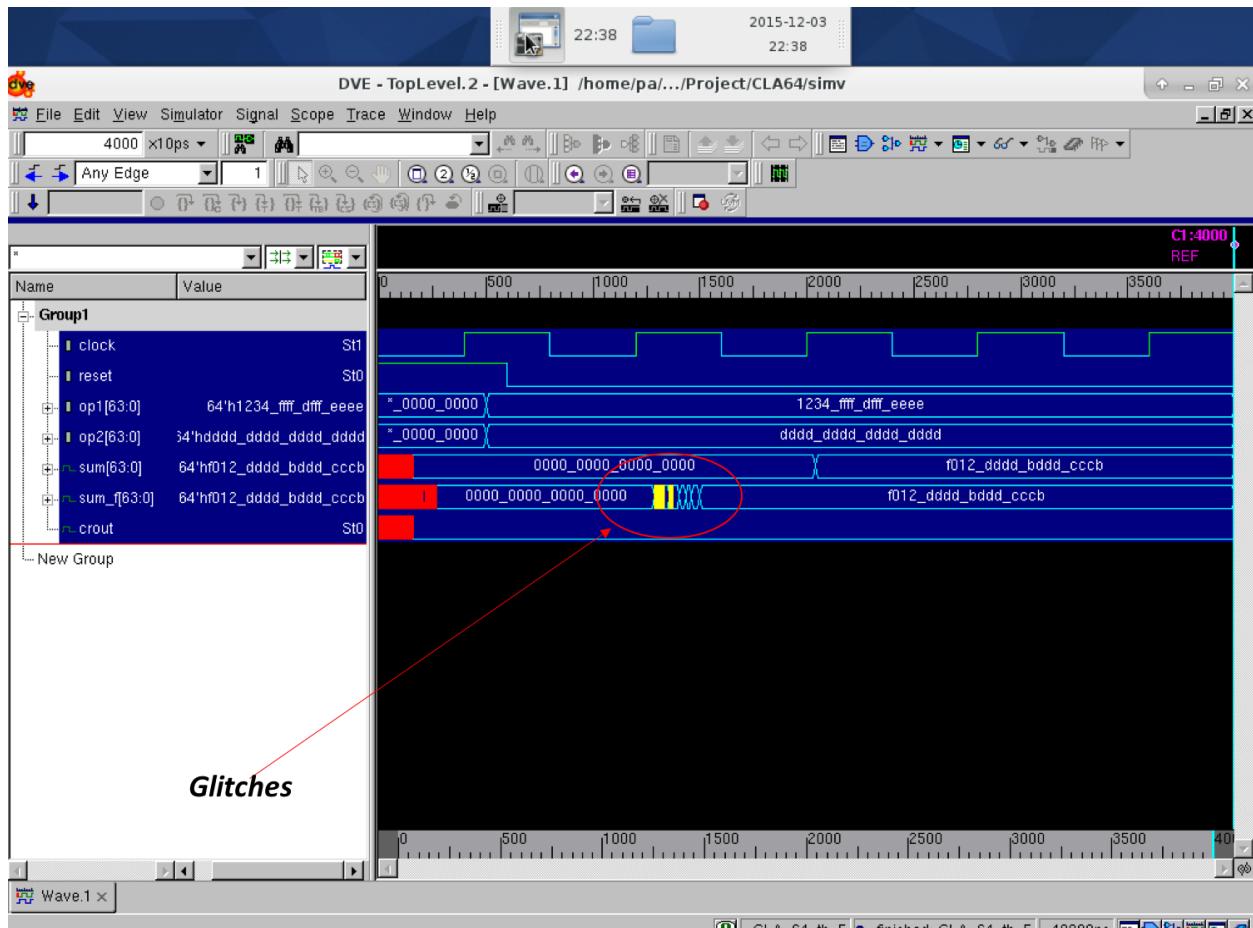


Figure V.6b: Post-synthesis (dynamic) simulation waveform that contains test case #6 for CLA-2L

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.13 ns

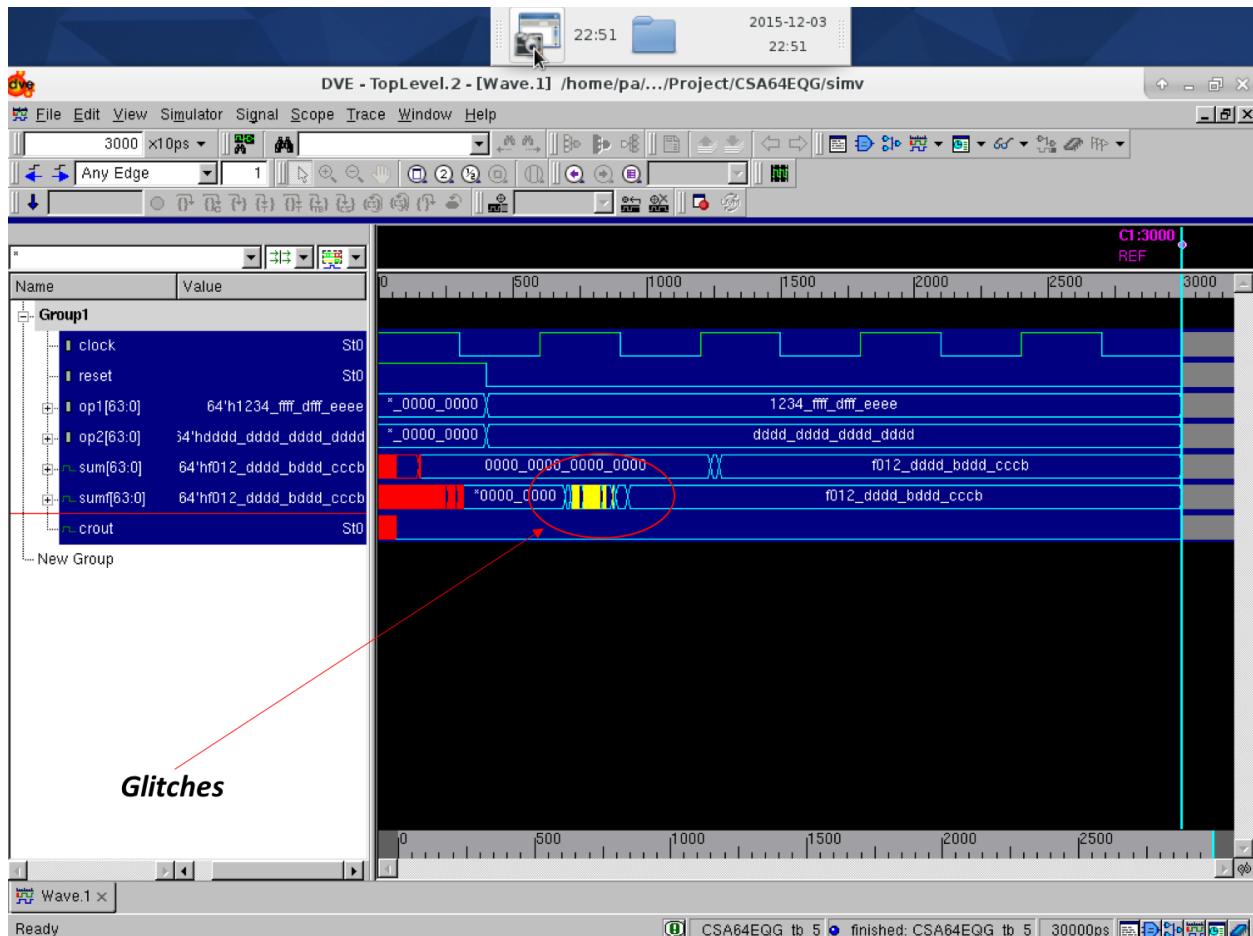


Figure V.6c: Post-synthesis (dynamic) simulation waveform that contains test case #6 for CSA-EQG

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.35 ns

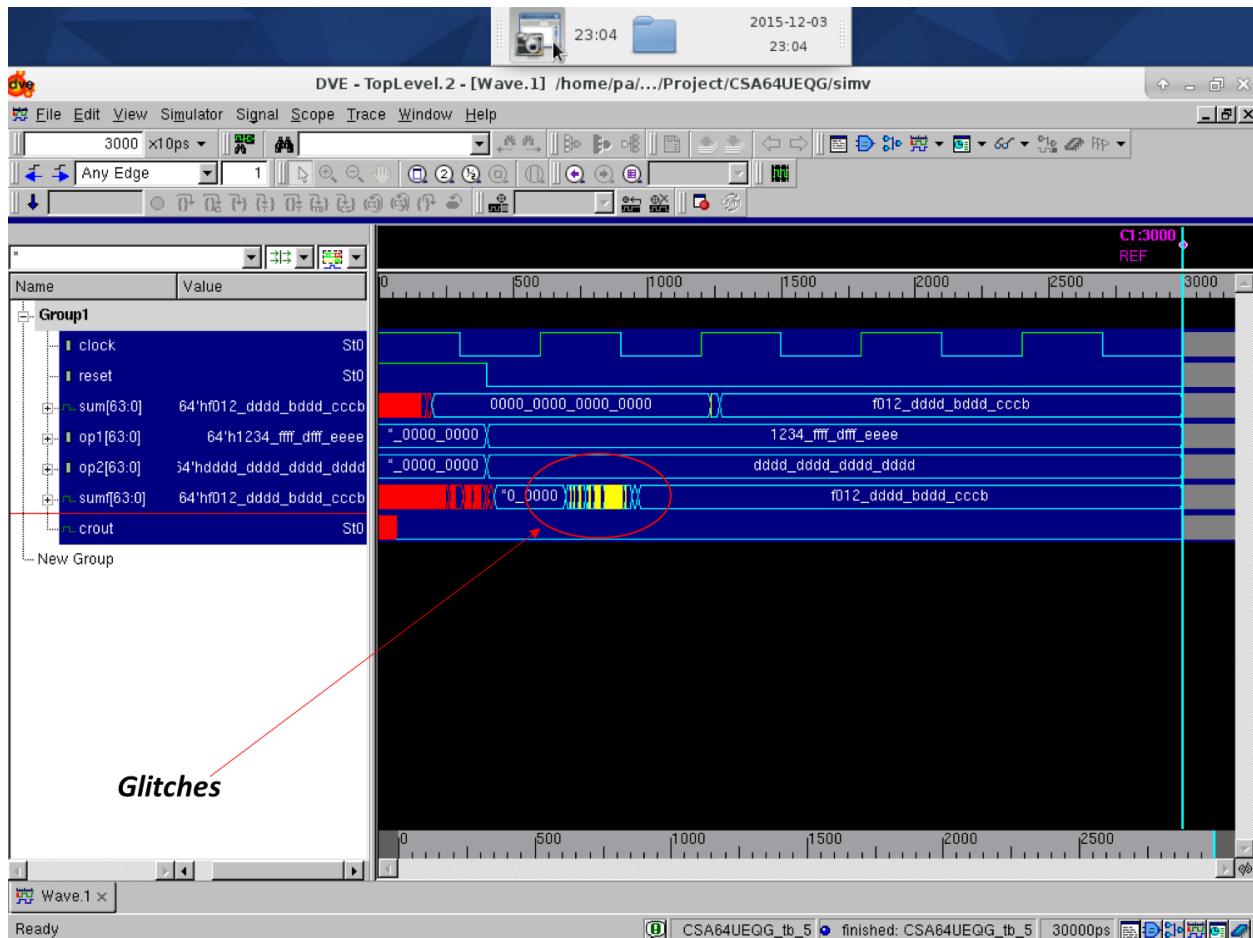


Figure V.6d: Post-synthesis (dynamic) simulation waveform that contains test case #6 for CSA-UEQG

The Glitches or fluctuation in circuit because of immediate data change in operands and wire delay. Glitch/Delay is 2.70 ns

From the post synthesis we got some delays in design that is because of gate delays and wire delays. To remove that glitches, we have to increase the clock period. Clock period will be more than half of time period i.e., **if time period is 8 ns then clock period must be around 5 ns.**

VI. Conclusion

After implementing and analyzing the different types of 64 bit adders, I observed that area of the circuit is inversely proportional to the time period. The power of the circuit is proportional to area of the circuit and inversely proportional to time period of the circuit. From analyzing the implementation, the carry select adder is fastest amongst all adders. Every adder has its own advantage. Ripple carry adder can be used for short bit length. Carry look ahead's 2 level structure can be used for long bit length. Carry Select Adder has good performance in propagation delay compare other two 64 bit adders.

Appendix A

A.1 Contents from EDA Tool Configurations and Setup Files

VCS tool setup environment file content

```
setenv VCS_HOME /apps/synopsys/I-2014.03-2
source ${VCS_HOME}/bin/environ.csh
```

A.2 Scripts and/or Commands Used for Simulation and Synthesis

RCA Synthesis Script

```
Set link_library
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
/apps/synopsys/SYNTH/libraries/syn/dw02.sldb
/apps/synopsys/SYNTH/libraries/syn/dw01.sldb}

Set_target_library
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}
read_verilog RCA64.v

current_design RCA64

check_design

create_clock clock -name clock -period 18.5600000

set_propagated_clock clock

set_clock_uncertainty 0.25 clock

set_propagated_clock clock

set_fix_hold [ get_clocks clock ]

compile -map_effort medium -incremental_mapping

update_timing

set_max_area 2500
```

```
report -cell  
report_timing -max_paths 10  
report_area  
report_power  
write -hierarchy -format verilog -output RCA64_1_nl.v  
quit
```

CLA-2L Synthesis.script

```
set link_library  
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25  
/apps/synopsys/SYNTH/libraries/syn/dw02.sldb  
/apps/synopsys/SYNTH/libraries/syn/dw01.sldb}  
  
set target_library  
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}  
  
read_verilog {CLA4.v, CLA4_2.v, CLA16.v CLA16_2.v, CLA_64.v}  
current_design CLA_64  
  
check_design  
  
create_clock clock -name clock -period 4.9500000  
set_propagated_clock clock  
  
set_clock_uncertainty 0.25 clock  
set_propagated_clock clock  
  
set_fix_hold [ get_clocks clock ]  
  
compile -map_effort medium -incremental_mapping  
  
update_timing  
  
set_max_area 2500  
  
report -cell
```

```
report_timing -max_paths 5  
report_area  
report_power  
write -hierarchy -format verilog -output CLA_64_1_nl.v  
quit
```

CSAEQG Synthesis script

```
set link_library  
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25  
/apps/synopsys/SYNTH/libraries/syn/dw02.sldb  
/apps/synopsys/SYNTH/libraries/syn/dw01.sldb}  
  
set target_library  
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}  
  
read_verilog {mux_carry.v,mux_sum.v,CSA64EQG.v}  
  
current_design CSA64EQG  
  
check_design  
  
create_clock clock -name clock -period 5.200000  
  
set_propagated_clock clock  
  
set_clock_uncertainty 0.25 clock  
  
set_propagated_clock clock  
  
set_fix_hold [ get_clocks clock ]  
  
compile -map_effort medium -incremental_mapping  
  
update_timing  
  
set_max_area 3100  
  
report -cell  
  
report_timing -max_paths 5
```

```
report_area  
report_power  
write -hierarchy -format verilog -output CSA64EQG_1_nl.v  
quit
```

CSAUEQG Synthesis.script

```
set link_library  
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25  
/apps/synopsys/SYNTH/libraries/syn/dw02.sldb  
/apps/synopsys/SYNTH/libraries/syn/dw01.sldb}  
  
set target_library  
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}  
  
read_verilog  
{FA.v,CSA2.v,CSA3.v,CSA4.v,CSA5.v,CSA6.v,CSA7.v,CSA8.v,CSA9.v,CS  
A10.v,CSA11.v,CSA64UEQG.v}  
  
current_design CSA64UEQG  
  
check_design  
  
create_clock clock -name clock -period 8.00000  
  
set_propagated_clock clock  
  
set_clock_uncertainty 0.25 clock  
  
set_propagated_clock clock  
  
set_fix_hold [ get_clocks clock ]  
  
compile -map_effort medium -incremental_mapping  
  
update_timing  
  
set_max_area 3200  
  
report -cell  
  
report_timing -max_paths 5
```

```
report_area  
report_power  
write -hierarchy -format verilog -output CSA64UEQG_nl.v  
quit
```

Commands

Simulation command

- vcs +v2k -gui design_file.v tb.v
- ./simv -gui
- vcs +v2k -debug_all -gui -y /apps/toshiba/sjsu/verilog/tc240c +libext+.tsbvlibp tb.v
design_netlist.v
- dc_shell -f synthesis.script | tee log.txt
- design_vision & DVE

Appendix B

Completed Verilog Source Codes and Testbenches

Verilog Code RCA64

```
'timescale 1ns/10ps
```

Half Adder Block

```
module HA(sum_ha, cout_ha, op1_ha, op2_ha);
output sum_ha, cout_ha;
input op1_ha, op2_ha;
assign sum_ha = op1_ha ^ op2_ha;
assign cout_ha = op1_ha & op2_ha;
endmodule
```

1-bit full adder block

```
module FA_1bit(sum_fa1, cout_fa1, op1_fa1, op2_fa1, cin);
output sum_fa1, cout_fa1;
input op1_fa1, op2_fa1, cin;
wire s1, c1, c2;

HA h1(.sum_ha(s1), .cout_ha(c1), .op1_ha(op1_fa1), .op2_ha(op2_fa1));
HA h2(.sum_ha(sum_fa1), .cout_ha(c2), .op1_ha(s1), .op2_ha(cin));

assign cout_fa1 = c1 | c2;
endmodule
```

4-bit full adder 1st block

```
module FA_4bit_1(sum_fa4, cout_fa4, op1_fa4, op2_fa4);
output [3:0]sum_fa4;
output cout_fa4;
input [3:0]op1_fa4;
input [3:0]op2_fa4;
wire cin1, cin2, cin3;

HA h1(.sum_ha(sum_fa4[0]), .cout_ha(cin1), .op1_ha(op1_fa4[0]), .op2_ha(op2_fa4[0]));
```

```

FA_1bit
f1(.sum_fa1(sum_fa4[1]), .cout_fa1(cin2), .op1_fa1(op1_fa4[1]), .op2_fa1(op2_fa4[1]), .cin(cin
1));
FA_1bit
f2(.sum_fa1(sum_fa4[2]), .cout_fa1(cin3), .op1_fa1(op1_fa4[2]), .op2_fa1(op2_fa4[2]), .cin(cin
2));
FA_1bit
f3(.sum_fa1(sum_fa4[3]), .cout_fa1(cout_fa4), .op1_fa1(op1_fa4[3]), .op2_fa1(op2_fa4[3]), .cin
(cin3));

endmodule

```

4-bit full adder 2nd block

```

module FA_4bit_2(sum_fa4_2, cout_fa4_2, op1_fa4_2, op2_fa4_2, cin_fa4);
output [3:0]sum_fa4_2;
output cout_fa4_2;
input [3:0]op1_fa4_2;
input [3:0]op2_fa4_2;
input cin_fa4;
wire cin1, cin2, cin3;

FA_1bit
f1(.sum_fa1(sum_fa4_2[0]), .cout_fa1(cin1), .op1_fa1(op1_fa4_2[0]), .op2_fa1(op2_fa4_2[0]), .
cin(cin_fa4));
FA_1bit
f2(.sum_fa1(sum_fa4_2[1]), .cout_fa1(cin2), .op1_fa1(op1_fa4_2[1]), .op2_fa1(op2_fa4_2[1]), .
cin(cin1));
FA_1bit
f3(.sum_fa1(sum_fa4_2[2]), .cout_fa1(cin3), .op1_fa1(op1_fa4_2[2]), .op2_fa1(op2_fa4_2[2]), .
cin(cin2));
FA_1bit
f4(.sum_fa1(sum_fa4_2[3]), .cout_fa1(cout_fa4_2), .op1_fa1(op1_fa4_2[3]), .op2_fa1(op2_fa4_
2[3]), .cin(cin3));

endmodule

```

64 Bit Ripple Carry Adder

```

module RCA64(sum, crout, op1, op2, clock, reset);
output [63:0]sum;
output crout;
input [63:0]op1;
input [63:0]op2;
input clock, reset;
reg [63:0]sum;
reg crout;

```

```

reg [63:0]op1f;
reg [63:0]op2f;
wire c1, c2, c3, c4, c5, c6, c7, c8, c9, c10, c11, c12, c13, c14, c15, croutf;
wire [63:0]sumf;

FA_4bit_1 F1(.sum_fa4(sumf[3:0]), .cout_fa4(c1), .op1_fa4(op1f[3:0]), .op2_fa4(op2f[3:0]));
FA_4bit_2
F2(.sum_fa4_2(sumf[7:4]), .cout_fa4_2(c2), .op1_fa4_2(op1f[7:4]), .op2_fa4_2(op2f[7:4]), .cin_fa4(c1));
FA_4bit_2
F3(.sum_fa4_2(sumf[11:8]), .cout_fa4_2(c3), .op1_fa4_2(op1f[11:8]), .op2_fa4_2(op2f[11:8]), .cin_fa4(c2));
FA_4bit_2
F4(.sum_fa4_2(sumf[15:12]), .cout_fa4_2(c4), .op1_fa4_2(op1f[15:12]), .op2_fa4_2(op2f[15:12]), .cin_fa4(c3));
FA_4bit_2
F5(.sum_fa4_2(sumf[19:16]), .cout_fa4_2(c5), .op1_fa4_2(op1f[19:16]), .op2_fa4_2(op2f[19:16]), .cin_fa4(c4));
FA_4bit_2
F6(.sum_fa4_2(sumf[23:20]), .cout_fa4_2(c6), .op1_fa4_2(op1f[23:20]), .op2_fa4_2(op2f[23:20]), .cin_fa4(c5));
FA_4bit_2
F7(.sum_fa4_2(sumf[27:24]), .cout_fa4_2(c7), .op1_fa4_2(op1f[27:24]), .op2_fa4_2(op2f[27:24]), .cin_fa4(c6));
FA_4bit_2
F8(.sum_fa4_2(sumf[31:28]), .cout_fa4_2(c8), .op1_fa4_2(op1f[31:28]), .op2_fa4_2(op2f[31:28]), .cin_fa4(c7));
FA_4bit_2
F9(.sum_fa4_2(sumf[35:32]), .cout_fa4_2(c9), .op1_fa4_2(op1f[35:32]), .op2_fa4_2(op2f[35:32]), .cin_fa4(c8));
FA_4bit_2
F10(.sum_fa4_2(sumf[39:36]), .cout_fa4_2(c10), .op1_fa4_2(op1f[39:36]), .op2_fa4_2(op2f[39:36]), .cin_fa4(c9));
FA_4bit_2
F11(.sum_fa4_2(sumf[43:40]), .cout_fa4_2(c11), .op1_fa4_2(op1f[43:40]), .op2_fa4_2(op2f[43:40]), .cin_fa4(c10));
FA_4bit_2
F12(.sum_fa4_2(sumf[47:44]), .cout_fa4_2(c12), .op1_fa4_2(op1f[47:44]), .op2_fa4_2(op2f[47:44]), .cin_fa4(c11));
FA_4bit_2
F13(.sum_fa4_2(sumf[51:48]), .cout_fa4_2(c13), .op1_fa4_2(op1f[51:48]), .op2_fa4_2(op2f[51:48]), .cin_fa4(c12));
FA_4bit_2
F14(.sum_fa4_2(sumf[55:52]), .cout_fa4_2(c14), .op1_fa4_2(op1f[55:52]), .op2_fa4_2(op2f[55:52]), .cin_fa4(c13));

```

```

FA_4bit_2
F15(.sum_fa4_2(sumf[59:56]), .cout_fa4_2(c15), .op1_fa4_2(op1f[59:56]), .op2_fa4_2(op2f[59:
56]), .cin_fa4(c14));
FA_4bit_2
F16(.sum_fa4_2(sumf[63:60]), .cout_fa4_2(croutf), .op1_fa4_2(op1f[63:60]), .op2_fa4_2(op2f[6
3:60]), .cin_fa4(c15));

always @(posedge clock or posedge reset)
begin
if(reset == 1)
begin
op1f <= 64'b0;
op2f <= 64'b0;
sum <= 64'b0;
crout <= 64'b0;
end

else
begin
op1f <= op1;
$display ("op1f= %h",op1f);
op2f <= op2;
$display ("op2f= %h",op2f);
sum <= sumf;
$display ("sumf= %h",sumf);
crout <= croutf;
$display ("croutf= %h",croutf);
end
end
endmodule

```

Testbench RCA64

CASE #1

```

`timescale 1 ns/ 10 ps
module RCA64_tb();
reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
RCA64 A (sum,crout,op1,op2,clock,reset);

```

```

initial begin

    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b1;

    #4;
    op1= 64'hf20f_ffff_ffff_ffff;
    op2= 64'hffff_ffff_ffff_ff50;

end
initial begin
    reset= 1'b1;
    #4;
    reset= 1'b0;

end

initial begin

    forever #12 clock=~clock;
end
initial begin
    #60;
    $finish;
end
initial begin
    $dumpfile("RCA64.vcd");
    $dumpvars(0,RCA64_tb);
end
endmodule

```

CASE #2

```

`timescale 1 ns/ 10 ps
module RCA64_tb_1();

reg [63:0]op1;
reg [63:0]op2;
reg clock;

```

```

reg reset;
wire [63:0]sum;
wire crout;
RCA64 A (sum,crout,op1,op2,clock,reset);

initial begin

    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b1;

    #4;
    op1= 64'h1010_1010_1199_ffff;
    op2= 64'habcd_1100_1100_dddd;

    end
initial begin
    reset= 1'b1;
    #4;
    reset= 1'b0;

end

initial begin
    forever #12 clock=~clock;
end
initial begin
    #60;
    $finish;
end
initial begin
    $dumpfile("RCA64_1.vcd");
    $dumpvars(0,RCA64_tb_1);
end
endmodule

```

CASE #3

```

`timescale 1 ns/ 10 ps
module RCA64_tb_2();

```

```

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;

```

```

RCA64 A (sum,crout,op1,op2,clock,reset);

initial begin

    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b1;

    #4;
    op1= 64'hffff_ffff_ffff_ffff;
    op2= 64'heeee_dddd_cccc_ffff;

    end
initial begin
    reset= 1'b1;
    #4;
    reset= 1'b0;

end

initial begin
    forever #12 clock=~clock;
end
initial begin
    #60;
    $finish;
end
initial begin
    $dumpfile("RCA64_2.vcd");
    $dumpvars(0,RCA64_tb_2);
end
endmodule

```

CASE #4

```

`timescale 1 ns/ 10 ps
module RCA64_tb_3();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
RCA64 A (sum,crout,op1,op2,clock,reset);

```

```

initial begin
    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b1;

    #4;
    op1= 64'hbbbb_cdc_d_aaaa_1111;
    op2= 64'hffff_ffff_ffff_dddd;

    end
initial begin
    reset= 1'b1;
    #4;
    reset= 1'b0;
end

initial begin
    forever #12 clock=~clock;
end
initial begin
    #60;
    $finish;
end
initial begin
    $dumpfile("RCA64_3.vcd");
    $dumpvars(0,RCA64_tb_3);
end
endmodule

```

CASE #5

```

`timescale 1 ns/ 10 ps
module RCA64_tb_4();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
RCA64 A (sum,crout,op1,op2,clock,reset);

initial begin

```

```

op1= 64'b0;
op2= 64'b0;
clock= 1'b1;

#4;
op1= 64'h0000_0000_1234_5678;
op2= 64'h0000_0000_90ab_cdef;

end
initial begin
  reset= 1'b1;
  #4;
  reset= 1'b0;

end

initial begin
  forever #12 clock=~clock;
end
initial begin
  #60;
  $finish;
end
initial begin
  $dumpfile("RCA64_4.vcd");
  $dumpvars(0,RCA64_tb_4);
end
endmodule

```

CASE #6

```

`timescale 1 ns/ 10 ps
module RCA64_tb_5();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
RCA64 A (sum,crout,op1,op2,clock,reset);

initial begin

```

```
  op1= 64'b0;
```

```
op2= 64'b0;
clock= 1'b1;

#4;
op1= 64'h1234_ffff_dfff_eeee;
op2= 64'hdddd_dddd_dddd_dddd;

end
initial begin
    reset= 1'b1;
    #4;
    reset= 1'b0;

end

initial begin
    forever #12 clock=~clock;
end
initial begin
    #60;
    $finish;
end
initial begin
    $dumpfile("RCA64_5.vcd");
    $dumpvars(0,RCA64_tb_5);
end
endmodule
```

Verilog Code CLA64

4-bit block

```
'timescale 1ns/10ps
```

```
module CLA4(sum,crout,P1,G1,op1,op2);
output [3:0]sum;
output crout;
output P1,G1;
input [3:0] op1,op2;
wire [3:0]G,P,C;

assign G = op1 & op2; //Generate
assign P = op1 ^ op2; //Propagate
assign C[0] = 0;
assign C[1] = G[0] | (P[0] & C[0]);
assign C[2] = G[1] | (P[1] & G[0]) | (P[1] & P[0] & C[0]);
assign C[3] = G[2] | (P[2] & G[1]) | (P[2] & P[1] & G[0]) | (P[2] & P[1] & P[0] & C[0]);
assign crout = G[3] | (P[3] & G[2]) | (P[3] & P[2] & G[1]) | (P[3] & P[2] & P[1] & G[0])
|(P[3] & P[2] & P[1] & P[0] & C[0]);
assign sum = P ^ C;

assign P1 = P[3] & P[2] & P[1] & P[0];
assign G1 = G[3] | (P[3] & G[2]) | (P[3] & P[2] & G[1]) | (P[3] & P[2] & P[1] & G[0]);
endmodule
```

2nd 4-bit block

```
'timescale 1ns/10ps
```

```
module CLA4_2(sum,crout,P2,G2,op1,op2,Cin);
output [3:0] sum;
output crout;
output P2,G2;
input [3:0]op1,op2;
input Cin;
wire [3:0]G,P,C;

assign G = op1 & op2; //Generate
assign P = op1 ^ op2; //Propagate
assign C[0] = Cin;
assign C[1] = G[0] | (P[0] & C[0]);
assign C[2] = G[1] | (P[1] & G[0]) | (P[1] & P[0] & C[0]);
assign C[3] = G[2] | (P[2] & G[1]) | (P[2] & P[1] & G[0]) | (P[2] & P[1] & P[0] & C[0]);
assign crout = G[3] | (P[3] & G[2]) | (P[3] & P[2] & G[1]) | (P[3] & P[2] & P[1] & G[0])
|(P[3] & P[2] & P[1] & P[0] & C[0]);
```

```

assign sum = P ^ C;

assign P2 = P[3] & P[2] & P[1] & P[0];
assign G2 = G[3] | (P[3] & G[2]) | (P[3] & P[2] & G[1]) | (P[3] & P[2] & P[1] & G[0]);
endmodule

```

1st 16-bit block

```
'timescale 1ns/10ps
```

```

module CLA16(sum_4,crout,op1_4,op2_4);
output [15:0]sum_4;
output crout;
input [15:0]op1_4,op2_4;
wire [15:0]sum_4;
wire p1,p2,p3;
wire [3:0]G,P;

CLA4 C1(.sum(sum_4[3:0]),.crout(p1),.P1(P[0]),.G1(G[0]),.op1(op1_4[3:0]),.op2(op2_4[3:0]));
CLA4_2
C2(.sum(sum_4[7:4]),.crout(p2),.P2(P[1]),.G2(G[1]),.op1(op1_4[7:4]),.op2(op2_4[7:4]),.Cin(p1)
);
CLA4_2
C3(.sum(sum_4[11:8]),.crout(p3),.P2(P[2]),.G2(G[2]),.op1(op1_4[11:8]),.op2(op2_4[11:8]),.Cin
(p2));
CLA4_2
C4(.sum(sum_4[15:12]),.crout(),.P2(P[3]),.G2(G[3]),.op1(op1_4[15:12]),.op2(op2_4[15:12]),.Ci
n(p3));

assign crout = G[3] | (G[2] & P[3]) | (G[1] & P[2] & P[3]) | (G[0] & P[1] & P[2] & P[3]);
endmodule

```

2nd 16-bit block

```
'timescale 1ns/10ps
```

```

module CLA16_2(sum_16,crout_16,op1_16,op2_16,Cin);
output [15:0]sum_16;
output crout_16;
input [15:0]op1_16,op2_16;
input Cin;
wire p1,p2,p3;
wire [3:0]G,P;

CLA4_2          A1(.sum(sum_16[3:0]),.crout(p1),           .P2(P[0]),           .G2(G[0]),
.op1(op1_16[3:0]),.op2(op2_16[3:0]),.Cin(Cin));

```

```

CLA4_2      A2(.sum(sum_16[7:4]),.crout(p2),    .P2(P[1]),.G2(G[1]),    .op1(op1_16[7:4]),
            .op2(op2_16[7:4]),.Cin(p1));
CLA4_2      A3(.sum(sum_16[11:8]),.crout(p3),   .P2(P[2]),.G2(G[2]),    .op1(op1_16[11:8]),
            .op2(op2_16[11:8]),.Cin(p2));
CLA4_2      A4(.sum(sum_16[15:12]),.crout(),     .P2(P[3]),.G2(G[3]),    .op1(op1_16[15:12]),
            .op2(op2_16[15:12]),.Cin(p3));

assign crout_16 = G[3] | (G[2] & P[3]) | (G[1] & P[2] & P[3]) | (G[0] & P[1] & P[2] & P[3]) |
        (Cin & P[0] & P[1] & P[2] & P[3]) ;

endmodule

```

64 bit CLA

```
`timescale 1ns/10ps
```

```

module CLA_64(sum, crout, op1, op2, clock, reset);
output [63:0]sum;
output crout;
input [63:0]op1;
input [63:0]op2;
input clock, reset;
reg [63:0]sum;
reg crout;
reg [63:0]op1f;
reg [63:0]op2f;
wire c1, c2, c3, croutf;
wire [63:0]sumf;

CLA16 A1(.sum_4(sum_f[15:0]), .crout(c1), .op1_4(op1_f[15:0]), .op2_4(op2_f[15:0]));
CLA16_2      A2(.sum_16(sum_f[31:16]),       .crout_16(c2),       .op1_16(op1_f[31:16]),
            .op2_16(op2_f[31:16]),.Cin(c1));
CLA16_2      A3(.sum_16(sum_f[47:32]),       .crout_16(c3),       .op1_16(op1_f[47:32]),
            .op2_16(op2_f[47:32]),.Cin(c2));
CLA16_2      A4(.sum_16(sum_f[63:48]),       .crout_16(croutf),   .op1_16(op1_f[63:48]),
            .op2_16(op2_f[63:48]),.Cin(c3));

```

```
always @(posedge clock or posedge reset)
```

```

begin
if(reset == 1)
begin
op1f <= 64'b0;
op2f <= 64'b0;
sum <= 64'b0;

crout <= 64'b0;
end

```

```

else
begin
op1f <= op1;
$display ("op1f= %h",op1f);
op2f <= op2;
$display ("op2f= %h",op2f);
sum <= sumf;
$display ("sumf= %h",sumf);
croutf <= croutf;
$display ("croutf= %h",croutf);
end
end

endmodule

```

Testbench CLA64

CASE #1

```

`timescale 1 ns/ 10 ps
module CLA_64_tb();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CLA_64 A (sum,crout,op1,op2,clock,reset);

initial begin

    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b0;

    #5;
    op1= 64'hf20f_ffff_ffff_ffff;
    op2= 64'hffff_ffff_ffff_ff50;
end
initial begin
    reset= 1'b1;
    #6;
    reset= 1'b0;
end

```

```

initial begin
    forever #4 clock=~clock;
end
initial begin
    #30;
    $finish;
end
initial begin
    $dumpfile("CLA_64.vcd");
    $dumpvars(0,CLA_64_tb);
end
endmodule

```

CASE #2

```

`timescale 1 ns/ 10 ps
module CLA_64_tb_1();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CLA_64 A (sum,crout,op1,op2,clock,reset);

initial begin

    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b0;

    #5;
    op1= 64'h1010_1010_1199_ffff;
    op2= 64'habcd_1100_1100_dddd;

end
initial begin
    reset= 1'b1;
    #6;
    reset= 1'b0;

end
initial begin

```

```

    forever #4 clock=~clock;
end
initial begin
#30;
$finish;
end
initial begin
$dumpfile("CLA_64_1.vcd");
$dumpvars(0,CLA_64_tb_1);
end
endmodule

```

CASE #3

```

`timescale 1 ns/ 10 ps
module CLA_64_tb_2();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CLA_64 A (sum,crout,op1,op2,clock,reset);

initial begin

op1= 64'b0;
op2= 64'b0;
clock= 1'b0;

#5;
op1= 64'hffff_ffff_ffff_ffff;
op2= 64'heeee_dddd_cccc_ffff;

end
initial begin
reset= 1'b1;
#6;
reset= 1'b0;

end

initial begin
forever #4 clock=~clock;
end
initial begin

```

```
#30;
$finish;
end
initial begin
$dumpfile("CLA_64_2.vcd");
$dumpvars(0,CLA_64_tb_2);
end
endmodule
```

CASE #4

```
'timescale 1 ns/ 10 ps
module CLA_64_tb_3();
reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CLA_64 A (sum,crout,op1,op2,clock,reset);

initial begin
op1= 64'b0;
op2= 64'b0;
clock= 1'b0;

#5;
op1= 64'hbbbb_cdcdaaaa_1111;
op2= 64'hffff_ffff_ffff_dddd;

end
initial begin
reset= 1'b1;
#6;
reset= 1'b0;

end

initial begin
forever #4 clock=~clock;
end
initial begin
#30;
$finish;
end
```

```

initial begin
$dumpfile("CLA_64_3.vcd");
$dumpvars(0,CLA_64_tb_3);
end
endmodule

```

CASE #5

```

`timescale 1 ns/ 10 ps
module CLA_64_tb_4();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CLA_64 A (sum,crout,op1,op2,clock,reset);

initial begin

op1= 64'b0;
op2= 64'b0;
clock= 1'b0;

#5;
op1= 64'h1234_5678_90ab_cdef;
op2= 64'h5555_5555_5555_dddd;

end
initial begin
reset= 1'b1;
#6;
reset= 1'b0;

end

initial begin
forever #4 clock=~clock;
end
initial begin
#30;
$finish;
end
initial begin
$dumpfile("CLA_64_4.vcd");
$dumpvars(0,CLA_64_tb_4);

```

```
end
endmodule
```

CASE #6

```
'timescale 1 ns/ 10 ps
module CLA_64_tb_5();
reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CLA_64 A (sum,crout,op1,op2,clock,reset);

initial begin
    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b0;
    #5;
    op1= 64'h1234_ffff_dfff_eeee;
    op2= 64'hdddd_dddd_dddd_dddd;
end
initial begin
    reset= 1'b1;
    #6;
    reset= 1'b0;
end
initial begin
    forever #4 clock=~clock;
end
initial begin
    #40;
    $finish;
end
initial begin
    $dumpfile("CLA_64_5.vcd");
    $dumpvars(0,CLA_64_tb_5);
end
endmodule
```

Verilog Code CSA64 Equal Group

```
`timescale 1ns/10ps
```

1 bit full adder

```
module FA(sum_fa, cout_fa, op1_fa, op2_fa, cin);
output sum_fa, cout_fa;
input op1_fa, op2_fa, cin;

assign sum_fa = op1_fa ^ op2_fa ^ cin;
assign cout_fa = ((op1_fa ^ op2_fa) & cin) | (op1_fa & op2_fa);

endmodule
```

4 bit CSA

```
module CSA4(sum_4, cout_4, op1_4, op2_4, cin_4);
output [3:0]sum_4;
output cout_4;
input [3:0]op1_4,op2_4;
input cin_4;
wire [3:0]sum0,sum1;
wire cout0,cout1;
wire c1, c2, c3, c4, c5, c6;
//sum for carry 0

FA f1(.sum_fa(sum0[0]), .cout_fa(c1), .op1_fa(op1_4[0]), .op2_fa(op2_4[0]), .cin(1'b0));
FA f2(.sum_fa(sum0[1]), .cout_fa(c2), .op1_fa(op1_4[1]), .op2_fa(op2_4[1]), .cin(c1));
FA f3(.sum_fa(sum0[2]), .cout_fa(c3), .op1_fa(op1_4[2]), .op2_fa(op2_4[2]), .cin(c2));
FA f4(.sum_fa(sum0[3]), .cout_fa(cout0), .op1_fa(op1_4[3]), .op2_fa(op2_4[3]), .cin(c3));

//sum for carry 1

FA f5(.sum_fa(sum1[0]), .cout_fa(c4), .op1_fa(op1_4[0]), .op2_fa(op2_4[0]), .cin(1'b1));
FA f6(.sum_fa(sum1[1]), .cout_fa(c5), .op1_fa(op1_4[1]), .op2_fa(op2_4[1]), .cin(c4));
FA f7(.sum_fa(sum1[2]), .cout_fa(c6), .op1_fa(op1_4[2]), .op2_fa(op2_4[2]), .cin(c5));
FA f8(.sum_fa(sum1[3]), .cout_fa(cout1), .op1_fa(op1_4[3]), .op2_fa(op2_4[3]), .cin(c6));

mux_sum m1(.sum(sum_4), .sum0(sum0), .sum1(sum1), .Cin(cin_4));
mux_carry m2(.cout(cout_4), .cout0(cout0), .cout1(cout1), .Cin(cin_4));

endmodule
```

64 bit CSA

```

module CSA64EQG(sum, crout, op1, op2, clock, reset);
output [63:0]sum;
output crout;
input [63:0]op1;
input [63:0]op2;
input clock, reset;
reg [63:0]sum;
reg crout;
reg [63:0]op1f;
reg [63:0]op2f;
wire [63:0]sumf;
wire C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, croutf;

assign CIN = 0;

CSA4 s1(.sum_4(sumf[3:0]), .cout_4(C1), .op1_4(op1f[3:0]), .op2_4(op2f[3:0]), .cin_4(CIN));
CSA4 s2(.sum_4(sumf[7:4]), .cout_4(C2), .op1_4(op1f[7:4]), .op2_4(op2f[7:4]), .cin_4(C1));
CSA4 s3(.sum_4(sumf[11:8]), .cout_4(C3), .op1_4(op1f[11:8]), .op2_4(op2f[11:8]), .cin_4(C2));
CSA4 s4(.sum_4(sumf[15:12]), .cout_4(C4), .op1_4(op1f[15:12]), .op2_4(op2f[15:12]), .cin_4(C3));
CSA4 s5(.sum_4(sumf[19:16]), .cout_4(C5), .op1_4(op1f[19:16]), .op2_4(op2f[19:16]), .cin_4(C4));
CSA4 s6(.sum_4(sumf[23:20]), .cout_4(C6), .op1_4(op1f[23:20]), .op2_4(op2f[23:20]), .cin_4(C5));
CSA4 s7(.sum_4(sumf[27:24]), .cout_4(C7), .op1_4(op1f[27:24]), .op2_4(op2f[27:24]), .cin_4(C6));
CSA4 s8(.sum_4(sumf[31:28]), .cout_4(C8), .op1_4(op1f[31:28]), .op2_4(op2f[31:28]), .cin_4(C7));
CSA4 s9(.sum_4(sumf[35:32]), .cout_4(C9), .op1_4(op1f[35:32]), .op2_4(op2f[35:32]), .cin_4(C8));
CSA4 s10(.sum_4(sumf[39:36]), .cout_4(C10), .op1_4(op1f[39:36]), .op2_4(op2f[39:36]), .cin_4(C9));
CSA4 s11(.sum_4(sumf[43:40]), .cout_4(C11), .op1_4(op1f[43:40]), .op2_4(op2f[43:40]), .cin_4(C10));
CSA4 s12(.sum_4(sumf[47:44]), .cout_4(C12), .op1_4(op1f[47:44]), .op2_4(op2f[47:44]), .cin_4(C11));
CSA4 s13(.sum_4(sumf[51:48]), .cout_4(C13), .op1_4(op1f[51:48]), .op2_4(op2f[51:48]), .cin_4(C12));
CSA4 s14(.sum_4(sumf[55:52]), .cout_4(C14), .op1_4(op1f[55:52]), .op2_4(op2f[55:52]), .cin_4(C13));
CSA4 s15(.sum_4(sumf[59:56]), .cout_4(C15), .op1_4(op1f[59:56]), .op2_4(op2f[59:56]), .cin_4(C14));

```

```

CSA4 s16(.sum_4(sumf[63:60]), .cout_4(croutf), .op1_4(op1f[63:60]), .op2_4(op2f[63:60]),
.cin_4(C15));

always @(posedge clock or posedge reset)
begin
if(reset == 1)
begin
op1f <= 64'b0;
op2f <= 64'b0;
sum <= 64'b0;
crout <= 64'b0;
end

else
begin
op1f <= op1;
$display ("op1f= %h",op1f);
op2f <= op2;
$display ("op2f= %h",op2f);
sum <= sumf;
$display ("sumf= %h",sumf);
crout <= croutf;
$display ("croutf= %h",croutf);
end
end
endmodule

```

Carry Mux

```
`timescale 1ns/10ps
```

```

//mux for carry
module mux_carry(cout, cout0, cout1, Cin);
output cout;
input cout0, cout1, Cin;

assign cout = Cin ? cout1 : cout0;

endmodule

```

Sum Mux

```
`timescale 1ns/10ps
```

```

//mux for sum;
module mux_sum(sum, sum0, sum1, Cin);

```

```

output [3:0]sum;
input [3:0]sum0, sum1;
input Cin;

assign sum = Cin ? sum1 : sum0;

endmodule

```

Testbench CSA64 EQG

CASE #1

```

`timescale 1 ns/ 10 ps
module CSA64EQG_tb();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CSA64EQG A (sum,crout,op1,op2,clock,reset);

initial begin
    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b1;

    #4;
    op1= 64'hf20f_ffff_ffff_ffff;
    op2= 64'hffff_ffff_ffff_ff50;
end
initial begin
    reset= 1'b1;
    #4;
    reset= 1'b0;
end

initial begin
    forever #3 clock=~clock;
end
initial begin
    #30;

```

```

$finish;
end
initial begin
  $dumpfile("CSA64EQG.vcd");
  $dumpvars(0,CSA64EQG_tb);
end
endmodule

```

CASE #2

```

`timescale 1 ns/ 10 ps
module CSA64EQG_tb_1();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CSA64EQG A (sum,crout,op1,op2,clock,reset);

initial begin

  op1= 64'b0;
  op2= 64'b0;
  clock= 1'b1;

  #4;
  op1= 64'h1010_1010_1199_ffff;
  op2= 64'habcd_1100_1100_dddd;

end
initial begin
  reset= 1'b1;
  #4;
  reset= 1'b0;

end

initial begin
  forever #3 clock=~clock;
end
initial begin
  #30;
  $finish;

```

```

end
initial begin
$dumpfile("CSA64EQG_1.vcd");
$dumpvars(0,CSA64EQG_tb_1);
end
endmodule

```

CASE #3

```

`timescale 1 ns/ 10 ps
module CSA64EQG_tb_2();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CSA64EQG A (sum,crout,op1,op2,clock,reset);

initial begin
    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b1;

    #4;
    op1= 64'hffff_ffff_ffff_ffff;
    op2= 64'heeee_dddd_cccc_ffff;

    end
initial begin
    reset= 1'b1;
    #1;
    reset= 1'b0;
end

initial begin
    forever #3 clock=~clock;
end
initial begin
    #30;
    $finish;
end
initial begin

```

```
$dumpfile("CSA64EQG_2.vcd");
$dumpvars(0,CSA64EQG_tb_2);
end
endmodule
```

CASE #4

```
'timescale 1 ns/ 10 ps
module CSA64EQG_tb_3();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CSA64EQG A (sum,crout,op1,op2,clock,reset);

initial begin

    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b1;

    #4;
    op1= 64'hbbbb_cdcd_aaaa_1111;
    op2= 64'hffff_ffff_ffff_dddd;

    end
initial begin
    reset= 1'b1;
    #4;
    reset= 1'b0;

end

initial begin
    forever #3 clock=~clock;
end
initial begin
    #30;
    $finish;
end
initial begin
    $dumpfile("CSA64EQG_3.vcd");
    $dumpvars(0,CSA64EQG_tb_3);
```

```
end
endmodule
```

CASE #5

```
'timescale 1 ns/ 10 ps
module CSA64EQG_tb_4();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CSA64EQG A (sum,crout,op1,op2,clock,reset);

initial begin

    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b1;

    #4;
    op1= 64'h1234_5678_90ab_cdef;
    op2= 64'h5555_5555_5555_dddd;

end
initial begin
    reset= 1'b1;
    #4;
    reset= 1'b0;
end

initial begin
    forever #3 clock=~clock;
end
initial begin
    #30;
    $finish;
end
initial begin
    $dumpfile("CSA64EQG_4.vcd");
    $dumpvars(0,CSA64EQG_tb_4);
end
endmodule
```

CASE #6

```

`timescale 1 ns/ 10 ps
module CSA64EQG_tb_5();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CSA64EQG A (sum,crout,op1,op2,clock,reset);

initial begin

    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b1;

    #4;
    op1= 64'h1234_ffff_dfff_eeee;
    op2= 64'hdddd_dddd_dddd_dddd;

end
initial begin
    reset= 1'b1;
    #4;
    reset= 1'b0;
end

initial begin
    forever #3 clock=~clock;
end
initial begin
    #30;
    $finish;
end
initial begin
    $dumpfile("CSA64EQG_5.vcd");
    $dumpvars(0,CSA64EQG_tb_5);
end
endmodule

```

Verilog code of CSA 64 Unequal Group

64 bit Unequal Group Carry Select Adder

```
'timescale 1ns/10ps
```

```
module CSA64UEQG(sum, crout, op1, op2, clock, reset);
output [63:0]sum;
output crout;
input [63:0]op1;
input [63:0]op2;
input clock, reset;
reg [63:0]sum;
reg crout;
reg [63:0]op1f;
reg [63:0]op2f;
wire [63:0]sumf;
wire C1, C2, C3, C4, C5, C6, croutf;

assign Cin = 0;

CSA4 P1(.sum_4(sumf[3:0]), .cout_4(C1), .op1_4(op1f[3:0]), .op2_4(op2f[3:0]), .cin_4(Cin));
CSA4 P2(.sum_4(sumf[7:4]), .cout_4(C2), .op1_4(op1f[7:4]), .op2_4(op2f[7:4]), .cin_4(C1));

CSA5 P3(.s(sumf[12:8]), .co(C3), .a(op1f[12:8]), .b(op2f[12:8]), .in(C2));

CSA6 P4(.s6(sumf[18:13]), .co6(C4), .a6(op1f[18:13]), .b6(op2f[18:13]), .in6(C3));
CSA7 P5(.s7(sumf[25:19]), .co7(C5), .a7(op1f[25:19]), .b7(op2f[25:19]), .in7(C4));

CSA8 P6(.s8(sumf[33:26]), .co8(C6), .a8(op1f[33:26]), .b8(op2f[33:26]), .in8(C5));
CSA9 P7(.s9(sumf[42:34]), .co9(C7), .a9(op1f[42:34]), .b9(op2f[42:34]), .in9(C6));

CSA10 P8(.s10(sumf[52:43]), .co10(C8), .a10(op1f[52:43]), .b10(op2f[52:43]), .in10(C7));

CSA11 P9(.s11(sumf[63:53]), .co11(croutf), .a11(op1f[63:53]), .b11(op2f[63:53]), .in11(C8));

always @(posedge clock or posedge reset)
begin
if(reset == 1)
begin
op1f <= 64'b0;
op2f <= 64'b0;
```

```

sum <= 64'b0;
crout <= 64'b0;
end

else
begin
op1f <= op1;
$display ("op1f= %h",op1f);
op2f <= op2;
$display ("op2f= %h",op2f);
sum <= sumf;
$display ("sumf= %h",sumf);
crout <= croutf;
$display ("croutf= %h",croutf);
end
end
endmodule

```

Full Adder

```
'timescale 1ns/10ps
```

```

//1 bit fulladder
module FA(sum_fa, cout_fa, op1_fa, op2_fa, cin);
output sum_fa, cout_fa;
input op1_fa, op2_fa, cin;

assign sum_fa = op1_fa ^ op2_fa ^ cin;
assign cout_fa = ((op1_fa ^ op2_fa) & cin) | (op1_fa & op2_fa);

endmodule

```

2 bit CSA

```
'timescale 1ns/10ps
```

```

module CSA2(sum_2, cout_2, op1_2, op2_2, cin_2);
output [1:0]sum_2;
output cout_2;
input [1:0]op1_2,op2_2;
input cin_2;
wire [1:0]sum0,sum1;
wire cout0, cout1;
wire crout1, crout2;

//sum for carry 0

```

```

FA f1(.sum_fa(sum0[0]), .cout_fa(crout1), .op1_fa(op1_2[0]), .op2_fa(op2_2[0]), .cin(1'b0));
FA f2(.sum_fa(sum0[1]), .cout_fa(cout0), .op1_fa(op1_2[1]), .op2_fa(op2_2[1]), .cin(crout1));

//sum for carry 1
FA f3(.sum_fa(sum1[0]), .cout_fa(crout2), .op1_fa(op1_2[0]), .op2_fa(op2_2[0]), .cin(1'b1));
FA f4(.sum_fa(sum1[1]), .cout_fa(cout1), .op1_fa(op1_2[1]), .op2_fa(op2_2[1]), .cin(crout2));

assign sum_2 = cin_2 ? sum1 : sum0;
assign cout_2 = cin_2 ? cout1 : cout0;
endmodule

```

3 bit CSA

```
'timescale 1ns/10ps
```

```

module CSA3(sum_3, cout_3, op1_3, op2_3, cin_3);
output [2:0]sum_3;
output cout_3;
input [2:0]op1_3,op2_3;
input cin_3;
wire [2:0]sum0,sum1;
wire cout0, cout1;
wire c1, c2, c3, c4;

//sum for carry 0
FA s1(.sum_fa(sum0[0]), .cout_fa(c1), .op1_fa(op1_3[0]), .op2_fa(op2_3[0]), .cin(1'b0));
FA s2(.sum_fa(sum0[1]), .cout_fa(c2), .op1_fa(op1_3[1]), .op2_fa(op2_3[1]), .cin(c1));
FA s3(.sum_fa(sum0[2]), .cout_fa(cout0), .op1_fa(op1_3[2]), .op2_fa(op2_3[2]), .cin(c2));

//sum for carry 1
FA s4(.sum_fa(sum1[0]), .cout_fa(c3), .op1_fa(op1_3[0]), .op2_fa(op2_3[0]), .cin(1'b1));
FA s5(.sum_fa(sum1[1]), .cout_fa(c4), .op1_fa(op1_3[1]), .op2_fa(op2_3[1]), .cin(c3));
FA s6(.sum_fa(sum1[2]), .cout_fa(cout1), .op1_fa(op1_3[2]), .op2_fa(op2_3[2]), .cin(c4));

assign sum_3 = cin_3 ? sum1 : sum0;
assign cout_3 = cin_3 ? cout1 : cout0;
endmodule

```

4 bit CSA

```
'timescale 1ns/10ps
```

```

module CSA4(sum_4, cout_4, op1_4, op2_4, cin_4);
output [3:0]sum_4;
output cout_4;
input [3:0]op1_4,op2_4;

```

```

input cin_4;
wire [3:0]sum0,sum1;
wire cout0, cout1;
wire c1, c2, c3, c4, c5, c6;
//sum for carry 0

FA f1(.sum_fa(sum0[0]), .cout_fa(c1), .op1_fa(op1_4[0]), .op2_fa(op2_4[0]), .cin(1'b0));
FA f2(.sum_fa(sum0[1]), .cout_fa(c2), .op1_fa(op1_4[1]), .op2_fa(op2_4[1]), .cin(c1));
FA f3(.sum_fa(sum0[2]), .cout_fa(c3), .op1_fa(op1_4[2]), .op2_fa(op2_4[2]), .cin(c2));
FA f4(.sum_fa(sum0[3]), .cout_fa(cout0), .op1_fa(op1_4[3]), .op2_fa(op2_4[3]), .cin(c3));

//sum for carry 1

FA f5(.sum_fa(sum1[0]), .cout_fa(c4), .op1_fa(op1_4[0]), .op2_fa(op2_4[0]), .cin(1'b1));
FA f6(.sum_fa(sum1[1]), .cout_fa(c5), .op1_fa(op1_4[1]), .op2_fa(op2_4[1]), .cin(c4));
FA f7(.sum_fa(sum1[2]), .cout_fa(c6), .op1_fa(op1_4[2]), .op2_fa(op2_4[2]), .cin(c5));
FA f8(.sum_fa(sum1[3]), .cout_fa(cout1), .op1_fa(op1_4[3]), .op2_fa(op2_4[3]), .cin(c6));

assign sum_4 = cin_4 ? sum1 : sum0;
assign cout_4 = cin_4 ? cout1 : cout0;
endmodule

```

5 bit CSA

```
`timescale 1ns/10ps
```

```

module CSA5(s,co,a,b,in);
output [4:0]s;
output co;
input [4:0]a,b;
input in;
wire [4:0]s;
wire c1;

CSA2 D1(.sum_2(s[1:0]),.cout_2(c1),.op1_2(a[1:0]),.op2_2(b[1:0]),.cin_2(in));
CSA3 D2(.sum_3(s[4:2]),.cout_3(co),.op1_3(a[4:2]),.op2_3(b[4:2]),.cin_3(c1));

endmodule

```

6 bit CSA

```
`timescale 1ns/10ps
```

```

module CSA6(s6,co6,a6,b6,in6);
output [5:0]s6;
output co6;

```

```

input [5:0]a6,b6;
input in6;
wire [5:0]s6;
wire c1;

CSA3 E1(.sum_3(s6[2:0]),.cout_3(c1),.op1_3(a6[2:0]),.op2_3(b6[2:0]),.cin_3(in6));
CSA3 E2(.sum_3(s6[5:3]),.cout_3(co6),.op1_3(a6[5:3]),.op2_3(b6[5:3]),.cin_3(c1));
endmodule

```

7 bit CSA

```
`timescale 1ns/10ps
```

```

module CSA7(s7,co7,a7,b7,in7);
output [6:0]s7;
output co7;
input [6:0]a7,b7;
input in7;
wire [6:0]s6;
wire c1;

```

```

CSA3 J1(.sum_3(s7[2:0]),.cout_3(c1),.op1_3(a7[2:0]),.op2_3(b7[2:0]),.cin_3(in7));
CSA4 J2(.sum_4(s7[6:3]),.cout_4(co7),.op1_4(a7[6:3]),.op2_4(b7[6:3]),.cin_4(c1));
endmodule

```

8 bit CSA

```
`timescale 1ns/10ps
```

```

module CSA8(s8,co8,a8,b8,in8);
output [7:0]s8;
output co8;
input [7:0]a8,b8;
input in8;
wire [7:0]s8;
wire c1;

```

```

CSA4 T1(.sum_4(s8[3:0]),.cout_4(c1),.op1_4(a8[3:0]),.op2_4(b8[3:0]),.cin_4(in8));
CSA4 T2(.sum_4(s8[7:4]),.cout_4(co8),.op1_4(a8[7:4]),.op2_4(b8[7:4]),.cin_4(c1));
endmodule

```

9 bit CSA

```
`timescale 1ns/10ps
```

```
module CSA9(s9,co9,a9,b9,in9);
```

```

output [8:0]s9;
output co9;
input [8:0]a9,b9;
input in9;
wire [8:0]s9;
wire c1,c2;

CSA3 V1(.sum_3(s9[2:0]),.cout_3(c1),.op1_3(a9[2:0]),.op2_3(b9[2:0]),.cin_3(in9));
CSA3 V2(.sum_3(s9[5:3]),.cout_3(c2),.op1_3(a9[5:3]),.op2_3(b9[5:3]),.cin_3(c1));
CSA3 V3(.sum_3(s9[8:6]),.cout_3(co9),.op1_3(a9[8:6]),.op2_3(b9[8:6]),.cin_3(c2));

endmodule

```

10 bit CSA

```
`timescale 1ns/10ps
```

```

module CSA10(s10,co10,a10,b10,in10);
output [9:0]s10;
output co10;
input [9:0]a10,b10;
input in10;
wire [9:0]s10;
wire c1,c2;

CSA2 J1(.sum_2(s10[1:0]),.cout_2(c1),.op1_2(a10[1:0]),.op2_2(b10[1:0]),.cin_2(in10));
CSA4 J2(.sum_4(s10[5:2]),.cout_4(c2),.op1_4(a10[5:2]),.op2_4(b10[5:2]),.cin_4(c1));
CSA4 J3(.sum_4(s10[9:6]),.cout_4(co10),.op1_4(a10[9:6]),.op2_4(b10[9:6]),.cin_4(c2));

endmodule

```

11 bit CSA

```
`timescale 1ns/10ps
```

```

module CSA11(s11,co11,a11,b11,in11);
output [10:0]s11;
output co11;
input [10:0]a11,b11;
input in11;
wire [10:0]s11;
wire c1,c2;

CSA3 R1(.sum_3(s11[2:0]),.cout_3(c1),.op1_3(a11[2:0]),.op2_3(b11[2:0]),.cin_3(in11));
CSA4 R2(.sum_4(s11[6:3]),.cout_4(c2),.op1_4(a11[6:3]),.op2_4(b11[6:3]),.cin_4(c1));
CSA4 R3(.sum_4(s11[10:7]),.cout_4(co11),.op1_4(a11[10:7]),.op2_4(b11[10:7]),.cin_4(c2));

```

```
endmodule
```

TESTBENCH of CSA Unequal Group

CASE #1

```
'timescale 1 ns/ 10 ps
module CSA64UEQG_tb();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CSA64UEQG A (sum,crout,op1,op2,clock,reset);

initial begin

    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b1;

    #4;
    op1= 64'hf20f_ffff_ffff_ffff;
    op2= 64'hffff_ffff_ffff_ff50;
end
initial begin
    reset= 1'b1;
    #4;
    reset= 1'b0;
end

initial begin
    forever #3 clock=~clock;
end
initial begin
    #30;
    $finish;
end
initial begin
    $dumpfile("CSA64UEQG.vcd");
    $dumpvars(0,CSA64UEQG_tb);
end
```

```
endmodule
```

CASE #2

```
'timescale 1 ns/ 10 ps
module CSA64UEQG_tb_1();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CSA64UEQG A (sum,crout,op1,op2,clock,reset);

initial begin

op1= 64'b0;
op2= 64'b0;
clock= 1'b1;

#4;
op1= 64'h1010_1010_1199_ffff;
op2= 64'habcd_1100_1100_dddd;

end
initial begin
reset= 1'b1;
#4;
reset= 1'b0;
end

initial begin
forever #3 clock=~clock;
end
initial begin
#30;
$finish;
end
initial begin
$dumpfile("CSA64UEQG_1.vcd");
$dumpvars(0,CSA64UEQG_tb_1);
end
endmodule
```

CASE #3

```
'timescale 1 ns/ 10 ps
module CSA64UEQG_tb_2();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CSA64UEQG A (sum,crout,op1,op2,clock,reset);

initial begin

    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b1;

    #2;
    op1= 64'hffff_ffff_ffff_ffff;
    op2= 64'heeee_dddd_cccc_ffff;

    end
initial begin
    reset= 1'b1;
    #4;
    reset= 1'b0;

end

initial begin
    forever #3 clock=~clock;
end
initial begin
    #30;
    $finish;
end
initial begin
    $dumpfile("CSA64UEQG_2.vcd");
    $dumpvars(0,CSA64UEQG_tb_2);
end
endmodule
```

CASE #4

```

`timescale 1 ns/ 10 ps
module CSA64UEQG_tb_3();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CSA64UEQG A (sum,crout,op1,op2,clock,reset);

initial begin

    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b1;

    #4;
    op1= 64'hbbbb_cdc_d_aaaa_1111;
    op2= 64'hffff_ffff_ffff_dddd;

    end
initial begin
    reset= 1'b1;
    #4;
    reset= 1'b0;
end

initial begin
    forever #3 clock=~clock;
end
initial begin
    #30;
    $finish;
end
initial begin
    $dumpfile("CSA64UEQG_3.vcd");
    $dumpvars(0,CSA64UEQG_tb_3);
end
endmodule

```

CASE #5

```
`timescale 1 ns/ 10 ps
```

```

module CSA64UEQG_tb_4();

reg [63:0]op1;
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CSA64UEQG A (sum,crout,op1,op2,clock,reset);

initial begin

    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b1;

    #2;
    op1= 64'h1234_5678_90ab_cdef;
    op2= 64'h5555_5555_5555_dddd;

end
initial begin
    reset= 1'b1;
    #4;
    reset= 1'b0;
end

initial begin
    forever #3 clock=~clock;
end
initial begin
    #30;
    $finish;
end
initial begin
    $dumpfile("CSA64UEQG_4.vcd");
    $dumpvars(0,CSA64UEQG_tb_4);
end
endmodule

```

CASE #6

```

`timescale 1 ns/ 10 ps
module CSA64UEQG_tb_5();

reg [63:0]op1;

```

```
reg [63:0]op2;
reg clock;
reg reset;
wire [63:0]sum;
wire crout;
CSA64UEQG A (sum,crout,op1,op2,clock,reset);

initial begin

    op1= 64'b0;
    op2= 64'b0;
    clock= 1'b1;

    #4;
    op1= 64'h1234_ffff_dfff_eeee;
    op2= 64'hdddd_dddd_dddd_dddd;

end
initial begin
    reset= 1'b1;
    #4;
    reset= 1'b0;
end

initial begin
    forever #3 clock=~clock;
end
initial begin
    #30;
    $finish;
end
initial begin
    $dumpfile("CSA64UEQG_5.vcd");
    $dumpvars(0,CSA64UEQG_tb_5);
end
endmodule
```

Appendix C

Reports and Circuits from EDA Tools

C.1 Reports from RTL (Pre-synthesis) Simulations

Pre Synthesis Report of Ripple Carry Adder

Chronologic VCS simulator copyright 1991-2014

Contains Synopsys proprietary information.

Compiler version I-2014.03-2; Runtime version I-2014.03-2; Dec 4 07:44 2015

op1f= 0000000000000000

op2f= 0000000000000000

sumf= 0000000000000000

croutf= 0

op1f= f20fffffffffffff

op2f= ffffffff50

sumf= f20ffffffffffff4f

croutf= 1

op1f= 101010101199ffff

op2f= abcd11001100dddd

sumf= bbdd2110229adddc

croutf= 0

op1f= ffffffffffffffff

op2f= eeeedddccccffff

```
sumf= eeeeddddccccfffe
croutf= 1
op1f= bbbbcdcdaaaa1111
op2f= ffffffffddd
sumf= bbbbcdcdaaa9eeee
croutf= 1
op1f= 0000000012345678
op2f= 0000000090abcdef
sumf= 00000000a2e02467
croutf= 0
op1f= 1234ffffdfffeeee
op2f= ddddddddddcccccc
sumf= f012ddddbddcccb
croutf= 0
op1f= f20fffffffffffff
op2f= ffffffff50
sumf= f20ffffffffffff4f
croutf= 1
op1f= 101010101199ffff
op2f= abcd11001100dddd
sumf= bbdd2110229adddc
croutf= 0
op1f= ffffffff
op2f= eeeeddddccccffff
sumf= eeeeddddccccfffe
croutf= 1
op1f= bbbbcdcdaaaa1111
op2f= ffffffffddd
sumf= bbbbcdcdaaa9eeee
croutf= 1
op1f= 0000000012345678
op2f= 0000000090abcdef
sumf= 00000000a2e02467
croutf= 0
op1f= 1234ffffdfffeeee
op2f= ddddddddddcccccc
sumf= f012ddddbddcccb
croutf= 0
op1f= f20fffffffffffff
op2f= ffffffff50
sumf= f20ffffffffffff4f
croutf= 1
op1f= 101010101199ffff
op2f= abcd11001100dddd
sumf= bbdd2110229adddc
croutf= 0
```

```

op1f= ffffffffffffffff
op2f= eeeeddddccccffff
sumf= eeeeddddccccfffe
croutf= 1
op1f= bbbbcdcdaaaa1111
op2f= ffffffffffffdfff
sumf= bbbbcdcdaaa9eeee
croutf= 1
op1f= 0000000012345678
op2f= 0000000090abcdef
sumf= 00000000a2e02467
croutf= 0
op1f= 1234ffffdfffeeee
op2f= ddddddddddcccccc
sumf= f012dddbddcccb
croutf= 0
$finish called from file "RCA64_tb.v", line 37.
$finish at simulation time      3000
          V C S   S i m u l a t i o n   R e p o r t
Time: 30000 ps
CPU Time:    0.280 seconds;    Data structure size:  0.1Mb
Fri Dec 4 07:44:22 2015

```

Pre Synthesis Report for CLA-2L

Chronologic VCS simulator copyright 1991-2014
 Contains Synopsys proprietary information.
 Compiler version I-2014.03-2; Runtime version I-2014.03-2; Dec 4 07:50 2015

```

op1_f= 0000000000000000
op2_f= 0000000000000000
sumf= 0000000000000000
croutf= 0
op1_f= 0000000000000000
op2_f= 0000000000000000
sumf= 0000000000000000
croutf= 0
op1_f= 0000000000000000
op2_f= 0000000000000000
sumf= 0000000000000000
croutf= 0
op1_f= 0000000000000000
op2_f= 0000000000000000
sumf= 0000000000000000

```

```
croutf= 0
op1_f= 0000000000000000
op2_f= 0000000000000000
sumf= 0000000000000000
croutf= 0
op1_f= 0000000000000000
op2_f= 0000000000000000
sumf= 0000000000000000
croutf= 0
op1_f= f20fffffffffffff
op2_f= fffffffffff50
sumf= f20ffffffff4f
croutf= 1
op1_f= 101010101199ffff
op2_f= abcd11001100dddd
sumf= bbdd2110229addc
croutf= 0
op1_f= ffffffff
op2_f= eeeedddcccccffff
sumf= eeeedddcccccffe
croutf= 1
op1_f= bbbbcdcdaaaa1111
op2_f= ffffffffffffdfff
sumf= bbbbcdcdaaa9eeee
croutf= 1
op1_f= 1234567890abcdef
op2_f= 5555555555555ddd
sumf= 6789abcde601abcc
croutf= 0
op1_f= 1234ffffdffffeee
op2_f= ddddddddddffffdd
sumf= f012dddbbddcccb
croutf= 0
op1_f= f20fffffffffffff
op2_f= fffffffffff50
sumf= f20ffffffff4f
croutf= 1
op1_f= 101010101199ffff
op2_f= abcd11001100dddd
sumf= bbdd2110229addc
```

```

croutf= 0
op1_f= ffffffffffffffff
op2_f= eeeeddddccccffff
sumf= eeeeddddccccffff
croutf= 1
op1_f= bbbbcdcdaaaa1111
op2_f= ffffffffffffdffff
sumf= bbbbcdcdaaa9eeee
croutf= 1
op1_f= 1234567890abcdef
op2_f= 5555555555555dfff
sumf= 6789abcde601abcc
croutf= 0
op1_f= 1234ffffdffffeeee
op2_f= ddddddddddffffddddd
sumf= f012dddbbddcccb
croutf= 0
$finish called from file "CLA_64_tb.v", line 34.
$finish at simulation time      3000

```

V C S S i m u l a t i o n R e p o r t

Time: 30000 ps
 CPU Time: 0.270 seconds; Data structure size: 0.0Mb
 Fri Dec 4 07:50:05 2015

Pre Synthesis Report for CSA EOG

Contains Synopsys proprietary information.

Compiler version I-2014.03-2; Runtime version I-2014.03-2; Dec 4 07:59 2015

```

op1f= 0000000000000000
op2f= 0000000000000000
sumf= 0000000000000000
croutf= 0
op1f= 0000000000000000
op2f= 0000000000000000
sumf= 0000000000000000
croutf= 0
op1f= 0000000000000000
op2f= 0000000000000000
sumf= 0000000000000000
croutf= 0
op1f= 0000000000000000
op2f= 0000000000000000

```

```
sumf= 0000000000000000
croutf= 0
op1f= 0000000000000000
op2f= 0000000000000000
sumf= 0000000000000000
croutf= 0
op1f= 0000000000000000
op2f= 0000000000000000
sumf= 0000000000000000
croutf= 0
op1f= f20fffffffffffff
op2f= ffffffff50
sumf= f20ffffffffffff4f
croutf= 1
op1f= 101010101199ffff
op2f= abcd11001100dddd
sumf= bbdd2110229adddc
croutf= 0
op1f= ffffffffffffffff
op2f= eeeeddddccccffff
sumf= eeeeddddccccfffe
croutf= 1
op1f= bbbbcdcdaaaa1111
op2f= ffffffffffffdfff
sumf= bbbbcdcdaaa9eeee
croutf= 1
op1f= 1234567890abcdef
op2f= 5555555555555555
sumf= 6789abcde601abcc
croutf= 0
op1f= 1234ffffdffffeee
op2f= ddddddBBBBBDDDDDD
sumf= f012dddbddcccb
croutf= 0
op1f= f20fffffffffffff
op2f= ffffffff50
sumf= f20ffffffffffff4f
croutf= 1
op1f= 101010101199ffff
op2f= abcd11001100dddd
sumf= bbdd2110229adddc
croutf= 0
op1f= ffffffffffffffff
op2f= eeeeddddccccffff
sumf= eeeeddddccccfffe
croutf= 1
```

```

op1f= bbbbcdcdaaaa1111
op2f= ffffffffddd
sumf= bbbbcdcdaaa9eeee
croutf= 1
op1f= 1234567890abcdef
op2f= 555555555555dddd
sumf= 6789abcde601abcc
croutf= 0
op1f= 1234ffffdffffeee
op2f= ddddddddddcccccc
sumf= f012dddbddcccb
croutf= 0
op1f= f20ffffffffffff
op2f= ffffffff50
sumf= f20ffffffff4f
croutf= 1
op1f= 101010101199ffff
op2f= abcd11001100dddd
sumf= bbdd2110229adddc
croutf= 0
op1f= fffffffffff
op2f= eeeedddccccffff
sumf= eeeedddccccfffe
croutf= 1
op1f= bbbbcdcdaaaa1111
op2f= ffffffffddd
sumf= bbbbcdcdaaa9eeee
croutf= 1
op1f= 1234567890abcdef
op2f= 555555555555dddd
sumf= 6789abcde601abcc
croutf= 0
op1f= 1234ffffdffffeee
op2f= ddddddddddcccccc
sumf= f012dddbddcccb
croutf= 0
$finish called from file "CSA64EQG_tb.v", line 34.
$finish at simulation time      3000
          V C S   S i m u l a t i o n   R e p o r t
Time: 30000 ps
CPU Time:    0.300 seconds;    Data structure size:  0.0Mb
Fri Dec 4 07:59:44 2015

```

Pre Synthesis Report for CSA UEQG

Chronologic VCS simulator copyright 1991-2014

Contains Synopsys proprietary information.

Compiler version I-2014.03-2; Runtime version I-2014.03-2; Dec 4 08:03 2015

op1f= 0000000000000000

op2f= 0000000000000000

sumf= 0000000000000000

croutf= 0

op1f= f20fffffffffffff

op2f= ffffffff50

sumf= f20ffffffffffff4f

croutf= 1

op1f= 101010101199ffff

op2f= abcd11001100dddd

sumf= bbdd2110229adddc

croutf= 0

op1f= ffffffffffffffff

op2f= eeeeddddccccffff

sumf= eeeeddddccccfffe

croutf= 1

op1f= bbbbcdcdaaaa1111

op2f= ffffffffffffdfff

sumf= bbbbcdcdaaa9eeee

croutf= 1

op1f= 1234567890abcdef

op2f= 5555555555555ddd

sumf= 6789abcde601abcc

croutf= 0

```
op1f= 1234ffffdfffeeee
op2f= ddddddddddcccccc
sumf= f012dddbddcccb
croutf= 0
op1f= f20fffffffffffff
op2f= fffffffffff50
sumf= f20ffffffffffff4f
croutf= 1
op1f= 101010101199ffff
op2f= abcd11001100dddd
sumf= bbdd2110229adddc
croutf= 0
op1f= ffffffffffffffff
op2f= eeeedddccccffff
sumf= eeeedddccccfffe
croutf= 1
op1f= bbbbbedcdaaaa1111
op2f= ffffffffffffdfff
sumf= bbbbcdcdaaa9eeee
croutf= 1
op1f= 1234567890abcdef
op2f= 555555555555dddd
sumf= 6789abcde601abcc
croutf= 0
op1f= 1234ffffdfffeeee
op2f= ddddddcccccc
sumf= f012dddbddcccb
croutf= 0
op1f= f20fffffffffffff
op2f= fffffffffff50
sumf= f20ffffffffffff4f
croutf= 1
op1f= 101010101199ffff
op2f= abcd11001100dddd
sumf= bbdd2110229adddc
croutf= 0
op1f= ffffffffffffffff
op2f= eeeedddccccffff
sumf= eeeedddccccfffe
croutf= 1
op1f= bbbbcdcdaaaa1111
op2f= ffffffffffffdfff
sumf= bbbbcdcdaaa9eeee
croutf= 1
op1f= 1234567890abcdef
op2f= 555555555555dddd
```

```

sumf= 6789abcde601abcc
croutf= 0
op1f= 1234ffffdfffeeee
op2f= ddddddddddccccb
sumf= f012dddbddcccb
croutf= 0
$finish called from file "CSA64UEQG_tb.v", line 34.
$finish at simulation time      3000
    V C S   S i m u l a t i o n   R e p o r t
Time: 30000 ps
CPU Time: 0.300 seconds; Data structure size: 0.0Mb
Fri Dec 4 08:03:53 2015

```

C.2 Reports (contents) from Netlist (Post-synthesis) Simulations (VCS or NCVERILOG)

RCA Post Synthesis

Warning-[LNX_OS_VERUN] Unsupported Linux version
 Linux version 'Fedora release 22 (Twenty Two)' is not supported on 'x86_64'
 officially, assuming linux compatibility by default. Set VCS_ARCH_OVERRIDE
 to linux or suse32 to override.
 Please refer to release notes for information on supported platforms.

Warning-[LNX_KRNL] Unsupported Linux kernel
 Linux kernel '4.2.6-200.fc22.x86_64' is not supported.
 Supported versions are 2.4* or 2.6*.

Chronologic VCS (TM)
 Version I-2014.03-2 -- Sat Dec 5 20:19:35 2015
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 controlling such use and disclosure.

Parsing design file 'RCA64_tb.v'
 Parsing design file 'RCA64_tb_1.v'
 Parsing design file 'RCA64_tb_2.v'
 Parsing design file 'RCA64_tb_3.v'
 Parsing design file 'RCA64_tb_4.v'
 Parsing design file 'RCA64_tb_5.v'
 Parsing design file 'RCA64_1_nl.v'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAN2X1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAN2XL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CDLY1X2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CDLY1XL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CDLY2X2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CENX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CENX2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CENXL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CEOX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CEOXL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD2QX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD2QX2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD2QX4.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD2QXL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD2X1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD3QX2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVDX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVX2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVX20.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVX4.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVXL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2IX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2IX2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2X1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2X2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CNIVX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CNR2IX2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CNR2X2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2QX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2QX2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2QX4.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2QXL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2X1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD3QX2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/TFDPRBNOprim.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/TFDPRBSBNOprim.tsbvlibp'

Top Level Modules:

- RCA64_tb
- RCA64_tb_1
- RCA64_tb_2
- RCA64_tb_3
- RCA64_tb_4
- RCA64_tb_5

TimeScale is 1 ns / 10 ps

Warning-[TFIPC] Too few instance port connections

RCA64_1_nl.v, 8

"CIVDX1 U1(.A (n3), .Z1 (sum_ha));"

The above instance has fewer port connections than the module definition.

Please use '+lint=TFIPC-L' to print out detailed information of unconnected ports.

Warning-[TFIPC] Too few instance port connections

RCA64_1_nl.v, 2880

"CFD2X1 crout_reg(.D (croutf), .CP (clock), .CD (n261), .Q (crout));"

The above instance has fewer port connections than the module definition.

Please use '+lint=TFIPC-L' to print out detailed information of unconnected ports.

Starting vcs inline pass...

33 modules and 2 UDPs read.

However, due to incremental compilation, no re-compilation is necessary.

```
rm -f _csrc*.so linux_scvhdl_*_.so pre_vcsobj_*_.so share_vcsobj_*_.so
ld -m elf_i386 -shared -o ../../simv.daidir/_csrc0.so SIM_1.o 5NrI_d.o 5NrIB_d.o
ld -m elf_i386 -shared -o ../../simv.daidir/pre_vcsobj_1_1.so --whole-archive pre_vcsobj_1_1.a -no-whole-archive
ld -m elf_i386 -shared -o ../../simv.daidir/pre_vcsobj_1_2.so --whole-archive pre_vcsobj_1_2.a -no-whole-archive
ld -m elf_i386 -shared -o ../../simv.daidir/pre_vcsobj_1_3.so --whole-archive pre_vcsobj_1_3.a -no-whole-archive
if [ -x ..simv ]; then chmod -x ..simv; fi
g++ -o ..simv -m32 -m32 -Wl,-rpath-link=../../simv.daidir -Wl,-rpath=$ORIGIN/simv.daidir -Wl,-rpath=$ORIGIN/simv.daidir//scsim.db.dir _csrc0.so pre_vcsobj_1_1.so pre_vcsobj_1_2.so pre_vcsobj_1_3.so rmapats_mop.o rmapats.o rmar.o /apps/synopsys/I-2014.03-2/linux/lib/libzzerosoft_rt_stubs.so /apps/synopsys/I-2014.03-2/linux/lib/libvirsim.so /apps/synopsys/I-2014.03-2/linux/lib/librterrorinf.so /apps/synopsys/I-2014.03-2/linux/lib/libsnpsmalloc.so /apps/synopsys/I-2014.03-2/linux/lib/libvcsnew.so /apps/synopsys/I-2014.03-2/linux/lib/libuclinative.so -Wl,-whole-archive /apps/synopsys/I-2014.03-2/linux/lib/libvesucli.so -Wl,-no-whole-archive /apps/synopsys/I-2014.03-2/linux/lib/vcs_save_restore_new.o /apps/synopsys/I-2014.03-2/linux/lib/ctype-stubs_32.a -ldl -lm -lc -lpthread -ldl
./simv up to date
```

CPU time: .423 seconds to compile + .016 seconds to elab + .124 seconds to link

CLA-2L Post Synthesis

Warning-[LNX_OS_VERUN] Unsupported Linux version

Linux version 'Fedora release 22 (Twenty Two)' is not supported on 'x86_64'
officially, assuming linux compatibility by default. Set VCS_ARCH_OVERRIDE

to linux or suse32 to override.

Please refer to release notes for information on supported platforms.

Warning-[LINX_KRNL] Unsupported Linux kernel
Linux kernel '4.2.6-200.fc22.x86_64' is not supported.
Supported versions are 2.4* or 2.6*.

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Version I-2014.03-2 -- Sat Dec 5 20:22:14 2015
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Parsing design file 'CLA_64_tb.v'
Parsing design file 'CLA_64_tb_1.v'
Parsing design file 'CLA_64_tb_2.v'
Parsing design file 'CLA_64_tb_3.v'
Parsing design file 'CLA_64_tb_4.v'
Parsing design file 'CLA_64_tb_5.v'
Parsing design file 'CLA_64_1_nl.v'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAN2X1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAN2X2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAN2XL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAN4X1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAN4XL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CANR2X1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CANR2X2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CANR2X4.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CANR2XL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAOR1X1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAOR2X1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CDLY1XL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CDLY2X2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CENX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CENXL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CEOX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CEOX2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CEOXL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD2QX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD2QX4.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD2QXL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVX1.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVX2.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVX20.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVXL.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2IX1.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2IX2.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2X1.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2X2.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2XL.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CNIVX1.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/COND1X2.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/COND2X1.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/COND2X2.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/COND2XL.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/COND4CX1.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/COND4CXL.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2QX1.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2QX4.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2QXL.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/TFDPRBNOPrim.tsbvlibp'

Top Level Modules:

- CLA_64_tb
- CLA_64_tb_1
- CLA_64_tb_2
- CLA_64_tb_3
- CLA_64_tb_4
- CLA_64_tb_5

TimeScale is 1 ns / 10 ps

Warning-[TFIPC] Too few instance port connections

CLA_64_1_nl.v, 148

"CLA4_C1(.sum (sum_4[3:0]), .crout (p1), .G1 (G[0]), .op1 (op1_4[3:0]), .op2 (op2_4[3:0]));"

The above instance has fewer port connections than the module definition.

Please use '+lint=TFIPC-L' to print out detailed information of unconnected ports.

Warning-[TFIPC] Too few instance port connections

CLA_64_1_nl.v, 154

"CLA4_2_13 C4(.sum (sum_4[15:12]), .P2 (P[3]), .G2 (G[3]), .op1 (op1_4[15:12]), .op2 (op2_4[15:12]), .Cin (p3));"

The above instance has fewer port connections than the module definition.

Please use '+lint=TFIPC-L' to print out detailed information of unconnected ports.

Warning-[TFIPC] Too few instance port connections

CLA_64_1_nl.v, 318

"CLA4_2_9 A4(.sum (sum_16[15:12]), .P2 (P[3]), .G2 (G[3]), .op1 (op1_16[15:12]), .op2 (op2_16[15:12]), .Cin (p3));"

The above instance has fewer port connections than the module definition.

Please use '+lint=TFIPC-L' to print out detailed information of unconnected ports.

Warning-[TFIPC] Too few instance port connections

CLA_64_1_nl.v, 506

"CLA4_2_5 A4(.sum (sum_16[15:12]), .P2 (P[3]), .G2 (G[3]), .op1 (op1_16[15:12]), .op2 (op2_16[15:12]), .Cin (p3));"

The above instance has fewer port connections than the module definition.

Please use '+lint=TFIPC-L' to print out detailed information of unconnected ports.

Warning-[TFIPC] Too few instance port connections

CLA_64_1_nl.v, 702

"CLA4_2_1 A4(.sum (sum_16[15:12]), .P2 (P[3]), .G2 (G[3]), .op1 (op1_16[15:12]), .op2 (op2_16[15:12]), .Cin (p3));"

The above instance has fewer port connections than the module definition.

Please use '+lint=TFIPC-L' to print out detailed information of unconnected ports.

Starting vcs inline pass...

30 modules and 1 UDP read.

However, due to incremental compilation, no re-compilation is necessary.

```
rm -f _csrc*.so linux_scvhdl_*_.so pre_vcsobj_*_.so share_vcsobj_*_.so
ld -m elf_i386 -shared -o ../../simv.daidir/_csrc0.so SIM_l.o 5NrI_d.o 5NrIB_d.o
ld -m elf_i386 -shared -o ../../simv.daidir/pre_vcsobj_1_1.so --whole-archive pre_vcsobj_1_1.a -no-whole-archive
ld -m elf_i386 -shared -o ../../simv.daidir/pre_vcsobj_1_2.so --whole-archive pre_vcsobj_1_2.a -no-whole-archive
if [ -x ../../simv ]; then chmod -x ../../simv; fi
g++ -o ../../simv -m32 -m32 -Wl,-rpath-link=../../simv.daidir -Wl,-rpath=$ORIGIN/simv.daidir/ -Wl,-rpath=$ORIGIN/simv.daidir//scsim.db.dir _csrc0.so pre_vcsobj_1_1.so pre_vcsobj_1_2.so
rmapats_mop.o rmapats.o rmar.o                                /apps/synopsys/I-2014.03-2/linux/lib/libvirsim.so
2/linux/lib/libzerosoft_rt_stubs.so                            /apps/synopsys/I-2014.03-2/linux/lib/libvirsnew.so
/apps/synopsys/I-2014.03-2/linux/lib/librterrorinf.so        /apps/synopsys/I-2014.03-2/linux/lib/libvcsmalloc.so
2/linux/lib/libsnpsmalloc.so                                 /apps/synopsys/I-2014.03-2/linux/lib/libvcsmalloc.so
/apps/synopsys/I-2014.03-2/linux/lib/libuclinative.so      -Wl,-whole-archive /apps/synopsys/I-2014.03-2/linux/lib/libvcscucli.so -Wl,-no-whole-archive          /apps/synopsys/I-2014.03-2/linux/lib/libctype-stubs_32.a -ldl -lm -lc -lpthread -ldl
```

./simv up to date

CPU time: .317 seconds to compile + .245 seconds to elab + .151 seconds to link

CSA Equal Post Synthesis

Warning-[LNX_OS_VERUN] Unsupported Linux version

Linux version 'Fedora release 22 (Twenty Two)' is not supported on 'x86_64'
officially, assuming linux compatibility by default. Set VCS_ARCH_OVERRIDE
to linux or suse32 to override.

Please refer to release notes for information on supported platforms.

Warning-[LINX_KRNL] Unsupported Linux kernel

Linux kernel '4.2.6-200.fc22.x86_64' is not supported.

Supported versions are 2.4* or 2.6*.

Chronologic VCS (TM)

Version I-2014.03-2 -- Sat Dec 5 20:24:38 2015

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Parsing design file 'CSA64EQG_tb.v'

Parsing design file 'CSA64EQG_tb_1.v'

Parsing design file 'CSA64EQG_tb_2.v'

Parsing design file 'CSA64EQG_tb_3.v'

Parsing design file 'CSA64EQG_tb_4.v'

Parsing design file 'CSA64EQG_tb_5.v'

Parsing design file 'CSA64EQG_1_nl.v'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAN2X1.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAN2X2.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAN2XL.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAOR2X1.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAOR2X2.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAOR2XL.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CDLY1X2.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CDLY1XL.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CENX1.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CENX2.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CENXL.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CEOX1.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CEOX2.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CEOXL.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD2QX1.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD2QX2.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD2X2.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVX1.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVX2.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVX20.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVX3.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVX8.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVXL.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2IX1.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2IX2.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2X1.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2X2.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2X4.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2XL.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CNIVX1.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/COND2X2.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/COND2XL.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/COR2X1.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2QX1.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2QX2.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2X2.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/TFDPRBNOprim.tsbvlibp'

Top Level Modules:

- CSA64EQG_tb
- CSA64EQG_tb_1
- CSA64EQG_tb_2
- CSA64EQG_tb_3
- CSA64EQG_tb_4
- CSA64EQG_tb_5

TimeScale is 1 ns / 10 ps

Warning-[TFIPC] Too few instance port connections

CSA64EQG_1_nl.v, 2536

"CFD2X2 \sum_reg[62] (.D (sumf[62]), .CP (clock), .CD (n266), .Q (sum[62]));"

The above instance has fewer port connections than the module definition.

Please use '+lint=TFIPC-L' to print out detailed information of unconnected ports.

Warning-[TFIPC] Too few instance port connections

CSA64EQG_1_nl.v, 2537

"CFD2X2 \sum_reg[61] (.D (sumf[61]), .CP (clock), .CD (n266), .Q (sum[61]));"

The above instance has fewer port connections than the module definition.

Please use '+lint=TFIPC-L' to print out detailed information of unconnected ports.

Warning-[TFIPC] Too few instance port connections

CSA64EQG_1_nl.v, 2538

"CFD2X2 \sum_reg[60] (.D (sumf[60]), .CP (clock), .CD (n266), .Q (sum[60]));"

The above instance has fewer port connections than the module definition.

Please use '+lint=TFIPC-L' to print out detailed information of unconnected ports.

Warning-[TFIPC] Too few instance port connections

CSA64EQG_1_nl.v, 2539

"CFD2X2 crout_reg(.D (croutf), .CP (clock), .CD (n266), .Q (crout));"

The above instance has fewer port connections than the module definition.

Please use '+lint=TFIPC-L' to print out detailed information of unconnected ports.

Starting vcs inline pass...

33 modules and 1 UDP read.

recompiling module CSA64EQG_tb because:

Some compilation options have been changed.

recompiling module CSA64EQG_tb_1 because:

Some compilation options have been changed.

recompiling module CSA64EQG_tb_2 because:

Some compilation options have been changed.

recompiling module CSA64EQG_tb_3 because:

Some compilation options have been changed.

recompiling module CSA64EQG_tb_4 because:

Some compilation options have been changed.

recompiling module CSA64EQG_tb_5 because:

Some compilation options have been changed.

recompiling module CSA4_0 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA4_15 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA4_14 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA4_13 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA4_12 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA4_11 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA4_10 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA4_9 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA4_8 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA4_7 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA4_6 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA4_5 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA4_4 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA4_3 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA4_2 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA4_1 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CSA64EQG because:

Some compilation options have been changed.

recompiling module CAOR2X1 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CAOR2X2 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CAOR2XL because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CDLY1X2 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.
recompiling module CDLY1XL because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CEOX1 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CFD2QX2 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CFD2X2 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CIVX8 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CNIVX1 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

All of 33 modules done

```
rm -f _csrc*.so linux_scvhdl_*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -m elf_i386 -shared -o ../../simv.daidir/_csrc1.so --whole-archive _vcsobj_1_1.a --no-whole-
archive
ld -m elf_i386 -shared -o ../../simv.daidir/_csrc0.so 5NrI_d.o 5NrIB_d.o SIM_1.o
if [ -x ./simv ]; then chmod -x ./simv; fi
g++ -o ./simv -m32 -m32 -Wl,-rpath-link= ./ -Wl,-rpath=$ORIGIN/simv.daidir/ -Wl,-
rpath=$ORIGIN/simv.daidir//scsim.db.dir _csrc1.so _csrc0.so rmapats_mop.o rmapats.o
rmar.o /apps/synopsys/I-2014.03-2/linux/lib/libzerosoft_rt_stubs.so /apps/synopsys/I-
2014.03-2/linux/lib/libvirsim.so /apps/synopsys/I-2014.03-2/linux/lib/librrorinf.so
/apps/synopsys/I-2014.03-2/linux/lib/libsnpsmalloc.so /apps/synopsys/I-2014.03-
2/linux/lib/libvcsnew.so /apps/synopsys/I-2014.03-2/linux/lib/libuclinative.so -Wl,-whole-
archive /apps/synopsys/I-2014.03-2/linux/lib/libvcsucli.so -Wl,-no-whole-archive
/apps/synopsys/I-2014.03-2/linux/lib/vcs_save_restore_new.o /apps/synopsys/I-2014.03-
2/linux/lib/ctype-stubs_32.a -ldl -lm -lc -lpthread -ldl
./simv up to date
```

CPU time: 1.132 seconds to compile + .265 seconds to elab + .152 seconds to link

CSA Unequal Post Synthesis

Warning-[LNX_OS_VERUN] Unsupported Linux version

Linux version 'Fedora release 22 (Twenty Two)' is not supported on 'x86_64'
officially, assuming linux compatibility by default. Set VCS_ARCH_OVERRIDE
to linux or suse32 to override.

Please refer to release notes for information on supported platforms.

Warning-[LINX_KRNL] Unsupported Linux kernel
Linux kernel '4.2.6-200.fc22.x86_64' is not supported.
Supported versions are 2.4* or 2.6*.

Chronologic VCS (TM)
Version I-2014.03-2 -- Sat Dec 5 20:26:17 2015
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Parsing design file 'CSA64UEQG_tb.v'
Parsing design file 'CSA64UEQG_tb_1.v'
Parsing design file 'CSA64UEQG_tb_2.v'
Parsing design file 'CSA64UEQG_tb_3.v'
Parsing design file 'CSA64UEQG_tb_4.v'
Parsing design file 'CSA64UEQG_tb_5.v'
Parsing design file 'CSA64UEQG_1_nl.v'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAN2XL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAOR2X1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CAOR2XL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CDLY1XL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CDLY2X2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CENX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CENX2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CEOX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CEOX2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CEOXL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD2QX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD2QX4.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD2QXL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CFD2X2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVX2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVX20.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CIVXL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2IX1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2IX2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2X1.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2X2.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CND2XL.tsbvlibp'
Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CNIVX1.tsbvlibp'

Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/CNIVXL.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/COND2X1.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/COND2XL.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2QX1.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2QX4.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2QXL.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2X2.tsbvlibp'
 Parsing library directory file '/apps/toshiba/sjsu/verilog/tc240c/TFDPRBNOprim.tsbvlibp'

Top Level Modules:

- CSA64UEQG_tb
- CSA64UEQG_tb_1
- CSA64UEQG_tb_2
- CSA64UEQG_tb_3
- CSA64UEQG_tb_4
- CSA64UEQG_tb_5

TimeScale is 1 ns / 10 ps

Warning-[TFIPC] Too few instance port connections

CSA64UEQG_1_nl.v, 2505

"CFD2X2 \sum_reg[62] (.D (sumf[62]), .CP (clock), .CD (n265), .Q (sum[62]));"

The above instance has fewer port connections than the module definition.

Please use '+lint=TFIPC-L' to print out detailed information of unconnected ports.

Warning-[TFIPC] Too few instance port connections

CSA64UEQG_1_nl.v, 2506

"CFD2X2 \sum_reg[61] (.D (sumf[61]), .CP (clock), .CD (n265), .Q (sum[61]));"

The above instance has fewer port connections than the module definition.

Please use '+lint=TFIPC-L' to print out detailed information of unconnected ports.

Warning-[TFIPC] Too few instance port connections

CSA64UEQG_1_nl.v, 2507

"CFD2X2 \sum_reg[60] (.D (sumf[60]), .CP (clock), .CD (n265), .Q (sum[60]));"

The above instance has fewer port connections than the module definition.

Please use '+lint=TFIPC-L' to print out detailed information of unconnected ports.

Starting vcs inline pass...

28 modules and 1 UDP read.

However, due to incremental compilation, only 28 modules need to be compiled.

recompiling module CSA64UEQG_tb because:

Some compilation options have been changed.

recompiling module CSA64UEQG_tb_1 because:

Some compilation options have been changed.
recompiling module CSA64UEQG_tb_2 because:

Some compilation options have been changed.
recompiling module CSA64UEQG_tb_3 because:

Some compilation options have been changed.
recompiling module CSA64UEQG_tb_4 because:

Some compilation options have been changed.
recompiling module CSA64UEQG_tb_5 because:

Some compilation options have been changed.
recompiling module CSA4_0 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.
recompiling module CSA4_8 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.
recompiling module CSA5 because:

Signal dependencies have changed

recompiling module CSA6 because:

Signal dependencies have changed

recompiling module CSA7 because:

Signal dependencies have changed

recompiling module CSA8 because:

Signal dependencies have changed

recompiling module CSA9 because:

Signal dependencies have changed

recompiling module CSA10 because:

Signal dependencies have changed

recompiling module CSA11 because:

Signal dependencies have changed

recompiling module CSA64UEQG because:

Some compilation options have been changed.

recompiling module CAOR2X1 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CAOR2XL because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CDLY1XL because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CDLY2X2 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CEOX1 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CFD2QX4 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CFD2QXL because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CFD2X2 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CIVX2 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module CNIVX1 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module COND2X1 because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

recompiling module COND2XL because:

Signal dependencies have changed

Some child instantiation or references (or ports) have been changed.

All of 28 modules done

```
rm -f _csrc*.so linux_scvhdl_*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -m elf_i386 -shared -o ../../simv.daidir/_csrc1.so --whole-archive _vcsobj_1_1.a --no-whole-archive
ld -m elf_i386 -shared -o ../../simv.daidir/_csrc0.so 5NrI_d.o 5NrIB_d.o SIM_1.o
ld -m elf_i386 -shared -o ../../simv.daidir/pre_vcsobj_1_1.so --whole-archive pre_vcsobj_1_1.a --no-whole-archive
if [ -x ../../simv ]; then chmod -x ../../simv; fi
g++ -o ../../simv -m32 -m32 -Wl,-rpath-link=../../simv.daidir/_csrc1.so _csrc0.so pre_vcsobj_1_1.so
rmapats_mop.o rmapats.o rmar.o /apps/synopsys/I-2014.03-2/linux/lib/libvirsim.so
2/linux/lib/libzerosoft_rt_stubs.so /apps/synopsys/I-2014.03-2/linux/lib/libvcsmalloc.so
/apps/synopsys/I-2014.03-2/linux/lib/librterrorinf.so /apps/synopsys/I-2014.03-2/linux/lib/libvcsnew.so
2/linux/lib/libsnpsmalloc.so /apps/synopsys/I-2014.03-2/linux/lib/libuclinative.so -Wl,-whole-archive /apps/synopsys/I-2014.03-2/linux/lib/libvcsucli.so -Wl,-no-whole-archive /apps/synopsys/I-2014.03-2/linux/lib/vcs_save_restore_new.o /apps/synopsys/I-2014.03-2/linux/lib/ctype-stubs_32.a -ldl -lm -lc -lpthread -ldl
../../simv up to date
```

CPU time: .935 seconds to compile + .274 seconds to elab + .156 seconds to link

C.3 Reports (contents) from Synthesis (Design Compiler)

Synthesis Report of RCA64

```

Initializing...
set                                link_library
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
/apps/synopsys/SYNTH/libraries/syn/dw02.sldb
/apps/synopsys/SYNTH/libraries/syn/dw01.sldb}
set                                target_library
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}
/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
read_verilog RCA64.v
Loading                      db          file
'/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25'
Loading                      db          file
'/apps/synopsys/SYNTH/libraries/syn/dw02.sldb'
Loading                      db          file
'/apps/synopsys/SYNTH/libraries/syn/dw01.sldb'
Loading                      db          file
'/apps/synopsys/SYNTH/libraries/syn/gtech.db'
Loading                      db          file
'/apps/synopsys/SYNTH/libraries/syn/standard.sldb'
    Loading link library 'tc240c'
Warning: Function '=' leaked 1 allocations for 16
bytes. (EQN-21)
    Loading link library 'gtech'
Loading                      verilog      file
'/home/pa/pand2610/Desktop/Project/RCA64/RCA64.v'
Detecting input file type automatically (-rtl or -
netlist).
Running DC verilog reader
Reading with Presto HDL Compiler (equivalent to -rtl
option).
Running PRESTO HDLC

```

Compiling source file
 /home/pa/pand2610/Desktop/Project/RCA64/RCA64.v

Inferred memory devices in process
 in routine RCA64 line 91 in file

'/home/pa/pand2610/Desktop/Project/RCA64/RCA64.v'.
 =====

	Register Name				Type	Width	Bus	MB	
AR	AS	SR	SS	ST					
<hr/>									
Y	N	N	N	N	Flip-flop	64	Y	N	
Y	N	N	N	N	Flip-flop	1	N	N	
Y	N	N	N	N	Flip-flop	64	Y	N	
Y	N	N	N	N	Flip-flop	64	Y	N	
<hr/>									

Presto compilation completed successfully.

Current design is now

'/home/pa/pand2610/Desktop/Project/RCA64/HA.db:HA'

Loaded 5 designs.

Current design is 'HA'.

HA FA_1bit FA_4bit_1 FA_4bit_2 RCA64

current_design RCA64

Current design is 'RCA64'.

{RCA64}

check_design

Information: Design 'RCA64' has multiply instantiated designs. Use the '-multiple_designs' switch for more information. (LINT-78)

1

set_drive 0 clock

1

set_drive 0 reset

```

1
set_dont_touch_network clock
1
create_clock clock -name clock -period 20.800000
1
set_propagated_clock clock
Information: set_input_delay values are added to the
propagated clock skew. (TIM-113)
1
set_clock_uncertainty 0.25 clock
1
set_propagated_clock clock
Information: set_input_delay values are added to the
propagated clock skew. (TIM-113)
1
#set_output_delay 0.5 -clock clock [all_outputs]
#set      all_inputs_wo_rst_clk      [remove_from_collection
[remove_from_collection  [all_inputs]  [get_port clk]]
[get_port rst]]
#set_driving_cell           -lib_cell          CND2X1
$all_inputs_wo_rst_clk
#set_input_delay 0.5 -clock clk $all_inputs_wo_rst_clk
#set_max_delay 48.5 -to [all_outputs]
#set_max_delay 48.5 -from $all_inputs_wo_rst_clk
set_fix_hold [ get_clocks clock ]
1
compile -map_effort medium -incremental_mapping
Information: Evaluating DesignWare library utilization.
(UISN-27)
=====
```

DesignWare Building Block Library	
Version	Available
Basic DW Building Blocks	C-2009.06-
DWBB_0912 *	
Licensed DW Building Blocks	C-2009.06-
DWBB_0912	

=====

=====

Warning: Operating condition WCCOM25 set on design
RCA64 has different process,
voltage and temperatures parameters than the parameters
at which target library
tc240c is characterized. Delays may be inaccurate as a
result. (OPT-998)

Beginning Pass 1 Mapping (Incremental)

Processing 'HA_0'
Processing 'FA_1bit_0'
Processing 'RCA64'

Updating timing information

Information: Updating design information... (UID-85)
Information: Input delay ('fall') on clock port 'clock'
will be added to the clock's propagated skew. (TIM-112)
Information: Input delay ('rise') on clock port 'clock'
will be added to the clock's propagated skew. (TIM-112)
Information: Input delay ('fall') on clock port 'clock'
will be added to the clock's propagated skew. (TIM-112)
Information: Input delay ('rise') on clock port 'clock'
will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Medium effort)
(Incremental)

Beginning Incremental Implementation Selection

Information: Input delay ('fall') on clock port 'clock'
will be added to the clock's propagated skew. (TIM-112)
Information: Input delay ('rise') on clock port 'clock'
will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

ELAPSED MIN DELAY	TIME ENDPOINT	AREA COST	WORST SLACK	NEG SLACK	TOTAL RULE	NEG COST	DESIGN
0:00:02		1891.0	7.04		67.9		1890.1
0.00							
0:00:02	crouut_reg/D	2062.5	5.58 0.00		46.2		0.0
0:00:03	crouut_reg/D	2150.0	5.19 0.00		40.6		0.0
0:00:03	crouut_reg/D	2183.0	5.19 0.00		40.6		0.0
0:00:03	crouut_reg/D	2207.0	5.15 0.00		40.2		0.0
0:00:03	crouut_reg/D	2231.5	5.14 0.00		40.2		0.0
0:00:04	crouut_reg/D	2229.5	5.14 0.00		40.2		0.0
0:00:04	crouut_reg/D	2240.0	5.14 0.00		40.2		0.0
0:00:04	crouut_reg/D	2241.5	5.14 0.00		40.2		0.0
0:00:04	crouut_reg/D	2252.0	5.14 0.00		40.2		0.0
0:00:05	crouut_reg/D	2255.5	5.14 0.00		40.2		0.0
0:00:05	crouut_reg/D	2253.5	5.14 0.00		40.2		0.0
0:00:05	crouut_reg/D	2257.0	5.13 0.00		40.5		0.0
0:00:06	crouut_reg/D	2269.5	5.11 0.00		40.7		0.0
0:00:06	crouut_reg/D	2275.5	5.08 0.00		40.8		0.0
0:00:06	crouut_reg/D	2287.0	5.04 0.00		41.8		0.0

	ELAPSED MIN DELAY	AREA	WORST NEG	TOTAL NEG	DESIGN RULE COST
0:00:06	2294.5	5.02	42.5	0.0	
crouut_reg/D		0.00			
0:00:07	2319.0	5.00	43.6	0.0	
crouut_reg/D		0.00			
0:00:07	2325.0	4.97	44.2	0.0	
crouut_reg/D		0.00			
0:00:08	2353.0	4.96	48.5	0.0	
crouut_reg/D		0.00			
0:00:09	2345.5	4.93	48.4	0.0	
crouut_reg/D		0.00			
0:00:12	2554.0	0.00	0.0	0.0	
-84.91					

Beginning Design Rule Fixing (min_path)

ELAPSED MIN DELAY	TIME ENDPOINT	AREA COST	WORST NEG	TOTAL NEG	DESIGN RULE COST
0:00:12	2554.0	0.00	0.0	0.0	0.0
-84.91					
0:00:12	3131.0	0.00	0.0	0.0	0.0
0.00					
Loading		db			file
'/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25'					

Optimization Complete

```

1
create_clock clk -name clock -period 21.000000
Warning: Can't find object 'clk' in design 'RCA64'.
(UID-95)
Error: Value for list 'source_objects' must have 1
elements. (CMD-036)
0
set_propagated_clock clock

```

Information: set_input_delay values are added to the propagated clock skew. (TIM-113)

1

set_clock_uncertainty 0.25 clock

1

set_propagated_clock clock

Information: set_input_delay values are added to the propagated clock skew. (TIM-113)

1

update_timing

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

1

report -cell

report_cell

Report : cell

Design : RCA64

Version: C-2009.06-SP5

Date : Wed Dec 2 22:10:53 2015

Attributes:

b - black box (unknown)

h - hierarchical

n - noncombinational

r - removable

u - contains unmapped logic

Cell Area	Attributes	Reference	Library

F1 62.000000 h			FA_4bit_1

F2		FA_4bit_2_0
72.000000 h		
F3		FA_4bit_2_14
71.000000 h		
F4		FA_4bit_2_13
72.000000 h		
F5		FA_4bit_2_12
70.000000 h		
F6		FA_4bit_2_11
72.000000 h		
F7		FA_4bit_2_10
71.000000 h		
F8		FA_4bit_2_9
70.000000 h		
F9		FA_4bit_2_8
72.000000 h		
F10		FA_4bit_2_7
72.000000 h		
F11		FA_4bit_2_6
72.000000 h		
F12		FA_4bit_2_5
72.000000 h		
F13		FA_4bit_2_4
72.000000 h		
F14		FA_4bit_2_3
68.500000 h		
F15		FA_4bit_2_2
67.000000 h		
F16		FA_4bit_2_1
54.000000 h		
U3	CIVX2	tc240c
1.000000		
U4	CDLY1XL	tc240c
3.500000		
U5	CNIVX1	tc240c
1.000000		
U6	CDLY1XL	tc240c
3.500000		
U7	CNIVX1	tc240c
1.000000		

U8	CDLY1XL	tc240c
3.500000		
U9	CNIVX1	tc240c
1.000000		
U10	CDLY1XL	tc240c
3.500000		
U11	CNIVX1	tc240c
1.000000		
U12	CDLY1XL	tc240c
3.500000		
U13	CNIVX1	tc240c
1.000000		
U14	CDLY1XL	tc240c
3.500000		
U15	CNIVX1	tc240c
1.000000		
U16	CDLY1XL	tc240c
3.500000		
U17	CNIVX1	tc240c
1.000000		
U18	CDLY1XL	tc240c
3.500000		
U19	CNIVX1	tc240c
1.000000		
U20	CDLY1XL	tc240c
3.500000		
U21	CNIVX1	tc240c
1.000000		
U22	CDLY1XL	tc240c
3.500000		
U23	CNIVX1	tc240c
1.000000		
U24	CDLY1XL	tc240c
3.500000		
U25	CNIVX1	tc240c
1.000000		
U26	CDLY1XL	tc240c
3.500000		
U27	CNIVX1	tc240c
1.000000		

U28	CDLY1XL	tc240c
3.500000		
U29	CNIVX1	tc240c
1.000000		
U30	CDLY1XL	tc240c
3.500000		
U31	CNIVX1	tc240c
1.000000		
U32	CDLY1XL	tc240c
3.500000		
U33	CNIVX1	tc240c
1.000000		
U34	CDLY1XL	tc240c
3.500000		
U35	CNIVX1	tc240c
1.000000		
U36	CDLY1XL	tc240c
3.500000		
U37	CNIVX1	tc240c
1.000000		
U38	CDLY1XL	tc240c
3.500000		
U39	CNIVX1	tc240c
1.000000		
U40	CDLY1XL	tc240c
3.500000		
U41	CNIVX1	tc240c
1.000000		
U42	CDLY1XL	tc240c
3.500000		
U43	CNIVX1	tc240c
1.000000		
U44	CDLY1XL	tc240c
3.500000		
U45	CNIVX1	tc240c
1.000000		
U46	CDLY1XL	tc240c
3.500000		
U47	CNIVX1	tc240c
1.000000		

U48	CDLY1XL	tc240c
3.500000		
U49	CNIVX1	tc240c
1.000000		
U50	CDLY1XL	tc240c
3.500000		
U51	CNIVX1	tc240c
1.000000		
U52	CDLY1XL	tc240c
3.500000		
U53	CNIVX1	tc240c
1.000000		
U54	CDLY1XL	tc240c
3.500000		
U55	CNIVX1	tc240c
1.000000		
U56	CDLY1XL	tc240c
3.500000		
U57	CNIVX1	tc240c
1.000000		
U58	CDLY1XL	tc240c
3.500000		
U59	CNIVX1	tc240c
1.000000		
U60	CDLY1XL	tc240c
3.500000		
U61	CNIVX1	tc240c
1.000000		
U62	CDLY1XL	tc240c
3.500000		
U63	CNIVX1	tc240c
1.000000		
U64	CDLY1XL	tc240c
3.500000		
U65	CNIVX1	tc240c
1.000000		
U66	CDLY1XL	tc240c
3.500000		
U67	CNIVX1	tc240c
1.000000		

U68	CDLY1XL	tc240c
3.500000		
U69	CNIVX1	tc240c
1.000000		
U70	CDLY1XL	tc240c
3.500000		
U71	CNIVX1	tc240c
1.000000		
U72	CDLY1XL	tc240c
3.500000		
U73	CNIVX1	tc240c
1.000000		
U74	CDLY1XL	tc240c
3.500000		
U75	CNIVX1	tc240c
1.000000		
U76	CDLY1XL	tc240c
3.500000		
U77	CNIVX1	tc240c
1.000000		
U78	CDLY1XL	tc240c
3.500000		
U79	CNIVX1	tc240c
1.000000		
U80	CDLY1XL	tc240c
3.500000		
U81	CNIVX1	tc240c
1.000000		
U82	CDLY1XL	tc240c
3.500000		
U83	CNIVX1	tc240c
1.000000		
U84	CDLY1XL	tc240c
3.500000		
U85	CNIVX1	tc240c
1.000000		
U86	CDLY1XL	tc240c
3.500000		
U87	CNIVX1	tc240c
1.000000		

U88	CDLY1XL	tc240c
3.500000		
U89	CNIVX1	tc240c
1.000000		
U90	CDLY1XL	tc240c
3.500000		
U91	CNIVX1	tc240c
1.000000		
U92	CDLY1XL	tc240c
3.500000		
U93	CNIVX1	tc240c
1.000000		
U94	CDLY1XL	tc240c
3.500000		
U95	CNIVX1	tc240c
1.000000		
U96	CDLY1XL	tc240c
3.500000		
U97	CNIVX1	tc240c
1.000000		
U98	CDLY1XL	tc240c
3.500000		
U99	CNIVX1	tc240c
1.000000		
U100	CDLY1XL	tc240c
3.500000		
U101	CNIVX1	tc240c
1.000000		
U102	CDLY1XL	tc240c
3.500000		
U103	CNIVX1	tc240c
1.000000		
U104	CDLY1XL	tc240c
3.500000		
U105	CNIVX1	tc240c
1.000000		
U106	CDLY1XL	tc240c
3.500000		
U107	CNIVX1	tc240c
1.000000		

U108	CDLY1XL	tc240c
3.500000		
U109	CNIVX1	tc240c
1.000000		
U110	CDLY1XL	tc240c
3.500000		
U111	CNIVX1	tc240c
1.000000		
U112	CDLY1XL	tc240c
3.500000		
U113	CNIVX1	tc240c
1.000000		
U114	CDLY1XL	tc240c
3.500000		
U115	CNIVX1	tc240c
1.000000		
U116	CDLY1XL	tc240c
3.500000		
U117	CNIVX1	tc240c
1.000000		
U118	CDLY1XL	tc240c
3.500000		
U119	CNIVX1	tc240c
1.000000		
U120	CDLY1XL	tc240c
3.500000		
U121	CNIVX1	tc240c
1.000000		
U122	CDLY1XL	tc240c
3.500000		
U123	CNIVX1	tc240c
1.000000		
U124	CDLY1XL	tc240c
3.500000		
U125	CNIVX1	tc240c
1.000000		
U126	CDLY1XL	tc240c
3.500000		
U127	CNIVX1	tc240c
1.000000		

U128	CDLY1XL	tc240c
3.500000		
U129	CNIVX1	tc240c
1.000000		
U130	CDLY1XL	tc240c
3.500000		
U131	CNIVX1	tc240c
1.000000		
U132	CDLY1XL	tc240c
3.500000		
U133	CNIVX1	tc240c
1.000000		
U134	CDLY1XL	tc240c
3.500000		
U135	CNIVX1	tc240c
1.000000		
U136	CDLY1XL	tc240c
3.500000		
U137	CNIVX1	tc240c
1.000000		
U138	CDLY1XL	tc240c
3.500000		
U139	CNIVX1	tc240c
1.000000		
U140	CDLY1XL	tc240c
3.500000		
U141	CNIVX1	tc240c
1.000000		
U142	CDLY1XL	tc240c
3.500000		
U143	CNIVX1	tc240c
1.000000		
U144	CDLY1XL	tc240c
3.500000		
U145	CNIVX1	tc240c
1.000000		
U146	CDLY1XL	tc240c
3.500000		
U147	CNIVX1	tc240c
1.000000		

U148	CDLY1XL	tc240c
3.500000		
U149	CNIVX1	tc240c
1.000000		
U150	CDLY1XL	tc240c
3.500000		
U151	CNIVX1	tc240c
1.000000		
U152	CDLY1XL	tc240c
3.500000		
U153	CNIVX1	tc240c
1.000000		
U154	CDLY1XL	tc240c
3.500000		
U155	CNIVX1	tc240c
1.000000		
U156	CDLY1XL	tc240c
3.500000		
U157	CNIVX1	tc240c
1.000000		
U158	CDLY1XL	tc240c
3.500000		
U159	CNIVX1	tc240c
1.000000		
U160	CDLY1XL	tc240c
3.500000		
U161	CNIVX1	tc240c
1.000000		
U162	CDLY1XL	tc240c
3.500000		
U163	CNIVX1	tc240c
1.000000		
U164	CDLY1XL	tc240c
3.500000		
U165	CNIVX1	tc240c
1.000000		
U166	CDLY1XL	tc240c
3.500000		
U167	CNIVX1	tc240c
1.000000		

U168	CDLY1XL	tc240c
3.500000		
U169	CNIVX1	tc240c
1.000000		
U170	CDLY1XL	tc240c
3.500000		
U171	CNIVX1	tc240c
1.000000		
U172	CDLY1XL	tc240c
3.500000		
U173	CNIVX1	tc240c
1.000000		
U174	CDLY1XL	tc240c
3.500000		
U175	CNIVX1	tc240c
1.000000		
U176	CDLY1XL	tc240c
3.500000		
U177	CNIVX1	tc240c
1.000000		
U178	CDLY1XL	tc240c
3.500000		
U179	CNIVX1	tc240c
1.000000		
U180	CDLY1XL	tc240c
3.500000		
U181	CNIVX1	tc240c
1.000000		
U182	CDLY1XL	tc240c
3.500000		
U183	CNIVX1	tc240c
1.000000		
U184	CDLY1XL	tc240c
3.500000		
U185	CNIVX1	tc240c
1.000000		
U186	CDLY1XL	tc240c
3.500000		
U187	CNIVX1	tc240c
1.000000		

U188	CDLY1XL	tc240c
3.500000		
U189	CNIVX1	tc240c
1.000000		
U190	CDLY1XL	tc240c
3.500000		
U191	CNIVX1	tc240c
1.000000		
U192	CDLY1XL	tc240c
3.500000		
U193	CNIVX1	tc240c
1.000000		
U194	CDLY1XL	tc240c
3.500000		
U195	CNIVX1	tc240c
1.000000		
U196	CDLY1XL	tc240c
3.500000		
U197	CNIVX1	tc240c
1.000000		
U198	CDLY1XL	tc240c
3.500000		
U199	CNIVX1	tc240c
1.000000		
U200	CDLY1XL	tc240c
3.500000		
U201	CNIVX1	tc240c
1.000000		
U202	CDLY1XL	tc240c
3.500000		
U203	CNIVX1	tc240c
1.000000		
U204	CDLY1XL	tc240c
3.500000		
U205	CNIVX1	tc240c
1.000000		
U206	CDLY1XL	tc240c
3.500000		
U207	CNIVX1	tc240c
1.000000		

U208	CDLY1XL	tc240c
3.500000		
U209	CNIVX1	tc240c
1.000000		
U210	CDLY1XL	tc240c
3.500000		
U211	CNIVX1	tc240c
1.000000		
U212	CDLY1XL	tc240c
3.500000		
U213	CNIVX1	tc240c
1.000000		
U214	CDLY1XL	tc240c
3.500000		
U215	CNIVX1	tc240c
1.000000		
U216	CDLY1XL	tc240c
3.500000		
U217	CNIVX1	tc240c
1.000000		
U218	CDLY1XL	tc240c
3.500000		
U219	CNIVX1	tc240c
1.000000		
U220	CDLY1XL	tc240c
3.500000		
U221	CNIVX1	tc240c
1.000000		
U222	CDLY1XL	tc240c
3.500000		
U223	CNIVX1	tc240c
1.000000		
U224	CDLY1XL	tc240c
3.500000		
U225	CNIVX1	tc240c
1.000000		
U226	CDLY1XL	tc240c
3.500000		
U227	CNIVX1	tc240c
1.000000		

U228	CDLY1XL	tc240c
3.500000		
U229	CNIVX1	tc240c
1.000000		
U230	CDLY1XL	tc240c
3.500000		
U231	CNIVX1	tc240c
1.000000		
U232	CDLY1XL	tc240c
3.500000		
U233	CNIVX1	tc240c
1.000000		
U234	CDLY1XL	tc240c
3.500000		
U235	CNIVX1	tc240c
1.000000		
U236	CDLY1XL	tc240c
3.500000		
U237	CNIVX1	tc240c
1.000000		
U238	CDLY1XL	tc240c
3.500000		
U239	CNIVX1	tc240c
1.000000		
U240	CDLY1XL	tc240c
3.500000		
U241	CNIVX1	tc240c
1.000000		
U242	CDLY1XL	tc240c
3.500000		
U243	CNIVX1	tc240c
1.000000		
U244	CDLY1XL	tc240c
3.500000		
U245	CNIVX1	tc240c
1.000000		
U246	CDLY1XL	tc240c
3.500000		
U247	CNIVX1	tc240c
1.000000		

U248	CDLY1XL	tc240c
3.500000		
U249	CNIVX1	tc240c
1.000000		
U250	CDLY1XL	tc240c
3.500000		
U251	CNIVX1	tc240c
1.000000		
U252	CDLY1XL	tc240c
3.500000		
U253	CNIVX1	tc240c
1.000000		
U254	CDLY1XL	tc240c
3.500000		
U255	CNIVX1	tc240c
1.000000		
U256	CDLY1XL	tc240c
3.500000		
U257	CNIVX1	tc240c
1.000000		
U258	CDLY1XL	tc240c
3.500000		
U259	CNIVX1	tc240c
1.000000		
U260	CDLY2X2	tc240c
7.000000		
U261	CDLY2X2	tc240c
7.000000		
U262	CDLY2X2	tc240c
7.000000		
U263	CDLY2X2	tc240c
7.000000		
U264	CDLY2X2	tc240c
7.000000		
U265	CDLY2X2	tc240c
7.000000		
U266	CDLY2X2	tc240c
7.000000		
U267	CDLY2X2	tc240c
7.000000		

U268	CDLY2X2	tc240c
7.000000		
U269	CDLY2X2	tc240c
7.000000		
U270	CDLY2X2	tc240c
7.000000		
U271	CDLY2X2	tc240c
7.000000		
U272	CDLY2X2	tc240c
7.000000		
U273	CDLY2X2	tc240c
7.000000		
U274	CDLY2X2	tc240c
7.000000		
U275	CDLY2X2	tc240c
7.000000		
U276	CDLY2X2	tc240c
7.000000		
crout_reg	CFD2X2	tc240c
8.000000 n		
op1f_reg[0]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[1]	CFD2QX2	tc240c
7.500000 n		
op1f_reg[2]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[3]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[4]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[5]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[6]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[7]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[8]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[9]	CFD2QX1	tc240c
7.000000 n		

op1f_reg[10]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[11]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[12]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[13]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[14]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[15]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[16]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[17]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[18]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[19]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[20]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[21]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[22]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[23]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[24]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[25]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[26]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[27]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[28]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[29]	CFD2QX1	tc240c
7.000000 n		

op1f_reg[30]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[31]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[32]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[33]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[34]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[35]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[36]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[37]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[38]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[39]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[40]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[41]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[42]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[43]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[44]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[45]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[46]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[47]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[48]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[49]	CFD2QX1	tc240c
7.000000 n		

op1f_reg[50]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[51]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[52]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[53]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[54]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[55]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[56]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[57]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[58]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[59]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[60]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[61]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[62]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[63]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[0]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[1]	CFD2QX2	tc240c
7.500000 n		
op2f_reg[2]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[3]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[4]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[5]	CFD2QX1	tc240c
7.000000 n		

op2f_reg[6]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[7]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[8]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[9]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[10]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[11]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[12]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[13]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[14]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[15]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[16]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[17]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[18]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[19]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[20]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[21]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[22]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[23]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[24]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[25]	CFD2QX1	tc240c
7.000000 n		

op2f_reg[26]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[27]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[28]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[29]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[30]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[31]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[32]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[33]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[34]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[35]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[36]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[37]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[38]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[39]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[40]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[41]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[42]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[43]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[44]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[45]	CFD2QX1	tc240c
7.000000 n		

op2f_reg[46]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[47]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[48]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[49]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[50]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[51]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[52]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[53]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[54]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[55]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[56]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[57]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[58]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[59]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[60]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[61]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[62]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[63]	CFD2QX1	tc240c
7.000000 n		
sum_reg[0]	CFD2QX1	tc240c
7.000000 n		
sum_reg[1]	CFD2QX1	tc240c
7.000000 n		

sum_reg[2]	CFD2QX1	tc240c
7.000000 n		
sum_reg[3]	CFD2QX1	tc240c
7.000000 n		
sum_reg[4]	CFD2QX1	tc240c
7.000000 n		
sum_reg[5]	CFD2QX1	tc240c
7.000000 n		
sum_reg[6]	CFD2QX1	tc240c
7.000000 n		
sum_reg[7]	CFD2QX1	tc240c
7.000000 n		
sum_reg[8]	CFD2QX1	tc240c
7.000000 n		
sum_reg[9]	CFD2QX1	tc240c
7.000000 n		
sum_reg[10]	CFD2QX1	tc240c
7.000000 n		
sum_reg[11]	CFD2QX1	tc240c
7.000000 n		
sum_reg[12]	CFD2QX1	tc240c
7.000000 n		
sum_reg[13]	CFD2QX1	tc240c
7.000000 n		
sum_reg[14]	CFD2QX1	tc240c
7.000000 n		
sum_reg[15]	CFD2QX1	tc240c
7.000000 n		
sum_reg[16]	CFD2QX1	tc240c
7.000000 n		
sum_reg[17]	CFD2QX1	tc240c
7.000000 n		
sum_reg[18]	CFD2QX1	tc240c
7.000000 n		
sum_reg[19]	CFD2QX1	tc240c
7.000000 n		
sum_reg[20]	CFD2QX1	tc240c
7.000000 n		
sum_reg[21]	CFD2QX1	tc240c
7.000000 n		

sum_reg[22]	CFD2QXL	tc240c
5.000000 n		
sum_reg[23]	CFD2QX1	tc240c
7.000000 n		
sum_reg[24]	CFD2QX1	tc240c
7.000000 n		
sum_reg[25]	CFD2QX1	tc240c
7.000000 n		
sum_reg[26]	CFD2QX1	tc240c
7.000000 n		
sum_reg[27]	CFD2QX1	tc240c
7.000000 n		
sum_reg[28]	CFD2QX1	tc240c
7.000000 n		
sum_reg[29]	CFD2QX1	tc240c
7.000000 n		
sum_reg[30]	CFD2QX1	tc240c
7.000000 n		
sum_reg[31]	CFD2QX1	tc240c
7.000000 n		
sum_reg[32]	CFD2QXL	tc240c
5.000000 n		
sum_reg[33]	CFD2QX1	tc240c
7.000000 n		
sum_reg[34]	CFD2QX1	tc240c
7.000000 n		
sum_reg[35]	CFD2QX1	tc240c
7.000000 n		
sum_reg[36]	CFD2QX1	tc240c
7.000000 n		
sum_reg[37]	CFD2QXL	tc240c
5.000000 n		
sum_reg[38]	CFD2QX1	tc240c
7.000000 n		
sum_reg[39]	CFD2QX1	tc240c
7.000000 n		
sum_reg[40]	CFD2QX1	tc240c
7.000000 n		
sum_reg[41]	CFD2QX1	tc240c
7.000000 n		

sum_reg[42]	CFD2QXL	tc240c
5.000000 n		
sum_reg[43]	CFD2QX1	tc240c
7.000000 n		
sum_reg[44]	CFD2QX1	tc240c
7.000000 n		
sum_reg[45]	CFD2QX1	tc240c
7.000000 n		
sum_reg[46]	CFD2QX1	tc240c
7.000000 n		
sum_reg[47]	CFD2QXL	tc240c
5.000000 n		
sum_reg[48]	CFD2QX1	tc240c
7.000000 n		
sum_reg[49]	CFD2QX1	tc240c
7.000000 n		
sum_reg[50]	CFD2QXL	tc240c
5.000000 n		
sum_reg[51]	CFD2QXL	tc240c
5.000000 n		
sum_reg[52]	CFD2QXL	tc240c
5.000000 n		
sum_reg[53]	CFD2QXL	tc240c
5.000000 n		
sum_reg[54]	CFD2QXL	tc240c
5.000000 n		
sum_reg[55]	CFD2QX1	tc240c
7.000000 n		
sum_reg[56]	CFD2QXL	tc240c
5.000000 n		
sum_reg[57]	CFD2QXL	tc240c
5.000000 n		
sum_reg[58]	CFD2QX1	tc240c
7.000000 n		
sum_reg[59]	CFD2QX1	tc240c
7.000000 n		
sum_reg[60]	CFD2QX1	tc240c
7.000000 n		
sum_reg[61]	CFD2QX2	tc240c
7.500000 n		

```

sum_reg[62]          CFD2QXL      tc240c
5.000000  n
sum_reg[63]          CFD2QXL      tc240c
5.000000  n
-----
-----
Total                483          cells
3131.000000
1
report_timing -max_paths 5
*****
Report : timing
    -path full
    -delay max
    -max_paths 5
Design : RCA64
Version: C-2009.06-SP5
Date   : Wed Dec  2 22:10:53 2015
*****


Operating Conditions: WCCOM25    Library: tc240c
Wire Load Model Mode: top

Startpoint: op2f_reg[1]
            (rising edge-triggered flip-flop clocked
by clock)
Endpoint: sum_reg[63]
            (rising edge-triggered flip-flop clocked by
clock)
Path Group: clock
Path Type: max

Point           Incr
Path
-----
-----
clock  clock  (rise edge)          0.00
0.00

```

clock network delay (propagated)	0.00
0.00	
op2f_reg[1]/CP (CFD2QX2)	0.00
0.00 r	
op2f_reg[1]/Q (CFD2QX2)	0.50
0.50 f	
F1/op2_fa4[1] (FA_4bit_1)	0.00
0.50 f	
F1/f1/op2_fa1 (FA_1bit_0)	0.00
0.50 f	
F1/f1/h1/op2_ha (HA_126)	0.00
0.50 f	
F1/f1/h1/U2/Z (CIVX2)	0.08
0.58 r	
F1/f1/h1/U4/Z (CND2X2)	0.09
0.67 f	
F1/f1/h1/U5/Z (CND2X2)	0.09
0.76 r	
F1/f1/h1/sum_ha (HA_126)	0.00
0.76 r	
F1/f1/h2/op1_ha (HA_125)	0.00
0.76 r	
F1/f1/h2/U1/Z (CND2X2)	0.09
0.85 f	
F1/f1/h2/U2/Z (CIVX2)	0.06
0.91 r	
F1/f1/h2/cout_ha (HA_125)	0.00
0.91 r	
F1/f1/U2/Z (CIVX2)	0.06
0.98 f	
F1/f1/U1/Z (CND2IX2)	0.07
1.05 r	
F1/f1/cout_fa1 (FA_1bit_0)	0.00
1.05 r	
F1/f2/cin (FA_1bit_62)	0.00
1.05 r	
F1/f2/h2/op2_ha (HA_123)	0.00
1.05 r	
F1/f2/h2/U1/Z (CND2X2)	0.09
1.14 f	

F1/f2/h2/U2/Z (CIVX2)	0.06
1.20 r	
F1/f2/h2/cout_ha (HA_123)	0.00
1.20 r	
F1/f2/U2/Z (CIVX2)	0.06
1.27 f	
F1/f2/U1/Z (CND2IX2)	0.07
1.34 r	
F1/f2/cout_fa1 (FA_1bit_62)	0.00
1.34 r	
F1/f3/cin (FA_1bit_61)	0.00
1.34 r	
F1/f3/h2/op2_ha (HA_121)	0.00
1.34 r	
F1/f3/h2/U1/Z (CND2X2)	0.09
1.43 f	
F1/f3/h2/U2/Z (CIVX2)	0.06
1.49 r	
F1/f3/h2/cout_ha (HA_121)	0.00
1.49 r	
F1/f3/U1/Z (CNR2IX2)	0.07
1.56 f	
F1/f3/U2/Z (CIVX2)	0.07
1.63 r	
F1/f3/cout_fa1 (FA_1bit_61)	0.00
1.63 r	
F1/cout_fa4 (FA_4bit_1)	0.00
1.63 r	
F2/cin_fa4 (FA_4bit_2_0)	0.00
1.63 r	
F2/f1/cin (FA_1bit_60)	0.00
1.63 r	
F2/f1/h2/op2_ha (HA_119)	0.00
1.63 r	
F2/f1/h2/U1/Z (CND2X2)	0.09
1.72 f	
F2/f1/h2/U2/Z (CIVX2)	0.06
1.78 r	
F2/f1/h2/cout_ha (HA_119)	0.00
1.78 r	

F2/f1/U1/Z (CNR2IX2)	0.07
1.85 f	
F2/f1/U2/Z (CIVX2)	0.07
1.91 r	
F2/f1/cout_fa1 (FA_1bit_60)	0.00
1.91 r	
F2/f2/cin (FA_1bit_59)	0.00
1.91 r	
F2/f2/h2/op2_ha (HA_117)	0.00
1.91 r	
F2/f2/h2/U1/Z (CND2X2)	0.09
2.00 f	
F2/f2/h2/U2/Z (CIVX2)	0.06
2.07 r	
F2/f2/h2/cout_ha (HA_117)	0.00
2.07 r	
F2/f2/U1/Z (CNR2IX2)	0.07
2.13 f	
F2/f2/U2/Z (CIVX2)	0.07
2.20 r	
F2/f2/cout_fa1 (FA_1bit_59)	0.00
2.20 r	
F2/f3/cin (FA_1bit_58)	0.00
2.20 r	
F2/f3/h2/op2_ha (HA_115)	0.00
2.20 r	
F2/f3/h2/U1/Z (CND2X2)	0.09
2.29 f	
F2/f3/h2/U2/Z (CIVX2)	0.06
2.35 r	
F2/f3/h2/cout_ha (HA_115)	0.00
2.35 r	
F2/f3/U1/Z (CNR2IX2)	0.07
2.42 f	
F2/f3/U3/Z (CIVX2)	0.07
2.49 r	
F2/f3/cout_fa1 (FA_1bit_58)	0.00
2.49 r	
F2/f4/cin (FA_1bit_57)	0.00
2.49 r	

F2/f4/h2/op2_ha (HA_113)	0.00
2.49 r	
F2/f4/h2/U2/Z (CND2X2)	0.09
2.58 f	
F2/f4/h2/U3/Z (CIVX2)	0.06
2.64 r	
F2/f4/h2/cout_ha (HA_113)	0.00
2.64 r	
F2/f4/U1/Z (CNR2IX2)	0.07
2.71 f	
F2/f4/U2/Z (CIVX2)	0.07
2.77 r	
F2/f4/cout_fa1 (FA_1bit_57)	0.00
2.77 r	
F2/cout_fa4_2 (FA_4bit_2_0)	0.00
2.77 r	
F3/cin_fa4 (FA_4bit_2_14)	0.00
2.77 r	
F3/f1/cin (FA_1bit_56)	0.00
2.77 r	
F3/f1/h2/op2_ha (HA_111)	0.00
2.77 r	
F3/f1/h2/U1/Z (CND2X2)	0.09
2.86 f	
F3/f1/h2/U2/Z (CIVX2)	0.06
2.93 r	
F3/f1/h2/cout_ha (HA_111)	0.00
2.93 r	
F3/f1/U1/Z (CNR2IX2)	0.07
2.99 f	
F3/f1/U2/Z (CIVX2)	0.07
3.06 r	
F3/f1/cout_fa1 (FA_1bit_56)	0.00
3.06 r	
F3/f2/cin (FA_1bit_55)	0.00
3.06 r	
F3/f2/h2/op2_ha (HA_109)	0.00
3.06 r	
F3/f2/h2/U1/Z (CND2X2)	0.09
3.15 f	

F3/f2/h2/U2/Z (CIVX2)	0.06
3.21 r	
F3/f2/h2/cout_ha (HA_109)	0.00
3.21 r	
F3/f2/U2/Z (CIVX2)	0.06
3.27 f	
F3/f2/U1/Z (CND2IX2)	0.07
3.35 r	
F3/f2/cout_fa1 (FA_1bit_55)	0.00
3.35 r	
F3/f3/cin (FA_1bit_54)	0.00
3.35 r	
F3/f3/h2/op2_ha (HA_107)	0.00
3.35 r	
F3/f3/h2/U1/Z (CND2X2)	0.09
3.44 f	
F3/f3/h2/U2/Z (CIVX2)	0.06
3.50 r	
F3/f3/h2/cout_ha (HA_107)	0.00
3.50 r	
F3/f3/U1/Z (CNR2IX2)	0.07
3.57 f	
F3/f3/U2/Z (CIVX2)	0.07
3.64 r	
F3/f3/cout_fa1 (FA_1bit_54)	0.00
3.64 r	
F3/f4/cin (FA_1bit_53)	0.00
3.64 r	
F3/f4/h2/op2_ha (HA_105)	0.00
3.64 r	
F3/f4/h2/U1/Z (CND2X2)	0.09
3.72 f	
F3/f4/h2/U2/Z (CIVX2)	0.06
3.79 r	
F3/f4/h2/cout_ha (HA_105)	0.00
3.79 r	
F3/f4/U1/Z (CNR2IX2)	0.07
3.85 f	
F3/f4/U2/Z (CIVX2)	0.07
3.92 r	

F3/f4/cout_fa1 (FA_1bit_53)	0.00
3.92 r	
F3/cout_fa4_2 (FA_4bit_2_14)	0.00
3.92 r	
F4/cin_fa4 (FA_4bit_2_13)	0.00
3.92 r	
F4/f1/cin (FA_1bit_52)	0.00
3.92 r	
F4/f1/h2/op2_ha (HA_103)	0.00
3.92 r	
F4/f1/h2/U1/Z (CND2X2)	0.09
4.01 f	
F4/f1/h2/U2/Z (CIVX2)	0.06
4.07 r	
F4/f1/h2/cout_ha (HA_103)	0.00
4.07 r	
F4/f1/U1/Z (CNR2IX2)	0.07
4.14 f	
F4/f1/U3/Z (CIVX2)	0.07
4.21 r	
F4/f1/cout_fa1 (FA_1bit_52)	0.00
4.21 r	
F4/f2/cin (FA_1bit_51)	0.00
4.21 r	
F4/f2/h2/op2_ha (HA_101)	0.00
4.21 r	
F4/f2/h2/U1/Z (CND2X2)	0.09
4.30 f	
F4/f2/h2/U2/Z (CIVX2)	0.06
4.36 r	
F4/f2/h2/cout_ha (HA_101)	0.00
4.36 r	
F4/f2/U1/Z (CNR2IX2)	0.07
4.43 f	
F4/f2/U2/Z (CIVX2)	0.07
4.49 r	
F4/f2/cout_fa1 (FA_1bit_51)	0.00
4.49 r	
F4/f3/cin (FA_1bit_50)	0.00
4.49 r	

F4/f3/h2/op2_ha (HA_99)	0.00
4.49 r	
F4/f3/h2/U1/Z (CND2X2)	0.09
4.58 f	
F4/f3/h2/U2/Z (CIVX2)	0.06
4.65 r	
F4/f3/h2/cout_ha (HA_99)	0.00
4.65 r	
F4/f3/U1/Z (CNR2IX2)	0.07
4.71 f	
F4/f3/U2/Z (CIVX2)	0.07
4.78 r	
F4/f3/cout_fa1 (FA_1bit_50)	0.00
4.78 r	
F4/f4/cin (FA_1bit_49)	0.00
4.78 r	
F4/f4/h2/op2_ha (HA_97)	0.00
4.78 r	
F4/f4/h2/U1/Z (CND2X2)	0.09
4.87 f	
F4/f4/h2/U2/Z (CIVX2)	0.06
4.93 r	
F4/f4/h2/cout_ha (HA_97)	0.00
4.93 r	
F4/f4/U1/Z (CNR2IX2)	0.07
5.00 f	
F4/f4/U2/Z (CIVX2)	0.07
5.07 r	
F4/f4/cout_fa1 (FA_1bit_49)	0.00
5.07 r	
F4/cout_fa4_2 (FA_4bit_2_13)	0.00
5.07 r	
F5/cin_fa4 (FA_4bit_2_12)	0.00
5.07 r	
F5/f1/cin (FA_1bit_48)	0.00
5.07 r	
F5/f1/h2/op2_ha (HA_95)	0.00
5.07 r	
F5/f1/h2/U1/Z (CND2X2)	0.09
5.16 f	

F5/f1/h2/U2/Z (CIVX2)	0.06
5.22 r	
F5/f1/h2/cout_ha (HA_95)	0.00
5.22 r	
F5/f1/U2/Z (CIVX2)	0.06
5.28 f	
F5/f1/U1/Z (CND2IX2)	0.07
5.35 r	
F5/f1/cout_fa1 (FA_1bit_48)	0.00
5.35 r	
F5/f2/cin (FA_1bit_47)	0.00
5.35 r	
F5/f2/h2/op2_ha (HA_93)	0.00
5.35 r	
F5/f2/h2/U1/Z (CND2X2)	0.09
5.45 f	
F5/f2/h2/U2/Z (CIVX2)	0.06
5.51 r	
F5/f2/h2/cout_ha (HA_93)	0.00
5.51 r	
F5/f2/U1/Z (CNR2IX2)	0.07
5.58 f	
F5/f2/U2/Z (CIVX2)	0.07
5.64 r	
F5/f2/cout_fa1 (FA_1bit_47)	0.00
5.64 r	
F5/f3/cin (FA_1bit_46)	0.00
5.64 r	
F5/f3/h2/op2_ha (HA_91)	0.00
5.64 r	
F5/f3/h2/U1/Z (CND2X2)	0.09
5.73 f	
F5/f3/h2/U2/Z (CIVX2)	0.06
5.79 r	
F5/f3/h2/cout_ha (HA_91)	0.00
5.79 r	
F5/f3/U1/Z (CNR2IX2)	0.07
5.86 f	
F5/f3/U2/Z (CIVX2)	0.07
5.93 r	

F5/f3/cout_fa1 (FA_1bit_46)	0.00
5.93 r	
F5/f4/cin (FA_1bit_45)	0.00
5.93 r	
F5/f4/h2/op2_ha (HA_89)	0.00
5.93 r	
F5/f4/h2/U1/Z (CND2X2)	0.09
6.02 f	
F5/f4/h2/U2/Z (CIVX2)	0.06
6.08 r	
F5/f4/h2/cout_ha (HA_89)	0.00
6.08 r	
F5/f4/U2/Z (CIVX2)	0.06
6.14 f	
F5/f4/U1/Z (CND2IX2)	0.07
6.22 r	
F5/f4/cout_fa1 (FA_1bit_45)	0.00
6.22 r	
F5/cout_fa4_2 (FA_4bit_2_12)	0.00
6.22 r	
F6/cin_fa4 (FA_4bit_2_11)	0.00
6.22 r	
F6/f1/cin (FA_1bit_44)	0.00
6.22 r	
F6/f1/h2/op2_ha (HA_87)	0.00
6.22 r	
F6/f1/h2/U1/Z (CND2X2)	0.09
6.31 f	
F6/f1/h2/U2/Z (CIVX2)	0.06
6.37 r	
F6/f1/h2/cout_ha (HA_87)	0.00
6.37 r	
F6/f1/U1/Z (CNR2IX2)	0.07
6.44 f	
F6/f1/U2/Z (CIVX2)	0.07
6.50 r	
F6/f1/cout_fa1 (FA_1bit_44)	0.00
6.50 r	
F6/f2/cin (FA_1bit_43)	0.00
6.50 r	

F6/f2/h2/op2_ha (HA_85)	0.00
6.50 r	
F6/f2/h2/U1/Z (CND2X2)	0.09
6.59 f	
F6/f2/h2/U2/Z (CIVX2)	0.06
6.66 r	
F6/f2/h2/cout_ha (HA_85)	0.00
6.66 r	
F6/f2/U1/Z (CNR2IX2)	0.07
6.72 f	
F6/f2/U2/Z (CIVX2)	0.07
6.79 r	
F6/f2/cout_fa1 (FA_1bit_43)	0.00
6.79 r	
F6/f3/cin (FA_1bit_42)	0.00
6.79 r	
F6/f3/h2/op2_ha (HA_83)	0.00
6.79 r	
F6/f3/h2/U1/Z (CND2X2)	0.09
6.88 f	
F6/f3/h2/U2/Z (CIVX2)	0.06
6.94 r	
F6/f3/h2/cout_ha (HA_83)	0.00
6.94 r	
F6/f3/U1/Z (CNR2IX2)	0.07
7.01 f	
F6/f3/U3/Z (CIVX2)	0.07
7.08 r	
F6/f3/cout_fa1 (FA_1bit_42)	0.00
7.08 r	
F6/f4/cin (FA_1bit_41)	0.00
7.08 r	
F6/f4/h2/op2_ha (HA_81)	0.00
7.08 r	
F6/f4/h2/U1/Z (CND2X2)	0.09
7.17 f	
F6/f4/h2/U2/Z (CIVX2)	0.06
7.23 r	
F6/f4/h2/cout_ha (HA_81)	0.00
7.23 r	

F6/f4/U1/Z (CNR2IX2)	0.07
7.30 f	
F6/f4/U2/Z (CIVX2)	0.07
7.36 r	
F6/f4/cout_fa1 (FA_1bit_41)	0.00
7.36 r	
F6/cout_fa4_2 (FA_4bit_2_11)	0.00
7.36 r	
F7/cin_fa4 (FA_4bit_2_10)	0.00
7.36 r	
F7/f1/cin (FA_1bit_40)	0.00
7.36 r	
F7/f1/h2/op2_ha (HA_79)	0.00
7.36 r	
F7/f1/h2/U1/Z (CND2X2)	0.09
7.45 f	
F7/f1/h2/U2/Z (CIVX2)	0.06
7.52 r	
F7/f1/h2/cout_ha (HA_79)	0.00
7.52 r	
F7/f1/U1/Z (CNR2IX2)	0.07
7.58 f	
F7/f1/U2/Z (CIVX2)	0.07
7.65 r	
F7/f1/cout_fa1 (FA_1bit_40)	0.00
7.65 r	
F7/f2/cin (FA_1bit_39)	0.00
7.65 r	
F7/f2/h2/op2_ha (HA_77)	0.00
7.65 r	
F7/f2/h2/U1/Z (CND2X2)	0.09
7.74 f	
F7/f2/h2/U2/Z (CIVX2)	0.06
7.80 r	
F7/f2/h2/cout_ha (HA_77)	0.00
7.80 r	
F7/f2/U1/Z (CNR2IX2)	0.07
7.87 f	
F7/f2/U3/Z (CIVX2)	0.07
7.94 r	

F7/f2/cout_fa1 (FA_1bit_39)	0.00
7.94 r	
F7/f3/cin (FA_1bit_38)	0.00
7.94 r	
F7/f3/h2/op2_ha (HA_75)	0.00
7.94 r	
F7/f3/h2/U1/Z (CND2X2)	0.09
8.02 f	
F7/f3/h2/U2/Z (CIVX2)	0.06
8.09 r	
F7/f3/h2/cout_ha (HA_75)	0.00
8.09 r	
F7/f3/U2/Z (CIVX2)	0.06
8.15 f	
F7/f3/U1/Z (CND2IX2)	0.07
8.22 r	
F7/f3/cout_fa1 (FA_1bit_38)	0.00
8.22 r	
F7/f4/cin (FA_1bit_37)	0.00
8.22 r	
F7/f4/h2/op2_ha (HA_73)	0.00
8.22 r	
F7/f4/h2/U1/Z (CND2X2)	0.09
8.31 f	
F7/f4/h2/U2/Z (CIVX2)	0.06
8.38 r	
F7/f4/h2/cout_ha (HA_73)	0.00
8.38 r	
F7/f4/U1/Z (CNR2IX2)	0.07
8.44 f	
F7/f4/U3/Z (CIVX2)	0.07
8.51 r	
F7/f4/cout_fa1 (FA_1bit_37)	0.00
8.51 r	
F7/cout_fa4_2 (FA_4bit_2_10)	0.00
8.51 r	
F8/cin_fa4 (FA_4bit_2_9)	0.00
8.51 r	
F8/f1/cin (FA_1bit_36)	0.00
8.51 r	

F8/f1/h2/op2_ha (HA_71)	0.00
8.51 r	
F8/f1/h2/U1/Z (CND2X2)	0.09
8.60 f	
F8/f1/h2/U2/Z (CIVX2)	0.06
8.66 r	
F8/f1/h2/cout_ha (HA_71)	0.00
8.66 r	
F8/f1/U2/Z (CIVX2)	0.06
8.73 f	
F8/f1/U1/Z (CND2IX2)	0.07
8.80 r	
F8/f1/cout_fa1 (FA_1bit_36)	0.00
8.80 r	
F8/f2/cin (FA_1bit_35)	0.00
8.80 r	
F8/f2/h2/op2_ha (HA_69)	0.00
8.80 r	
F8/f2/h2/U1/Z (CND2X2)	0.09
8.89 f	
F8/f2/h2/U2/Z (CIVX2)	0.06
8.95 r	
F8/f2/h2/cout_ha (HA_69)	0.00
8.95 r	
F8/f2/U2/Z (CIVX2)	0.06
9.02 f	
F8/f2/U1/Z (CND2IX2)	0.07
9.09 r	
F8/f2/cout_fa1 (FA_1bit_35)	0.00
9.09 r	
F8/f3/cin (FA_1bit_34)	0.00
9.09 r	
F8/f3/h2/op2_ha (HA_67)	0.00
9.09 r	
F8/f3/h2/U2/Z (CIVX2)	0.07
9.16 f	
F8/f3/h2/U1/Z (CNR2X2)	0.11
9.27 r	
F8/f3/h2/cout_ha (HA_67)	0.00
9.27 r	

F8/f3/U2/Z (CIVX2)	0.08
9.36 f	
F8/f3/U1/Z (CND2IX2)	0.07
9.43 r	
F8/f3/cout_fa1 (FA_1bit_34)	0.00
9.43 r	
F8/f4/cin (FA_1bit_33)	0.00
9.43 r	
F8/f4/h2/op2_ha (HA_65)	0.00
9.43 r	
F8/f4/h2/U2/Z (CIVX2)	0.07
9.50 f	
F8/f4/h2/U1/Z (CNR2X2)	0.11
9.61 r	
F8/f4/h2/cout_ha (HA_65)	0.00
9.61 r	
F8/f4/U2/Z (CIVX2)	0.08
9.70 f	
F8/f4/U1/Z (CND2IX2)	0.07
9.77 r	
F8/f4/cout_fa1 (FA_1bit_33)	0.00
9.77 r	
F8/cout_fa4_2 (FA_4bit_2_9)	0.00
9.77 r	
F9/cin_fa4 (FA_4bit_2_8)	0.00
9.77 r	
F9/f1/cin (FA_1bit_32)	0.00
9.77 r	
F9/f1/h2/op2_ha (HA_63)	0.00
9.77 r	
F9/f1/h2/U2/Z (CIVX2)	0.07
9.84 f	
F9/f1/h2/U1/Z (CNR2X2)	0.11
9.95 r	
F9/f1/h2/cout_ha (HA_63)	0.00
9.95 r	
F9/f1/U2/Z (CIVX2)	0.08
10.04 f	
F9/f1/U1/Z (CND2IX2)	0.07
10.11 r	

F9/f1/cout_fa1 (FA_1bit_32)	0.00
10.11 r	
F9/f2/cin (FA_1bit_31)	0.00
10.11 r	
F9/f2/h2/op2_ha (HA_61)	0.00
10.11 r	
F9/f2/h2/U2/Z (CIVX2)	0.07
10.18 f	
F9/f2/h2/U1/Z (CNR2X2)	0.11
10.29 r	
F9/f2/h2/cout_ha (HA_61)	0.00
10.29 r	
F9/f2/U2/Z (CIVX2)	0.08
10.38 f	
F9/f2/U1/Z (CND2IX2)	0.07
10.45 r	
F9/f2/cout_fa1 (FA_1bit_31)	0.00
10.45 r	
F9/f3/cin (FA_1bit_30)	0.00
10.45 r	
F9/f3/h2/op2_ha (HA_59)	0.00
10.45 r	
F9/f3/h2/U2/Z (CIVX2)	0.07
10.52 f	
F9/f3/h2/U1/Z (CNR2X2)	0.11
10.63 r	
F9/f3/h2/cout_ha (HA_59)	0.00
10.63 r	
F9/f3/U2/Z (CIVX2)	0.08
10.72 f	
F9/f3/U1/Z (CND2IX2)	0.07
10.79 r	
F9/f3/cout_fa1 (FA_1bit_30)	0.00
10.79 r	
F9/f4/cin (FA_1bit_29)	0.00
10.79 r	
F9/f4/h2/op2_ha (HA_57)	0.00
10.79 r	
F9/f4/h2/U2/Z (CIVX2)	0.07
10.86 f	

F9/f4/h2/U1/Z (CNR2X2)	0.11
10.97 r	
F9/f4/h2/cout_ha (HA_57)	0.00
10.97 r	
F9/f4/U2/Z (CIVX2)	0.08
11.06 f	
F9/f4/U1/Z (CND2IX2)	0.07
11.13 r	
F9/f4/cout_fa1 (FA_1bit_29)	0.00
11.13 r	
F9/cout_fa4_2 (FA_4bit_2_8)	0.00
11.13 r	
F10/cin_fa4 (FA_4bit_2_7)	0.00
11.13 r	
F10/f1/cin (FA_1bit_28)	0.00
11.13 r	
F10/f1/h2/op2_ha (HA_55)	0.00
11.13 r	
F10/f1/h2/U2/Z (CIVX2)	0.07
11.20 f	
F10/f1/h2/U1/Z (CNR2X2)	0.11
11.31 r	
F10/f1/h2/cout_ha (HA_55)	0.00
11.31 r	
F10/f1/U2/Z (CIVX2)	0.08
11.40 f	
F10/f1/U1/Z (CND2IX2)	0.07
11.47 r	
F10/f1/cout_fa1 (FA_1bit_28)	0.00
11.47 r	
F10/f2/cin (FA_1bit_27)	0.00
11.47 r	
F10/f2/h2/op2_ha (HA_53)	0.00
11.47 r	
F10/f2/h2/U2/Z (CIVX2)	0.07
11.54 f	
F10/f2/h2/U1/Z (CNR2X2)	0.11
11.65 r	
F10/f2/h2/cout_ha (HA_53)	0.00
11.65 r	

F10/f2/U2/Z (CIVX2)	0.08
11.74 f	
F10/f2/U1/Z (CND2IX2)	0.07
11.81 r	
F10/f2/cout_fa1 (FA_1bit_27)	0.00
11.81 r	
F10/f3/cin (FA_1bit_26)	0.00
11.81 r	
F10/f3/h2/op2_ha (HA_51)	0.00
11.81 r	
F10/f3/h2/U2/Z (CIVX2)	0.07
11.88 f	
F10/f3/h2/U1/Z (CNR2X2)	0.11
11.99 r	
F10/f3/h2/cout_ha (HA_51)	0.00
11.99 r	
F10/f3/U2/Z (CIVX2)	0.08
12.08 f	
F10/f3/U1/Z (CND2IX2)	0.07
12.15 r	
F10/f3/cout_fa1 (FA_1bit_26)	0.00
12.15 r	
F10/f4/cin (FA_1bit_25)	0.00
12.15 r	
F10/f4/h2/op2_ha (HA_49)	0.00
12.15 r	
F10/f4/h2/U2/Z (CIVX2)	0.07
12.22 f	
F10/f4/h2/U1/Z (CNR2X2)	0.11
12.33 r	
F10/f4/h2/cout_ha (HA_49)	0.00
12.33 r	
F10/f4/U2/Z (CIVX2)	0.08
12.42 f	
F10/f4/U1/Z (CND2IX2)	0.07
12.49 r	
F10/f4/cout_fa1 (FA_1bit_25)	0.00
12.49 r	
F10/cout_fa4_2 (FA_4bit_2_7)	0.00
12.49 r	

F11/cin_fa4 (FA_4bit_2_6)	0.00
12.49 r	
F11/f1/cin (FA_1bit_24)	0.00
12.49 r	
F11/f1/h2/op2_ha (HA_47)	0.00
12.49 r	
F11/f1/h2/U2/Z (CIVX2)	0.07
12.56 f	
F11/f1/h2/U1/Z (CNR2X2)	0.11
12.67 r	
F11/f1/h2/cout_ha (HA_47)	0.00
12.67 r	
F11/f1/U2/Z (CIVX2)	0.08
12.76 f	
F11/f1/U1/Z (CND2IX2)	0.07
12.83 r	
F11/f1/cout_fa1 (FA_1bit_24)	0.00
12.83 r	
F11/f2/cin (FA_1bit_23)	0.00
12.83 r	
F11/f2/h2/op2_ha (HA_45)	0.00
12.83 r	
F11/f2/h2/U2/Z (CIVX2)	0.07
12.90 f	
F11/f2/h2/U1/Z (CNR2X2)	0.11
13.01 r	
F11/f2/h2/cout_ha (HA_45)	0.00
13.01 r	
F11/f2/U2/Z (CIVX2)	0.08
13.10 f	
F11/f2/U1/Z (CND2IX2)	0.07
13.17 r	
F11/f2/cout_fa1 (FA_1bit_23)	0.00
13.17 r	
F11/f3/cin (FA_1bit_22)	0.00
13.17 r	
F11/f3/h2/op2_ha (HA_43)	0.00
13.17 r	
F11/f3/h2/U2/Z (CIVX2)	0.07
13.24 f	

F11/f3/h2/U1/Z (CNR2X2)	0.11
13.35 r	
F11/f3/h2/cout_ha (HA_43)	0.00
13.35 r	
F11/f3/U2/Z (CIVX2)	0.08
13.44 f	
F11/f3/U1/Z (CND2IX2)	0.07
13.51 r	
F11/f3/cout_fa1 (FA_1bit_22)	0.00
13.51 r	
F11/f4/cin (FA_1bit_21)	0.00
13.51 r	
F11/f4/h2/op2_ha (HA_41)	0.00
13.51 r	
F11/f4/h2/U2/Z (CIVX2)	0.07
13.58 f	
F11/f4/h2/U1/Z (CNR2X2)	0.11
13.69 r	
F11/f4/h2/cout_ha (HA_41)	0.00
13.69 r	
F11/f4/U2/Z (CIVX2)	0.08
13.78 f	
F11/f4/U1/Z (CND2IX2)	0.07
13.85 r	
F11/f4/cout_fa1 (FA_1bit_21)	0.00
13.85 r	
F11/cout_fa4_2 (FA_4bit_2_6)	0.00
13.85 r	
F12/cin_fa4 (FA_4bit_2_5)	0.00
13.85 r	
F12/f1/cin (FA_1bit_20)	0.00
13.85 r	
F12/f1/h2/op2_ha (HA_39)	0.00
13.85 r	
F12/f1/h2/U2/Z (CIVX2)	0.07
13.92 f	
F12/f1/h2/U1/Z (CNR2X2)	0.11
14.03 r	
F12/f1/h2/cout_ha (HA_39)	0.00
14.03 r	

F12/f1/U2/Z (CIVX2)	0.08
14.12 f	
F12/f1/U1/Z (CND2IX2)	0.07
14.19 r	
F12/f1/cout_fa1 (FA_1bit_20)	0.00
14.19 r	
F12/f2/cin (FA_1bit_19)	0.00
14.19 r	
F12/f2/h2/op2_ha (HA_37)	0.00
14.19 r	
F12/f2/h2/U2/Z (CIVX2)	0.07
14.26 f	
F12/f2/h2/U1/Z (CNR2X2)	0.11
14.37 r	
F12/f2/h2/cout_ha (HA_37)	0.00
14.37 r	
F12/f2/U2/Z (CIVX2)	0.08
14.46 f	
F12/f2/U1/Z (CND2IX2)	0.07
14.53 r	
F12/f2/cout_fa1 (FA_1bit_19)	0.00
14.53 r	
F12/f3/cin (FA_1bit_18)	0.00
14.53 r	
F12/f3/h2/op2_ha (HA_35)	0.00
14.53 r	
F12/f3/h2/U2/Z (CIVX2)	0.07
14.60 f	
F12/f3/h2/U1/Z (CNR2X2)	0.11
14.71 r	
F12/f3/h2/cout_ha (HA_35)	0.00
14.71 r	
F12/f3/U2/Z (CIVX2)	0.08
14.80 f	
F12/f3/U1/Z (CND2IX2)	0.07
14.87 r	
F12/f3/cout_fa1 (FA_1bit_18)	0.00
14.87 r	
F12/f4/cin (FA_1bit_17)	0.00
14.87 r	

F12/f4/h2/op2_ha (HA_33)	0.00
14.87 r	
F12/f4/h2/U2/Z (CIVX2)	0.07
14.94 f	
F12/f4/h2/U1/Z (CNR2X2)	0.11
15.05 r	
F12/f4/h2/cout_ha (HA_33)	0.00
15.05 r	
F12/f4/U2/Z (CIVX2)	0.08
15.14 f	
F12/f4/U1/Z (CND2IX2)	0.07
15.21 r	
F12/f4/cout_fa1 (FA_1bit_17)	0.00
15.21 r	
F12/cout_fa4_2 (FA_4bit_2_5)	0.00
15.21 r	
F13/cin_fa4 (FA_4bit_2_4)	0.00
15.21 r	
F13/f1/cin (FA_1bit_16)	0.00
15.21 r	
F13/f1/h2/op2_ha (HA_31)	0.00
15.21 r	
F13/f1/h2/U2/Z (CIVX2)	0.07
15.28 f	
F13/f1/h2/U1/Z (CNR2X2)	0.11
15.39 r	
F13/f1/h2/cout_ha (HA_31)	0.00
15.39 r	
F13/f1/U2/Z (CIVX2)	0.08
15.48 f	
F13/f1/U1/Z (CND2IX2)	0.07
15.55 r	
F13/f1/cout_fa1 (FA_1bit_16)	0.00
15.55 r	
F13/f2/cin (FA_1bit_15)	0.00
15.55 r	
F13/f2/h2/op2_ha (HA_29)	0.00
15.55 r	
F13/f2/h2/U2/Z (CIVX2)	0.07
15.62 f	

F13/f2/h2/U1/Z (CNR2X2)	0.11
15.73 r	
F13/f2/h2/cout_ha (HA_29)	0.00
15.73 r	
F13/f2/U2/Z (CIVX2)	0.08
15.82 f	
F13/f2/U1/Z (CND2IX2)	0.07
15.89 r	
F13/f2/cout_fa1 (FA_1bit_15)	0.00
15.89 r	
F13/f3/cin (FA_1bit_14)	0.00
15.89 r	
F13/f3/h2/op2_ha (HA_27)	0.00
15.89 r	
F13/f3/h2/U2/Z (CIVX2)	0.07
15.96 f	
F13/f3/h2/U1/Z (CNR2X2)	0.10
16.06 r	
F13/f3/h2/cout_ha (HA_27)	0.00
16.06 r	
F13/f3/U1/Z (CNR2IX1)	0.10
16.16 f	
F13/f3/U3/Z (CIVX2)	0.09
16.24 r	
F13/f3/cout_fa1 (FA_1bit_14)	0.00
16.24 r	
F13/f4/cin (FA_1bit_13)	0.00
16.24 r	
F13/f4/h2/op2_ha (HA_25)	0.00
16.24 r	
F13/f4/h2/U1/Z (CND2X2)	0.10
16.34 f	
F13/f4/h2/U2/Z (CIVX2)	0.06
16.40 r	
F13/f4/h2/cout_ha (HA_25)	0.00
16.40 r	
F13/f4/U2/Z (CIVX2)	0.06
16.47 f	
F13/f4/U1/Z (CND2IX2)	0.07
16.54 r	

F13/f4/cout_fa1 (FA_1bit_13)	0.00
16.54 r	
F13/cout_fa4_2 (FA_4bit_2_4)	0.00
16.54 r	
F14/cin_fa4 (FA_4bit_2_3)	0.00
16.54 r	
F14/f1/cin (FA_1bit_12)	0.00
16.54 r	
F14/f1/h2/op2_ha (HA_23)	0.00
16.54 r	
F14/f1/h2/U1/Z (CND2X2)	0.09
16.63 f	
F14/f1/h2/U2/Z (CIVX2)	0.06
16.69 r	
F14/f1/h2/cout_ha (HA_23)	0.00
16.69 r	
F14/f1/U2/Z (CIVX2)	0.06
16.76 f	
F14/f1/U1/Z (CND2IX2)	0.09
16.84 r	
F14/f1/cout_fa1 (FA_1bit_12)	0.00
16.84 r	
F14/f2/cin (FA_1bit_11)	0.00
16.84 r	
F14/f2/h2/op2_ha (HA_21)	0.00
16.84 r	
F14/f2/h2/U1/Z (CND2X2)	0.10
16.94 f	
F14/f2/h2/U2/Z (CIVX2)	0.06
17.00 r	
F14/f2/h2/cout_ha (HA_21)	0.00
17.00 r	
F14/f2/U2/Z (CIVX2)	0.06
17.07 f	
F14/f2/U1/Z (CND2IX2)	0.07
17.14 r	
F14/f2/cout_fa1 (FA_1bit_11)	0.00
17.14 r	
F14/f3/cin (FA_1bit_10)	0.00
17.14 r	

F14/f3/h2/op2_ha (HA_19)	0.00
17.14 r	
F14/f3/h2/U1/Z (CND2X2)	0.09
17.23 f	
F14/f3/h2/U2/Z (CIVX2)	0.06
17.29 r	
F14/f3/h2/cout_ha (HA_19)	0.00
17.29 r	
F14/f3/U2/Z (CIVX2)	0.06
17.36 f	
F14/f3/U1/Z (CND2IX2)	0.07
17.43 r	
F14/f3/cout_fa1 (FA_1bit_10)	0.00
17.43 r	
F14/f4/cin (FA_1bit_9)	0.00
17.43 r	
F14/f4/h2/op2_ha (HA_17)	0.00
17.43 r	
F14/f4/h2/U1/Z (CND2X2)	0.09
17.52 f	
F14/f4/h2/U2/Z (CIVX2)	0.06
17.58 r	
F14/f4/h2/cout_ha (HA_17)	0.00
17.58 r	
F14/f4/U2/Z (CIVX2)	0.06
17.65 f	
F14/f4/U1/Z (CND2IX2)	0.07
17.72 r	
F14/f4/cout_fa1 (FA_1bit_9)	0.00
17.72 r	
F14/cout_fa4_2 (FA_4bit_2_3)	0.00
17.72 r	
F15/cin_fa4 (FA_4bit_2_2)	0.00
17.72 r	
F15/f1/cin (FA_1bit_8)	0.00
17.72 r	
F15/f1/h2/op2_ha (HA_15)	0.00
17.72 r	
F15/f1/h2/U1/Z (CND2X2)	0.09
17.81 f	

F15/f1/h2/U2/Z (CIVX2)	0.06
17.87 r	
F15/f1/h2/cout_ha (HA_15)	0.00
17.87 r	
F15/f1/U2/Z (CIVX2)	0.06
17.94 f	
F15/f1/U1/Z (CND2IX2)	0.07
18.01 r	
F15/f1/cout_fa1 (FA_1bit_8)	0.00
18.01 r	
F15/f2/cin (FA_1bit_7)	0.00
18.01 r	
F15/f2/h2/op2_ha (HA_13)	0.00
18.01 r	
F15/f2/h2/U1/Z (CND2X2)	0.09
18.10 f	
F15/f2/h2/U2/Z (CIVX2)	0.06
18.16 r	
F15/f2/h2/cout_ha (HA_13)	0.00
18.16 r	
F15/f2/U2/Z (CIVX2)	0.06
18.23 f	
F15/f2/U1/Z (CND2IX2)	0.07
18.30 r	
F15/f2/cout_fa1 (FA_1bit_7)	0.00
18.30 r	
F15/f3/cin (FA_1bit_6)	0.00
18.30 r	
F15/f3/h2/op2_ha (HA_11)	0.00
18.30 r	
F15/f3/h2/U1/Z (CND2X2)	0.09
18.39 f	
F15/f3/h2/U2/Z (CIVX2)	0.06
18.45 r	
F15/f3/h2/cout_ha (HA_11)	0.00
18.45 r	
F15/f3/U2/Z (CIVX2)	0.06
18.52 f	
F15/f3/U1/Z (CND2IX2)	0.07
18.59 r	

F15/f3/cout_fa1 (FA_1bit_6)	0.00
18.59 r	
F15/f4/cin (FA_1bit_5)	0.00
18.59 r	
F15/f4/h2/op2_ha (HA_9)	0.00
18.59 r	
F15/f4/h2/U2/Z (CIVX2)	0.07
18.66 f	
F15/f4/h2/U1/Z (CNR2X2)	0.10
18.76 r	
F15/f4/h2/cout_ha (HA_9)	0.00
18.76 r	
F15/f4/U2/Z (CIVX1)	0.10
18.85 f	
F15/f4/U1/Z (CND2IX2)	0.08
18.93 r	
F15/f4/cout_fa1 (FA_1bit_5)	0.00
18.93 r	
F15/cout_fa4_2 (FA_4bit_2_2)	0.00
18.93 r	
F16/cin_fa4 (FA_4bit_2_1)	0.00
18.93 r	
F16/f1/cin (FA_1bit_4)	0.00
18.93 r	
F16/f1/h2/op2_ha (HA_7)	0.00
18.93 r	
F16/f1/h2/U1/Z (CND2X2)	0.09
19.02 f	
F16/f1/h2/U2/Z (CIVX2)	0.06
19.08 r	
F16/f1/h2/cout_ha (HA_7)	0.00
19.08 r	
F16/f1/U2/Z (CIVX2)	0.06
19.15 f	
F16/f1/U1/Z (CND2IX2)	0.07
19.22 r	
F16/f1/cout_fa1 (FA_1bit_4)	0.00
19.22 r	
F16/f2/cin (FA_1bit_3)	0.00
19.22 r	

F16/f2/h2/op2_ha (HA_5)	0.00
19.22 r	
F16/f2/h2/U2/Z (CIVX2)	0.07
19.29 f	
F16/f2/h2/U1/Z (CNR2X2)	0.10
19.39 r	
F16/f2/h2/cout_ha (HA_5)	0.00
19.39 r	
F16/f2/U1/Z (CNR2IX1)	0.10
19.49 f	
F16/f2/U3/Z (CIVX2)	0.06
19.55 r	
F16/f2/cout_fa1 (FA_1bit_3)	0.00
19.55 r	
F16/f3/cin (FA_1bit_2)	0.00
19.55 r	
F16/f3/h2/op2_ha (HA_3)	0.00
19.55 r	
F16/f3/h2/U3/Z (CIVX2)	0.07
19.62 f	
F16/f3/h2/U1/Z (CNR2X2)	0.10
19.72 r	
F16/f3/h2/cout_ha (HA_3)	0.00
19.72 r	
F16/f3/U1/Z (CNR2IX1)	0.10
19.82 f	
F16/f3/U3/Z (CIVX2)	0.07
19.89 r	
F16/f3/cout_fa1 (FA_1bit_2)	0.00
19.89 r	
F16/f4/cin (FA_1bit_1)	0.00
19.89 r	
F16/f4/h2/op2_ha (HA_1)	0.00
19.89 r	
F16/f4/h2/U1/Z (CEOX1)	0.26
20.16 r	
F16/f4/h2/sum_ha (HA_1)	0.00
20.16 r	
F16/f4/sum_fa1 (FA_1bit_1)	0.00
20.16 r	

F16/sum_fa4_2[3] (FA_4bit_2_1)	0.00
20.16 r	
sum_reg[63]/D (CFD2QXL)	0.00
20.16 r	
data	arrival
20.16	time
clock clock (rise edge)	20.80
20.80	
clock network delay (propagated)	0.00
20.80	
clock uncertainty	-0.25
20.55	
sum_reg[63]/CP (CFD2QXL)	0.00
20.55 r	
library setup time	-0.38
20.17	
data	required
20.17	time

data	required
20.17	time
data arrival time	-
20.16	

slack	(MET)
0.01	

Startpoint: op2f_reg[1]
 (rising edge-triggered flip-flop clocked
 by clock)
 Endpoint: crout_reg (rising edge-triggered flip-flop
 clocked by clock)
 Path Group: clock
 Path Type: max

Point Path	Incr
clock clock (rise edge)	0.00
0.00	
clock network delay (propagated)	0.00
0.00	
op2f_reg[1]/CP (CFD2QX2)	0.00
0.00 r	
op2f_reg[1]/Q (CFD2QX2)	0.47
0.47 r	
F1/op2_fa4[1] (FA_4bit_1)	0.00
0.47 r	
F1/f1/op2_fa1 (FA_1bit_0)	0.00
0.47 r	
F1/f1/h1/op2_ha (HA_126)	0.00
0.47 r	
F1/f1/h1/U2/Z (CIVX2)	0.09
0.55 f	
F1/f1/h1/U4/Z (CND2X2)	0.07
0.62 r	
F1/f1/h1/U5/Z (CND2X2)	0.10
0.72 f	
F1/f1/h1/sum_ha (HA_126)	0.00
0.72 f	
F1/f1/h2/op1_ha (HA_125)	0.00
0.72 f	
F1/f1/h2/U1/Z (CND2X2)	0.07
0.79 r	
F1/f1/h2/U2/Z (CIVX2)	0.06
0.86 f	
F1/f1/h2/cout_ha (HA_125)	0.00
0.86 f	
F1/f1/U2/Z (CIVX2)	0.06
0.92 r	
F1/f1/U1/Z (CND2IX2)	0.09
1.01 f	
F1/f1/cout_fa1 (FA_1bit_0)	0.00
1.01 f	

F1/f2/cin (FA_1bit_62)	0.00
1.01 f	
F1/f2/h2/op2_ha (HA_123)	0.00
1.01 f	
F1/f2/h2/U1/Z (CND2X2)	0.07
1.08 r	
F1/f2/h2/U2/Z (CIVX2)	0.06
1.15 f	
F1/f2/h2/cout_ha (HA_123)	0.00
1.15 f	
F1/f2/U2/Z (CIVX2)	0.06
1.21 r	
F1/f2/U1/Z (CND2IX2)	0.09
1.30 f	
F1/f2/cout_fa1 (FA_1bit_62)	0.00
1.30 f	
F1/f3/cin (FA_1bit_61)	0.00
1.30 f	
F1/f3/h2/op2_ha (HA_121)	0.00
1.30 f	
F1/f3/h2/U1/Z (CND2X2)	0.07
1.37 r	
F1/f3/h2/U2/Z (CIVX2)	0.07
1.43 f	
F1/f3/h2/cout_ha (HA_121)	0.00
1.43 f	
F1/f3/U1/Z (CNR2IX2)	0.11
1.55 r	
F1/f3/U2/Z (CIVX2)	0.09
1.64 f	
F1/f3/cout_fa1 (FA_1bit_61)	0.00
1.64 f	
F1/cout_fa4 (FA_4bit_1)	0.00
1.64 f	
F2/cin_fa4 (FA_4bit_2_0)	0.00
1.64 f	
F2/f1/cin (FA_1bit_60)	0.00
1.64 f	
F2/f1/h2/op2_ha (HA_119)	0.00
1.64 f	

F2/f1/h2/U1/Z (CND2X2)	0.07
1.70 r	
F2/f1/h2/U2/Z (CIVX2)	0.07
1.77 f	
F2/f1/h2/cout_ha (HA_119)	0.00
1.77 f	
F2/f1/U1/Z (CNR2IX2)	0.11
1.88 r	
F2/f1/U2/Z (CIVX2)	0.09
1.97 f	
F2/f1/cout_fa1 (FA_1bit_60)	0.00
1.97 f	
F2/f2/cin (FA_1bit_59)	0.00
1.97 f	
F2/f2/h2/op2_ha (HA_117)	0.00
1.97 f	
F2/f2/h2/U1/Z (CND2X2)	0.07
2.04 r	
F2/f2/h2/U2/Z (CIVX2)	0.07
2.11 f	
F2/f2/h2/cout_ha (HA_117)	0.00
2.11 f	
F2/f2/U1/Z (CNR2IX2)	0.11
2.22 r	
F2/f2/U2/Z (CIVX2)	0.09
2.31 f	
F2/f2/cout_fa1 (FA_1bit_59)	0.00
2.31 f	
F2/f3/cin (FA_1bit_58)	0.00
2.31 f	
F2/f3/h2/op2_ha (HA_115)	0.00
2.31 f	
F2/f3/h2/U1/Z (CND2X2)	0.07
2.37 r	
F2/f3/h2/U2/Z (CIVX2)	0.07
2.44 f	
F2/f3/h2/cout_ha (HA_115)	0.00
2.44 f	
F2/f3/U1/Z (CNR2IX2)	0.11
2.55 r	

F2/f3/U3/Z (CIVX2)	0.09
2.64 f	
F2/f3/cout_fa1 (FA_1bit_58)	0.00
2.64 f	
F2/f4/cin (FA_1bit_57)	0.00
2.64 f	
F2/f4/h2/op2_ha (HA_113)	0.00
2.64 f	
F2/f4/h2/U2/Z (CND2X2)	0.07
2.71 r	
F2/f4/h2/U3/Z (CIVX2)	0.07
2.78 f	
F2/f4/h2/cout_ha (HA_113)	0.00
2.78 f	
F2/f4/U1/Z (CNR2IX2)	0.11
2.89 r	
F2/f4/U2/Z (CIVX2)	0.09
2.98 f	
F2/f4/cout_fa1 (FA_1bit_57)	0.00
2.98 f	
F2/cout_fa4_2 (FA_4bit_2_0)	0.00
2.98 f	
F3/cin_fa4 (FA_4bit_2_14)	0.00
2.98 f	
F3/f1/cin (FA_1bit_56)	0.00
2.98 f	
F3/f1/h2/op2_ha (HA_111)	0.00
2.98 f	
F3/f1/h2/U1/Z (CND2X2)	0.07
3.04 r	
F3/f1/h2/U2/Z (CIVX2)	0.07
3.11 f	
F3/f1/h2/cout_ha (HA_111)	0.00
3.11 f	
F3/f1/U1/Z (CNR2IX2)	0.11
3.22 r	
F3/f1/U2/Z (CIVX2)	0.09
3.31 f	
F3/f1/cout_fa1 (FA_1bit_56)	0.00
3.31 f	

F3/f2/cin (FA_1bit_55)	0.00
3.31 f	
F3/f2/h2/op2_ha (HA_109)	0.00
3.31 f	
F3/f2/h2/U1/Z (CND2X2)	0.07
3.38 r	
F3/f2/h2/U2/Z (CIVX2)	0.06
3.44 f	
F3/f2/h2/cout_ha (HA_109)	0.00
3.44 f	
F3/f2/U2/Z (CIVX2)	0.06
3.51 r	
F3/f2/U1/Z (CND2IX2)	0.09
3.60 f	
F3/f2/cout_fa1 (FA_1bit_55)	0.00
3.60 f	
F3/f3/cin (FA_1bit_54)	0.00
3.60 f	
F3/f3/h2/op2_ha (HA_107)	0.00
3.60 f	
F3/f3/h2/U1/Z (CND2X2)	0.07
3.67 r	
F3/f3/h2/U2/Z (CIVX2)	0.07
3.73 f	
F3/f3/h2/cout_ha (HA_107)	0.00
3.73 f	
F3/f3/U1/Z (CNR2IX2)	0.11
3.85 r	
F3/f3/U2/Z (CIVX2)	0.09
3.93 f	
F3/f3/cout_fa1 (FA_1bit_54)	0.00
3.93 f	
F3/f4/cin (FA_1bit_53)	0.00
3.93 f	
F3/f4/h2/op2_ha (HA_105)	0.00
3.93 f	
F3/f4/h2/U1/Z (CND2X2)	0.07
4.00 r	
F3/f4/h2/U2/Z (CIVX2)	0.07
4.07 f	

F3/f4/h2/cout_ha (HA_105)	0.00
4.07 f	
F3/f4/U1/Z (CNR2IX2)	0.11
4.18 r	
F3/f4/U2/Z (CIVX2)	0.09
4.27 f	
F3/f4/cout_fa1 (FA_1bit_53)	0.00
4.27 f	
F3/cout_fa4_2 (FA_4bit_2_14)	0.00
4.27 f	
F4/cin_fa4 (FA_4bit_2_13)	0.00
4.27 f	
F4/f1/cin (FA_1bit_52)	0.00
4.27 f	
F4/f1/h2/op2_ha (HA_103)	0.00
4.27 f	
F4/f1/h2/U1/Z (CND2X2)	0.07
4.34 r	
F4/f1/h2/U2/Z (CIVX2)	0.07
4.40 f	
F4/f1/h2/cout_ha (HA_103)	0.00
4.40 f	
F4/f1/U1/Z (CNR2IX2)	0.11
4.52 r	
F4/f1/U3/Z (CIVX2)	0.09
4.60 f	
F4/f1/cout_fa1 (FA_1bit_52)	0.00
4.60 f	
F4/f2/cin (FA_1bit_51)	0.00
4.60 f	
F4/f2/h2/op2_ha (HA_101)	0.00
4.60 f	
F4/f2/h2/U1/Z (CND2X2)	0.07
4.67 r	
F4/f2/h2/U2/Z (CIVX2)	0.07
4.74 f	
F4/f2/h2/cout_ha (HA_101)	0.00
4.74 f	
F4/f2/U1/Z (CNR2IX2)	0.11
4.85 r	

F4/f2/U2/Z (CIVX2)	0.09
4.94 f	
F4/f2/cout_fa1 (FA_1bit_51)	0.00
4.94 f	
F4/f3/cin (FA_1bit_50)	0.00
4.94 f	
F4/f3/h2/op2_ha (HA_99)	0.00
4.94 f	
F4/f3/h2/U1/Z (CND2X2)	0.07
5.01 r	
F4/f3/h2/U2/Z (CIVX2)	0.07
5.07 f	
F4/f3/h2/cout_ha (HA_99)	0.00
5.07 f	
F4/f3/U1/Z (CNR2IX2)	0.11
5.19 r	
F4/f3/U2/Z (CIVX2)	0.09
5.28 f	
F4/f3/cout_fa1 (FA_1bit_50)	0.00
5.28 f	
F4/f4/cin (FA_1bit_49)	0.00
5.28 f	
F4/f4/h2/op2_ha (HA_97)	0.00
5.28 f	
F4/f4/h2/U1/Z (CND2X2)	0.07
5.34 r	
F4/f4/h2/U2/Z (CIVX2)	0.07
5.41 f	
F4/f4/h2/cout_ha (HA_97)	0.00
5.41 f	
F4/f4/U1/Z (CNR2IX2)	0.11
5.52 r	
F4/f4/U2/Z (CIVX2)	0.09
5.61 f	
F4/f4/cout_fa1 (FA_1bit_49)	0.00
5.61 f	
F4/cout_fa4_2 (FA_4bit_2_13)	0.00
5.61 f	
F5/cin_fa4 (FA_4bit_2_12)	0.00
5.61 f	

F5/f1/cin (FA_1bit_48)	0.00
5.61 f	
F5/f1/h2/op2_ha (HA_95)	0.00
5.61 f	
F5/f1/h2/U1/Z (CND2X2)	0.07
5.68 r	
F5/f1/h2/U2/Z (CIVX2)	0.06
5.74 f	
F5/f1/h2/cout_ha (HA_95)	0.00
5.74 f	
F5/f1/U2/Z (CIVX2)	0.06
5.80 r	
F5/f1/U1/Z (CND2IX2)	0.09
5.90 f	
F5/f1/cout_fa1 (FA_1bit_48)	0.00
5.90 f	
F5/f2/cin (FA_1bit_47)	0.00
5.90 f	
F5/f2/h2/op2_ha (HA_93)	0.00
5.90 f	
F5/f2/h2/U1/Z (CND2X2)	0.07
5.96 r	
F5/f2/h2/U2/Z (CIVX2)	0.07
6.03 f	
F5/f2/h2/cout_ha (HA_93)	0.00
6.03 f	
F5/f2/U1/Z (CNR2IX2)	0.11
6.14 r	
F5/f2/U2/Z (CIVX2)	0.09
6.23 f	
F5/f2/cout_fa1 (FA_1bit_47)	0.00
6.23 f	
F5/f3/cin (FA_1bit_46)	0.00
6.23 f	
F5/f3/h2/op2_ha (HA_91)	0.00
6.23 f	
F5/f3/h2/U1/Z (CND2X2)	0.07
6.30 r	
F5/f3/h2/U2/Z (CIVX2)	0.07
6.37 f	

F5/f3/h2/cout_ha (HA_91)	0.00
6.37 f	
F5/f3/U1/Z (CNR2IX2)	0.11
6.48 r	
F5/f3/U2/Z (CIVX2)	0.09
6.57 f	
F5/f3/cout_fa1 (FA_1bit_46)	0.00
6.57 f	
F5/f4/cin (FA_1bit_45)	0.00
6.57 f	
F5/f4/h2/op2_ha (HA_89)	0.00
6.57 f	
F5/f4/h2/U1/Z (CND2X2)	0.07
6.64 r	
F5/f4/h2/U2/Z (CIVX2)	0.06
6.70 f	
F5/f4/h2/cout_ha (HA_89)	0.00
6.70 f	
F5/f4/U2/Z (CIVX2)	0.06
6.76 r	
F5/f4/U1/Z (CND2IX2)	0.09
6.85 f	
F5/f4/cout_fa1 (FA_1bit_45)	0.00
6.85 f	
F5/cout_fa4_2 (FA_4bit_2_12)	0.00
6.85 f	
F6/cin_fa4 (FA_4bit_2_11)	0.00
6.85 f	
F6/f1/cin (FA_1bit_44)	0.00
6.85 f	
F6/f1/h2/op2_ha (HA_87)	0.00
6.85 f	
F6/f1/h2/U1/Z (CND2X2)	0.07
6.92 r	
F6/f1/h2/U2/Z (CIVX2)	0.07
6.99 f	
F6/f1/h2/cout_ha (HA_87)	0.00
6.99 f	
F6/f1/U1/Z (CNR2IX2)	0.11
7.10 r	

F6/f1/U2/Z (CIVX2)	0.09
7.19 f	
F6/f1/cout_fa1 (FA_1bit_44)	0.00
7.19 f	
F6/f2/cin (FA_1bit_43)	0.00
7.19 f	
F6/f2/h2/op2_ha (HA_85)	0.00
7.19 f	
F6/f2/h2/U1/Z (CND2X2)	0.07
7.26 r	
F6/f2/h2/U2/Z (CIVX2)	0.07
7.32 f	
F6/f2/h2/cout_ha (HA_85)	0.00
7.32 f	
F6/f2/U1/Z (CNR2IX2)	0.11
7.44 r	
F6/f2/U2/Z (CIVX2)	0.09
7.53 f	
F6/f2/cout_fa1 (FA_1bit_43)	0.00
7.53 f	
F6/f3/cin (FA_1bit_42)	0.00
7.53 f	
F6/f3/h2/op2_ha (HA_83)	0.00
7.53 f	
F6/f3/h2/U1/Z (CND2X2)	0.07
7.59 r	
F6/f3/h2/U2/Z (CIVX2)	0.07
7.66 f	
F6/f3/h2/cout_ha (HA_83)	0.00
7.66 f	
F6/f3/U1/Z (CNR2IX2)	0.11
7.77 r	
F6/f3/U3/Z (CIVX2)	0.09
7.86 f	
F6/f3/cout_fa1 (FA_1bit_42)	0.00
7.86 f	
F6/f4/cin (FA_1bit_41)	0.00
7.86 f	
F6/f4/h2/op2_ha (HA_81)	0.00
7.86 f	

F6/f4/h2/U1/Z (CND2X2)	0.07
7.93 r	
F6/f4/h2/U2/Z (CIVX2)	0.07
7.99 f	
F6/f4/h2/cout_ha (HA_81)	0.00
7.99 f	
F6/f4/U1/Z (CNR2IX2)	0.11
8.11 r	
F6/f4/U2/Z (CIVX2)	0.09
8.20 f	
F6/f4/cout_fa1 (FA_1bit_41)	0.00
8.20 f	
F6/cout_fa4_2 (FA_4bit_2_11)	0.00
8.20 f	
F7/cin_fa4 (FA_4bit_2_10)	0.00
8.20 f	
F7/f1/cin (FA_1bit_40)	0.00
8.20 f	
F7/f1/h2/op2_ha (HA_79)	0.00
8.20 f	
F7/f1/h2/U1/Z (CND2X2)	0.07
8.26 r	
F7/f1/h2/U2/Z (CIVX2)	0.07
8.33 f	
F7/f1/h2/cout_ha (HA_79)	0.00
8.33 f	
F7/f1/U1/Z (CNR2IX2)	0.11
8.44 r	
F7/f1/U2/Z (CIVX2)	0.09
8.53 f	
F7/f1/cout_fa1 (FA_1bit_40)	0.00
8.53 f	
F7/f2/cin (FA_1bit_39)	0.00
8.53 f	
F7/f2/h2/op2_ha (HA_77)	0.00
8.53 f	
F7/f2/h2/U1/Z (CND2X2)	0.07
8.60 r	
F7/f2/h2/U2/Z (CIVX2)	0.07
8.66 f	

F7/f2/h2/cout_ha (HA_77)	0.00
8.66 f	
F7/f2/U1/Z (CNR2IX2)	0.11
8.78 r	
F7/f2/U3/Z (CIVX2)	0.09
8.87 f	
F7/f2/cout_fa1 (FA_1bit_39)	0.00
8.87 f	
F7/f3/cin (FA_1bit_38)	0.00
8.87 f	
F7/f3/h2/op2_ha (HA_75)	0.00
8.87 f	
F7/f3/h2/U1/Z (CND2X2)	0.07
8.93 r	
F7/f3/h2/U2/Z (CIVX2)	0.06
9.00 f	
F7/f3/h2/cout_ha (HA_75)	0.00
9.00 f	
F7/f3/U2/Z (CIVX2)	0.06
9.06 r	
F7/f3/U1/Z (CND2IX2)	0.09
9.15 f	
F7/f3/cout_fa1 (FA_1bit_38)	0.00
9.15 f	
F7/f4/cin (FA_1bit_37)	0.00
9.15 f	
F7/f4/h2/op2_ha (HA_73)	0.00
9.15 f	
F7/f4/h2/U1/Z (CND2X2)	0.07
9.22 r	
F7/f4/h2/U2/Z (CIVX2)	0.07
9.29 f	
F7/f4/h2/cout_ha (HA_73)	0.00
9.29 f	
F7/f4/U1/Z (CNR2IX2)	0.11
9.40 r	
F7/f4/U3/Z (CIVX2)	0.09
9.49 f	
F7/f4/cout_fa1 (FA_1bit_37)	0.00
9.49 f	

F7/cout_fa4_2 (FA_4bit_2_10)	0.00
9.49 f	
F8/cin_fa4 (FA_4bit_2_9)	0.00
9.49 f	
F8/f1/cin (FA_1bit_36)	0.00
9.49 f	
F8/f1/h2/op2_ha (HA_71)	0.00
9.49 f	
F8/f1/h2/U1/Z (CND2X2)	0.07
9.56 r	
F8/f1/h2/U2/Z (CIVX2)	0.06
9.62 f	
F8/f1/h2/cout_ha (HA_71)	0.00
9.62 f	
F8/f1/U2/Z (CIVX2)	0.06
9.68 r	
F8/f1/U1/Z (CND2IX2)	0.09
9.77 f	
F8/f1/cout_fa1 (FA_1bit_36)	0.00
9.77 f	
F8/f2/cin (FA_1bit_35)	0.00
9.77 f	
F8/f2/h2/op2_ha (HA_69)	0.00
9.77 f	
F8/f2/h2/U1/Z (CND2X2)	0.07
9.84 r	
F8/f2/h2/U2/Z (CIVX2)	0.06
9.91 f	
F8/f2/h2/cout_ha (HA_69)	0.00
9.91 f	
F8/f2/U2/Z (CIVX2)	0.06
9.97 r	
F8/f2/U1/Z (CND2IX2)	0.09
10.06 f	
F8/f2/cout_fa1 (FA_1bit_35)	0.00
10.06 f	
F8/f3/cin (FA_1bit_34)	0.00
10.06 f	
F8/f3/h2/op2_ha (HA_67)	0.00
10.06 f	

F8/f3/h2/U2/Z (CIVX2)	0.07
10.12 r	
F8/f3/h2/U1/Z (CNR2X2)	0.07
10.19 f	
F8/f3/h2/cout_ha (HA_67)	0.00
10.19 f	
F8/f3/U2/Z (CIVX2)	0.06
10.25 r	
F8/f3/U1/Z (CND2IX2)	0.09
10.34 f	
F8/f3/cout_fa1 (FA_1bit_34)	0.00
10.34 f	
F8/f4/cin (FA_1bit_33)	0.00
10.34 f	
F8/f4/h2/op2_ha (HA_65)	0.00
10.34 f	
F8/f4/h2/U2/Z (CIVX2)	0.07
10.41 r	
F8/f4/h2/U1/Z (CNR2X2)	0.07
10.48 f	
F8/f4/h2/cout_ha (HA_65)	0.00
10.48 f	
F8/f4/U2/Z (CIVX2)	0.06
10.54 r	
F8/f4/U1/Z (CND2IX2)	0.09
10.63 f	
F8/f4/cout_fa1 (FA_1bit_33)	0.00
10.63 f	
F8/cout_fa4_2 (FA_4bit_2_9)	0.00
10.63 f	
F9/cin_fa4 (FA_4bit_2_8)	0.00
10.63 f	
F9/f1/cin (FA_1bit_32)	0.00
10.63 f	
F9/f1/h2/op2_ha (HA_63)	0.00
10.63 f	
F9/f1/h2/U2/Z (CIVX2)	0.07
10.69 r	
F9/f1/h2/U1/Z (CNR2X2)	0.07
10.76 f	

F9/f1/h2/cout_ha (HA_63)	0.00
10.76 f	
F9/f1/U2/Z (CIVX2)	0.06
10.82 r	
F9/f1/U1/Z (CND2IX2)	0.09
10.91 f	
F9/f1/cout_fa1 (FA_1bit_32)	0.00
10.91 f	
F9/f2/cin (FA_1bit_31)	0.00
10.91 f	
F9/f2/h2/op2_ha (HA_61)	0.00
10.91 f	
F9/f2/h2/U2/Z (CIVX2)	0.07
10.98 r	
F9/f2/h2/U1/Z (CNR2X2)	0.07
11.04 f	
F9/f2/h2/cout_ha (HA_61)	0.00
11.04 f	
F9/f2/U2/Z (CIVX2)	0.06
11.11 r	
F9/f2/U1/Z (CND2IX2)	0.09
11.20 f	
F9/f2/cout_fa1 (FA_1bit_31)	0.00
11.20 f	
F9/f3/cin (FA_1bit_30)	0.00
11.20 f	
F9/f3/h2/op2_ha (HA_59)	0.00
11.20 f	
F9/f3/h2/U2/Z (CIVX2)	0.07
11.26 r	
F9/f3/h2/U1/Z (CNR2X2)	0.07
11.33 f	
F9/f3/h2/cout_ha (HA_59)	0.00
11.33 f	
F9/f3/U2/Z (CIVX2)	0.06
11.39 r	
F9/f3/U1/Z (CND2IX2)	0.09
11.48 f	
F9/f3/cout_fa1 (FA_1bit_30)	0.00
11.48 f	

F9/f4/cin (FA_1bit_29)	0.00
11.48 f	
F9/f4/h2/op2_ha (HA_57)	0.00
11.48 f	
F9/f4/h2/U2/Z (CIVX2)	0.07
11.55 r	
F9/f4/h2/U1/Z (CNR2X2)	0.07
11.61 f	
F9/f4/h2/cout_ha (HA_57)	0.00
11.61 f	
F9/f4/U2/Z (CIVX2)	0.06
11.67 r	
F9/f4/U1/Z (CND2IX2)	0.09
11.76 f	
F9/f4/cout_fa1 (FA_1bit_29)	0.00
11.76 f	
F9/cout_fa4_2 (FA_4bit_2_8)	0.00
11.76 f	
F10/cin_fa4 (FA_4bit_2_7)	0.00
11.76 f	
F10/f1/cin (FA_1bit_28)	0.00
11.76 f	
F10/f1/h2/op2_ha (HA_55)	0.00
11.76 f	
F10/f1/h2/U2/Z (CIVX2)	0.07
11.83 r	
F10/f1/h2/U1/Z (CNR2X2)	0.07
11.90 f	
F10/f1/h2/cout_ha (HA_55)	0.00
11.90 f	
F10/f1/U2/Z (CIVX2)	0.06
11.96 r	
F10/f1/U1/Z (CND2IX2)	0.09
12.05 f	
F10/f1/cout_fa1 (FA_1bit_28)	0.00
12.05 f	
F10/f2/cin (FA_1bit_27)	0.00
12.05 f	
F10/f2/h2/op2_ha (HA_53)	0.00
12.05 f	

F10/f2/h2/U2/Z (CIVX2)	0.07
12.11 r	
F10/f2/h2/U1/Z (CNR2X2)	0.07
12.18 f	
F10/f2/h2/cout_ha (HA_53)	0.00
12.18 f	
F10/f2/U2/Z (CIVX2)	0.06
12.24 r	
F10/f2/U1/Z (CND2IX2)	0.09
12.33 f	
F10/f2/cout_fa1 (FA_1bit_27)	0.00
12.33 f	
F10/f3/cin (FA_1bit_26)	0.00
12.33 f	
F10/f3/h2/op2_ha (HA_51)	0.00
12.33 f	
F10/f3/h2/U2/Z (CIVX2)	0.07
12.40 r	
F10/f3/h2/U1/Z (CNR2X2)	0.07
12.47 f	
F10/f3/h2/cout_ha (HA_51)	0.00
12.47 f	
F10/f3/U2/Z (CIVX2)	0.06
12.53 r	
F10/f3/U1/Z (CND2IX2)	0.09
12.62 f	
F10/f3/cout_fa1 (FA_1bit_26)	0.00
12.62 f	
F10/f4/cin (FA_1bit_25)	0.00
12.62 f	
F10/f4/h2/op2_ha (HA_49)	0.00
12.62 f	
F10/f4/h2/U2/Z (CIVX2)	0.07
12.68 r	
F10/f4/h2/U1/Z (CNR2X2)	0.07
12.75 f	
F10/f4/h2/cout_ha (HA_49)	0.00
12.75 f	
F10/f4/U2/Z (CIVX2)	0.06
12.81 r	

F10/f4/U1/Z (CND2IX2)	0.09
12.90 f	
F10/f4/cout_fa1 (FA_1bit_25)	0.00
12.90 f	
F10/cout_fa4_2 (FA_4bit_2_7)	0.00
12.90 f	
F11/cin_fa4 (FA_4bit_2_6)	0.00
12.90 f	
F11/f1/cin (FA_1bit_24)	0.00
12.90 f	
F11/f1/h2/op2_ha (HA_47)	0.00
12.90 f	
F11/f1/h2/U2/Z (CIVX2)	0.07
12.97 r	
F11/f1/h2/U1/Z (CNR2X2)	0.07
13.04 f	
F11/f1/h2/cout_ha (HA_47)	0.00
13.04 f	
F11/f1/U2/Z (CIVX2)	0.06
13.10 r	
F11/f1/U1/Z (CND2IX2)	0.09
13.19 f	
F11/f1/cout_fa1 (FA_1bit_24)	0.00
13.19 f	
F11/f2/cin (FA_1bit_23)	0.00
13.19 f	
F11/f2/h2/op2_ha (HA_45)	0.00
13.19 f	
F11/f2/h2/U2/Z (CIVX2)	0.07
13.25 r	
F11/f2/h2/U1/Z (CNR2X2)	0.07
13.32 f	
F11/f2/h2/cout_ha (HA_45)	0.00
13.32 f	
F11/f2/U2/Z (CIVX2)	0.06
13.38 r	
F11/f2/U1/Z (CND2IX2)	0.09
13.47 f	
F11/f2/cout_fa1 (FA_1bit_23)	0.00
13.47 f	

F11/f3/cin (FA_1bit_22)	0.00
13.47 f	
F11/f3/h2/op2_ha (HA_43)	0.00
13.47 f	
F11/f3/h2/U2/Z (CIVX2)	0.07
13.54 r	
F11/f3/h2/U1/Z (CNR2X2)	0.07
13.60 f	
F11/f3/h2/cout_ha (HA_43)	0.00
13.60 f	
F11/f3/U2/Z (CIVX2)	0.06
13.67 r	
F11/f3/U1/Z (CND2IX2)	0.09
13.75 f	
F11/f3/cout_fa1 (FA_1bit_22)	0.00
13.75 f	
F11/f4/cin (FA_1bit_21)	0.00
13.75 f	
F11/f4/h2/op2_ha (HA_41)	0.00
13.75 f	
F11/f4/h2/U2/Z (CIVX2)	0.07
13.82 r	
F11/f4/h2/U1/Z (CNR2X2)	0.07
13.89 f	
F11/f4/h2/cout_ha (HA_41)	0.00
13.89 f	
F11/f4/U2/Z (CIVX2)	0.06
13.95 r	
F11/f4/U1/Z (CND2IX2)	0.09
14.04 f	
F11/f4/cout_fa1 (FA_1bit_21)	0.00
14.04 f	
F11/cout_fa4_2 (FA_4bit_2_6)	0.00
14.04 f	
F12/cin_fa4 (FA_4bit_2_5)	0.00
14.04 f	
F12/f1/cin (FA_1bit_20)	0.00
14.04 f	
F12/f1/h2/op2_ha (HA_39)	0.00
14.04 f	

F12/f1/h2/U2/Z (CIVX2)	0.07
14.10 r	
F12/f1/h2/U1/Z (CNR2X2)	0.07
14.17 f	
F12/f1/h2/cout_ha (HA_39)	0.00
14.17 f	
F12/f1/U2/Z (CIVX2)	0.06
14.23 r	
F12/f1/U1/Z (CND2IX2)	0.09
14.32 f	
F12/f1/cout_fa1 (FA_1bit_20)	0.00
14.32 f	
F12/f2/cin (FA_1bit_19)	0.00
14.32 f	
F12/f2/h2/op2_ha (HA_37)	0.00
14.32 f	
F12/f2/h2/U2/Z (CIVX2)	0.07
14.39 r	
F12/f2/h2/U1/Z (CNR2X2)	0.07
14.46 f	
F12/f2/h2/cout_ha (HA_37)	0.00
14.46 f	
F12/f2/U2/Z (CIVX2)	0.06
14.52 r	
F12/f2/U1/Z (CND2IX2)	0.09
14.61 f	
F12/f2/cout_fa1 (FA_1bit_19)	0.00
14.61 f	
F12/f3/cin (FA_1bit_18)	0.00
14.61 f	
F12/f3/h2/op2_ha (HA_35)	0.00
14.61 f	
F12/f3/h2/U2/Z (CIVX2)	0.07
14.67 r	
F12/f3/h2/U1/Z (CNR2X2)	0.07
14.74 f	
F12/f3/h2/cout_ha (HA_35)	0.00
14.74 f	
F12/f3/U2/Z (CIVX2)	0.06
14.80 r	

F12/f3/U1/Z (CND2IX2)	0.09
14.89 f	
F12/f3/cout_fa1 (FA_1bit_18)	0.00
14.89 f	
F12/f4/cin (FA_1bit_17)	0.00
14.89 f	
F12/f4/h2/op2_ha (HA_33)	0.00
14.89 f	
F12/f4/h2/U2/Z (CIVX2)	0.07
14.96 r	
F12/f4/h2/U1/Z (CNR2X2)	0.07
15.03 f	
F12/f4/h2/cout_ha (HA_33)	0.00
15.03 f	
F12/f4/U2/Z (CIVX2)	0.06
15.09 r	
F12/f4/U1/Z (CND2IX2)	0.09
15.18 f	
F12/f4/cout_fa1 (FA_1bit_17)	0.00
15.18 f	
F12/cout_fa4_2 (FA_4bit_2_5)	0.00
15.18 f	
F13/cin_fa4 (FA_4bit_2_4)	0.00
15.18 f	
F13/f1/cin (FA_1bit_16)	0.00
15.18 f	
F13/f1/h2/op2_ha (HA_31)	0.00
15.18 f	
F13/f1/h2/U2/Z (CIVX2)	0.07
15.24 r	
F13/f1/h2/U1/Z (CNR2X2)	0.07
15.31 f	
F13/f1/h2/cout_ha (HA_31)	0.00
15.31 f	
F13/f1/U2/Z (CIVX2)	0.06
15.37 r	
F13/f1/U1/Z (CND2IX2)	0.09
15.46 f	
F13/f1/cout_fa1 (FA_1bit_16)	0.00
15.46 f	

F13/f2/cin (FA_1bit_15)	0.00
15.46 f	
F13/f2/h2/op2_ha (HA_29)	0.00
15.46 f	
F13/f2/h2/U2/Z (CIVX2)	0.07
15.53 r	
F13/f2/h2/U1/Z (CNR2X2)	0.07
15.59 f	
F13/f2/h2/cout_ha (HA_29)	0.00
15.59 f	
F13/f2/U2/Z (CIVX2)	0.06
15.66 r	
F13/f2/U1/Z (CND2IX2)	0.09
15.74 f	
F13/f2/cout_fa1 (FA_1bit_15)	0.00
15.74 f	
F13/f3/cin (FA_1bit_14)	0.00
15.74 f	
F13/f3/h2/op2_ha (HA_27)	0.00
15.74 f	
F13/f3/h2/U2/Z (CIVX2)	0.07
15.81 r	
F13/f3/h2/U1/Z (CNR2X2)	0.06
15.87 f	
F13/f3/h2/cout_ha (HA_27)	0.00
15.87 f	
F13/f3/U1/Z (CNR2IX1)	0.15
16.02 r	
F13/f3/U3/Z (CIVX2)	0.12
16.14 f	
F13/f3/cout_fa1 (FA_1bit_14)	0.00
16.14 f	
F13/f4/cin (FA_1bit_13)	0.00
16.14 f	
F13/f4/h2/op2_ha (HA_25)	0.00
16.14 f	
F13/f4/h2/U1/Z (CND2X2)	0.07
16.21 r	
F13/f4/h2/U2/Z (CIVX2)	0.06
16.28 f	

F13/f4/h2/cout_ha (HA_25)	0.00
16.28 f	
F13/f4/U2/Z (CIVX2)	0.06
16.34 r	
F13/f4/U1/Z (CND2IX2)	0.09
16.43 f	
F13/f4/cout_fa1 (FA_1bit_13)	0.00
16.43 f	
F13/cout_fa4_2 (FA_4bit_2_4)	0.00
16.43 f	
F14/cin_fa4 (FA_4bit_2_3)	0.00
16.43 f	
F14/f1/cin (FA_1bit_12)	0.00
16.43 f	
F14/f1/h2/op2_ha (HA_23)	0.00
16.43 f	
F14/f1/h2/U1/Z (CND2X2)	0.07
16.50 r	
F14/f1/h2/U2/Z (CIVX2)	0.06
16.56 f	
F14/f1/h2/cout_ha (HA_23)	0.00
16.56 f	
F14/f1/U2/Z (CIVX2)	0.06
16.62 r	
F14/f1/U1/Z (CND2IX2)	0.11
16.73 f	
F14/f1/cout_fa1 (FA_1bit_12)	0.00
16.73 f	
F14/f2/cin (FA_1bit_11)	0.00
16.73 f	
F14/f2/h2/op2_ha (HA_21)	0.00
16.73 f	
F14/f2/h2/U1/Z (CND2X2)	0.07
16.80 r	
F14/f2/h2/U2/Z (CIVX2)	0.06
16.87 f	
F14/f2/h2/cout_ha (HA_21)	0.00
16.87 f	
F14/f2/U2/Z (CIVX2)	0.06
16.93 r	

F14/f2/U1/Z (CND2IX2)	0.09
17.02 f	
F14/f2/cout_fa1 (FA_1bit_11)	0.00
17.02 f	
F14/f3/cin (FA_1bit_10)	0.00
17.02 f	
F14/f3/h2/op2_ha (HA_19)	0.00
17.02 f	
F14/f3/h2/U1/Z (CND2X2)	0.07
17.09 r	
F14/f3/h2/U2/Z (CIVX2)	0.06
17.15 f	
F14/f3/h2/cout_ha (HA_19)	0.00
17.15 f	
F14/f3/U2/Z (CIVX2)	0.06
17.22 r	
F14/f3/U1/Z (CND2IX2)	0.09
17.31 f	
F14/f3/cout_fa1 (FA_1bit_10)	0.00
17.31 f	
F14/f4/cin (FA_1bit_9)	0.00
17.31 f	
F14/f4/h2/op2_ha (HA_17)	0.00
17.31 f	
F14/f4/h2/U1/Z (CND2X2)	0.07
17.38 r	
F14/f4/h2/U2/Z (CIVX2)	0.06
17.44 f	
F14/f4/h2/cout_ha (HA_17)	0.00
17.44 f	
F14/f4/U2/Z (CIVX2)	0.06
17.50 r	
F14/f4/U1/Z (CND2IX2)	0.09
17.59 f	
F14/f4/cout_fa1 (FA_1bit_9)	0.00
17.59 f	
F14/cout_fa4_2 (FA_4bit_2_3)	0.00
17.59 f	
F15/cin_fa4 (FA_4bit_2_2)	0.00
17.59 f	

F15/f1/cin (FA_1bit_8)	0.00
17.59 f	
F15/f1/h2/op2_ha (HA_15)	0.00
17.59 f	
F15/f1/h2/U1/Z (CND2X2)	0.07
17.66 r	
F15/f1/h2/U2/Z (CIVX2)	0.06
17.73 f	
F15/f1/h2/cout_ha (HA_15)	0.00
17.73 f	
F15/f1/U2/Z (CIVX2)	0.06
17.79 r	
F15/f1/U1/Z (CND2IX2)	0.09
17.88 f	
F15/f1/cout_fa1 (FA_1bit_8)	0.00
17.88 f	
F15/f2/cin (FA_1bit_7)	0.00
17.88 f	
F15/f2/h2/op2_ha (HA_13)	0.00
17.88 f	
F15/f2/h2/U1/Z (CND2X2)	0.07
17.95 r	
F15/f2/h2/U2/Z (CIVX2)	0.06
18.02 f	
F15/f2/h2/cout_ha (HA_13)	0.00
18.02 f	
F15/f2/U2/Z (CIVX2)	0.06
18.08 r	
F15/f2/U1/Z (CND2IX2)	0.09
18.17 f	
F15/f2/cout_fa1 (FA_1bit_7)	0.00
18.17 f	
F15/f3/cin (FA_1bit_6)	0.00
18.17 f	
F15/f3/h2/op2_ha (HA_11)	0.00
18.17 f	
F15/f3/h2/U1/Z (CND2X2)	0.07
18.24 r	
F15/f3/h2/U2/Z (CIVX2)	0.06
18.30 f	

F15/f3/h2/cout_ha (HA_11)	0.00
18.30 f	
F15/f3/U2/Z (CIVX2)	0.06
18.36 r	
F15/f3/U1/Z (CND2IX2)	0.09
18.45 f	
F15/f3/cout_fa1 (FA_1bit_6)	0.00
18.45 f	
F15/f4/cin (FA_1bit_5)	0.00
18.45 f	
F15/f4/h2/op2_ha (HA_9)	0.00
18.45 f	
F15/f4/h2/U2/Z (CIVX2)	0.07
18.52 r	
F15/f4/h2/U1/Z (CNR2X2)	0.06
18.58 f	
F15/f4/h2/cout_ha (HA_9)	0.00
18.58 f	
F15/f4/U2/Z (CIVX1)	0.08
18.66 r	
F15/f4/U1/Z (CND2IX2)	0.10
18.77 f	
F15/f4/cout_fa1 (FA_1bit_5)	0.00
18.77 f	
F15/cout_fa4_2 (FA_4bit_2_2)	0.00
18.77 f	
F16/cin_fa4 (FA_4bit_2_1)	0.00
18.77 f	
F16/f1/cin (FA_1bit_4)	0.00
18.77 f	
F16/f1/h2/op2_ha (HA_7)	0.00
18.77 f	
F16/f1/h2/U1/Z (CND2X2)	0.07
18.84 r	
F16/f1/h2/U2/Z (CIVX2)	0.06
18.90 f	
F16/f1/h2/cout_ha (HA_7)	0.00
18.90 f	
F16/f1/U2/Z (CIVX2)	0.06
18.96 r	

F16/f1/U1/Z (CND2IX2)	0.09
19.06 f	
F16/f1/cout_fa1 (FA_1bit_4)	0.00
19.06 f	
F16/f2/cin (FA_1bit_3)	0.00
19.06 f	
F16/f2/h2/op2_ha (HA_5)	0.00
19.06 f	
F16/f2/h2/U2/Z (CIVX2)	0.07
19.12 r	
F16/f2/h2/U1/Z (CNR2X2)	0.06
19.18 f	
F16/f2/h2/cout_ha (HA_5)	0.00
19.18 f	
F16/f2/U1/Z (CNR2IX1)	0.15
19.33 r	
F16/f2/U3/Z (CIVX2)	0.10
19.43 f	
F16/f2/cout_fa1 (FA_1bit_3)	0.00
19.43 f	
F16/f3/cin (FA_1bit_2)	0.00
19.43 f	
F16/f3/h2/op2_ha (HA_3)	0.00
19.43 f	
F16/f3/h2/U3/Z (CIVX2)	0.07
19.50 r	
F16/f3/h2/U1/Z (CNR2X2)	0.06
19.56 f	
F16/f3/cout_ha (HA_3)	0.00
19.56 f	
F16/f3/U1/Z (CNR2IX1)	0.15
19.71 r	
F16/f3/U3/Z (CIVX2)	0.10
19.81 f	
F16/f3/cout_fa1 (FA_1bit_2)	0.00
19.81 f	
F16/f4/cin (FA_1bit_1)	0.00
19.81 f	
F16/f4/h2/op2_ha (HA_1)	0.00
19.81 f	

F16/f4/h2/U2/Z (CAN2X1)	0.15
19.97 f	
F16/f4/h2/cout_ha (HA_1)	0.00
19.97 f	
F16/f4/U1/Z (COR2X1)	0.22
20.19 f	
F16/f4/cout_fa1 (FA_1bit_1)	0.00
20.19 f	
F16/cout_fa4_2 (FA_4bit_2_1)	0.00
20.19 f	
crout_reg/D (CFD2X2)	0.00
20.19 f	
data	arrival
20.19	time
 clock clock (rise edge)	20.80
20.80	
clock network delay (propagated)	0.00
20.80	
clock uncertainty	-0.25
20.55	
crout_reg/CP (CFD2X2)	0.00
20.55 r	
library setup time	-0.34
20.21	
data	required
20.21	time
 ----- -----	
data	required
20.21	time
data arrival time	-
20.19	
 ----- -----	
slack	(MET)
0.02	

Startpoint: op2f_reg[1]

(rising edge-triggered flip-flop clocked by clock)
 Endpoint: sum_reg[60]
 (rising edge-triggered flip-flop clocked by clock)
 Path Group: clock
 Path Type: max

Point	Incr
Path	
clock	
clock clock (rise edge)	0.00
0.00	
clock network delay (propagated)	0.00
0.00	
op2f_reg[1]/CP (CFD2QX2)	0.00
0.00 r	
op2f_reg[1]/Q (CFD2QX2)	0.50
0.50 f	
F1/op2_fa4[1] (FA_4bit_1)	0.00
0.50 f	
F1/f1/op2_fa1 (FA_1bit_0)	0.00
0.50 f	
F1/f1/h1/op2_ha (HA_126)	0.00
0.50 f	
F1/f1/h1/U2/Z (CIVX2)	0.08
0.58 r	
F1/f1/h1/U4/Z (CND2X2)	0.09
0.67 f	
F1/f1/h1/U5/Z (CND2X2)	0.09
0.76 r	
F1/f1/h1/sum_ha (HA_126)	0.00
0.76 r	
F1/f1/h2/op1_ha (HA_125)	0.00
0.76 r	
F1/f1/h2/U1/Z (CND2X2)	0.09
0.85 f	
F1/f1/h2/U2/Z (CIVX2)	0.06
0.91 r	

F1/f1/h2/cout_ha (HA_125)	0.00
0.91 r	
F1/f1/U2/Z (CIVX2)	0.06
0.98 f	
F1/f1/U1/Z (CND2IX2)	0.07
1.05 r	
F1/f1/cout_fa1 (FA_1bit_0)	0.00
1.05 r	
F1/f2/cin (FA_1bit_62)	0.00
1.05 r	
F1/f2/h2/op2_ha (HA_123)	0.00
1.05 r	
F1/f2/h2/U1/Z (CND2X2)	0.09
1.14 f	
F1/f2/h2/U2/Z (CIVX2)	0.06
1.20 r	
F1/f2/h2/cout_ha (HA_123)	0.00
1.20 r	
F1/f2/U2/Z (CIVX2)	0.06
1.27 f	
F1/f2/U1/Z (CND2IX2)	0.07
1.34 r	
F1/f2/cout_fa1 (FA_1bit_62)	0.00
1.34 r	
F1/f3/cin (FA_1bit_61)	0.00
1.34 r	
F1/f3/h2/op2_ha (HA_121)	0.00
1.34 r	
F1/f3/h2/U1/Z (CND2X2)	0.09
1.43 f	
F1/f3/h2/U2/Z (CIVX2)	0.06
1.49 r	
F1/f3/h2/cout_ha (HA_121)	0.00
1.49 r	
F1/f3/U1/Z (CNR2IX2)	0.07
1.56 f	
F1/f3/U2/Z (CIVX2)	0.07
1.63 r	
F1/f3/cout_fa1 (FA_1bit_61)	0.00
1.63 r	

F1/cout_fa4 (FA_4bit_1)	0.00
1.63 r	
F2/cin_fa4 (FA_4bit_2_0)	0.00
1.63 r	
F2/f1/cin (FA_1bit_60)	0.00
1.63 r	
F2/f1/h2/op2_ha (HA_119)	0.00
1.63 r	
F2/f1/h2/U1/Z (CND2X2)	0.09
1.72 f	
F2/f1/h2/U2/Z (CIVX2)	0.06
1.78 r	
F2/f1/h2/cout_ha (HA_119)	0.00
1.78 r	
F2/f1/U1/Z (CNR2IX2)	0.07
1.85 f	
F2/f1/U2/Z (CIVX2)	0.07
1.91 r	
F2/f1/cout_fa1 (FA_1bit_60)	0.00
1.91 r	
F2/f2/cin (FA_1bit_59)	0.00
1.91 r	
F2/f2/h2/op2_ha (HA_117)	0.00
1.91 r	
F2/f2/h2/U1/Z (CND2X2)	0.09
2.00 f	
F2/f2/h2/U2/Z (CIVX2)	0.06
2.07 r	
F2/f2/h2/cout_ha (HA_117)	0.00
2.07 r	
F2/f2/U1/Z (CNR2IX2)	0.07
2.13 f	
F2/f2/U2/Z (CIVX2)	0.07
2.20 r	
F2/f2/cout_fa1 (FA_1bit_59)	0.00
2.20 r	
F2/f3/cin (FA_1bit_58)	0.00
2.20 r	
F2/f3/h2/op2_ha (HA_115)	0.00
2.20 r	

F2/f3/h2/U1/Z (CND2X2)	0.09
2.29 f	
F2/f3/h2/U2/Z (CIVX2)	0.06
2.35 r	
F2/f3/h2/cout_ha (HA_115)	0.00
2.35 r	
F2/f3/U1/Z (CNR2IX2)	0.07
2.42 f	
F2/f3/U3/Z (CIVX2)	0.07
2.49 r	
F2/f3/cout_fa1 (FA_1bit_58)	0.00
2.49 r	
F2/f4/cin (FA_1bit_57)	0.00
2.49 r	
F2/f4/h2/op2_ha (HA_113)	0.00
2.49 r	
F2/f4/h2/U2/Z (CND2X2)	0.09
2.58 f	
F2/f4/h2/U3/Z (CIVX2)	0.06
2.64 r	
F2/f4/h2/cout_ha (HA_113)	0.00
2.64 r	
F2/f4/U1/Z (CNR2IX2)	0.07
2.71 f	
F2/f4/U2/Z (CIVX2)	0.07
2.77 r	
F2/f4/cout_fa1 (FA_1bit_57)	0.00
2.77 r	
F2/cout_fa4_2 (FA_4bit_2_0)	0.00
2.77 r	
F3/cin_fa4 (FA_4bit_2_14)	0.00
2.77 r	
F3/f1/cin (FA_1bit_56)	0.00
2.77 r	
F3/f1/h2/op2_ha (HA_111)	0.00
2.77 r	
F3/f1/h2/U1/Z (CND2X2)	0.09
2.86 f	
F3/f1/h2/U2/Z (CIVX2)	0.06
2.93 r	

F3/f1/h2/cout_ha (HA_111)	0.00
2.93 r	
F3/f1/U1/Z (CNR2IX2)	0.07
2.99 f	
F3/f1/U2/Z (CIVX2)	0.07
3.06 r	
F3/f1/cout_fa1 (FA_1bit_56)	0.00
3.06 r	
F3/f2/cin (FA_1bit_55)	0.00
3.06 r	
F3/f2/h2/op2_ha (HA_109)	0.00
3.06 r	
F3/f2/h2/U1/Z (CND2X2)	0.09
3.15 f	
F3/f2/h2/U2/Z (CIVX2)	0.06
3.21 r	
F3/f2/h2/cout_ha (HA_109)	0.00
3.21 r	
F3/f2/U2/Z (CIVX2)	0.06
3.27 f	
F3/f2/U1/Z (CND2IX2)	0.07
3.35 r	
F3/f2/cout_fa1 (FA_1bit_55)	0.00
3.35 r	
F3/f3/cin (FA_1bit_54)	0.00
3.35 r	
F3/f3/h2/op2_ha (HA_107)	0.00
3.35 r	
F3/f3/h2/U1/Z (CND2X2)	0.09
3.44 f	
F3/f3/h2/U2/Z (CIVX2)	0.06
3.50 r	
F3/f3/h2/cout_ha (HA_107)	0.00
3.50 r	
F3/f3/U1/Z (CNR2IX2)	0.07
3.57 f	
F3/f3/U2/Z (CIVX2)	0.07
3.64 r	
F3/f3/cout_fa1 (FA_1bit_54)	0.00
3.64 r	

F3/f4/cin (FA_1bit_53)	0.00
3.64 r	
F3/f4/h2/op2_ha (HA_105)	0.00
3.64 r	
F3/f4/h2/U1/Z (CND2X2)	0.09
3.72 f	
F3/f4/h2/U2/Z (CIVX2)	0.06
3.79 r	
F3/f4/h2/cout_ha (HA_105)	0.00
3.79 r	
F3/f4/U1/Z (CNR2IX2)	0.07
3.85 f	
F3/f4/U2/Z (CIVX2)	0.07
3.92 r	
F3/f4/cout_fa1 (FA_1bit_53)	0.00
3.92 r	
F3/cout_fa4_2 (FA_4bit_2_14)	0.00
3.92 r	
F4/cin_fa4 (FA_4bit_2_13)	0.00
3.92 r	
F4/f1/cin (FA_1bit_52)	0.00
3.92 r	
F4/f1/h2/op2_ha (HA_103)	0.00
3.92 r	
F4/f1/h2/U1/Z (CND2X2)	0.09
4.01 f	
F4/f1/h2/U2/Z (CIVX2)	0.06
4.07 r	
F4/f1/h2/cout_ha (HA_103)	0.00
4.07 r	
F4/f1/U1/Z (CNR2IX2)	0.07
4.14 f	
F4/f1/U3/Z (CIVX2)	0.07
4.21 r	
F4/f1/cout_fa1 (FA_1bit_52)	0.00
4.21 r	
F4/f2/cin (FA_1bit_51)	0.00
4.21 r	
F4/f2/h2/op2_ha (HA_101)	0.00
4.21 r	

F4/f2/h2/U1/Z (CND2X2)	0.09
4.30 f	
F4/f2/h2/U2/Z (CIVX2)	0.06
4.36 r	
F4/f2/h2/cout_ha (HA_101)	0.00
4.36 r	
F4/f2/U1/Z (CNR2IX2)	0.07
4.43 f	
F4/f2/U2/Z (CIVX2)	0.07
4.49 r	
F4/f2/cout_fa1 (FA_1bit_51)	0.00
4.49 r	
F4/f3/cin (FA_1bit_50)	0.00
4.49 r	
F4/f3/h2/op2_ha (HA_99)	0.00
4.49 r	
F4/f3/h2/U1/Z (CND2X2)	0.09
4.58 f	
F4/f3/h2/U2/Z (CIVX2)	0.06
4.65 r	
F4/f3/h2/cout_ha (HA_99)	0.00
4.65 r	
F4/f3/U1/Z (CNR2IX2)	0.07
4.71 f	
F4/f3/U2/Z (CIVX2)	0.07
4.78 r	
F4/f3/cout_fa1 (FA_1bit_50)	0.00
4.78 r	
F4/f4/cin (FA_1bit_49)	0.00
4.78 r	
F4/f4/h2/op2_ha (HA_97)	0.00
4.78 r	
F4/f4/h2/U1/Z (CND2X2)	0.09
4.87 f	
F4/f4/h2/U2/Z (CIVX2)	0.06
4.93 r	
F4/f4/h2/cout_ha (HA_97)	0.00
4.93 r	
F4/f4/U1/Z (CNR2IX2)	0.07
5.00 f	

F4/f4/U2/Z (CIVX2)	0.07
5.07 r	
F4/f4/cout_fa1 (FA_1bit_49)	0.00
5.07 r	
F4/cout_fa4_2 (FA_4bit_2_13)	0.00
5.07 r	
F5/cin_fa4 (FA_4bit_2_12)	0.00
5.07 r	
F5/f1/cin (FA_1bit_48)	0.00
5.07 r	
F5/f1/h2/op2_ha (HA_95)	0.00
5.07 r	
F5/f1/h2/U1/Z (CND2X2)	0.09
5.16 f	
F5/f1/h2/U2/Z (CIVX2)	0.06
5.22 r	
F5/f1/h2/cout_ha (HA_95)	0.00
5.22 r	
F5/f1/U2/Z (CIVX2)	0.06
5.28 f	
F5/f1/U1/Z (CND2IX2)	0.07
5.35 r	
F5/f1/cout_fa1 (FA_1bit_48)	0.00
5.35 r	
F5/f2/cin (FA_1bit_47)	0.00
5.35 r	
F5/f2/h2/op2_ha (HA_93)	0.00
5.35 r	
F5/f2/h2/U1/Z (CND2X2)	0.09
5.45 f	
F5/f2/h2/U2/Z (CIVX2)	0.06
5.51 r	
F5/f2/h2/cout_ha (HA_93)	0.00
5.51 r	
F5/f2/U1/Z (CNR2IX2)	0.07
5.58 f	
F5/f2/U2/Z (CIVX2)	0.07
5.64 r	
F5/f2/cout_fa1 (FA_1bit_47)	0.00
5.64 r	

F5/f3/cin (FA_1bit_46)	0.00
5.64 r	
F5/f3/h2/op2_ha (HA_91)	0.00
5.64 r	
F5/f3/h2/U1/Z (CND2X2)	0.09
5.73 f	
F5/f3/h2/U2/Z (CIVX2)	0.06
5.79 r	
F5/f3/h2/cout_ha (HA_91)	0.00
5.79 r	
F5/f3/U1/Z (CNR2IX2)	0.07
5.86 f	
F5/f3/U2/Z (CIVX2)	0.07
5.93 r	
F5/f3/cout_fa1 (FA_1bit_46)	0.00
5.93 r	
F5/f4/cin (FA_1bit_45)	0.00
5.93 r	
F5/f4/h2/op2_ha (HA_89)	0.00
5.93 r	
F5/f4/h2/U1/Z (CND2X2)	0.09
6.02 f	
F5/f4/h2/U2/Z (CIVX2)	0.06
6.08 r	
F5/f4/h2/cout_ha (HA_89)	0.00
6.08 r	
F5/f4/U2/Z (CIVX2)	0.06
6.14 f	
F5/f4/U1/Z (CND2IX2)	0.07
6.22 r	
F5/f4/cout_fa1 (FA_1bit_45)	0.00
6.22 r	
F5/cout_fa4_2 (FA_4bit_2_12)	0.00
6.22 r	
F6/cin_fa4 (FA_4bit_2_11)	0.00
6.22 r	
F6/f1/cin (FA_1bit_44)	0.00
6.22 r	
F6/f1/h2/op2_ha (HA_87)	0.00
6.22 r	

F6/f1/h2/U1/Z (CND2X2)	0.09
6.31 f	
F6/f1/h2/U2/Z (CIVX2)	0.06
6.37 r	
F6/f1/h2/cout_ha (HA_87)	0.00
6.37 r	
F6/f1/U1/Z (CNR2IX2)	0.07
6.44 f	
F6/f1/U2/Z (CIVX2)	0.07
6.50 r	
F6/f1/cout_fa1 (FA_1bit_44)	0.00
6.50 r	
F6/f2/cin (FA_1bit_43)	0.00
6.50 r	
F6/f2/h2/op2_ha (HA_85)	0.00
6.50 r	
F6/f2/h2/U1/Z (CND2X2)	0.09
6.59 f	
F6/f2/h2/U2/Z (CIVX2)	0.06
6.66 r	
F6/f2/h2/cout_ha (HA_85)	0.00
6.66 r	
F6/f2/U1/Z (CNR2IX2)	0.07
6.72 f	
F6/f2/U2/Z (CIVX2)	0.07
6.79 r	
F6/f2/cout_fa1 (FA_1bit_43)	0.00
6.79 r	
F6/f3/cin (FA_1bit_42)	0.00
6.79 r	
F6/f3/h2/op2_ha (HA_83)	0.00
6.79 r	
F6/f3/h2/U1/Z (CND2X2)	0.09
6.88 f	
F6/f3/h2/U2/Z (CIVX2)	0.06
6.94 r	
F6/f3/h2/cout_ha (HA_83)	0.00
6.94 r	
F6/f3/U1/Z (CNR2IX2)	0.07
7.01 f	

F6/f3/U3/Z (CIVX2)	0.07
7.08 r	
F6/f3/cout_fa1 (FA_1bit_42)	0.00
7.08 r	
F6/f4/cin (FA_1bit_41)	0.00
7.08 r	
F6/f4/h2/op2_ha (HA_81)	0.00
7.08 r	
F6/f4/h2/U1/Z (CND2X2)	0.09
7.17 f	
F6/f4/h2/U2/Z (CIVX2)	0.06
7.23 r	
F6/f4/h2/cout_ha (HA_81)	0.00
7.23 r	
F6/f4/U1/Z (CNR2IX2)	0.07
7.30 f	
F6/f4/U2/Z (CIVX2)	0.07
7.36 r	
F6/f4/cout_fa1 (FA_1bit_41)	0.00
7.36 r	
F6/cout_fa4_2 (FA_4bit_2_11)	0.00
7.36 r	
F7/cin_fa4 (FA_4bit_2_10)	0.00
7.36 r	
F7/f1/cin (FA_1bit_40)	0.00
7.36 r	
F7/f1/h2/op2_ha (HA_79)	0.00
7.36 r	
F7/f1/h2/U1/Z (CND2X2)	0.09
7.45 f	
F7/f1/h2/U2/Z (CIVX2)	0.06
7.52 r	
F7/f1/h2/cout_ha (HA_79)	0.00
7.52 r	
F7/f1/U1/Z (CNR2IX2)	0.07
7.58 f	
F7/f1/U2/Z (CIVX2)	0.07
7.65 r	
F7/f1/cout_fa1 (FA_1bit_40)	0.00
7.65 r	

F7/f2/cin (FA_1bit_39)	0.00
7.65 r	
F7/f2/h2/op2_ha (HA_77)	0.00
7.65 r	
F7/f2/h2/U1/Z (CND2X2)	0.09
7.74 f	
F7/f2/h2/U2/Z (CIVX2)	0.06
7.80 r	
F7/f2/h2/cout_ha (HA_77)	0.00
7.80 r	
F7/f2/U1/Z (CNR2IX2)	0.07
7.87 f	
F7/f2/U3/Z (CIVX2)	0.07
7.94 r	
F7/f2/cout_fa1 (FA_1bit_39)	0.00
7.94 r	
F7/f3/cin (FA_1bit_38)	0.00
7.94 r	
F7/f3/h2/op2_ha (HA_75)	0.00
7.94 r	
F7/f3/h2/U1/Z (CND2X2)	0.09
8.02 f	
F7/f3/h2/U2/Z (CIVX2)	0.06
8.09 r	
F7/f3/h2/cout_ha (HA_75)	0.00
8.09 r	
F7/f3/U2/Z (CIVX2)	0.06
8.15 f	
F7/f3/U1/Z (CND2IX2)	0.07
8.22 r	
F7/f3/cout_fa1 (FA_1bit_38)	0.00
8.22 r	
F7/f4/cin (FA_1bit_37)	0.00
8.22 r	
F7/f4/h2/op2_ha (HA_73)	0.00
8.22 r	
F7/f4/h2/U1/Z (CND2X2)	0.09
8.31 f	
F7/f4/h2/U2/Z (CIVX2)	0.06
8.38 r	

F7/f4/h2/cout_ha (HA_73)	0.00
8.38 r	
F7/f4/U1/Z (CNR2IX2)	0.07
8.44 f	
F7/f4/U3/Z (CIVX2)	0.07
8.51 r	
F7/f4/cout_fa1 (FA_1bit_37)	0.00
8.51 r	
F7/cout_fa4_2 (FA_4bit_2_10)	0.00
8.51 r	
F8/cin_fa4 (FA_4bit_2_9)	0.00
8.51 r	
F8/f1/cin (FA_1bit_36)	0.00
8.51 r	
F8/f1/h2/op2_ha (HA_71)	0.00
8.51 r	
F8/f1/h2/U1/Z (CND2X2)	0.09
8.60 f	
F8/f1/h2/U2/Z (CIVX2)	0.06
8.66 r	
F8/f1/h2/cout_ha (HA_71)	0.00
8.66 r	
F8/f1/U2/Z (CIVX2)	0.06
8.73 f	
F8/f1/U1/Z (CND2IX2)	0.07
8.80 r	
F8/f1/cout_fa1 (FA_1bit_36)	0.00
8.80 r	
F8/f2/cin (FA_1bit_35)	0.00
8.80 r	
F8/f2/h2/op2_ha (HA_69)	0.00
8.80 r	
F8/f2/h2/U1/Z (CND2X2)	0.09
8.89 f	
F8/f2/h2/U2/Z (CIVX2)	0.06
8.95 r	
F8/f2/h2/cout_ha (HA_69)	0.00
8.95 r	
F8/f2/U2/Z (CIVX2)	0.06
9.02 f	

F8/f2/U1/Z (CND2IX2)	0.07
9.09 r	
F8/f2/cout_fa1 (FA_1bit_35)	0.00
9.09 r	
F8/f3/cin (FA_1bit_34)	0.00
9.09 r	
F8/f3/h2/op2_ha (HA_67)	0.00
9.09 r	
F8/f3/h2/U2/Z (CIVX2)	0.07
9.16 f	
F8/f3/h2/U1/Z (CNR2X2)	0.11
9.27 r	
F8/f3/h2/cout_ha (HA_67)	0.00
9.27 r	
F8/f3/U2/Z (CIVX2)	0.08
9.36 f	
F8/f3/U1/Z (CND2IX2)	0.07
9.43 r	
F8/f3/cout_fa1 (FA_1bit_34)	0.00
9.43 r	
F8/f4/cin (FA_1bit_33)	0.00
9.43 r	
F8/f4/h2/op2_ha (HA_65)	0.00
9.43 r	
F8/f4/h2/U2/Z (CIVX2)	0.07
9.50 f	
F8/f4/h2/U1/Z (CNR2X2)	0.11
9.61 r	
F8/f4/h2/cout_ha (HA_65)	0.00
9.61 r	
F8/f4/U2/Z (CIVX2)	0.08
9.70 f	
F8/f4/U1/Z (CND2IX2)	0.07
9.77 r	
F8/f4/cout_fa1 (FA_1bit_33)	0.00
9.77 r	
F8/cout_fa4_2 (FA_4bit_2_9)	0.00
9.77 r	
F9/cin_fa4 (FA_4bit_2_8)	0.00
9.77 r	

F9/f1/cin (FA_1bit_32)	0.00
9.77 r	
F9/f1/h2/op2_ha (HA_63)	0.00
9.77 r	
F9/f1/h2/U2/Z (CIVX2)	0.07
9.84 f	
F9/f1/h2/U1/Z (CNR2X2)	0.11
9.95 r	
F9/f1/h2/cout_ha (HA_63)	0.00
9.95 r	
F9/f1/U2/Z (CIVX2)	0.08
10.04 f	
F9/f1/U1/Z (CND2IX2)	0.07
10.11 r	
F9/f1/cout_fa1 (FA_1bit_32)	0.00
10.11 r	
F9/f2/cin (FA_1bit_31)	0.00
10.11 r	
F9/f2/h2/op2_ha (HA_61)	0.00
10.11 r	
F9/f2/h2/U2/Z (CIVX2)	0.07
10.18 f	
F9/f2/h2/U1/Z (CNR2X2)	0.11
10.29 r	
F9/f2/h2/cout_ha (HA_61)	0.00
10.29 r	
F9/f2/U2/Z (CIVX2)	0.08
10.38 f	
F9/f2/U1/Z (CND2IX2)	0.07
10.45 r	
F9/f2/cout_fa1 (FA_1bit_31)	0.00
10.45 r	
F9/f3/cin (FA_1bit_30)	0.00
10.45 r	
F9/f3/h2/op2_ha (HA_59)	0.00
10.45 r	
F9/f3/h2/U2/Z (CIVX2)	0.07
10.52 f	
F9/f3/h2/U1/Z (CNR2X2)	0.11
10.63 r	

F9/f3/h2/cout_ha (HA_59)	0.00
10.63 r	
F9/f3/U2/Z (CIVX2)	0.08
10.72 f	
F9/f3/U1/Z (CND2IX2)	0.07
10.79 r	
F9/f3/cout_fa1 (FA_1bit_30)	0.00
10.79 r	
F9/f4/cin (FA_1bit_29)	0.00
10.79 r	
F9/f4/h2/op2_ha (HA_57)	0.00
10.79 r	
F9/f4/h2/U2/Z (CIVX2)	0.07
10.86 f	
F9/f4/h2/U1/Z (CNR2X2)	0.11
10.97 r	
F9/f4/h2/cout_ha (HA_57)	0.00
10.97 r	
F9/f4/U2/Z (CIVX2)	0.08
11.06 f	
F9/f4/U1/Z (CND2IX2)	0.07
11.13 r	
F9/f4/cout_fa1 (FA_1bit_29)	0.00
11.13 r	
F9/cout_fa4_2 (FA_4bit_2_8)	0.00
11.13 r	
F10/cin_fa4 (FA_4bit_2_7)	0.00
11.13 r	
F10/f1/cin (FA_1bit_28)	0.00
11.13 r	
F10/f1/h2/op2_ha (HA_55)	0.00
11.13 r	
F10/f1/h2/U2/Z (CIVX2)	0.07
11.20 f	
F10/f1/h2/U1/Z (CNR2X2)	0.11
11.31 r	
F10/f1/h2/cout_ha (HA_55)	0.00
11.31 r	
F10/f1/U2/Z (CIVX2)	0.08
11.40 f	

F10/f1/U1/Z (CND2IX2)	0.07
11.47 r	
F10/f1/cout_fa1 (FA_1bit_28)	0.00
11.47 r	
F10/f2/cin (FA_1bit_27)	0.00
11.47 r	
F10/f2/h2/op2_ha (HA_53)	0.00
11.47 r	
F10/f2/h2/U2/Z (CIVX2)	0.07
11.54 f	
F10/f2/h2/U1/Z (CNR2X2)	0.11
11.65 r	
F10/f2/h2/cout_ha (HA_53)	0.00
11.65 r	
F10/f2/U2/Z (CIVX2)	0.08
11.74 f	
F10/f2/U1/Z (CND2IX2)	0.07
11.81 r	
F10/f2/cout_fa1 (FA_1bit_27)	0.00
11.81 r	
F10/f3/cin (FA_1bit_26)	0.00
11.81 r	
F10/f3/h2/op2_ha (HA_51)	0.00
11.81 r	
F10/f3/h2/U2/Z (CIVX2)	0.07
11.88 f	
F10/f3/h2/U1/Z (CNR2X2)	0.11
11.99 r	
F10/f3/h2/cout_ha (HA_51)	0.00
11.99 r	
F10/f3/U2/Z (CIVX2)	0.08
12.08 f	
F10/f3/U1/Z (CND2IX2)	0.07
12.15 r	
F10/f3/cout_fa1 (FA_1bit_26)	0.00
12.15 r	
F10/f4/cin (FA_1bit_25)	0.00
12.15 r	
F10/f4/h2/op2_ha (HA_49)	0.00
12.15 r	

F10/f4/h2/U2/Z (CIVX2)	0.07
12.22 f	
F10/f4/h2/U1/Z (CNR2X2)	0.11
12.33 r	
F10/f4/h2/cout_ha (HA_49)	0.00
12.33 r	
F10/f4/U2/Z (CIVX2)	0.08
12.42 f	
F10/f4/U1/Z (CND2IX2)	0.07
12.49 r	
F10/cout_fa1 (FA_1bit_25)	0.00
12.49 r	
F10/cout_fa4_2 (FA_4bit_2_7)	0.00
12.49 r	
F11/cin_fa4 (FA_4bit_2_6)	0.00
12.49 r	
F11/f1/cin (FA_1bit_24)	0.00
12.49 r	
F11/f1/h2/op2_ha (HA_47)	0.00
12.49 r	
F11/f1/h2/U2/Z (CIVX2)	0.07
12.56 f	
F11/f1/h2/U1/Z (CNR2X2)	0.11
12.67 r	
F11/f1/h2/cout_ha (HA_47)	0.00
12.67 r	
F11/f1/U2/Z (CIVX2)	0.08
12.76 f	
F11/f1/U1/Z (CND2IX2)	0.07
12.83 r	
F11/f1/cout_fa1 (FA_1bit_24)	0.00
12.83 r	
F11/f2/cin (FA_1bit_23)	0.00
12.83 r	
F11/f2/h2/op2_ha (HA_45)	0.00
12.83 r	
F11/f2/h2/U2/Z (CIVX2)	0.07
12.90 f	
F11/f2/h2/U1/Z (CNR2X2)	0.11
13.01 r	

F11/f2/h2/cout_ha (HA_45)	0.00
13.01 r	
F11/f2/U2/Z (CIVX2)	0.08
13.10 f	
F11/f2/U1/Z (CND2IX2)	0.07
13.17 r	
F11/f2/cout_fa1 (FA_1bit_23)	0.00
13.17 r	
F11/f3/cin (FA_1bit_22)	0.00
13.17 r	
F11/f3/h2/op2_ha (HA_43)	0.00
13.17 r	
F11/f3/h2/U2/Z (CIVX2)	0.07
13.24 f	
F11/f3/h2/U1/Z (CNR2X2)	0.11
13.35 r	
F11/f3/h2/cout_ha (HA_43)	0.00
13.35 r	
F11/f3/U2/Z (CIVX2)	0.08
13.44 f	
F11/f3/U1/Z (CND2IX2)	0.07
13.51 r	
F11/f3/cout_fa1 (FA_1bit_22)	0.00
13.51 r	
F11/f4/cin (FA_1bit_21)	0.00
13.51 r	
F11/f4/h2/op2_ha (HA_41)	0.00
13.51 r	
F11/f4/h2/U2/Z (CIVX2)	0.07
13.58 f	
F11/f4/h2/U1/Z (CNR2X2)	0.11
13.69 r	
F11/f4/h2/cout_ha (HA_41)	0.00
13.69 r	
F11/f4/U2/Z (CIVX2)	0.08
13.78 f	
F11/f4/U1/Z (CND2IX2)	0.07
13.85 r	
F11/f4/cout_fa1 (FA_1bit_21)	0.00
13.85 r	

F11/cout_fa4_2 (FA_4bit_2_6)	0.00
13.85 r	
F12/cin_fa4 (FA_4bit_2_5)	0.00
13.85 r	
F12/f1/cin (FA_1bit_20)	0.00
13.85 r	
F12/f1/h2/op2_ha (HA_39)	0.00
13.85 r	
F12/f1/h2/U2/Z (CIVX2)	0.07
13.92 f	
F12/f1/h2/U1/Z (CNR2X2)	0.11
14.03 r	
F12/f1/h2/cout_ha (HA_39)	0.00
14.03 r	
F12/f1/U2/Z (CIVX2)	0.08
14.12 f	
F12/f1/U1/Z (CND2IX2)	0.07
14.19 r	
F12/f1/cout_fa1 (FA_1bit_20)	0.00
14.19 r	
F12/f2/cin (FA_1bit_19)	0.00
14.19 r	
F12/f2/h2/op2_ha (HA_37)	0.00
14.19 r	
F12/f2/h2/U2/Z (CIVX2)	0.07
14.26 f	
F12/f2/h2/U1/Z (CNR2X2)	0.11
14.37 r	
F12/f2/h2/cout_ha (HA_37)	0.00
14.37 r	
F12/f2/U2/Z (CIVX2)	0.08
14.46 f	
F12/f2/U1/Z (CND2IX2)	0.07
14.53 r	
F12/f2/cout_fa1 (FA_1bit_19)	0.00
14.53 r	
F12/f3/cin (FA_1bit_18)	0.00
14.53 r	
F12/f3/h2/op2_ha (HA_35)	0.00
14.53 r	

F12/f3/h2/U2/Z (CIVX2)	0.07
14.60 f	
F12/f3/h2/U1/Z (CNR2X2)	0.11
14.71 r	
F12/f3/h2/cout_ha (HA_35)	0.00
14.71 r	
F12/f3/U2/Z (CIVX2)	0.08
14.80 f	
F12/f3/U1/Z (CND2IX2)	0.07
14.87 r	
F12/f3/cout_fa1 (FA_1bit_18)	0.00
14.87 r	
F12/f4/cin (FA_1bit_17)	0.00
14.87 r	
F12/f4/h2/op2_ha (HA_33)	0.00
14.87 r	
F12/f4/h2/U2/Z (CIVX2)	0.07
14.94 f	
F12/f4/h2/U1/Z (CNR2X2)	0.11
15.05 r	
F12/f4/h2/cout_ha (HA_33)	0.00
15.05 r	
F12/f4/U2/Z (CIVX2)	0.08
15.14 f	
F12/f4/U1/Z (CND2IX2)	0.07
15.21 r	
F12/f4/cout_fa1 (FA_1bit_17)	0.00
15.21 r	
F12/cout_fa4_2 (FA_4bit_2_5)	0.00
15.21 r	
F13/cin_fa4 (FA_4bit_2_4)	0.00
15.21 r	
F13/f1/cin (FA_1bit_16)	0.00
15.21 r	
F13/f1/h2/op2_ha (HA_31)	0.00
15.21 r	
F13/f1/h2/U2/Z (CIVX2)	0.07
15.28 f	
F13/f1/h2/U1/Z (CNR2X2)	0.11
15.39 r	

F13/f1/h2/cout_ha (HA_31)	0.00
15.39 r	
F13/f1/U2/Z (CIVX2)	0.08
15.48 f	
F13/f1/U1/Z (CND2IX2)	0.07
15.55 r	
F13/f1/cout_fa1 (FA_1bit_16)	0.00
15.55 r	
F13/f2/cin (FA_1bit_15)	0.00
15.55 r	
F13/f2/h2/op2_ha (HA_29)	0.00
15.55 r	
F13/f2/h2/U2/Z (CIVX2)	0.07
15.62 f	
F13/f2/h2/U1/Z (CNR2X2)	0.11
15.73 r	
F13/f2/h2/cout_ha (HA_29)	0.00
15.73 r	
F13/f2/U2/Z (CIVX2)	0.08
15.82 f	
F13/f2/U1/Z (CND2IX2)	0.07
15.89 r	
F13/f2/cout_fa1 (FA_1bit_15)	0.00
15.89 r	
F13/f3/cin (FA_1bit_14)	0.00
15.89 r	
F13/f3/h2/op2_ha (HA_27)	0.00
15.89 r	
F13/f3/h2/U2/Z (CIVX2)	0.07
15.96 f	
F13/f3/h2/U1/Z (CNR2X2)	0.10
16.06 r	
F13/f3/h2/cout_ha (HA_27)	0.00
16.06 r	
F13/f3/U1/Z (CNR2IX1)	0.10
16.16 f	
F13/f3/U3/Z (CIVX2)	0.09
16.24 r	
F13/f3/cout_fa1 (FA_1bit_14)	0.00
16.24 r	

F13/f4/cin (FA_1bit_13)	0.00
16.24 r	
F13/f4/h2/op2_ha (HA_25)	0.00
16.24 r	
F13/f4/h2/U1/Z (CND2X2)	0.10
16.34 f	
F13/f4/h2/U2/Z (CIVX2)	0.06
16.40 r	
F13/f4/h2/cout_ha (HA_25)	0.00
16.40 r	
F13/f4/U2/Z (CIVX2)	0.06
16.47 f	
F13/f4/U1/Z (CND2IX2)	0.07
16.54 r	
F13/f4/cout_fa1 (FA_1bit_13)	0.00
16.54 r	
F13/cout_fa4_2 (FA_4bit_2_4)	0.00
16.54 r	
F14/cin_fa4 (FA_4bit_2_3)	0.00
16.54 r	
F14/f1/cin (FA_1bit_12)	0.00
16.54 r	
F14/f1/h2/op2_ha (HA_23)	0.00
16.54 r	
F14/f1/h2/U1/Z (CND2X2)	0.09
16.63 f	
F14/f1/h2/U2/Z (CIVX2)	0.06
16.69 r	
F14/f1/h2/cout_ha (HA_23)	0.00
16.69 r	
F14/f1/U2/Z (CIVX2)	0.06
16.76 f	
F14/f1/U1/Z (CND2IX2)	0.09
16.84 r	
F14/f1/cout_fa1 (FA_1bit_12)	0.00
16.84 r	
F14/f2/cin (FA_1bit_11)	0.00
16.84 r	
F14/f2/h2/op2_ha (HA_21)	0.00
16.84 r	

F14/f2/h2/U1/Z (CND2X2)	0.10
16.94 f	
F14/f2/h2/U2/Z (CIVX2)	0.06
17.00 r	
F14/f2/h2/cout_ha (HA_21)	0.00
17.00 r	
F14/f2/U2/Z (CIVX2)	0.06
17.07 f	
F14/f2/U1/Z (CND2IX2)	0.07
17.14 r	
F14/f2/cout_fa1 (FA_1bit_11)	0.00
17.14 r	
F14/f3/cin (FA_1bit_10)	0.00
17.14 r	
F14/f3/h2/op2_ha (HA_19)	0.00
17.14 r	
F14/f3/h2/U1/Z (CND2X2)	0.09
17.23 f	
F14/f3/h2/U2/Z (CIVX2)	0.06
17.29 r	
F14/f3/h2/cout_ha (HA_19)	0.00
17.29 r	
F14/f3/U2/Z (CIVX2)	0.06
17.36 f	
F14/f3/U1/Z (CND2IX2)	0.07
17.43 r	
F14/f3/cout_fa1 (FA_1bit_10)	0.00
17.43 r	
F14/f4/cin (FA_1bit_9)	0.00
17.43 r	
F14/f4/h2/op2_ha (HA_17)	0.00
17.43 r	
F14/f4/h2/U1/Z (CND2X2)	0.09
17.52 f	
F14/f4/h2/U2/Z (CIVX2)	0.06
17.58 r	
F14/f4/h2/cout_ha (HA_17)	0.00
17.58 r	
F14/f4/U2/Z (CIVX2)	0.06
17.65 f	

F14/f4/U1/Z (CND2IX2)	0.07
17.72 r	
F14/f4/cout_fa1 (FA_1bit_9)	0.00
17.72 r	
F14/cout_fa4_2 (FA_4bit_2_3)	0.00
17.72 r	
F15/cin_fa4 (FA_4bit_2_2)	0.00
17.72 r	
F15/f1/cin (FA_1bit_8)	0.00
17.72 r	
F15/f1/h2/op2_ha (HA_15)	0.00
17.72 r	
F15/f1/h2/U1/Z (CND2X2)	0.09
17.81 f	
F15/f1/h2/U2/Z (CIVX2)	0.06
17.87 r	
F15/f1/h2/cout_ha (HA_15)	0.00
17.87 r	
F15/f1/U2/Z (CIVX2)	0.06
17.94 f	
F15/f1/U1/Z (CND2IX2)	0.07
18.01 r	
F15/f1/cout_fa1 (FA_1bit_8)	0.00
18.01 r	
F15/f2/cin (FA_1bit_7)	0.00
18.01 r	
F15/f2/h2/op2_ha (HA_13)	0.00
18.01 r	
F15/f2/h2/U1/Z (CND2X2)	0.09
18.10 f	
F15/f2/h2/U2/Z (CIVX2)	0.06
18.16 r	
F15/f2/h2/cout_ha (HA_13)	0.00
18.16 r	
F15/f2/U2/Z (CIVX2)	0.06
18.23 f	
F15/f2/U1/Z (CND2IX2)	0.07
18.30 r	
F15/f2/cout_fa1 (FA_1bit_7)	0.00
18.30 r	

F15/f3/cin (FA_1bit_6)	0.00
18.30 r	
F15/f3/h2/op2_ha (HA_11)	0.00
18.30 r	
F15/f3/h2/U1/Z (CND2X2)	0.09
18.39 f	
F15/f3/h2/U2/Z (CIVX2)	0.06
18.45 r	
F15/f3/h2/cout_ha (HA_11)	0.00
18.45 r	
F15/f3/U2/Z (CIVX2)	0.06
18.52 f	
F15/f3/U1/Z (CND2IX2)	0.07
18.59 r	
F15/f3/cout_fa1 (FA_1bit_6)	0.00
18.59 r	
F15/f4/cin (FA_1bit_5)	0.00
18.59 r	
F15/f4/h2/op2_ha (HA_9)	0.00
18.59 r	
F15/f4/h2/U2/Z (CIVX2)	0.07
18.66 f	
F15/f4/h2/U1/Z (CNR2X2)	0.10
18.76 r	
F15/f4/h2/cout_ha (HA_9)	0.00
18.76 r	
F15/f4/U2/Z (CIVX1)	0.10
18.85 f	
F15/f4/U1/Z (CND2IX2)	0.08
18.93 r	
F15/f4/cout_fa1 (FA_1bit_5)	0.00
18.93 r	
F15/cout_fa4_2 (FA_4bit_2_2)	0.00
18.93 r	
F16/cin_fa4 (FA_4bit_2_1)	0.00
18.93 r	
F16/f1/cin (FA_1bit_4)	0.00
18.93 r	
F16/f1/h2/op2_ha (HA_7)	0.00
18.93 r	

F16/f1/h2/U3/Z (CDLY1XL)	0.62	
19.55 r		
F16/f1/h2/U4/Z (CIVXL)	0.08	
19.62 f		
F16/f1/h2/U5/Z (CIVXL)	0.10	
19.72 r		
F16/f1/h2/U6/Z (CEOXL)	0.35	
20.08 r		
F16/f1/h2/sum_ha (HA_7)	0.00	
20.08 r		
F16/f1/sum_fa1 (FA_1bit_4)	0.00	
20.08 r		
F16/sum_fa4_2[0] (FA_4bit_2_1)	0.00	
20.08 r		
sum_reg[60]/D (CFD2QX1)	0.00	
20.08 r		
data	arrival	time
20.08		
 clock clock (rise edge)	20.80	
20.80		
clock network delay (propagated)	0.00	
20.80		
clock uncertainty	-0.25	
20.55		
sum_reg[60]/CP (CFD2QX1)	0.00	
20.55 r		
library setup time	-0.34	
20.21		
data	required	time
20.21		

data	required	time
20.21		
data arrival time	-	
20.08		

slack (MET)
0.13

Startpoint: op2f_reg[1]
 (rising edge-triggered flip-flop clocked
 by clock)
 Endpoint: sum_reg[62]
 (rising edge-triggered flip-flop clocked by
 clock)
 Path Group: clock
 Path Type: max

Point	Incr
Path	
-----	-----
clock clock (rise edge)	0.00
0.00	
clock network delay (propagated)	0.00
0.00	
op2f_reg[1]/CP (CFD2QX2)	0.00
0.00 r	
op2f_reg[1]/Q (CFD2QX2)	0.50
0.50 f	
F1/op2_fa4[1] (FA_4bit_1)	0.00
0.50 f	
F1/f1/op2_fa1 (FA_1bit_0)	0.00
0.50 f	
F1/f1/h1/op2_ha (HA_126)	0.00
0.50 f	
F1/f1/h1/U2/Z (CIVX2)	0.08
0.58 r	
F1/f1/h1/U4/Z (CND2X2)	0.09
0.67 f	
F1/f1/h1/U5/Z (CND2X2)	0.09
0.76 r	
F1/f1/h1/sum_ha (HA_126)	0.00
0.76 r	

F1/f1/h2/op1_ha (HA_125)	0.00
0.76 r	
F1/f1/h2/U1/Z (CND2X2)	0.09
0.85 f	
F1/f1/h2/U2/Z (CIVX2)	0.06
0.91 r	
F1/f1/h2/cout_ha (HA_125)	0.00
0.91 r	
F1/f1/U2/Z (CIVX2)	0.06
0.98 f	
F1/f1/U1/Z (CND2IX2)	0.07
1.05 r	
F1/f1/cout_fa1 (FA_1bit_0)	0.00
1.05 r	
F1/f2/cin (FA_1bit_62)	0.00
1.05 r	
F1/f2/h2/op2_ha (HA_123)	0.00
1.05 r	
F1/f2/h2/U1/Z (CND2X2)	0.09
1.14 f	
F1/f2/h2/U2/Z (CIVX2)	0.06
1.20 r	
F1/f2/h2/cout_ha (HA_123)	0.00
1.20 r	
F1/f2/U2/Z (CIVX2)	0.06
1.27 f	
F1/f2/U1/Z (CND2IX2)	0.07
1.34 r	
F1/f2/cout_fa1 (FA_1bit_62)	0.00
1.34 r	
F1/f3/cin (FA_1bit_61)	0.00
1.34 r	
F1/f3/h2/op2_ha (HA_121)	0.00
1.34 r	
F1/f3/h2/U1/Z (CND2X2)	0.09
1.43 f	
F1/f3/h2/U2/Z (CIVX2)	0.06
1.49 r	
F1/f3/h2/cout_ha (HA_121)	0.00
1.49 r	

F1/f3/U1/Z (CNR2IX2)	0.07
1.56 f	
F1/f3/U2/Z (CIVX2)	0.07
1.63 r	
F1/f3/cout_fa1 (FA_1bit_61)	0.00
1.63 r	
F1/cout_fa4 (FA_4bit_1)	0.00
1.63 r	
F2/cin_fa4 (FA_4bit_2_0)	0.00
1.63 r	
F2/f1/cin (FA_1bit_60)	0.00
1.63 r	
F2/f1/h2/op2_ha (HA_119)	0.00
1.63 r	
F2/f1/h2/U1/Z (CND2X2)	0.09
1.72 f	
F2/f1/h2/U2/Z (CIVX2)	0.06
1.78 r	
F2/f1/h2/cout_ha (HA_119)	0.00
1.78 r	
F2/f1/U1/Z (CNR2IX2)	0.07
1.85 f	
F2/f1/U2/Z (CIVX2)	0.07
1.91 r	
F2/f1/cout_fa1 (FA_1bit_60)	0.00
1.91 r	
F2/f2/cin (FA_1bit_59)	0.00
1.91 r	
F2/f2/h2/op2_ha (HA_117)	0.00
1.91 r	
F2/f2/h2/U1/Z (CND2X2)	0.09
2.00 f	
F2/f2/h2/U2/Z (CIVX2)	0.06
2.07 r	
F2/f2/h2/cout_ha (HA_117)	0.00
2.07 r	
F2/f2/U1/Z (CNR2IX2)	0.07
2.13 f	
F2/f2/U2/Z (CIVX2)	0.07
2.20 r	

F2/f2/cout_fa1 (FA_1bit_59)	0.00
2.20 r	
F2/f3/cin (FA_1bit_58)	0.00
2.20 r	
F2/f3/h2/op2_ha (HA_115)	0.00
2.20 r	
F2/f3/h2/U1/Z (CND2X2)	0.09
2.29 f	
F2/f3/h2/U2/Z (CIVX2)	0.06
2.35 r	
F2/f3/h2/cout_ha (HA_115)	0.00
2.35 r	
F2/f3/U1/Z (CNR2IX2)	0.07
2.42 f	
F2/f3/U3/Z (CIVX2)	0.07
2.49 r	
F2/f3/cout_fa1 (FA_1bit_58)	0.00
2.49 r	
F2/f4/cin (FA_1bit_57)	0.00
2.49 r	
F2/f4/h2/op2_ha (HA_113)	0.00
2.49 r	
F2/f4/h2/U2/Z (CND2X2)	0.09
2.58 f	
F2/f4/h2/U3/Z (CIVX2)	0.06
2.64 r	
F2/f4/h2/cout_ha (HA_113)	0.00
2.64 r	
F2/f4/U1/Z (CNR2IX2)	0.07
2.71 f	
F2/f4/U2/Z (CIVX2)	0.07
2.77 r	
F2/f4/cout_fa1 (FA_1bit_57)	0.00
2.77 r	
F2/cout_fa4_2 (FA_4bit_2_0)	0.00
2.77 r	
F3/cin_fa4 (FA_4bit_2_14)	0.00
2.77 r	
F3/f1/cin (FA_1bit_56)	0.00
2.77 r	

F3/f1/h2/op2_ha (HA_111)	0.00
2.77 r	
F3/f1/h2/U1/Z (CND2X2)	0.09
2.86 f	
F3/f1/h2/U2/Z (CIVX2)	0.06
2.93 r	
F3/f1/h2/cout_ha (HA_111)	0.00
2.93 r	
F3/f1/U1/Z (CNR2IX2)	0.07
2.99 f	
F3/f1/U2/Z (CIVX2)	0.07
3.06 r	
F3/f1/cout_fa1 (FA_1bit_56)	0.00
3.06 r	
F3/f2/cin (FA_1bit_55)	0.00
3.06 r	
F3/f2/h2/op2_ha (HA_109)	0.00
3.06 r	
F3/f2/h2/U1/Z (CND2X2)	0.09
3.15 f	
F3/f2/h2/U2/Z (CIVX2)	0.06
3.21 r	
F3/f2/h2/cout_ha (HA_109)	0.00
3.21 r	
F3/f2/U2/Z (CIVX2)	0.06
3.27 f	
F3/f2/U1/Z (CND2IX2)	0.07
3.35 r	
F3/f2/cout_fa1 (FA_1bit_55)	0.00
3.35 r	
F3/f3/cin (FA_1bit_54)	0.00
3.35 r	
F3/f3/h2/op2_ha (HA_107)	0.00
3.35 r	
F3/f3/h2/U1/Z (CND2X2)	0.09
3.44 f	
F3/f3/h2/U2/Z (CIVX2)	0.06
3.50 r	
F3/f3/h2/cout_ha (HA_107)	0.00
3.50 r	

F3/f3/U1/Z (CNR2IX2)	0.07
3.57 f	
F3/f3/U2/Z (CIVX2)	0.07
3.64 r	
F3/f3/cout_fa1 (FA_1bit_54)	0.00
3.64 r	
F3/f4/cin (FA_1bit_53)	0.00
3.64 r	
F3/f4/h2/op2_ha (HA_105)	0.00
3.64 r	
F3/f4/h2/U1/Z (CND2X2)	0.09
3.72 f	
F3/f4/h2/U2/Z (CIVX2)	0.06
3.79 r	
F3/f4/h2/cout_ha (HA_105)	0.00
3.79 r	
F3/f4/U1/Z (CNR2IX2)	0.07
3.85 f	
F3/f4/U2/Z (CIVX2)	0.07
3.92 r	
F3/f4/cout_fa1 (FA_1bit_53)	0.00
3.92 r	
F3/cout_fa4_2 (FA_4bit_2_14)	0.00
3.92 r	
F4/cin_fa4 (FA_4bit_2_13)	0.00
3.92 r	
F4/f1/cin (FA_1bit_52)	0.00
3.92 r	
F4/f1/h2/op2_ha (HA_103)	0.00
3.92 r	
F4/f1/h2/U1/Z (CND2X2)	0.09
4.01 f	
F4/f1/h2/U2/Z (CIVX2)	0.06
4.07 r	
F4/f1/h2/cout_ha (HA_103)	0.00
4.07 r	
F4/f1/U1/Z (CNR2IX2)	0.07
4.14 f	
F4/f1/U3/Z (CIVX2)	0.07
4.21 r	

F4/f1/cout_fa1 (FA_1bit_52)	0.00
4.21 r	
F4/f2/cin (FA_1bit_51)	0.00
4.21 r	
F4/f2/h2/op2_ha (HA_101)	0.00
4.21 r	
F4/f2/h2/U1/Z (CND2X2)	0.09
4.30 f	
F4/f2/h2/U2/Z (CIVX2)	0.06
4.36 r	
F4/f2/h2/cout_ha (HA_101)	0.00
4.36 r	
F4/f2/U1/Z (CNR2IX2)	0.07
4.43 f	
F4/f2/U2/Z (CIVX2)	0.07
4.49 r	
F4/f2/cout_fa1 (FA_1bit_51)	0.00
4.49 r	
F4/f3/cin (FA_1bit_50)	0.00
4.49 r	
F4/f3/h2/op2_ha (HA_99)	0.00
4.49 r	
F4/f3/h2/U1/Z (CND2X2)	0.09
4.58 f	
F4/f3/h2/U2/Z (CIVX2)	0.06
4.65 r	
F4/f3/h2/cout_ha (HA_99)	0.00
4.65 r	
F4/f3/U1/Z (CNR2IX2)	0.07
4.71 f	
F4/f3/U2/Z (CIVX2)	0.07
4.78 r	
F4/f3/cout_fa1 (FA_1bit_50)	0.00
4.78 r	
F4/f4/cin (FA_1bit_49)	0.00
4.78 r	
F4/f4/h2/op2_ha (HA_97)	0.00
4.78 r	
F4/f4/h2/U1/Z (CND2X2)	0.09
4.87 f	

F4/f4/h2/U2/Z (CIVX2)	0.06
4.93 r	
F4/f4/h2/cout_ha (HA_97)	0.00
4.93 r	
F4/f4/U1/Z (CNR2IX2)	0.07
5.00 f	
F4/f4/U2/Z (CIVX2)	0.07
5.07 r	
F4/f4/cout_fa1 (FA_1bit_49)	0.00
5.07 r	
F4/cout_fa4_2 (FA_4bit_2_13)	0.00
5.07 r	
F5/cin_fa4 (FA_4bit_2_12)	0.00
5.07 r	
F5/f1/cin (FA_1bit_48)	0.00
5.07 r	
F5/f1/h2/op2_ha (HA_95)	0.00
5.07 r	
F5/f1/h2/U1/Z (CND2X2)	0.09
5.16 f	
F5/f1/h2/U2/Z (CIVX2)	0.06
5.22 r	
F5/f1/h2/cout_ha (HA_95)	0.00
5.22 r	
F5/f1/U2/Z (CIVX2)	0.06
5.28 f	
F5/f1/U1/Z (CND2IX2)	0.07
5.35 r	
F5/f1/cout_fa1 (FA_1bit_48)	0.00
5.35 r	
F5/f2/cin (FA_1bit_47)	0.00
5.35 r	
F5/f2/h2/op2_ha (HA_93)	0.00
5.35 r	
F5/f2/h2/U1/Z (CND2X2)	0.09
5.45 f	
F5/f2/h2/U2/Z (CIVX2)	0.06
5.51 r	
F5/f2/h2/cout_ha (HA_93)	0.00
5.51 r	

F5/f2/U1/Z (CNR2IX2)	0.07
5.58 f	
F5/f2/U2/Z (CIVX2)	0.07
5.64 r	
F5/f2/cout_fa1 (FA_1bit_47)	0.00
5.64 r	
F5/f3/cin (FA_1bit_46)	0.00
5.64 r	
F5/f3/h2/op2_ha (HA_91)	0.00
5.64 r	
F5/f3/h2/U1/Z (CND2X2)	0.09
5.73 f	
F5/f3/h2/U2/Z (CIVX2)	0.06
5.79 r	
F5/f3/h2/cout_ha (HA_91)	0.00
5.79 r	
F5/f3/U1/Z (CNR2IX2)	0.07
5.86 f	
F5/f3/U2/Z (CIVX2)	0.07
5.93 r	
F5/f3/cout_fa1 (FA_1bit_46)	0.00
5.93 r	
F5/f4/cin (FA_1bit_45)	0.00
5.93 r	
F5/f4/h2/op2_ha (HA_89)	0.00
5.93 r	
F5/f4/h2/U1/Z (CND2X2)	0.09
6.02 f	
F5/f4/h2/U2/Z (CIVX2)	0.06
6.08 r	
F5/f4/h2/cout_ha (HA_89)	0.00
6.08 r	
F5/f4/U2/Z (CIVX2)	0.06
6.14 f	
F5/f4/U1/Z (CND2IX2)	0.07
6.22 r	
F5/f4/cout_fa1 (FA_1bit_45)	0.00
6.22 r	
F5/cout_fa4_2 (FA_4bit_2_12)	0.00
6.22 r	

F6/cin_fa4 (FA_4bit_2_11)	0.00
6.22 r	
F6/f1/cin (FA_1bit_44)	0.00
6.22 r	
F6/f1/h2/op2_ha (HA_87)	0.00
6.22 r	
F6/f1/h2/U1/Z (CND2X2)	0.09
6.31 f	
F6/f1/h2/U2/Z (CIVX2)	0.06
6.37 r	
F6/f1/h2/cout_ha (HA_87)	0.00
6.37 r	
F6/f1/U1/Z (CNR2IX2)	0.07
6.44 f	
F6/f1/U2/Z (CIVX2)	0.07
6.50 r	
F6/f1/cout_fa1 (FA_1bit_44)	0.00
6.50 r	
F6/f2/cin (FA_1bit_43)	0.00
6.50 r	
F6/f2/h2/op2_ha (HA_85)	0.00
6.50 r	
F6/f2/h2/U1/Z (CND2X2)	0.09
6.59 f	
F6/f2/h2/U2/Z (CIVX2)	0.06
6.66 r	
F6/f2/h2/cout_ha (HA_85)	0.00
6.66 r	
F6/f2/U1/Z (CNR2IX2)	0.07
6.72 f	
F6/f2/U2/Z (CIVX2)	0.07
6.79 r	
F6/f2/cout_fa1 (FA_1bit_43)	0.00
6.79 r	
F6/f3/cin (FA_1bit_42)	0.00
6.79 r	
F6/f3/h2/op2_ha (HA_83)	0.00
6.79 r	
F6/f3/h2/U1/Z (CND2X2)	0.09
6.88 f	

F6/f3/h2/U2/Z (CIVX2)	0.06
6.94 r	
F6/f3/h2/cout_ha (HA_83)	0.00
6.94 r	
F6/f3/U1/Z (CNR2IX2)	0.07
7.01 f	
F6/f3/U3/Z (CIVX2)	0.07
7.08 r	
F6/f3/cout_fa1 (FA_1bit_42)	0.00
7.08 r	
F6/f4/cin (FA_1bit_41)	0.00
7.08 r	
F6/f4/h2/op2_ha (HA_81)	0.00
7.08 r	
F6/f4/h2/U1/Z (CND2X2)	0.09
7.17 f	
F6/f4/h2/U2/Z (CIVX2)	0.06
7.23 r	
F6/f4/h2/cout_ha (HA_81)	0.00
7.23 r	
F6/f4/U1/Z (CNR2IX2)	0.07
7.30 f	
F6/f4/U2/Z (CIVX2)	0.07
7.36 r	
F6/f4/cout_fa1 (FA_1bit_41)	0.00
7.36 r	
F6/cout_fa4_2 (FA_4bit_2_11)	0.00
7.36 r	
F7/cin_fa4 (FA_4bit_2_10)	0.00
7.36 r	
F7/f1/cin (FA_1bit_40)	0.00
7.36 r	
F7/f1/h2/op2_ha (HA_79)	0.00
7.36 r	
F7/f1/h2/U1/Z (CND2X2)	0.09
7.45 f	
F7/f1/h2/U2/Z (CIVX2)	0.06
7.52 r	
F7/f1/h2/cout_ha (HA_79)	0.00
7.52 r	

F7/f1/U1/Z (CNR2IX2)	0.07
7.58 f	
F7/f1/U2/Z (CIVX2)	0.07
7.65 r	
F7/f1/cout_fa1 (FA_1bit_40)	0.00
7.65 r	
F7/f2/cin (FA_1bit_39)	0.00
7.65 r	
F7/f2/h2/op2_ha (HA_77)	0.00
7.65 r	
F7/f2/h2/U1/Z (CND2X2)	0.09
7.74 f	
F7/f2/h2/U2/Z (CIVX2)	0.06
7.80 r	
F7/f2/h2/cout_ha (HA_77)	0.00
7.80 r	
F7/f2/U1/Z (CNR2IX2)	0.07
7.87 f	
F7/f2/U3/Z (CIVX2)	0.07
7.94 r	
F7/f2/cout_fa1 (FA_1bit_39)	0.00
7.94 r	
F7/f3/cin (FA_1bit_38)	0.00
7.94 r	
F7/f3/h2/op2_ha (HA_75)	0.00
7.94 r	
F7/f3/h2/U1/Z (CND2X2)	0.09
8.02 f	
F7/f3/h2/U2/Z (CIVX2)	0.06
8.09 r	
F7/f3/h2/cout_ha (HA_75)	0.00
8.09 r	
F7/f3/U2/Z (CIVX2)	0.06
8.15 f	
F7/f3/U1/Z (CND2IX2)	0.07
8.22 r	
F7/f3/cout_fa1 (FA_1bit_38)	0.00
8.22 r	
F7/f4/cin (FA_1bit_37)	0.00
8.22 r	

F7/f4/h2/op2_ha (HA_73)	0.00
8.22 r	
F7/f4/h2/U1/Z (CND2X2)	0.09
8.31 f	
F7/f4/h2/U2/Z (CIVX2)	0.06
8.38 r	
F7/f4/h2/cout_ha (HA_73)	0.00
8.38 r	
F7/f4/U1/Z (CNR2IX2)	0.07
8.44 f	
F7/f4/U3/Z (CIVX2)	0.07
8.51 r	
F7/f4/cout_fa1 (FA_1bit_37)	0.00
8.51 r	
F7/cout_fa4_2 (FA_4bit_2_10)	0.00
8.51 r	
F8/cin_fa4 (FA_4bit_2_9)	0.00
8.51 r	
F8/f1/cin (FA_1bit_36)	0.00
8.51 r	
F8/f1/h2/op2_ha (HA_71)	0.00
8.51 r	
F8/f1/h2/U1/Z (CND2X2)	0.09
8.60 f	
F8/f1/h2/U2/Z (CIVX2)	0.06
8.66 r	
F8/f1/h2/cout_ha (HA_71)	0.00
8.66 r	
F8/f1/U2/Z (CIVX2)	0.06
8.73 f	
F8/f1/U1/Z (CND2IX2)	0.07
8.80 r	
F8/f1/cout_fa1 (FA_1bit_36)	0.00
8.80 r	
F8/f2/cin (FA_1bit_35)	0.00
8.80 r	
F8/f2/h2/op2_ha (HA_69)	0.00
8.80 r	
F8/f2/h2/U1/Z (CND2X2)	0.09
8.89 f	

F8/f2/h2/U2/Z (CIVX2)	0.06
8.95 r	
F8/f2/h2/cout_ha (HA_69)	0.00
8.95 r	
F8/f2/U2/Z (CIVX2)	0.06
9.02 f	
F8/f2/U1/Z (CND2IX2)	0.07
9.09 r	
F8/f2/cout_fa1 (FA_1bit_35)	0.00
9.09 r	
F8/f3/cin (FA_1bit_34)	0.00
9.09 r	
F8/f3/h2/op2_ha (HA_67)	0.00
9.09 r	
F8/f3/h2/U2/Z (CIVX2)	0.07
9.16 f	
F8/f3/h2/U1/Z (CNR2X2)	0.11
9.27 r	
F8/f3/h2/cout_ha (HA_67)	0.00
9.27 r	
F8/f3/U2/Z (CIVX2)	0.08
9.36 f	
F8/f3/U1/Z (CND2IX2)	0.07
9.43 r	
F8/f3/cout_fa1 (FA_1bit_34)	0.00
9.43 r	
F8/f4/cin (FA_1bit_33)	0.00
9.43 r	
F8/f4/h2/op2_ha (HA_65)	0.00
9.43 r	
F8/f4/h2/U2/Z (CIVX2)	0.07
9.50 f	
F8/f4/h2/U1/Z (CNR2X2)	0.11
9.61 r	
F8/f4/h2/cout_ha (HA_65)	0.00
9.61 r	
F8/f4/U2/Z (CIVX2)	0.08
9.70 f	
F8/f4/U1/Z (CND2IX2)	0.07
9.77 r	

F8/f4/cout_fa1 (FA_1bit_33)	0.00
9.77 r	
F8/cout_fa4_2 (FA_4bit_2_9)	0.00
9.77 r	
F9/cin_fa4 (FA_4bit_2_8)	0.00
9.77 r	
F9/f1/cin (FA_1bit_32)	0.00
9.77 r	
F9/f1/h2/op2_ha (HA_63)	0.00
9.77 r	
F9/f1/h2/U2/Z (CIVX2)	0.07
9.84 f	
F9/f1/h2/U1/Z (CNR2X2)	0.11
9.95 r	
F9/f1/h2/cout_ha (HA_63)	0.00
9.95 r	
F9/f1/U2/Z (CIVX2)	0.08
10.04 f	
F9/f1/U1/Z (CND2IX2)	0.07
10.11 r	
F9/f1/cout_fa1 (FA_1bit_32)	0.00
10.11 r	
F9/f2/cin (FA_1bit_31)	0.00
10.11 r	
F9/f2/h2/op2_ha (HA_61)	0.00
10.11 r	
F9/f2/h2/U2/Z (CIVX2)	0.07
10.18 f	
F9/f2/h2/U1/Z (CNR2X2)	0.11
10.29 r	
F9/f2/h2/cout_ha (HA_61)	0.00
10.29 r	
F9/f2/U2/Z (CIVX2)	0.08
10.38 f	
F9/f2/U1/Z (CND2IX2)	0.07
10.45 r	
F9/f2/cout_fa1 (FA_1bit_31)	0.00
10.45 r	
F9/f3/cin (FA_1bit_30)	0.00
10.45 r	

F9/f3/h2/op2_ha (HA_59)	0.00
10.45 r	
F9/f3/h2/U2/Z (CIVX2)	0.07
10.52 f	
F9/f3/h2/U1/Z (CNR2X2)	0.11
10.63 r	
F9/f3/h2/cout_ha (HA_59)	0.00
10.63 r	
F9/f3/U2/Z (CIVX2)	0.08
10.72 f	
F9/f3/U1/Z (CND2IX2)	0.07
10.79 r	
F9/f3/cout_fa1 (FA_1bit_30)	0.00
10.79 r	
F9/f4/cin (FA_1bit_29)	0.00
10.79 r	
F9/f4/h2/op2_ha (HA_57)	0.00
10.79 r	
F9/f4/h2/U2/Z (CIVX2)	0.07
10.86 f	
F9/f4/h2/U1/Z (CNR2X2)	0.11
10.97 r	
F9/f4/h2/cout_ha (HA_57)	0.00
10.97 r	
F9/f4/U2/Z (CIVX2)	0.08
11.06 f	
F9/f4/U1/Z (CND2IX2)	0.07
11.13 r	
F9/f4/cout_fa1 (FA_1bit_29)	0.00
11.13 r	
F9/cout_fa4_2 (FA_4bit_2_8)	0.00
11.13 r	
F10/cin_fa4 (FA_4bit_2_7)	0.00
11.13 r	
F10/f1/cin (FA_1bit_28)	0.00
11.13 r	
F10/f1/h2/op2_ha (HA_55)	0.00
11.13 r	
F10/f1/h2/U2/Z (CIVX2)	0.07
11.20 f	

F10/f1/h2/U1/Z (CNR2X2)	0.11
11.31 r	
F10/f1/h2/cout_ha (HA_55)	0.00
11.31 r	
F10/f1/U2/Z (CIVX2)	0.08
11.40 f	
F10/f1/U1/Z (CND2IX2)	0.07
11.47 r	
F10/f1/cout_fa1 (FA_1bit_28)	0.00
11.47 r	
F10/f2/cin (FA_1bit_27)	0.00
11.47 r	
F10/f2/h2/op2_ha (HA_53)	0.00
11.47 r	
F10/f2/h2/U2/Z (CIVX2)	0.07
11.54 f	
F10/f2/h2/U1/Z (CNR2X2)	0.11
11.65 r	
F10/f2/h2/cout_ha (HA_53)	0.00
11.65 r	
F10/f2/U2/Z (CIVX2)	0.08
11.74 f	
F10/f2/U1/Z (CND2IX2)	0.07
11.81 r	
F10/f2/cout_fa1 (FA_1bit_27)	0.00
11.81 r	
F10/f3/cin (FA_1bit_26)	0.00
11.81 r	
F10/f3/h2/op2_ha (HA_51)	0.00
11.81 r	
F10/f3/h2/U2/Z (CIVX2)	0.07
11.88 f	
F10/f3/h2/U1/Z (CNR2X2)	0.11
11.99 r	
F10/f3/h2/cout_ha (HA_51)	0.00
11.99 r	
F10/f3/U2/Z (CIVX2)	0.08
12.08 f	
F10/f3/U1/Z (CND2IX2)	0.07
12.15 r	

F10/f3/cout_fa1 (FA_1bit_26)	0.00
12.15 r	
F10/f4/cin (FA_1bit_25)	0.00
12.15 r	
F10/f4/h2/op2_ha (HA_49)	0.00
12.15 r	
F10/f4/h2/U2/Z (CIVX2)	0.07
12.22 f	
F10/f4/h2/U1/Z (CNR2X2)	0.11
12.33 r	
F10/f4/h2/cout_ha (HA_49)	0.00
12.33 r	
F10/f4/U2/Z (CIVX2)	0.08
12.42 f	
F10/f4/U1/Z (CND2IX2)	0.07
12.49 r	
F10/f4/cout_fa1 (FA_1bit_25)	0.00
12.49 r	
F10/cout_fa4_2 (FA_4bit_2_7)	0.00
12.49 r	
F11/cin_fa4 (FA_4bit_2_6)	0.00
12.49 r	
F11/f1/cin (FA_1bit_24)	0.00
12.49 r	
F11/f1/h2/op2_ha (HA_47)	0.00
12.49 r	
F11/f1/h2/U2/Z (CIVX2)	0.07
12.56 f	
F11/f1/h2/U1/Z (CNR2X2)	0.11
12.67 r	
F11/f1/h2/cout_ha (HA_47)	0.00
12.67 r	
F11/f1/U2/Z (CIVX2)	0.08
12.76 f	
F11/f1/U1/Z (CND2IX2)	0.07
12.83 r	
F11/f1/cout_fa1 (FA_1bit_24)	0.00
12.83 r	
F11/f2/cin (FA_1bit_23)	0.00
12.83 r	

F11/f2/h2/op2_ha (HA_45)	0.00
12.83 r	
F11/f2/h2/U2/Z (CIVX2)	0.07
12.90 f	
F11/f2/h2/U1/Z (CNR2X2)	0.11
13.01 r	
F11/f2/h2/cout_ha (HA_45)	0.00
13.01 r	
F11/f2/U2/Z (CIVX2)	0.08
13.10 f	
F11/f2/U1/Z (CND2IX2)	0.07
13.17 r	
F11/f2/cout_fa1 (FA_1bit_23)	0.00
13.17 r	
F11/f3/cin (FA_1bit_22)	0.00
13.17 r	
F11/f3/h2/op2_ha (HA_43)	0.00
13.17 r	
F11/f3/h2/U2/Z (CIVX2)	0.07
13.24 f	
F11/f3/h2/U1/Z (CNR2X2)	0.11
13.35 r	
F11/f3/h2/cout_ha (HA_43)	0.00
13.35 r	
F11/f3/U2/Z (CIVX2)	0.08
13.44 f	
F11/f3/U1/Z (CND2IX2)	0.07
13.51 r	
F11/f3/cout_fa1 (FA_1bit_22)	0.00
13.51 r	
F11/f4/cin (FA_1bit_21)	0.00
13.51 r	
F11/f4/h2/op2_ha (HA_41)	0.00
13.51 r	
F11/f4/h2/U2/Z (CIVX2)	0.07
13.58 f	
F11/f4/h2/U1/Z (CNR2X2)	0.11
13.69 r	
F11/f4/h2/cout_ha (HA_41)	0.00
13.69 r	

F11/f4/U2/Z (CIVX2)	0.08
13.78 f	
F11/f4/U1/Z (CND2IX2)	0.07
13.85 r	
F11/f4/cout_fa1 (FA_1bit_21)	0.00
13.85 r	
F11/cout_fa4_2 (FA_4bit_2_6)	0.00
13.85 r	
F12/cin_fa4 (FA_4bit_2_5)	0.00
13.85 r	
F12/f1/cin (FA_1bit_20)	0.00
13.85 r	
F12/f1/h2/op2_ha (HA_39)	0.00
13.85 r	
F12/f1/h2/U2/Z (CIVX2)	0.07
13.92 f	
F12/f1/h2/U1/Z (CNR2X2)	0.11
14.03 r	
F12/f1/h2/cout_ha (HA_39)	0.00
14.03 r	
F12/f1/U2/Z (CIVX2)	0.08
14.12 f	
F12/f1/U1/Z (CND2IX2)	0.07
14.19 r	
F12/f1/cout_fa1 (FA_1bit_20)	0.00
14.19 r	
F12/f2/cin (FA_1bit_19)	0.00
14.19 r	
F12/f2/h2/op2_ha (HA_37)	0.00
14.19 r	
F12/f2/h2/U2/Z (CIVX2)	0.07
14.26 f	
F12/f2/h2/U1/Z (CNR2X2)	0.11
14.37 r	
F12/f2/h2/cout_ha (HA_37)	0.00
14.37 r	
F12/f2/U2/Z (CIVX2)	0.08
14.46 f	
F12/f2/U1/Z (CND2IX2)	0.07
14.53 r	

F12/f2/cout_fa1 (FA_1bit_19)	0.00
14.53 r	
F12/f3/cin (FA_1bit_18)	0.00
14.53 r	
F12/f3/h2/op2_ha (HA_35)	0.00
14.53 r	
F12/f3/h2/U2/Z (CIVX2)	0.07
14.60 f	
F12/f3/h2/U1/Z (CNR2X2)	0.11
14.71 r	
F12/f3/h2/cout_ha (HA_35)	0.00
14.71 r	
F12/f3/U2/Z (CIVX2)	0.08
14.80 f	
F12/f3/U1/Z (CND2IX2)	0.07
14.87 r	
F12/f3/cout_fa1 (FA_1bit_18)	0.00
14.87 r	
F12/f4/cin (FA_1bit_17)	0.00
14.87 r	
F12/f4/h2/op2_ha (HA_33)	0.00
14.87 r	
F12/f4/h2/U2/Z (CIVX2)	0.07
14.94 f	
F12/f4/h2/U1/Z (CNR2X2)	0.11
15.05 r	
F12/f4/h2/cout_ha (HA_33)	0.00
15.05 r	
F12/f4/U2/Z (CIVX2)	0.08
15.14 f	
F12/f4/U1/Z (CND2IX2)	0.07
15.21 r	
F12/f4/cout_fa1 (FA_1bit_17)	0.00
15.21 r	
F12/cout_fa4_2 (FA_4bit_2_5)	0.00
15.21 r	
F13/cin_fa4 (FA_4bit_2_4)	0.00
15.21 r	
F13/f1/cin (FA_1bit_16)	0.00
15.21 r	

F13/f1/h2/op2_ha (HA_31)	0.00
15.21 r	
F13/f1/h2/U2/Z (CIVX2)	0.07
15.28 f	
F13/f1/h2/U1/Z (CNR2X2)	0.11
15.39 r	
F13/f1/h2/cout_ha (HA_31)	0.00
15.39 r	
F13/f1/U2/Z (CIVX2)	0.08
15.48 f	
F13/f1/U1/Z (CND2IX2)	0.07
15.55 r	
F13/f1/cout_fa1 (FA_1bit_16)	0.00
15.55 r	
F13/f2/cin (FA_1bit_15)	0.00
15.55 r	
F13/f2/h2/op2_ha (HA_29)	0.00
15.55 r	
F13/f2/h2/U2/Z (CIVX2)	0.07
15.62 f	
F13/f2/h2/U1/Z (CNR2X2)	0.11
15.73 r	
F13/f2/h2/cout_ha (HA_29)	0.00
15.73 r	
F13/f2/U2/Z (CIVX2)	0.08
15.82 f	
F13/f2/U1/Z (CND2IX2)	0.07
15.89 r	
F13/f2/cout_fa1 (FA_1bit_15)	0.00
15.89 r	
F13/f3/cin (FA_1bit_14)	0.00
15.89 r	
F13/f3/h2/op2_ha (HA_27)	0.00
15.89 r	
F13/f3/h2/U2/Z (CIVX2)	0.07
15.96 f	
F13/f3/h2/U1/Z (CNR2X2)	0.10
16.06 r	
F13/f3/h2/cout_ha (HA_27)	0.00
16.06 r	

F13/f3/U1/Z (CNR2IX1)	0.10
16.16 f	
F13/f3/U3/Z (CIVX2)	0.09
16.24 r	
F13/f3/cout_fa1 (FA_1bit_14)	0.00
16.24 r	
F13/f4/cin (FA_1bit_13)	0.00
16.24 r	
F13/f4/h2/op2_ha (HA_25)	0.00
16.24 r	
F13/f4/h2/U1/Z (CND2IX2)	0.10
16.34 f	
F13/f4/h2/U2/Z (CIVX2)	0.06
16.40 r	
F13/f4/h2/cout_ha (HA_25)	0.00
16.40 r	
F13/f4/U2/Z (CIVX2)	0.06
16.47 f	
F13/f4/U1/Z (CND2IX2)	0.07
16.54 r	
F13/f4/cout_fa1 (FA_1bit_13)	0.00
16.54 r	
F13/cout_fa4_2 (FA_4bit_2_4)	0.00
16.54 r	
F14/cin_fa4 (FA_4bit_2_3)	0.00
16.54 r	
F14/f1/cin (FA_1bit_12)	0.00
16.54 r	
F14/f1/h2/op2_ha (HA_23)	0.00
16.54 r	
F14/f1/h2/U1/Z (CND2IX2)	0.09
16.63 f	
F14/f1/h2/U2/Z (CIVX2)	0.06
16.69 r	
F14/f1/h2/cout_ha (HA_23)	0.00
16.69 r	
F14/f1/U2/Z (CIVX2)	0.06
16.76 f	
F14/f1/U1/Z (CND2IX2)	0.09
16.84 r	

F14/f1/cout_fa1 (FA_1bit_12)	0.00
16.84 r	
F14/f2/cin (FA_1bit_11)	0.00
16.84 r	
F14/f2/h2/op2_ha (HA_21)	0.00
16.84 r	
F14/f2/h2/U1/Z (CND2X2)	0.10
16.94 f	
F14/f2/h2/U2/Z (CIVX2)	0.06
17.00 r	
F14/f2/h2/cout_ha (HA_21)	0.00
17.00 r	
F14/f2/U2/Z (CIVX2)	0.06
17.07 f	
F14/f2/U1/Z (CND2IX2)	0.07
17.14 r	
F14/f2/cout_fa1 (FA_1bit_11)	0.00
17.14 r	
F14/f3/cin (FA_1bit_10)	0.00
17.14 r	
F14/f3/h2/op2_ha (HA_19)	0.00
17.14 r	
F14/f3/h2/U1/Z (CND2X2)	0.09
17.23 f	
F14/f3/h2/U2/Z (CIVX2)	0.06
17.29 r	
F14/f3/h2/cout_ha (HA_19)	0.00
17.29 r	
F14/f3/U2/Z (CIVX2)	0.06
17.36 f	
F14/f3/U1/Z (CND2IX2)	0.07
17.43 r	
F14/f3/cout_fa1 (FA_1bit_10)	0.00
17.43 r	
F14/f4/cin (FA_1bit_9)	0.00
17.43 r	
F14/f4/h2/op2_ha (HA_17)	0.00
17.43 r	
F14/f4/h2/U1/Z (CND2X2)	0.09
17.52 f	

F14/f4/h2/U2/Z (CIVX2)	0.06
17.58 r	
F14/f4/h2/cout_ha (HA_17)	0.00
17.58 r	
F14/f4/U2/Z (CIVX2)	0.06
17.65 f	
F14/f4/U1/Z (CND2IX2)	0.07
17.72 r	
F14/f4/cout_fa1 (FA_1bit_9)	0.00
17.72 r	
F14/cout_fa4_2 (FA_4bit_2_3)	0.00
17.72 r	
F15/cin_fa4 (FA_4bit_2_2)	0.00
17.72 r	
F15/f1/cin (FA_1bit_8)	0.00
17.72 r	
F15/f1/h2/op2_ha (HA_15)	0.00
17.72 r	
F15/f1/h2/U1/Z (CND2X2)	0.09
17.81 f	
F15/f1/h2/U2/Z (CIVX2)	0.06
17.87 r	
F15/f1/h2/cout_ha (HA_15)	0.00
17.87 r	
F15/f1/U2/Z (CIVX2)	0.06
17.94 f	
F15/f1/U1/Z (CND2IX2)	0.07
18.01 r	
F15/f1/cout_fa1 (FA_1bit_8)	0.00
18.01 r	
F15/f2/cin (FA_1bit_7)	0.00
18.01 r	
F15/f2/h2/op2_ha (HA_13)	0.00
18.01 r	
F15/f2/h2/U1/Z (CND2X2)	0.09
18.10 f	
F15/f2/h2/U2/Z (CIVX2)	0.06
18.16 r	
F15/f2/h2/cout_ha (HA_13)	0.00
18.16 r	

F15/f2/U2/Z (CIVX2)	0.06
18.23 f	
F15/f2/U1/Z (CND2IX2)	0.07
18.30 r	
F15/f2/cout_fa1 (FA_1bit_7)	0.00
18.30 r	
F15/f3/cin (FA_1bit_6)	0.00
18.30 r	
F15/f3/h2/op2_ha (HA_11)	0.00
18.30 r	
F15/f3/h2/U1/Z (CND2X2)	0.09
18.39 f	
F15/f3/h2/U2/Z (CIVX2)	0.06
18.45 r	
F15/f3/h2/cout_ha (HA_11)	0.00
18.45 r	
F15/f3/U2/Z (CIVX2)	0.06
18.52 f	
F15/f3/U1/Z (CND2IX2)	0.07
18.59 r	
F15/f3/cout_fa1 (FA_1bit_6)	0.00
18.59 r	
F15/f4/cin (FA_1bit_5)	0.00
18.59 r	
F15/f4/h2/op2_ha (HA_9)	0.00
18.59 r	
F15/f4/h2/U2/Z (CIVX2)	0.07
18.66 f	
F15/f4/h2/U1/Z (CNR2X2)	0.10
18.76 r	
F15/f4/h2/cout_ha (HA_9)	0.00
18.76 r	
F15/f4/U2/Z (CIVX1)	0.10
18.85 f	
F15/f4/U1/Z (CND2IX2)	0.08
18.93 r	
F15/f4/cout_fa1 (FA_1bit_5)	0.00
18.93 r	
F15/cout_fa4_2 (FA_4bit_2_2)	0.00
18.93 r	

F16/cin_fa4 (FA_4bit_2_1)	0.00
18.93 r	
F16/f1/cin (FA_1bit_4)	0.00
18.93 r	
F16/f1/h2/op2_ha (HA_7)	0.00
18.93 r	
F16/f1/h2/U1/Z (CND2X2)	0.09
19.02 f	
F16/f1/h2/U2/Z (CIVX2)	0.06
19.08 r	
F16/f1/h2/cout_ha (HA_7)	0.00
19.08 r	
F16/f1/U2/Z (CIVX2)	0.06
19.15 f	
F16/f1/U1/Z (CND2IX2)	0.07
19.22 r	
F16/f1/cout_fa1 (FA_1bit_4)	0.00
19.22 r	
F16/f2/cin (FA_1bit_3)	0.00
19.22 r	
F16/f2/h2/op2_ha (HA_5)	0.00
19.22 r	
F16/f2/h2/U2/Z (CIVX2)	0.07
19.29 f	
F16/f2/h2/U1/Z (CNR2X2)	0.10
19.39 r	
F16/f2/h2/cout_ha (HA_5)	0.00
19.39 r	
F16/f2/U1/Z (CNR2IX1)	0.10
19.49 f	
F16/f2/U3/Z (CIVX2)	0.06
19.55 r	
F16/f2/cout_fa1 (FA_1bit_3)	0.00
19.55 r	
F16/f3/cin (FA_1bit_2)	0.00
19.55 r	
F16/f3/h2/op2_ha (HA_3)	0.00
19.55 r	
F16/f3/h2/U3/Z (CIVX2)	0.07
19.62 f	

F16/f3/h2/U4/Z (CIVXL)	0.10
19.73 r	
F16/f3/h2/U5/Z (CEOXL)	0.30
20.02 r	
F16/f3/h2/sum_ha (HA_3)	0.00
20.02 r	
F16/f3/sum_fa1 (FA_1bit_2)	0.00
20.02 r	
F16/sum_fa4_2[2] (FA_4bit_2_1)	0.00
20.02 r	
sum_reg[62]/D (CFD2QXL)	0.00
20.02 r	
data arrival	time
20.02	
 clock clock (rise edge)	20.80
20.80	
clock network delay (propagated)	0.00
20.80	
clock uncertainty	-0.25
20.55	
sum_reg[62]/CP (CFD2QXL)	0.00
20.55 r	
library setup time	-0.38
20.17	
data required	time
20.17	

data required	time
20.17	
data arrival time	-
20.02	

slack	(MET)
0.14	

Startpoint: op2f_reg[1]

(rising edge-triggered flip-flop clocked by clock)
 Endpoint: sum_reg[59]
 (rising edge-triggered flip-flop clocked by clock)
 Path Group: clock
 Path Type: max

Point	Incr
Path	
clock clock (rise edge)	0.00
0.00	
clock network delay (propagated)	0.00
0.00	
op2f_reg[1]/CP (CFD2QX2)	0.00
0.00 r	
op2f_reg[1]/Q (CFD2QX2)	0.50
0.50 f	
F1/op2_fa4[1] (FA_4bit_1)	0.00
0.50 f	
F1/f1/op2_fa1 (FA_1bit_0)	0.00
0.50 f	
F1/f1/h1/op2_ha (HA_126)	0.00
0.50 f	
F1/f1/h1/U2/Z (CIVX2)	0.08
0.58 r	
F1/f1/h1/U4/Z (CND2X2)	0.09
0.67 f	
F1/f1/h1/U5/Z (CND2X2)	0.09
0.76 r	
F1/f1/h1/sum_ha (HA_126)	0.00
0.76 r	
F1/f1/h2/op1_ha (HA_125)	0.00
0.76 r	
F1/f1/h2/U1/Z (CND2X2)	0.09
0.85 f	
F1/f1/h2/U2/Z (CIVX2)	0.06
0.91 r	

F1/f1/h2/cout_ha (HA_125)	0.00
0.91 r	
F1/f1/U2/Z (CIVX2)	0.06
0.98 f	
F1/f1/U1/Z (CND2IX2)	0.07
1.05 r	
F1/f1/cout_fa1 (FA_1bit_0)	0.00
1.05 r	
F1/f2/cin (FA_1bit_62)	0.00
1.05 r	
F1/f2/h2/op2_ha (HA_123)	0.00
1.05 r	
F1/f2/h2/U1/Z (CND2X2)	0.09
1.14 f	
F1/f2/h2/U2/Z (CIVX2)	0.06
1.20 r	
F1/f2/h2/cout_ha (HA_123)	0.00
1.20 r	
F1/f2/U2/Z (CIVX2)	0.06
1.27 f	
F1/f2/U1/Z (CND2IX2)	0.07
1.34 r	
F1/f2/cout_fa1 (FA_1bit_62)	0.00
1.34 r	
F1/f3/cin (FA_1bit_61)	0.00
1.34 r	
F1/f3/h2/op2_ha (HA_121)	0.00
1.34 r	
F1/f3/h2/U1/Z (CND2X2)	0.09
1.43 f	
F1/f3/h2/U2/Z (CIVX2)	0.06
1.49 r	
F1/f3/h2/cout_ha (HA_121)	0.00
1.49 r	
F1/f3/U1/Z (CNR2IX2)	0.07
1.56 f	
F1/f3/U2/Z (CIVX2)	0.07
1.63 r	
F1/f3/cout_fa1 (FA_1bit_61)	0.00
1.63 r	

F1/cout_fa4 (FA_4bit_1)	0.00
1.63 r	
F2/cin_fa4 (FA_4bit_2_0)	0.00
1.63 r	
F2/f1/cin (FA_1bit_60)	0.00
1.63 r	
F2/f1/h2/op2_ha (HA_119)	0.00
1.63 r	
F2/f1/h2/U1/Z (CND2X2)	0.09
1.72 f	
F2/f1/h2/U2/Z (CIVX2)	0.06
1.78 r	
F2/f1/h2/cout_ha (HA_119)	0.00
1.78 r	
F2/f1/U1/Z (CNR2IX2)	0.07
1.85 f	
F2/f1/U2/Z (CIVX2)	0.07
1.91 r	
F2/f1/cout_fa1 (FA_1bit_60)	0.00
1.91 r	
F2/f2/cin (FA_1bit_59)	0.00
1.91 r	
F2/f2/h2/op2_ha (HA_117)	0.00
1.91 r	
F2/f2/h2/U1/Z (CND2X2)	0.09
2.00 f	
F2/f2/h2/U2/Z (CIVX2)	0.06
2.07 r	
F2/f2/h2/cout_ha (HA_117)	0.00
2.07 r	
F2/f2/U1/Z (CNR2IX2)	0.07
2.13 f	
F2/f2/U2/Z (CIVX2)	0.07
2.20 r	
F2/f2/cout_fa1 (FA_1bit_59)	0.00
2.20 r	
F2/f3/cin (FA_1bit_58)	0.00
2.20 r	
F2/f3/h2/op2_ha (HA_115)	0.00
2.20 r	

F2/f3/h2/U1/Z (CND2X2)	0.09
2.29 f	
F2/f3/h2/U2/Z (CIVX2)	0.06
2.35 r	
F2/f3/h2/cout_ha (HA_115)	0.00
2.35 r	
F2/f3/U1/Z (CNR2IX2)	0.07
2.42 f	
F2/f3/U3/Z (CIVX2)	0.07
2.49 r	
F2/f3/cout_fa1 (FA_1bit_58)	0.00
2.49 r	
F2/f4/cin (FA_1bit_57)	0.00
2.49 r	
F2/f4/h2/op2_ha (HA_113)	0.00
2.49 r	
F2/f4/h2/U2/Z (CND2X2)	0.09
2.58 f	
F2/f4/h2/U3/Z (CIVX2)	0.06
2.64 r	
F2/f4/h2/cout_ha (HA_113)	0.00
2.64 r	
F2/f4/U1/Z (CNR2IX2)	0.07
2.71 f	
F2/f4/U2/Z (CIVX2)	0.07
2.77 r	
F2/f4/cout_fa1 (FA_1bit_57)	0.00
2.77 r	
F2/cout_fa4_2 (FA_4bit_2_0)	0.00
2.77 r	
F3/cin_fa4 (FA_4bit_2_14)	0.00
2.77 r	
F3/f1/cin (FA_1bit_56)	0.00
2.77 r	
F3/f1/h2/op2_ha (HA_111)	0.00
2.77 r	
F3/f1/h2/U1/Z (CND2X2)	0.09
2.86 f	
F3/f1/h2/U2/Z (CIVX2)	0.06
2.93 r	

F3/f1/h2/cout_ha (HA_111)	0.00
2.93 r	
F3/f1/U1/Z (CNR2IX2)	0.07
2.99 f	
F3/f1/U2/Z (CIVX2)	0.07
3.06 r	
F3/f1/cout_fa1 (FA_1bit_56)	0.00
3.06 r	
F3/f2/cin (FA_1bit_55)	0.00
3.06 r	
F3/f2/h2/op2_ha (HA_109)	0.00
3.06 r	
F3/f2/h2/U1/Z (CND2X2)	0.09
3.15 f	
F3/f2/h2/U2/Z (CIVX2)	0.06
3.21 r	
F3/f2/h2/cout_ha (HA_109)	0.00
3.21 r	
F3/f2/U2/Z (CIVX2)	0.06
3.27 f	
F3/f2/U1/Z (CND2IX2)	0.07
3.35 r	
F3/f2/cout_fa1 (FA_1bit_55)	0.00
3.35 r	
F3/f3/cin (FA_1bit_54)	0.00
3.35 r	
F3/f3/h2/op2_ha (HA_107)	0.00
3.35 r	
F3/f3/h2/U1/Z (CND2X2)	0.09
3.44 f	
F3/f3/h2/U2/Z (CIVX2)	0.06
3.50 r	
F3/f3/h2/cout_ha (HA_107)	0.00
3.50 r	
F3/f3/U1/Z (CNR2IX2)	0.07
3.57 f	
F3/f3/U2/Z (CIVX2)	0.07
3.64 r	
F3/f3/cout_fa1 (FA_1bit_54)	0.00
3.64 r	

F3/f4/cin (FA_1bit_53)	0.00
3.64 r	
F3/f4/h2/op2_ha (HA_105)	0.00
3.64 r	
F3/f4/h2/U1/Z (CND2X2)	0.09
3.72 f	
F3/f4/h2/U2/Z (CIVX2)	0.06
3.79 r	
F3/f4/h2/cout_ha (HA_105)	0.00
3.79 r	
F3/f4/U1/Z (CNR2IX2)	0.07
3.85 f	
F3/f4/U2/Z (CIVX2)	0.07
3.92 r	
F3/f4/cout_fa1 (FA_1bit_53)	0.00
3.92 r	
F3/cout_fa4_2 (FA_4bit_2_14)	0.00
3.92 r	
F4/cin_fa4 (FA_4bit_2_13)	0.00
3.92 r	
F4/f1/cin (FA_1bit_52)	0.00
3.92 r	
F4/f1/h2/op2_ha (HA_103)	0.00
3.92 r	
F4/f1/h2/U1/Z (CND2X2)	0.09
4.01 f	
F4/f1/h2/U2/Z (CIVX2)	0.06
4.07 r	
F4/f1/h2/cout_ha (HA_103)	0.00
4.07 r	
F4/f1/U1/Z (CNR2IX2)	0.07
4.14 f	
F4/f1/U3/Z (CIVX2)	0.07
4.21 r	
F4/f1/cout_fa1 (FA_1bit_52)	0.00
4.21 r	
F4/f2/cin (FA_1bit_51)	0.00
4.21 r	
F4/f2/h2/op2_ha (HA_101)	0.00
4.21 r	

F4/f2/h2/U1/Z (CND2X2)	0.09
4.30 f	
F4/f2/h2/U2/Z (CIVX2)	0.06
4.36 r	
F4/f2/h2/cout_ha (HA_101)	0.00
4.36 r	
F4/f2/U1/Z (CNR2IX2)	0.07
4.43 f	
F4/f2/U2/Z (CIVX2)	0.07
4.49 r	
F4/f2/cout_fa1 (FA_1bit_51)	0.00
4.49 r	
F4/f3/cin (FA_1bit_50)	0.00
4.49 r	
F4/f3/h2/op2_ha (HA_99)	0.00
4.49 r	
F4/f3/h2/U1/Z (CND2X2)	0.09
4.58 f	
F4/f3/h2/U2/Z (CIVX2)	0.06
4.65 r	
F4/f3/h2/cout_ha (HA_99)	0.00
4.65 r	
F4/f3/U1/Z (CNR2IX2)	0.07
4.71 f	
F4/f3/U2/Z (CIVX2)	0.07
4.78 r	
F4/f3/cout_fa1 (FA_1bit_50)	0.00
4.78 r	
F4/f4/cin (FA_1bit_49)	0.00
4.78 r	
F4/f4/h2/op2_ha (HA_97)	0.00
4.78 r	
F4/f4/h2/U1/Z (CND2X2)	0.09
4.87 f	
F4/f4/h2/U2/Z (CIVX2)	0.06
4.93 r	
F4/f4/h2/cout_ha (HA_97)	0.00
4.93 r	
F4/f4/U1/Z (CNR2IX2)	0.07
5.00 f	

F4/f4/U2/Z (CIVX2)	0.07
5.07 r	
F4/f4/cout_fa1 (FA_1bit_49)	0.00
5.07 r	
F4/cout_fa4_2 (FA_4bit_2_13)	0.00
5.07 r	
F5/cin_fa4 (FA_4bit_2_12)	0.00
5.07 r	
F5/f1/cin (FA_1bit_48)	0.00
5.07 r	
F5/f1/h2/op2_ha (HA_95)	0.00
5.07 r	
F5/f1/h2/U1/Z (CND2X2)	0.09
5.16 f	
F5/f1/h2/U2/Z (CIVX2)	0.06
5.22 r	
F5/f1/h2/cout_ha (HA_95)	0.00
5.22 r	
F5/f1/U2/Z (CIVX2)	0.06
5.28 f	
F5/f1/U1/Z (CND2IX2)	0.07
5.35 r	
F5/f1/cout_fa1 (FA_1bit_48)	0.00
5.35 r	
F5/f2/cin (FA_1bit_47)	0.00
5.35 r	
F5/f2/h2/op2_ha (HA_93)	0.00
5.35 r	
F5/f2/h2/U1/Z (CND2X2)	0.09
5.45 f	
F5/f2/h2/U2/Z (CIVX2)	0.06
5.51 r	
F5/f2/h2/cout_ha (HA_93)	0.00
5.51 r	
F5/f2/U1/Z (CNR2IX2)	0.07
5.58 f	
F5/f2/U2/Z (CIVX2)	0.07
5.64 r	
F5/f2/cout_fa1 (FA_1bit_47)	0.00
5.64 r	

F5/f3/cin (FA_1bit_46)	0.00
5.64 r	
F5/f3/h2/op2_ha (HA_91)	0.00
5.64 r	
F5/f3/h2/U1/Z (CND2X2)	0.09
5.73 f	
F5/f3/h2/U2/Z (CIVX2)	0.06
5.79 r	
F5/f3/h2/cout_ha (HA_91)	0.00
5.79 r	
F5/f3/U1/Z (CNR2IX2)	0.07
5.86 f	
F5/f3/U2/Z (CIVX2)	0.07
5.93 r	
F5/f3/cout_fa1 (FA_1bit_46)	0.00
5.93 r	
F5/f4/cin (FA_1bit_45)	0.00
5.93 r	
F5/f4/h2/op2_ha (HA_89)	0.00
5.93 r	
F5/f4/h2/U1/Z (CND2X2)	0.09
6.02 f	
F5/f4/h2/U2/Z (CIVX2)	0.06
6.08 r	
F5/f4/h2/cout_ha (HA_89)	0.00
6.08 r	
F5/f4/U2/Z (CIVX2)	0.06
6.14 f	
F5/f4/U1/Z (CND2IX2)	0.07
6.22 r	
F5/f4/cout_fa1 (FA_1bit_45)	0.00
6.22 r	
F5/cout_fa4_2 (FA_4bit_2_12)	0.00
6.22 r	
F6/cin_fa4 (FA_4bit_2_11)	0.00
6.22 r	
F6/f1/cin (FA_1bit_44)	0.00
6.22 r	
F6/f1/h2/op2_ha (HA_87)	0.00
6.22 r	

F6/f1/h2/U1/Z (CND2X2)	0.09
6.31 f	
F6/f1/h2/U2/Z (CIVX2)	0.06
6.37 r	
F6/f1/h2/cout_ha (HA_87)	0.00
6.37 r	
F6/f1/U1/Z (CNR2IX2)	0.07
6.44 f	
F6/f1/U2/Z (CIVX2)	0.07
6.50 r	
F6/f1/cout_fa1 (FA_1bit_44)	0.00
6.50 r	
F6/f2/cin (FA_1bit_43)	0.00
6.50 r	
F6/f2/h2/op2_ha (HA_85)	0.00
6.50 r	
F6/f2/h2/U1/Z (CND2X2)	0.09
6.59 f	
F6/f2/h2/U2/Z (CIVX2)	0.06
6.66 r	
F6/f2/h2/cout_ha (HA_85)	0.00
6.66 r	
F6/f2/U1/Z (CNR2IX2)	0.07
6.72 f	
F6/f2/U2/Z (CIVX2)	0.07
6.79 r	
F6/f2/cout_fa1 (FA_1bit_43)	0.00
6.79 r	
F6/f3/cin (FA_1bit_42)	0.00
6.79 r	
F6/f3/h2/op2_ha (HA_83)	0.00
6.79 r	
F6/f3/h2/U1/Z (CND2X2)	0.09
6.88 f	
F6/f3/h2/U2/Z (CIVX2)	0.06
6.94 r	
F6/f3/h2/cout_ha (HA_83)	0.00
6.94 r	
F6/f3/U1/Z (CNR2IX2)	0.07
7.01 f	

F6/f3/U3/Z (CIVX2)	0.07
7.08 r	
F6/f3/cout_fa1 (FA_1bit_42)	0.00
7.08 r	
F6/f4/cin (FA_1bit_41)	0.00
7.08 r	
F6/f4/h2/op2_ha (HA_81)	0.00
7.08 r	
F6/f4/h2/U1/Z (CND2X2)	0.09
7.17 f	
F6/f4/h2/U2/Z (CIVX2)	0.06
7.23 r	
F6/f4/h2/cout_ha (HA_81)	0.00
7.23 r	
F6/f4/U1/Z (CNR2IX2)	0.07
7.30 f	
F6/f4/U2/Z (CIVX2)	0.07
7.36 r	
F6/f4/cout_fa1 (FA_1bit_41)	0.00
7.36 r	
F6/cout_fa4_2 (FA_4bit_2_11)	0.00
7.36 r	
F7/cin_fa4 (FA_4bit_2_10)	0.00
7.36 r	
F7/f1/cin (FA_1bit_40)	0.00
7.36 r	
F7/f1/h2/op2_ha (HA_79)	0.00
7.36 r	
F7/f1/h2/U1/Z (CND2X2)	0.09
7.45 f	
F7/f1/h2/U2/Z (CIVX2)	0.06
7.52 r	
F7/f1/h2/cout_ha (HA_79)	0.00
7.52 r	
F7/f1/U1/Z (CNR2IX2)	0.07
7.58 f	
F7/f1/U2/Z (CIVX2)	0.07
7.65 r	
F7/f1/cout_fa1 (FA_1bit_40)	0.00
7.65 r	

F7/f2/cin (FA_1bit_39)	0.00
7.65 r	
F7/f2/h2/op2_ha (HA_77)	0.00
7.65 r	
F7/f2/h2/U1/Z (CND2X2)	0.09
7.74 f	
F7/f2/h2/U2/Z (CIVX2)	0.06
7.80 r	
F7/f2/h2/cout_ha (HA_77)	0.00
7.80 r	
F7/f2/U1/Z (CNR2IX2)	0.07
7.87 f	
F7/f2/U3/Z (CIVX2)	0.07
7.94 r	
F7/f2/cout_fa1 (FA_1bit_39)	0.00
7.94 r	
F7/f3/cin (FA_1bit_38)	0.00
7.94 r	
F7/f3/h2/op2_ha (HA_75)	0.00
7.94 r	
F7/f3/h2/U1/Z (CND2X2)	0.09
8.02 f	
F7/f3/h2/U2/Z (CIVX2)	0.06
8.09 r	
F7/f3/h2/cout_ha (HA_75)	0.00
8.09 r	
F7/f3/U2/Z (CIVX2)	0.06
8.15 f	
F7/f3/U1/Z (CND2IX2)	0.07
8.22 r	
F7/f3/cout_fa1 (FA_1bit_38)	0.00
8.22 r	
F7/f4/cin (FA_1bit_37)	0.00
8.22 r	
F7/f4/h2/op2_ha (HA_73)	0.00
8.22 r	
F7/f4/h2/U1/Z (CND2X2)	0.09
8.31 f	
F7/f4/h2/U2/Z (CIVX2)	0.06
8.38 r	

F7/f4/h2/cout_ha (HA_73)	0.00
8.38 r	
F7/f4/U1/Z (CNR2IX2)	0.07
8.44 f	
F7/f4/U3/Z (CIVX2)	0.07
8.51 r	
F7/f4/cout_fa1 (FA_1bit_37)	0.00
8.51 r	
F7/cout_fa4_2 (FA_4bit_2_10)	0.00
8.51 r	
F8/cin_fa4 (FA_4bit_2_9)	0.00
8.51 r	
F8/f1/cin (FA_1bit_36)	0.00
8.51 r	
F8/f1/h2/op2_ha (HA_71)	0.00
8.51 r	
F8/f1/h2/U1/Z (CND2X2)	0.09
8.60 f	
F8/f1/h2/U2/Z (CIVX2)	0.06
8.66 r	
F8/f1/h2/cout_ha (HA_71)	0.00
8.66 r	
F8/f1/U2/Z (CIVX2)	0.06
8.73 f	
F8/f1/U1/Z (CND2IX2)	0.07
8.80 r	
F8/f1/cout_fa1 (FA_1bit_36)	0.00
8.80 r	
F8/f2/cin (FA_1bit_35)	0.00
8.80 r	
F8/f2/h2/op2_ha (HA_69)	0.00
8.80 r	
F8/f2/h2/U1/Z (CND2X2)	0.09
8.89 f	
F8/f2/h2/U2/Z (CIVX2)	0.06
8.95 r	
F8/f2/h2/cout_ha (HA_69)	0.00
8.95 r	
F8/f2/U2/Z (CIVX2)	0.06
9.02 f	

F8/f2/U1/Z (CND2IX2)	0.07
9.09 r	
F8/f2/cout_fa1 (FA_1bit_35)	0.00
9.09 r	
F8/f3/cin (FA_1bit_34)	0.00
9.09 r	
F8/f3/h2/op2_ha (HA_67)	0.00
9.09 r	
F8/f3/h2/U2/Z (CIVX2)	0.07
9.16 f	
F8/f3/h2/U1/Z (CNR2X2)	0.11
9.27 r	
F8/f3/h2/cout_ha (HA_67)	0.00
9.27 r	
F8/f3/U2/Z (CIVX2)	0.08
9.36 f	
F8/f3/U1/Z (CND2IX2)	0.07
9.43 r	
F8/f3/cout_fa1 (FA_1bit_34)	0.00
9.43 r	
F8/f4/cin (FA_1bit_33)	0.00
9.43 r	
F8/f4/h2/op2_ha (HA_65)	0.00
9.43 r	
F8/f4/h2/U2/Z (CIVX2)	0.07
9.50 f	
F8/f4/h2/U1/Z (CNR2X2)	0.11
9.61 r	
F8/f4/h2/cout_ha (HA_65)	0.00
9.61 r	
F8/f4/U2/Z (CIVX2)	0.08
9.70 f	
F8/f4/U1/Z (CND2IX2)	0.07
9.77 r	
F8/f4/cout_fa1 (FA_1bit_33)	0.00
9.77 r	
F8/cout_fa4_2 (FA_4bit_2_9)	0.00
9.77 r	
F9/cin_fa4 (FA_4bit_2_8)	0.00
9.77 r	

F9/f1/cin (FA_1bit_32)	0.00
9.77 r	
F9/f1/h2/op2_ha (HA_63)	0.00
9.77 r	
F9/f1/h2/U2/Z (CIVX2)	0.07
9.84 f	
F9/f1/h2/U1/Z (CNR2X2)	0.11
9.95 r	
F9/f1/h2/cout_ha (HA_63)	0.00
9.95 r	
F9/f1/U2/Z (CIVX2)	0.08
10.04 f	
F9/f1/U1/Z (CND2IX2)	0.07
10.11 r	
F9/f1/cout_fa1 (FA_1bit_32)	0.00
10.11 r	
F9/f2/cin (FA_1bit_31)	0.00
10.11 r	
F9/f2/h2/op2_ha (HA_61)	0.00
10.11 r	
F9/f2/h2/U2/Z (CIVX2)	0.07
10.18 f	
F9/f2/h2/U1/Z (CNR2X2)	0.11
10.29 r	
F9/f2/h2/cout_ha (HA_61)	0.00
10.29 r	
F9/f2/U2/Z (CIVX2)	0.08
10.38 f	
F9/f2/U1/Z (CND2IX2)	0.07
10.45 r	
F9/f2/cout_fa1 (FA_1bit_31)	0.00
10.45 r	
F9/f3/cin (FA_1bit_30)	0.00
10.45 r	
F9/f3/h2/op2_ha (HA_59)	0.00
10.45 r	
F9/f3/h2/U2/Z (CIVX2)	0.07
10.52 f	
F9/f3/h2/U1/Z (CNR2X2)	0.11
10.63 r	

F9/f3/h2/cout_ha (HA_59)	0.00
10.63 r	
F9/f3/U2/Z (CIVX2)	0.08
10.72 f	
F9/f3/U1/Z (CND2IX2)	0.07
10.79 r	
F9/f3/cout_fa1 (FA_1bit_30)	0.00
10.79 r	
F9/f4/cin (FA_1bit_29)	0.00
10.79 r	
F9/f4/h2/op2_ha (HA_57)	0.00
10.79 r	
F9/f4/h2/U2/Z (CIVX2)	0.07
10.86 f	
F9/f4/h2/U1/Z (CNR2X2)	0.11
10.97 r	
F9/f4/h2/cout_ha (HA_57)	0.00
10.97 r	
F9/f4/U2/Z (CIVX2)	0.08
11.06 f	
F9/f4/U1/Z (CND2IX2)	0.07
11.13 r	
F9/f4/cout_fa1 (FA_1bit_29)	0.00
11.13 r	
F9/cout_fa4_2 (FA_4bit_2_8)	0.00
11.13 r	
F10/cin_fa4 (FA_4bit_2_7)	0.00
11.13 r	
F10/f1/cin (FA_1bit_28)	0.00
11.13 r	
F10/f1/h2/op2_ha (HA_55)	0.00
11.13 r	
F10/f1/h2/U2/Z (CIVX2)	0.07
11.20 f	
F10/f1/h2/U1/Z (CNR2X2)	0.11
11.31 r	
F10/f1/h2/cout_ha (HA_55)	0.00
11.31 r	
F10/f1/U2/Z (CIVX2)	0.08
11.40 f	

F10/f1/U1/Z (CND2IX2)	0.07
11.47 r	
F10/f1/cout_fa1 (FA_1bit_28)	0.00
11.47 r	
F10/f2/cin (FA_1bit_27)	0.00
11.47 r	
F10/f2/h2/op2_ha (HA_53)	0.00
11.47 r	
F10/f2/h2/U2/Z (CIVX2)	0.07
11.54 f	
F10/f2/h2/U1/Z (CNR2X2)	0.11
11.65 r	
F10/f2/h2/cout_ha (HA_53)	0.00
11.65 r	
F10/f2/U2/Z (CIVX2)	0.08
11.74 f	
F10/f2/U1/Z (CND2IX2)	0.07
11.81 r	
F10/f2/cout_fa1 (FA_1bit_27)	0.00
11.81 r	
F10/f3/cin (FA_1bit_26)	0.00
11.81 r	
F10/f3/h2/op2_ha (HA_51)	0.00
11.81 r	
F10/f3/h2/U2/Z (CIVX2)	0.07
11.88 f	
F10/f3/h2/U1/Z (CNR2X2)	0.11
11.99 r	
F10/f3/h2/cout_ha (HA_51)	0.00
11.99 r	
F10/f3/U2/Z (CIVX2)	0.08
12.08 f	
F10/f3/U1/Z (CND2IX2)	0.07
12.15 r	
F10/f3/cout_fa1 (FA_1bit_26)	0.00
12.15 r	
F10/f4/cin (FA_1bit_25)	0.00
12.15 r	
F10/f4/h2/op2_ha (HA_49)	0.00
12.15 r	

F10/f4/h2/U2/Z (CIVX2)	0.07
12.22 f	
F10/f4/h2/U1/Z (CNR2X2)	0.11
12.33 r	
F10/f4/h2/cout_ha (HA_49)	0.00
12.33 r	
F10/f4/U2/Z (CIVX2)	0.08
12.42 f	
F10/f4/U1/Z (CND2IX2)	0.07
12.49 r	
F10/cout_fa1 (FA_1bit_25)	0.00
12.49 r	
F10/cout_fa4_2 (FA_4bit_2_7)	0.00
12.49 r	
F11/cin_fa4 (FA_4bit_2_6)	0.00
12.49 r	
F11/f1/cin (FA_1bit_24)	0.00
12.49 r	
F11/f1/h2/op2_ha (HA_47)	0.00
12.49 r	
F11/f1/h2/U2/Z (CIVX2)	0.07
12.56 f	
F11/f1/h2/U1/Z (CNR2X2)	0.11
12.67 r	
F11/f1/h2/cout_ha (HA_47)	0.00
12.67 r	
F11/f1/U2/Z (CIVX2)	0.08
12.76 f	
F11/f1/U1/Z (CND2IX2)	0.07
12.83 r	
F11/f1/cout_fa1 (FA_1bit_24)	0.00
12.83 r	
F11/f2/cin (FA_1bit_23)	0.00
12.83 r	
F11/f2/h2/op2_ha (HA_45)	0.00
12.83 r	
F11/f2/h2/U2/Z (CIVX2)	0.07
12.90 f	
F11/f2/h2/U1/Z (CNR2X2)	0.11
13.01 r	

F11/f2/h2/cout_ha (HA_45)	0.00
13.01 r	
F11/f2/U2/Z (CIVX2)	0.08
13.10 f	
F11/f2/U1/Z (CND2IX2)	0.07
13.17 r	
F11/f2/cout_fa1 (FA_1bit_23)	0.00
13.17 r	
F11/f3/cin (FA_1bit_22)	0.00
13.17 r	
F11/f3/h2/op2_ha (HA_43)	0.00
13.17 r	
F11/f3/h2/U2/Z (CIVX2)	0.07
13.24 f	
F11/f3/h2/U1/Z (CNR2X2)	0.11
13.35 r	
F11/f3/h2/cout_ha (HA_43)	0.00
13.35 r	
F11/f3/U2/Z (CIVX2)	0.08
13.44 f	
F11/f3/U1/Z (CND2IX2)	0.07
13.51 r	
F11/f3/cout_fa1 (FA_1bit_22)	0.00
13.51 r	
F11/f4/cin (FA_1bit_21)	0.00
13.51 r	
F11/f4/h2/op2_ha (HA_41)	0.00
13.51 r	
F11/f4/h2/U2/Z (CIVX2)	0.07
13.58 f	
F11/f4/h2/U1/Z (CNR2X2)	0.11
13.69 r	
F11/f4/h2/cout_ha (HA_41)	0.00
13.69 r	
F11/f4/U2/Z (CIVX2)	0.08
13.78 f	
F11/f4/U1/Z (CND2IX2)	0.07
13.85 r	
F11/f4/cout_fa1 (FA_1bit_21)	0.00
13.85 r	

F11/cout_fa4_2 (FA_4bit_2_6)	0.00
13.85 r	
F12/cin_fa4 (FA_4bit_2_5)	0.00
13.85 r	
F12/f1/cin (FA_1bit_20)	0.00
13.85 r	
F12/f1/h2/op2_ha (HA_39)	0.00
13.85 r	
F12/f1/h2/U2/Z (CIVX2)	0.07
13.92 f	
F12/f1/h2/U1/Z (CNR2X2)	0.11
14.03 r	
F12/f1/h2/cout_ha (HA_39)	0.00
14.03 r	
F12/f1/U2/Z (CIVX2)	0.08
14.12 f	
F12/f1/U1/Z (CND2IX2)	0.07
14.19 r	
F12/f1/cout_fa1 (FA_1bit_20)	0.00
14.19 r	
F12/f2/cin (FA_1bit_19)	0.00
14.19 r	
F12/f2/h2/op2_ha (HA_37)	0.00
14.19 r	
F12/f2/h2/U2/Z (CIVX2)	0.07
14.26 f	
F12/f2/h2/U1/Z (CNR2X2)	0.11
14.37 r	
F12/f2/h2/cout_ha (HA_37)	0.00
14.37 r	
F12/f2/U2/Z (CIVX2)	0.08
14.46 f	
F12/f2/U1/Z (CND2IX2)	0.07
14.53 r	
F12/f2/cout_fa1 (FA_1bit_19)	0.00
14.53 r	
F12/f3/cin (FA_1bit_18)	0.00
14.53 r	
F12/f3/h2/op2_ha (HA_35)	0.00
14.53 r	

F12/f3/h2/U2/Z (CIVX2)	0.07
14.60 f	
F12/f3/h2/U1/Z (CNR2X2)	0.11
14.71 r	
F12/f3/h2/cout_ha (HA_35)	0.00
14.71 r	
F12/f3/U2/Z (CIVX2)	0.08
14.80 f	
F12/f3/U1/Z (CND2IX2)	0.07
14.87 r	
F12/f3/cout_fa1 (FA_1bit_18)	0.00
14.87 r	
F12/f4/cin (FA_1bit_17)	0.00
14.87 r	
F12/f4/h2/op2_ha (HA_33)	0.00
14.87 r	
F12/f4/h2/U2/Z (CIVX2)	0.07
14.94 f	
F12/f4/h2/U1/Z (CNR2X2)	0.11
15.05 r	
F12/f4/h2/cout_ha (HA_33)	0.00
15.05 r	
F12/f4/U2/Z (CIVX2)	0.08
15.14 f	
F12/f4/U1/Z (CND2IX2)	0.07
15.21 r	
F12/f4/cout_fa1 (FA_1bit_17)	0.00
15.21 r	
F12/cout_fa4_2 (FA_4bit_2_5)	0.00
15.21 r	
F13/cin_fa4 (FA_4bit_2_4)	0.00
15.21 r	
F13/f1/cin (FA_1bit_16)	0.00
15.21 r	
F13/f1/h2/op2_ha (HA_31)	0.00
15.21 r	
F13/f1/h2/U2/Z (CIVX2)	0.07
15.28 f	
F13/f1/h2/U1/Z (CNR2X2)	0.11
15.39 r	

F13/f1/h2/cout_ha (HA_31)	0.00
15.39 r	
F13/f1/U2/Z (CIVX2)	0.08
15.48 f	
F13/f1/U1/Z (CND2IX2)	0.07
15.55 r	
F13/f1/cout_fa1 (FA_1bit_16)	0.00
15.55 r	
F13/f2/cin (FA_1bit_15)	0.00
15.55 r	
F13/f2/h2/op2_ha (HA_29)	0.00
15.55 r	
F13/f2/h2/U2/Z (CIVX2)	0.07
15.62 f	
F13/f2/h2/U1/Z (CNR2X2)	0.11
15.73 r	
F13/f2/h2/cout_ha (HA_29)	0.00
15.73 r	
F13/f2/U2/Z (CIVX2)	0.08
15.82 f	
F13/f2/U1/Z (CND2IX2)	0.07
15.89 r	
F13/f2/cout_fa1 (FA_1bit_15)	0.00
15.89 r	
F13/f3/cin (FA_1bit_14)	0.00
15.89 r	
F13/f3/h2/op2_ha (HA_27)	0.00
15.89 r	
F13/f3/h2/U2/Z (CIVX2)	0.07
15.96 f	
F13/f3/h2/U1/Z (CNR2X2)	0.10
16.06 r	
F13/f3/h2/cout_ha (HA_27)	0.00
16.06 r	
F13/f3/U1/Z (CNR2IX1)	0.10
16.16 f	
F13/f3/U3/Z (CIVX2)	0.09
16.24 r	
F13/f3/cout_fa1 (FA_1bit_14)	0.00
16.24 r	

F13/f4/cin (FA_1bit_13)	0.00
16.24 r	
F13/f4/h2/op2_ha (HA_25)	0.00
16.24 r	
F13/f4/h2/U1/Z (CND2X2)	0.10
16.34 f	
F13/f4/h2/U2/Z (CIVX2)	0.06
16.40 r	
F13/f4/h2/cout_ha (HA_25)	0.00
16.40 r	
F13/f4/U2/Z (CIVX2)	0.06
16.47 f	
F13/f4/U1/Z (CND2IX2)	0.07
16.54 r	
F13/f4/cout_fa1 (FA_1bit_13)	0.00
16.54 r	
F13/cout_fa4_2 (FA_4bit_2_4)	0.00
16.54 r	
F14/cin_fa4 (FA_4bit_2_3)	0.00
16.54 r	
F14/f1/cin (FA_1bit_12)	0.00
16.54 r	
F14/f1/h2/op2_ha (HA_23)	0.00
16.54 r	
F14/f1/h2/U1/Z (CND2X2)	0.09
16.63 f	
F14/f1/h2/U2/Z (CIVX2)	0.06
16.69 r	
F14/f1/h2/cout_ha (HA_23)	0.00
16.69 r	
F14/f1/U2/Z (CIVX2)	0.06
16.76 f	
F14/f1/U1/Z (CND2IX2)	0.09
16.84 r	
F14/f1/cout_fa1 (FA_1bit_12)	0.00
16.84 r	
F14/f2/cin (FA_1bit_11)	0.00
16.84 r	
F14/f2/h2/op2_ha (HA_21)	0.00
16.84 r	

F14/f2/h2/U1/Z (CND2X2)	0.10
16.94 f	
F14/f2/h2/U2/Z (CIVX2)	0.06
17.00 r	
F14/f2/h2/cout_ha (HA_21)	0.00
17.00 r	
F14/f2/U2/Z (CIVX2)	0.06
17.07 f	
F14/f2/U1/Z (CND2IX2)	0.07
17.14 r	
F14/f2/cout_fa1 (FA_1bit_11)	0.00
17.14 r	
F14/f3/cin (FA_1bit_10)	0.00
17.14 r	
F14/f3/h2/op2_ha (HA_19)	0.00
17.14 r	
F14/f3/h2/U1/Z (CND2X2)	0.09
17.23 f	
F14/f3/h2/U2/Z (CIVX2)	0.06
17.29 r	
F14/f3/h2/cout_ha (HA_19)	0.00
17.29 r	
F14/f3/U2/Z (CIVX2)	0.06
17.36 f	
F14/f3/U1/Z (CND2IX2)	0.07
17.43 r	
F14/f3/cout_fa1 (FA_1bit_10)	0.00
17.43 r	
F14/f4/cin (FA_1bit_9)	0.00
17.43 r	
F14/f4/h2/op2_ha (HA_17)	0.00
17.43 r	
F14/f4/h2/U1/Z (CND2X2)	0.09
17.52 f	
F14/f4/h2/U2/Z (CIVX2)	0.06
17.58 r	
F14/f4/h2/cout_ha (HA_17)	0.00
17.58 r	
F14/f4/U2/Z (CIVX2)	0.06
17.65 f	

F14/f4/U1/Z (CND2IX2)	0.07
17.72 r	
F14/f4/cout_fa1 (FA_1bit_9)	0.00
17.72 r	
F14/cout_fa4_2 (FA_4bit_2_3)	0.00
17.72 r	
F15/cin_fa4 (FA_4bit_2_2)	0.00
17.72 r	
F15/f1/cin (FA_1bit_8)	0.00
17.72 r	
F15/f1/h2/op2_ha (HA_15)	0.00
17.72 r	
F15/f1/h2/U1/Z (CND2X2)	0.09
17.81 f	
F15/f1/h2/U2/Z (CIVX2)	0.06
17.87 r	
F15/f1/h2/cout_ha (HA_15)	0.00
17.87 r	
F15/f1/U2/Z (CIVX2)	0.06
17.94 f	
F15/f1/U1/Z (CND2IX2)	0.07
18.01 r	
F15/f1/cout_fa1 (FA_1bit_8)	0.00
18.01 r	
F15/f2/cin (FA_1bit_7)	0.00
18.01 r	
F15/f2/h2/op2_ha (HA_13)	0.00
18.01 r	
F15/f2/h2/U1/Z (CND2X2)	0.09
18.10 f	
F15/f2/h2/U2/Z (CIVX2)	0.06
18.16 r	
F15/f2/h2/cout_ha (HA_13)	0.00
18.16 r	
F15/f2/U2/Z (CIVX2)	0.06
18.23 f	
F15/f2/U1/Z (CND2IX2)	0.07
18.30 r	
F15/f2/cout_fa1 (FA_1bit_7)	0.00
18.30 r	

F15/f3/cin (FA_1bit_6)	0.00
18.30 r	
F15/f3/h2/op2_ha (HA_11)	0.00
18.30 r	
F15/f3/h2/U1/Z (CND2X2)	0.09
18.39 f	
F15/f3/h2/U2/Z (CIVX2)	0.06
18.45 r	
F15/f3/h2/cout_ha (HA_11)	0.00
18.45 r	
F15/f3/U2/Z (CIVX2)	0.06
18.52 f	
F15/f3/U1/Z (CND2IX2)	0.07
18.59 r	
F15/f3/cout_fa1 (FA_1bit_6)	0.00
18.59 r	
F15/f4/cin (FA_1bit_5)	0.00
18.59 r	
F15/f4/h2/op2_ha (HA_9)	0.00
18.59 r	
F15/f4/h2/U4/Z (CDLY1XL)	0.62
19.20 r	
F15/f4/h2/U5/Z (CIVXL)	0.08
19.28 f	
F15/f4/h2/U6/Z (CIVXL)	0.10
19.38 r	
F15/f4/h2/U7/Z (CEOXL)	0.35
19.73 r	
F15/f4/h2/sum_ha (HA_9)	0.00
19.73 r	
F15/f4/sum_fa1 (FA_1bit_5)	0.00
19.73 r	
F15/sum_fa4_2[3] (FA_4bit_2_2)	0.00
19.73 r	
sum_reg[59]/D (CFD2QX1)	0.00
19.73 r	
data	arrival
19.73	time

clock	clock (rise edge)	20.80
20.80		
clock	network delay (propagated)	0.00
20.80		
clock	uncertainty	-0.25
20.55		
sum_reg[59]/CP (CFD2QX1)		0.00
20.55 r		
library	setup time	-0.34
20.21		
data	required	time
20.21		
<hr/>		

data	required	time
20.21		
data arrival time		-
19.73		
<hr/>		

slack		(MET)
0.48		

1
report_area

```
*****
Report : area
Design : RCA64
Version: C-2009.06-SP5
Date   : Wed Dec  2 22:10:53 2015
*****
```

Library(s) Used:

tc240c (File:
 /apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25)

Number of ports: 195

Number of nets: 677
Number of cells: 483
Number of references: 24

Combinational area: 1805.500000
Noncombinational area: 1325.500000
Net Interconnect area: undefined (No wire load specified)

Total cell area: 3131.000000
Total area: undefined
1
report_power
Loading db file
'/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25'
Warning: Main library 'tc240c' does not specify the following unit required for power: 'Leakage Power'. (PWR-424)
Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

Report : power
-analysis_effort low
Design : RCA64
Version: C-2009.06-SP5
Date : Wed Dec 2 22:10:54 2015

Library(s) Used:

tc240c (File:
'/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25')

Operating Conditions: WCCOM25 Library: tc240c
Wire Load Model Mode: top

Global Operating Voltage = 2.3

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000ff

Time Units = 1ns

Dynamic Power Units = 1uW (derived from V, C, T units)

Leakage Power Units = Unitless

Cell Internal Power = 4.8942 mW (95%)

Net Switching Power = 239.9675 uW (5%)

Total Dynamic Power = 5.1342 mW (100%)

Cell Leakage Power = 0.0000

1

write -hierarchy -format verilog -output RCA64_1_nl.v
Writing verilog file

'/home/pa/pand2610/Desktop/Project/RCA64/RCA64_1_nl.v'.

1

quit

Thank you...

Synthesis Report of CLA-2L

DC Professional (TM)
DC Expert (TM)
DC Ultra (TM)
FloorPlan Manager (TM)
HDL Compiler (TM)
VHDL Compiler (TM)
Library Compiler (TM)
DesignWare Developer (TM)

DFT Compiler (TM)
 BSD Compiler
 Power Compiler (TM)

Version C-2009.06-SP5 for linux -- Jan 15, 2010
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Initializing...

```
set                                         link_library
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
/apps/synopsys/SYNTH/libraries/syn/dw02.sldb
/apps/synopsys/SYNTH/libraries/syn/dw01.sldb}
/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
/apps/synopsys/SYNTH/libraries/syn/dw02.sldb
/apps/synopsys/SYNTH/libraries/syn/dw01.sldb
set                                         target_library
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}
/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
read_verilog {CLA4.v, CLA4_2.v, CLA16.v CLA16_2.v, CLA_64.v}
Loading                               db             file
'/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25'
Loading db file '/apps/synopsys/SYNTH/libraries/syn/dw02.sldb'
Loading db file '/apps/synopsys/SYNTH/libraries/syn/dw01.sldb'
Loading db file '/apps/synopsys/SYNTH/libraries/syn/gtech.db'
Loading                               db             file
'/apps/synopsys/SYNTH/libraries/syn/standard.sldb'
  Loading link library 'tc240c'
Warning: Function '=' leaked 1 allocations for 16 bytes. (EQN-21)
  Loading link library 'gtech'
Loading                               verilog        files:
'/home/pa/pand2610/Desktop/Project/CLA64/CLA4.v'
```

```
'/home/pa/pand2610/Desktop/Project/CLA64/CLA4_2.v'
'/home/pa/pand2610/Desktop/Project/CLA64/CLA16.v'
'/home/pa/pand2610/Desktop/Project/CLA64/CLA16_2.v'
'/home/pa/pand2610/Desktop/Project/CLA64/CLA_64.v'
Detecting input file type automatically (-rtl or -netlist).
Running DC verilog reader
Reading with Presto HDL Compiler (equivalent to -rtl option).
Running PRESTO HDLC
Compiling source file
/home/pa/pand2610/Desktop/Project/CLA64/CLA4.v
Compiling source file
/home/pa/pand2610/Desktop/Project/CLA64/CLA4_2.v
Compiling source file
/home/pa/pand2610/Desktop/Project/CLA64/CLA16.v
Compiling source file
/home/pa/pand2610/Desktop/Project/CLA64/CLA16_2.v
Compiling source file
/home/pa/pand2610/Desktop/Project/CLA64/CLA_64.v

Inferred memory devices in process
    in routine CLA_64 line 21 in file
        '/home/pa/pand2610/Desktop/Project/CLA64/CLA_64.v'.
=====
=====
|      Register Name      |      Type       | Width | Bus | MB | AR | AS |
SR | SS | ST |
=====
=====
|      sum_reg           | Flip-flop | 64   | Y   | N  | Y  | N  |
N  | N  | N  |
|      crout_reg         | Flip-flop | 1    | N   | N  | Y  | N  |
N  | N  | N  |
|      op1_f_reg         | Flip-flop | 64   | Y   | N  | Y  | N  |
N  | N  | N  |
|      op2_f_reg         | Flip-flop | 64   | Y   | N  | Y  | N  |
N  | N  | N  |
=====
=====
Presto compilation completed successfully.
Current design is now
'/home/pa/pand2610/Desktop/Project/CLA64/CLA4.db:CLA4'
Loaded 5 designs.
Current design is 'CLA4'.
CLA4 CLA4_2 CLA16 CLA16_2 CLA_64
current_design CLA_64
Current design is 'CLA_64'.
{CLA_64}
```

```

check_design
Warning: In design 'CLA_64', net 'A1/P[0]' driven by pin
'A1/C1/P1' has no loads. (LINT-2)
Information: Design 'CLA_64' has multiply instantiated designs.
Use the '-multiple_designs' switch for more information. (LINT-
78)
1
set_drive 0 clock
1
set_drive 0 reset
1
set_dont_touch_network clock
1
create_clock clock -name clock -period 7.9500000
1
set_propagated_clock clock
Information: set_input_delay values are added to the propagated
clock skew. (TIM-113)
1
set_clock_uncertainty 0.25 clock
1
set_propagated_clock clock
Information: set_input_delay values are added to the propagated
clock skew. (TIM-113)
1
#set_output_delay 0.5 -clock clock [all_outputs]
#set           all_inputs_wo_rst_clk          [remove_from_collection
[remove_from_collection [all_inputs] [get_port clk]] [get_port
rst]]
#set_driving_cell -lib_cell CND2X1 $all_inputs_wo_rst_clk
#set_input_delay 0.5 -clock clk $all_inputs_wo_rst_clk
#set_max_delay 48.5 -to [all_outputs]
#set_max_delay 48.5 -from $all_inputs_wo_rst_clk
set_fix_hold [ get_clocks clock ]
1
compile -map_effort medium -incremental_mapping
Information: Evaluating DesignWare library utilization. (UISN-
27)

=====
=====

| DesignWare Building Block Library | Version | 
Available |
=====

=====

| Basic DW Building Blocks | C-2009.06-DWBB_0912
| * | 
```

Licensed DW Building Blocks	C-2009.06-DWBB_0912
=====	=====
=====	

Information: There are 1 potential problems in your design.
Please run 'check_design' for more information. (LINT-99)

Warning: Operating condition WCCOM25 set on design CLA_64 has different process,
voltage and temperatures parameters than the parameters at which target library
tc240c is characterized. Delays may be inaccurate as a result.
(OPT-998)

Beginning Pass 1 Mapping (Incremental)

Processing 'CLA4_2_0'
Processing 'CLA16_2_0'
Processing 'CLA4'
Processing 'CLA16'
Processing 'CLA_64'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Medium effort)
(Incremental)

Beginning Incremental Implementation Selection

Information: Input delay ('fall') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

ELAPSED MIN DELAY	TIME ENDPOINT	AREA COST	WORST SLACK	NEG SLACK	TOTAL RULE	NEG COST	DESIGN
0:00:01 0.00		1981.0	0.66		1.2		1890.1
-84.96	0:00:01	2119.5	0.00		0.0		0.0

Beginning Design Rule Fixing (min_path)

ELAPSED MIN DELAY	TIME ENDPOINT	AREA COST	WORST SLACK	NEG SLACK	TOTAL RULE	NEG COST	DESIGN
0:00:01 -84.96	0:00:01	2119.5	0.00		0.0		0.0
0.00	0:00:02	2696.5	0.00		0.0		0.0
Loading			db				file
'/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25'							

Optimization Complete

```

1
create_clock clk -name clock -period 7.000000
Warning: Can't find object 'clk' in design 'CLA_64'. (UID-95)
Error: Value for list 'source_objects' must have 1 elements.
(CMD-036)
0
set_propagated_clock clock
Information: set_input_delay values are added to the propagated
clock skew. (TIM-113)
1
set_clock_uncertainty 0.25 clock
1
set_propagated_clock clock

```

Information: set_input_delay values are added to the propagated clock skew. (TIM-113)

1

update_timing

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

1

report -cell

report_cell

Report : cell

Design : CLA_64

Version: C-2009.06-SP5

Date : Thu Dec 3 01:28:45 2015

Attributes:

b - black box (unknown)

h - hierarchical

n - noncombinational

r - removable

u - contains unmapped logic

Cell Area	Attributes	Reference	Library
A1			CL16
150.000000			
h			
A2			CL16_2_0
161.500000			
h			
A3			CL16_2_2
161.500000			
h			
A4			CL16_2_1
178.500000			
h			

U3	CIVX2	tc240c
1.000000		
U4	CDLY1XL	tc240c
3.500000		
U5	CNIVX1	tc240c
1.000000		
U6	CDLY1XL	tc240c
3.500000		
U7	CNIVX1	tc240c
1.000000		
U8	CDLY1XL	tc240c
3.500000		
U9	CNIVX1	tc240c
1.000000		
U10	CDLY1XL	tc240c
3.500000		
U11	CNIVX1	tc240c
1.000000		
U12	CDLY1XL	tc240c
3.500000		
U13	CNIVX1	tc240c
1.000000		
U14	CDLY1XL	tc240c
3.500000		
U15	CNIVX1	tc240c
1.000000		
U16	CDLY1XL	tc240c
3.500000		
U17	CNIVX1	tc240c
1.000000		
U18	CDLY1XL	tc240c
3.500000		
U19	CNIVX1	tc240c
1.000000		
U20	CDLY1XL	tc240c
3.500000		
U21	CNIVX1	tc240c
1.000000		
U22	CDLY1XL	tc240c
3.500000		
U23	CNIVX1	tc240c
1.000000		
U24	CDLY1XL	tc240c
3.500000		
U25	CNIVX1	tc240c
1.000000		

U26	CDLY1XL	tc240c
3.500000		
U27	CNIVX1	tc240c
1.000000		
U28	CDLY1XL	tc240c
3.500000		
U29	CNIVX1	tc240c
1.000000		
U30	CDLY1XL	tc240c
3.500000		
U31	CNIVX1	tc240c
1.000000		
U32	CDLY1XL	tc240c
3.500000		
U33	CNIVX1	tc240c
1.000000		
U34	CDLY1XL	tc240c
3.500000		
U35	CNIVX1	tc240c
1.000000		
U36	CDLY1XL	tc240c
3.500000		
U37	CNIVX1	tc240c
1.000000		
U38	CDLY1XL	tc240c
3.500000		
U39	CNIVX1	tc240c
1.000000		
U40	CDLY1XL	tc240c
3.500000		
U41	CNIVX1	tc240c
1.000000		
U42	CDLY1XL	tc240c
3.500000		
U43	CNIVX1	tc240c
1.000000		
U44	CDLY1XL	tc240c
3.500000		
U45	CNIVX1	tc240c
1.000000		
U46	CDLY1XL	tc240c
3.500000		
U47	CNIVX1	tc240c
1.000000		
U48	CDLY1XL	tc240c
3.500000		

U49	CNIVX1	tc240c
1.000000		
U50	CDLY1XL	tc240c
3.500000		
U51	CNIVX1	tc240c
1.000000		
U52	CDLY1XL	tc240c
3.500000		
U53	CNIVX1	tc240c
1.000000		
U54	CDLY1XL	tc240c
3.500000		
U55	CNIVX1	tc240c
1.000000		
U56	CDLY1XL	tc240c
3.500000		
U57	CNIVX1	tc240c
1.000000		
U58	CDLY1XL	tc240c
3.500000		
U59	CNIVX1	tc240c
1.000000		
U60	CDLY1XL	tc240c
3.500000		
U61	CNIVX1	tc240c
1.000000		
U62	CDLY1XL	tc240c
3.500000		
U63	CNIVX1	tc240c
1.000000		
U64	CDLY1XL	tc240c
3.500000		
U65	CNIVX1	tc240c
1.000000		
U66	CDLY1XL	tc240c
3.500000		
U67	CNIVX1	tc240c
1.000000		
U68	CDLY1XL	tc240c
3.500000		
U69	CNIVX1	tc240c
1.000000		
U70	CDLY1XL	tc240c
3.500000		
U71	CNIVX1	tc240c
1.000000		

U72	CDLY1XL	tc240c
3.500000		
U73	CNIVX1	tc240c
1.000000		
U74	CDLY1XL	tc240c
3.500000		
U75	CNIVX1	tc240c
1.000000		
U76	CDLY1XL	tc240c
3.500000		
U77	CNIVX1	tc240c
1.000000		
U78	CDLY1XL	tc240c
3.500000		
U79	CNIVX1	tc240c
1.000000		
U80	CDLY1XL	tc240c
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U81	CNIVX1	tc240c
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U82	CDLY1XL	tc240c
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U83	CNIVX1	tc240c
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U84	CDLY1XL	tc240c
3.500000		
U85	CNIVX1	tc240c
1.000000		
U86	CDLY1XL	tc240c
3.500000		
U87	CNIVX1	tc240c
1.000000		
U88	CDLY1XL	tc240c
3.500000		
U89	CNIVX1	tc240c
1.000000		
U90	CDLY1XL	tc240c
3.500000		
U91	CNIVX1	tc240c
1.000000		
U92	CDLY1XL	tc240c
3.500000		
U93	CNIVX1	tc240c
1.000000		
U94	CDLY1XL	tc240c
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U95	CNIVX1	tc240c
1.000000		
U96	CDLY1XL	tc240c
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U97	CNIVX1	tc240c
1.000000		
U98	CDLY1XL	tc240c
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U99	CNIVX1	tc240c
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U100	CDLY1XL	tc240c
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U101	CNIVX1	tc240c
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U103	CNIVX1	tc240c
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U104	CDLY1XL	tc240c
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U105	CNIVX1	tc240c
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U106	CDLY1XL	tc240c
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U107	CNIVX1	tc240c
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U108	CDLY1XL	tc240c
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U109	CNIVX1	tc240c
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U200	CDLY1XL	tc240c
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U201	CNIVX1	tc240c
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U202	CDLY1XL	tc240c
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U203	CNIVX1	tc240c
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U208	CDLY1XL	tc240c
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U209	CNIVX1	tc240c
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U210	CDLY1XL	tc240c
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U211	CNIVX1	tc240c
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U212	CDLY1XL	tc240c
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U213	CNIVX1	tc240c
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U214	CDLY1XL	tc240c
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U215	CNIVX1	tc240c
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U216	CDLY1XL	tc240c
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U217	CNIVX1	tc240c
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U218	CDLY1XL	tc240c
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U219	CNIVX1	tc240c
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U220	CDLY1XL	tc240c
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U221	CNIVX1	tc240c
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U222	CDLY1XL	tc240c
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U223	CNIVX1	tc240c
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U225	CNIVX1	tc240c
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U226	CDLY1XL	tc240c
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U227	CNIVX1	tc240c
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U228	CDLY1XL	tc240c
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U229	CNIVX1	tc240c
1.000000		
U230	CDLY1XL	tc240c
3.500000		
U231	CNIVX1	tc240c
1.000000		
U232	CDLY1XL	tc240c
3.500000		

U233	CNIVX1	tc240c
1.000000		
U234	CDLY1XL	tc240c
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U235	CNIVX1	tc240c
1.000000		
U236	CDLY1XL	tc240c
3.500000		
U237	CNIVX1	tc240c
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U238	CDLY1XL	tc240c
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U239	CNIVX1	tc240c
1.000000		
U240	CDLY1XL	tc240c
3.500000		
U241	CNIVX1	tc240c
1.000000		
U242	CDLY1XL	tc240c
3.500000		
U243	CNIVX1	tc240c
1.000000		
U244	CDLY1XL	tc240c
3.500000		
U245	CNIVX1	tc240c
1.000000		
U246	CDLY1XL	tc240c
3.500000		
U247	CNIVX1	tc240c
1.000000		
U248	CDLY1XL	tc240c
3.500000		
U249	CNIVX1	tc240c
1.000000		
U250	CDLY1XL	tc240c
3.500000		
U251	CNIVX1	tc240c
1.000000		
U252	CDLY1XL	tc240c
3.500000		
U253	CNIVX1	tc240c
1.000000		
U254	CDLY1XL	tc240c
3.500000		
U255	CNIVX1	tc240c
1.000000		

U256	CDLY1XL	tc240c
3.500000		
U257	CNIVX1	tc240c
1.000000		
U258	CDLY1XL	tc240c
3.500000		
U259	CNIVX1	tc240c
1.000000		
U260	CDLY2X2	tc240c
7.000000		
U261	CDLY2X2	tc240c
7.000000		
U262	CDLY2X2	tc240c
7.000000		
U263	CDLY2X2	tc240c
7.000000		
U264	CDLY2X2	tc240c
7.000000		
U265	CDLY2X2	tc240c
7.000000		
U266	CDLY2X2	tc240c
7.000000		
U267	CDLY2X2	tc240c
7.000000		
U268	CDLY2X2	tc240c
7.000000		
U269	CDLY2X2	tc240c
7.000000		
U270	CDLY2X2	tc240c
7.000000		
U271	CDLY2X2	tc240c
7.000000		
U272	CDLY2X2	tc240c
7.000000		
U273	CDLY2X2	tc240c
7.000000		
U274	CDLY2X2	tc240c
7.000000		
U275	CDLY2X2	tc240c
7.000000		
U276	CDLY2X2	tc240c
7.000000		
crout_reg	CFD2QX1	tc240c
7.000000 n		
opl_f_reg[0]	CFD2QX1	tc240c
7.000000 n		

op1_f_reg[1]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[2]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[3]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[4]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[5]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[6]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[7]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[8]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[9]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[10]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[11]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[12]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[13]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[14]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[15]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[16]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[17]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[18]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[19]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[20]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[21]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[22]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[23]	CFD2QX1	tc240c
7.000000 n		

op1_f_reg[24]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[25]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[26]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[27]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[28]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[29]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[30]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[31]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[32]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[33]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[34]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[35]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[36]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[37]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[38]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[39]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[40]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[41]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[42]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[43]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[44]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[45]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[46]	CFD2QX1	tc240c
7.000000 n		

op1_f_reg[47]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[48]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[49]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[50]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[51]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[52]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[53]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[54]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[55]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[56]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[57]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[58]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[59]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[60]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[61]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[62]	CFD2QX1	tc240c
7.000000 n		
op1_f_reg[63]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[0]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[1]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[2]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[3]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[4]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[5]	CFD2QX1	tc240c
7.000000 n		

op2_f_reg[6]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[7]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[8]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[9]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[10]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[11]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[12]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[13]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[14]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[15]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[16]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[17]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[18]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[19]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[20]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[21]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[22]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[23]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[24]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[25]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[26]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[27]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[28]	CFD2QX1	tc240c
7.000000 n		

op2_f_reg[29]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[30]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[31]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[32]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[33]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[34]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[35]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[36]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[37]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[38]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[39]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[40]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[41]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[42]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[43]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[44]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[45]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[46]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[47]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[48]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[49]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[50]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[51]	CFD2QX1	tc240c
7.000000 n		

op2_f_reg[52]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[53]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[54]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[55]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[56]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[57]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[58]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[59]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[60]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[61]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[62]	CFD2QX1	tc240c
7.000000 n		
op2_f_reg[63]	CFD2QXL	tc240c
5.000000 n		
sum_reg[0]	CFD2QX1	tc240c
7.000000 n		
sum_reg[1]	CFD2QX1	tc240c
7.000000 n		
sum_reg[2]	CFD2QX1	tc240c
7.000000 n		
sum_reg[3]	CFD2QX1	tc240c
7.000000 n		
sum_reg[4]	CFD2QX1	tc240c
7.000000 n		
sum_reg[5]	CFD2QX1	tc240c
7.000000 n		
sum_reg[6]	CFD2QX1	tc240c
7.000000 n		
sum_reg[7]	CFD2QX1	tc240c
7.000000 n		
sum_reg[8]	CFD2QX1	tc240c
7.000000 n		
sum_reg[9]	CFD2QX1	tc240c
7.000000 n		
sum_reg[10]	CFD2QX1	tc240c
7.000000 n		

sum_reg[11]	CFD2QX1	tc240c
7.000000 n		
sum_reg[12]	CFD2QX1	tc240c
7.000000 n		
sum_reg[13]	CFD2QX1	tc240c
7.000000 n		
sum_reg[14]	CFD2QX1	tc240c
7.000000 n		
sum_reg[15]	CFD2QX1	tc240c
7.000000 n		
sum_reg[16]	CFD2QX1	tc240c
7.000000 n		
sum_reg[17]	CFD2QX1	tc240c
7.000000 n		
sum_reg[18]	CFD2QX1	tc240c
7.000000 n		
sum_reg[19]	CFD2QX1	tc240c
7.000000 n		
sum_reg[20]	CFD2QX1	tc240c
7.000000 n		
sum_reg[21]	CFD2QX1	tc240c
7.000000 n		
sum_reg[22]	CFD2QX1	tc240c
7.000000 n		
sum_reg[23]	CFD2QX1	tc240c
7.000000 n		
sum_reg[24]	CFD2QX1	tc240c
7.000000 n		
sum_reg[25]	CFD2QX1	tc240c
7.000000 n		
sum_reg[26]	CFD2QX1	tc240c
7.000000 n		
sum_reg[27]	CFD2QX1	tc240c
7.000000 n		
sum_reg[28]	CFD2QX1	tc240c
7.000000 n		
sum_reg[29]	CFD2QX1	tc240c
7.000000 n		
sum_reg[30]	CFD2QX1	tc240c
7.000000 n		
sum_reg[31]	CFD2QX1	tc240c
7.000000 n		
sum_reg[32]	CFD2QX1	tc240c
7.000000 n		
sum_reg[33]	CFD2QX1	tc240c
7.000000 n		

sum_reg[34]	CFD2QX1	tc240c
7.000000 n		
sum_reg[35]	CFD2QX1	tc240c
7.000000 n		
sum_reg[36]	CFD2QX1	tc240c
7.000000 n		
sum_reg[37]	CFD2QX1	tc240c
7.000000 n		
sum_reg[38]	CFD2QX1	tc240c
7.000000 n		
sum_reg[39]	CFD2QX1	tc240c
7.000000 n		
sum_reg[40]	CFD2QX1	tc240c
7.000000 n		
sum_reg[41]	CFD2QX1	tc240c
7.000000 n		
sum_reg[42]	CFD2QX1	tc240c
7.000000 n		
sum_reg[43]	CFD2QX1	tc240c
7.000000 n		
sum_reg[44]	CFD2QX1	tc240c
7.000000 n		
sum_reg[45]	CFD2QX1	tc240c
7.000000 n		
sum_reg[46]	CFD2QX1	tc240c
7.000000 n		
sum_reg[47]	CFD2QX1	tc240c
7.000000 n		
sum_reg[48]	CFD2QX1	tc240c
7.000000 n		
sum_reg[49]	CFD2QX1	tc240c
7.000000 n		
sum_reg[50]	CFD2QX1	tc240c
7.000000 n		
sum_reg[51]	CFD2QX1	tc240c
7.000000 n		
sum_reg[52]	CFD2QX1	tc240c
7.000000 n		
sum_reg[53]	CFD2QX1	tc240c
7.000000 n		
sum_reg[54]	CFD2QX1	tc240c
7.000000 n		
sum_reg[55]	CFD2QX1	tc240c
7.000000 n		
sum_reg[56]	CFD2QX1	tc240c
7.000000 n		

sum_reg[57]	CFD2QX1	tc240c
7.000000 n		
sum_reg[58]	CFD2QX1	tc240c
7.000000 n		
sum_reg[59]	CFD2QX1	tc240c
7.000000 n		
sum_reg[60]	CFD2QX1	tc240c
7.000000 n		
sum_reg[61]	CFD2QX1	tc240c
7.000000 n		
sum_reg[62]	CFD2QX1	tc240c
7.000000 n		
sum_reg[63]	CFD2QX1	tc240c
7.000000 n		

Total	471	cells
2696.500000		
1		

report_timing -max_paths 5

Report : timing
 -path full
 -delay max
 -max_paths 5

Design : CLA_64
 Version: C-2009.06-SP5

Date : Thu Dec 3 01:28:45 2015

Operating Conditions: WCCOM25 Library: tc240c
 Wire Load Model Mode: top

Startpoint: op2_f_reg[1]
 (rising edge-triggered flip-flop clocked by clock)
 Endpoint: sum_reg[63]
 (rising edge-triggered flip-flop clocked by clock)
 Path Group: clock
 Path Type: max

Point	Incr	Path
<hr/>		
clock clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.00	0.00
op2_f_reg[1]/CP (CFD2QX1)	0.00	0.00 r
op2_f_reg[1]/Q (CFD2QX1)	0.49	0.49 f

A1/op2_4[1] (CLA16)	0.00	0.49	f
A1/C1/op2[1] (CLA4)	0.00	0.49	f
A1/C1/U5/Z (CEOX2)	0.26	0.75	f
A1/C1/U11/Z (CAOR2X1)	0.32	1.07	f
A1/C1/U9/Z (CAOR2X1)	0.32	1.38	f
A1/C1/U7/Z (CAOR2X1)	0.34	1.73	f
A1/C1/G1 (CLA4)	0.00	1.73	f
A1/U3/Z (COND4CX1)	0.17	1.90	r
A1/U2/Z (CND2IX1)	0.13	2.03	f
A1/U1/Z (CAOR1X1)	0.29	2.31	f
A1/crout (CLA16)	0.00	2.31	f
A2/Cin (CLA16_2_0)	0.00	2.31	f
A2/U4/Z (COND4CX1)	0.18	2.49	r
A2/U3/Z (CND2IX1)	0.13	2.62	f
A2/U2/Z (COND4CX1)	0.21	2.83	r
A2/U1/Z (CND2IX2)	0.16	2.99	f
A2/crout_16 (CLA16_2_0)	0.00	2.99	f
A3/Cin (CLA16_2_2)	0.00	2.99	f
A3/U4/Z (COND4CX1)	0.17	3.16	r
A3/U3/Z (CND2IX1)	0.13	3.29	f
A3/U2/Z (COND4CX1)	0.21	3.50	r
A3/U1/Z (CND2IX2)	0.15	3.65	f
A3/crout_16 (CLA16_2_2)	0.00	3.65	f
A4/Cin (CLA16_2_1)	0.00	3.65	f
A4/A1/Cin (CLA4_2_4)	0.00	3.65	f
A4/A1/U4/Z (CND2X2)	0.07	3.72	r
A4/A1/U9/Z (CIVX1)	0.06	3.79	f
A4/A1/U8/Z (CAOR1X1)	0.28	4.06	f
A4/A1/U6/Z (CANR2X2)	0.28	4.34	r
A4/A1/U10/Z (COND2X2)	0.18	4.52	f
A4/A1/crout (CLA4_2_4)	0.00	4.52	f
A4/A2/Cin (CLA4_2_3)	0.00	4.52	f
A4/A2/U10/Z (CND2X1)	0.11	4.63	r
A4/A2/U9/Z (CIVX1)	0.09	4.72	f
A4/A2/U8/Z (CAOR1X1)	0.28	4.99	f
A4/A2/U2/Z (CANR2X2)	0.28	5.27	r
A4/A2/U7/Z (COND2X2)	0.21	5.48	f
A4/A2/crout (CLA4_2_3)	0.00	5.48	f
A4/A3/Cin (CLA4_2_2)	0.00	5.48	f
A4/A3/U7/Z (CND2X2)	0.09	5.57	r
A4/A3/U2/Z (CIVX2)	0.06	5.63	f
A4/A3/U8/Z (CAOR1X1)	0.28	5.90	f
A4/A3/U6/Z (CANR2X2)	0.28	6.18	r
A4/A3/U10/Z (COND2X2)	0.18	6.36	f
A4/A3/crout (CLA4_2_2)	0.00	6.36	f
A4/A4/Cin (CLA4_2_1)	0.00	6.36	f
A4/A4/U10/Z (CND2X1)	0.11	6.47	r

A4/A4/U9/Z (CIVX1)	0.09	6.55	f
A4/A4/U8/Z (CAOR1X1)	0.28	6.83	f
A4/A4/U5/Z (CANR2X2)	0.26	7.10	r
A4/A4/U2/Z (CENX1)	0.28	7.37	r
A4/A4/sum[3] (CLA4_2_1)	0.00	7.37	r
A4/sum_16[15] (CLA16_2_1)	0.00	7.37	r
sum_reg[63]/D (CFD2QX1)	0.00	7.37	r
data arrival time		7.37	

clock clock (rise edge)	7.95	7.95	
clock network delay (propagated)	0.00	7.95	
clock uncertainty	-0.25	7.70	
sum_reg[63]/CP (CFD2QX1)	0.00	7.70	r
library setup time	-0.32	7.38	
data required time		7.38	

data required time		7.38	
data arrival time		-7.37	

slack (MET)		0.00	

Startpoint: op2_f_reg[1]
 (rising edge-triggered flip-flop clocked by clock)
 Endpoint: sum_reg[47]
 (rising edge-triggered flip-flop clocked by clock)
 Path Group: clock
 Path Type: max

Point	Incr	Path
clock clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.00	0.00
op2_f_reg[1]/CP (CFD2QX1)	0.00	0.00 r
op2_f_reg[1]/Q (CFD2QX1)	0.49	0.49 f
A1/op2_4[1] (CLA16)	0.00	0.49 f
A1/C1/op2[1] (CLA4)	0.00	0.49 f
A1/C1/U5/Z (CEOX2)	0.26	0.75 f
A1/C1/U11/Z (CAOR2X1)	0.32	1.07 f
A1/C1/U9/Z (CAOR2X1)	0.32	1.38 f
A1/C1/U7/Z (CAOR2X1)	0.34	1.73 f
A1/C1/G1 (CLA4)	0.00	1.73 f
A1/U3/Z (COND4CX1)	0.17	1.90 r
A1/U2/Z (CND2IX1)	0.13	2.03 f
A1/U1/Z (CAOR1X1)	0.29	2.31 f
A1/crout (CLA16)	0.00	2.31 f
A2/Cin (CLA16_2_0)	0.00	2.31 f

A2/U4/Z (COND4CX1)	0.18	2.49	r
A2/U3/Z (CND2IX1)	0.13	2.62	f
A2/U2/Z (COND4CX1)	0.21	2.83	r
A2/U1/Z (CND2IX2)	0.16	2.99	f
A2/crout_16 (CLA16_2_0)	0.00	2.99	f
A3/Cin (CLA16_2_2)	0.00	2.99	f
A3/A1/Cin (CLA4_2_8)	0.00	2.99	f
A3/A1/U10/Z (CND2X1)	0.11	3.09	r
A3/A1/U9/Z (CIVX1)	0.09	3.18	f
A3/A1/U8/Z (CAOR1X1)	0.27	3.45	f
A3/A1/U7/Z (CANR2X1)	0.33	3.78	r
A3/A1/U6/Z (COND2X1)	0.28	4.06	f
A3/A1/crout (CLA4_2_8)	0.00	4.06	f
A3/A2/Cin (CLA4_2_7)	0.00	4.06	f
A3/A2/U10/Z (CND2X1)	0.12	4.17	r
A3/A2/U9/Z (CIVX1)	0.09	4.26	f
A3/A2/U8/Z (CAOR1X1)	0.27	4.53	f
A3/A2/U7/Z (CANR2X1)	0.33	4.86	r
A3/A2/U6/Z (COND2X1)	0.28	5.14	f
A3/A2/crout (CLA4_2_7)	0.00	5.14	f
A3/A3/Cin (CLA4_2_6)	0.00	5.14	f
A3/A3/U10/Z (CND2X1)	0.12	5.25	r
A3/A3/U9/Z (CIVX1)	0.09	5.34	f
A3/A3/U8/Z (CAOR1X1)	0.27	5.61	f
A3/A3/U7/Z (CANR2X1)	0.33	5.94	r
A3/A3/U6/Z (COND2X1)	0.28	6.22	f
A3/A3/crout (CLA4_2_6)	0.00	6.22	f
A3/A4/Cin (CLA4_2_5)	0.00	6.22	f
A3/A4/U10/Z (CND2X1)	0.12	6.33	r
A3/A4/U9/Z (CIVX1)	0.09	6.42	f
A3/A4/U8/Z (CAOR1X1)	0.27	6.69	f
A3/A4/U7/Z (CANR2X1)	0.33	7.02	r
A3/A4/U1/Z (CENX1)	0.30	7.32	r
A3/A4/sum[3] (CLA4_2_5)	0.00	7.32	r
A3/sum_16[15] (CLA16_2_2)	0.00	7.32	r
sum_reg[47]/D (CFD2QX1)	0.00	7.32	r
data arrival time		7.32	
clock clock (rise edge)	7.95	7.95	
clock network delay (propagated)	0.00	7.95	
clock uncertainty	-0.25	7.70	
sum_reg[47]/CP (CFD2QX1)	0.00	7.70	r
library setup time	-0.32	7.38	
data required time		7.38	

data required time		7.38	
data arrival time		-7.32	

slack (MET)	0.06
Startpoint: op2_f_reg[1]	
(rising edge-triggered flip-flop clocked by clock)	
Endpoint: sum_reg[62]	
(rising edge-triggered flip-flop clocked by clock)	
Path Group: clock	
Path Type: max	

Point	Incr	Path
<hr/>		
clock clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.00	0.00
op2_f_reg[1]/CP (CFD2QX1)	0.00	0.00 r
op2_f_reg[1]/Q (CFD2QX1)	0.49	0.49 f
A1/op2_4[1] (CLA16)	0.00	0.49 f
A1/C1/op2[1] (CLA4)	0.00	0.49 f
A1/C1/U5/Z (CEOX2)	0.26	0.75 f
A1/C1/U11/Z (CAOR2X1)	0.32	1.07 f
A1/C1/U9/Z (CAOR2X1)	0.32	1.38 f
A1/C1/U7/Z (CAOR2X1)	0.34	1.73 f
A1/C1/G1 (CLA4)	0.00	1.73 f
A1/U3/Z (COND4CX1)	0.17	1.90 r
A1/U2/Z (CND2IX1)	0.13	2.03 f
A1/U1/Z (CAOR1X1)	0.29	2.31 f
A1/crout (CLA16)	0.00	2.31 f
A2/Cin (CLA16_2_0)	0.00	2.31 f
A2/U4/Z (COND4CX1)	0.18	2.49 r
A2/U3/Z (CND2IX1)	0.13	2.62 f
A2/U2/Z (COND4CX1)	0.21	2.83 r
A2/U1/Z (CND2IX2)	0.16	2.99 f
A2/crout_16 (CLA16_2_0)	0.00	2.99 f
A3/Cin (CLA16_2_2)	0.00	2.99 f
A3/U4/Z (COND4CX1)	0.17	3.16 r
A3/U3/Z (CND2IX1)	0.13	3.29 f
A3/U2/Z (COND4CX1)	0.21	3.50 r
A3/U1/Z (CND2IX2)	0.15	3.65 f
A3/crout_16 (CLA16_2_2)	0.00	3.65 f
A4/Cin (CLA16_2_1)	0.00	3.65 f
A4/A1/Cin (CLA4_2_4)	0.00	3.65 f
A4/A1/U4/Z (CND2X2)	0.07	3.72 r
A4/A1/U9/Z (CIVX1)	0.06	3.79 f
A4/A1/U8/Z (CAOR1X1)	0.28	4.06 f
A4/A1/U6/Z (CANR2X2)	0.28	4.34 r
A4/A1/U10/Z (COND2X2)	0.18	4.52 f

A4/A1/crout (CLA4_2_4)	0.00	4.52	f
A4/A2/Cin (CLA4_2_3)	0.00	4.52	f
A4/A2/U10/Z (CND2X1)	0.11	4.63	r
A4/A2/U9/Z (CIVX1)	0.09	4.72	f
A4/A2/U8/Z (CAOR1X1)	0.28	4.99	f
A4/A2/U2/Z (CANR2X2)	0.28	5.27	r
A4/A2/U7/Z (COND2X2)	0.21	5.48	f
A4/A2/crout (CLA4_2_3)	0.00	5.48	f
A4/A3/Cin (CLA4_2_2)	0.00	5.48	f
A4/A3/U7/Z (CND2X2)	0.09	5.57	r
A4/A3/U2/Z (CIVX2)	0.06	5.63	f
A4/A3/U8/Z (CAOR1X1)	0.28	5.90	f
A4/A3/U6/Z (CANR2X2)	0.28	6.18	r
A4/A3/U10/Z (COND2X2)	0.18	6.36	f
A4/A3/crout (CLA4_2_2)	0.00	6.36	f
A4/A4/Cin (CLA4_2_1)	0.00	6.36	f
A4/A4/U10/Z (CND2X1)	0.11	6.47	r
A4/A4/U9/Z (CIVX1)	0.09	6.55	f
A4/A4/U8/Z (CAOR1X1)	0.28	6.83	f
A4/A4/U1/Z (CEOXL)	0.36	7.19	f
A4/A4/sum[2] (CLA4_2_1)	0.00	7.19	f
A4/sum_16[14] (CLA16_2_1)	0.00	7.19	f
sum_reg[62]/D (CFD2QX1)	0.00	7.19	f
data arrival time		7.19	
clock clock (rise edge)	7.95	7.95	
clock network delay (propagated)	0.00	7.95	
clock uncertainty	-0.25	7.70	
sum_reg[62]/CP (CFD2QX1)	0.00	7.70	r
library setup time	-0.36	7.34	
data required time		7.34	

data required time		7.34	
data arrival time		-7.19	

slack (MET)		0.15	

Startpoint: op2_f_reg[1]
 (rising edge-triggered flip-flop clocked by clock)
 Endpoint: sum_reg[46]
 (rising edge-triggered flip-flop clocked by clock)
 Path Group: clock
 Path Type: max

Point	Incr	Path

clock	clock	(rise edge)	0.00	0.00
clock	network	delay (propagated)	0.00	0.00
op2_f_reg[1]/CP	(CFD2QX1)		0.00	0.00 r
op2_f_reg[1]/Q	(CFD2QX1)		0.49	0.49 f
A1/op2_4[1]	(CLA16)		0.00	0.49 f
A1/C1/op2[1]	(CLA4)		0.00	0.49 f
A1/C1/U5/Z	(CEOX2)		0.26	0.75 f
A1/C1/U11/Z	(CAOR2X1)		0.32	1.07 f
A1/C1/U9/Z	(CAOR2X1)		0.32	1.38 f
A1/C1/U7/Z	(CAOR2X1)		0.34	1.73 f
A1/C1/G1	(CLA4)		0.00	1.73 f
A1/U3/Z	(COND4CX1)		0.17	1.90 r
A1/U2/Z	(CND2IX1)		0.13	2.03 f
A1/U1/Z	(CAOR1X1)		0.29	2.31 f
A1/crout	(CLA16)		0.00	2.31 f
A2/Cin	(CLA16_2_0)		0.00	2.31 f
A2/U4/Z	(COND4CX1)		0.18	2.49 r
A2/U3/Z	(CND2IX1)		0.13	2.62 f
A2/U2/Z	(COND4CX1)		0.21	2.83 r
A2/U1/Z	(CND2IX2)		0.16	2.99 f
A2/crout_16	(CLA16_2_0)		0.00	2.99 f
A3/Cin	(CLA16_2_2)		0.00	2.99 f
A3/A1/Cin	(CLA4_2_8)		0.00	2.99 f
A3/A1/U10/Z	(CND2X1)		0.11	3.09 r
A3/A1/U9/Z	(CIVX1)		0.09	3.18 f
A3/A1/U8/Z	(CAOR1X1)		0.27	3.45 f
A3/A1/U7/Z	(CANR2X1)		0.33	3.78 r
A3/A1/U6/Z	(COND2X1)		0.28	4.06 f
A3/A1/crout	(CLA4_2_8)		0.00	4.06 f
A3/A2/Cin	(CLA4_2_7)		0.00	4.06 f
A3/A2/U10/Z	(CND2X1)		0.12	4.17 r
A3/A2/U9/Z	(CIVX1)		0.09	4.26 f
A3/A2/U8/Z	(CAOR1X1)		0.27	4.53 f
A3/A2/U7/Z	(CANR2X1)		0.33	4.86 r
A3/A2/U6/Z	(COND2X1)		0.28	5.14 f
A3/A2/crout	(CLA4_2_7)		0.00	5.14 f
A3/A3/Cin	(CLA4_2_6)		0.00	5.14 f
A3/A3/U10/Z	(CND2X1)		0.12	5.25 r
A3/A3/U9/Z	(CIVX1)		0.09	5.34 f
A3/A3/U8/Z	(CAOR1X1)		0.27	5.61 f
A3/A3/U7/Z	(CANR2X1)		0.33	5.94 r
A3/A3/U6/Z	(COND2X1)		0.28	6.22 f
A3/A3/crout	(CLA4_2_6)		0.00	6.22 f
A3/A4/Cin	(CLA4_2_5)		0.00	6.22 f
A3/A4/U10/Z	(CND2X1)		0.12	6.33 r
A3/A4/U9/Z	(CIVX1)		0.09	6.42 f
A3/A4/U8/Z	(CAOR1X1)		0.27	6.69 f

A3/A4/U2/Z (CEOX1)	0.30	6.99	f
A3/A4/sum[2] (CLA4_2_5)	0.00	6.99	f
A3/sum_16[14] (CLA16_2_2)	0.00	6.99	f
sum_reg[46]/D (CFD2QX1)	0.00	6.99	f
data arrival time		6.99	

clock clock (rise edge)	7.95	7.95	
clock network delay (propagated)	0.00	7.95	
clock uncertainty	-0.25	7.70	
sum_reg[46]/CP (CFD2QX1)	0.00	7.70	r
library setup time	-0.36	7.34	
data required time		7.34	

data required time		7.34	
data arrival time		-6.99	

slack (MET)		0.35	

Startpoint: op2_f_reg[1]
 (rising edge-triggered flip-flop clocked by clock)
 Endpoint: sum_reg[61]
 (rising edge-triggered flip-flop clocked by clock)
 Path Group: clock
 Path Type: max

Point	Incr	Path
clock clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.00	0.00
op2_f_reg[1]/CP (CFD2QX1)	0.00	0.00 r
op2_f_reg[1]/Q (CFD2QX1)	0.49	0.49 f
A1/op2_4[1] (CLA16)	0.00	0.49 f
A1/C1/op2[1] (CLA4)	0.00	0.49 f
A1/C1/U5/Z (CEOX2)	0.26	0.75 f
A1/C1/U11/Z (CAOR2X1)	0.32	1.07 f
A1/C1/U9/Z (CAOR2X1)	0.32	1.38 f
A1/C1/U7/Z (CAOR2X1)	0.34	1.73 f
A1/C1/G1 (CLA4)	0.00	1.73 f
A1/U3/Z (COND4CX1)	0.17	1.90 r
A1/U2/Z (CND2IX1)	0.13	2.03 f
A1/U1/Z (CAOR1X1)	0.29	2.31 f
A1/crout (CLA16)	0.00	2.31 f
A2/Cin (CLA16_2_0)	0.00	2.31 f
A2/U4/Z (COND4CX1)	0.18	2.49 r
A2/U3/Z (CND2IX1)	0.13	2.62 f
A2/U2/Z (COND4CX1)	0.21	2.83 r

A2/U1/Z (CND2IX2)	0.16	2.99	f
A2/crout_16 (CLA16_2_0)	0.00	2.99	f
A3/Cin (CLA16_2_2)	0.00	2.99	f
A3/U4/Z (COND4CX1)	0.17	3.16	r
A3/U3/Z (CND2IX1)	0.13	3.29	f
A3/U2/Z (COND4CX1)	0.21	3.50	r
A3/U1/Z (CND2IX2)	0.15	3.65	f
A3/crout_16 (CLA16_2_2)	0.00	3.65	f
A4/Cin (CLA16_2_1)	0.00	3.65	f
A4/A1/Cin (CLA4_2_4)	0.00	3.65	f
A4/A1/U4/Z (CND2X2)	0.07	3.72	r
A4/A1/U9/Z (CIVX1)	0.06	3.79	f
A4/A1/U8/Z (CAOR1X1)	0.28	4.06	f
A4/A1/U6/Z (CANR2X2)	0.28	4.34	r
A4/A1/U10/Z (COND2X2)	0.18	4.52	f
A4/A1/crout (CLA4_2_4)	0.00	4.52	f
A4/A2/Cin (CLA4_2_3)	0.00	4.52	f
A4/A2/U10/Z (CND2X1)	0.11	4.63	r
A4/A2/U9/Z (CIVX1)	0.09	4.72	f
A4/A2/U8/Z (CAOR1X1)	0.28	4.99	f
A4/A2/U2/Z (CANR2X2)	0.28	5.27	r
A4/A2/U7/Z (COND2X2)	0.21	5.48	f
A4/A2/crout (CLA4_2_3)	0.00	5.48	f
A4/A3/Cin (CLA4_2_2)	0.00	5.48	f
A4/A3/U7/Z (CND2X2)	0.09	5.57	r
A4/A3/U2/Z (CIVX2)	0.06	5.63	f
A4/A3/U8/Z (CAOR1X1)	0.28	5.90	f
A4/A3/U6/Z (CANR2X2)	0.28	6.18	r
A4/A3/U10/Z (COND2X2)	0.18	6.36	f
A4/A3/crout (CLA4_2_2)	0.00	6.36	f
A4/A4/Cin (CLA4_2_1)	0.00	6.36	f
A4/A4/U10/Z (CND2X1)	0.11	6.47	r
A4/A4/U4/Z (CND2X1)	0.14	6.61	f
A4/A4/U3/Z (CEOX1)	0.30	6.91	f
A4/A4/sum[1] (CLA4_2_1)	0.00	6.91	f
A4/sum_16[13] (CLA16_2_1)	0.00	6.91	f
sum_reg[61]/D (CFD2QX1)	0.00	6.91	f
data arrival time		6.91	
clock clock (rise edge)	7.95	7.95	
clock network delay (propagated)	0.00	7.95	
clock uncertainty	-0.25	7.70	
sum_reg[61]/CP (CFD2QX1)	0.00	7.70	r
library setup time	-0.36	7.34	
data required time		7.34	

data required time		7.34	

data arrival time	-6.91
-----	-----
slack (MET)	0.43

```

1
report_area
*****
Report : area
Design : CLA_64
Version: C-2009.06-SP5
Date   : Thu Dec  3 01:28:45 2015
*****

```

Library(s) Used:

tc240c (File:
 /apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25)

Number of ports: 195
 Number of nets: 665
 Number of cells: 471
 Number of references: 10

Combinational area: 1347.500000
 Noncombinational area: 1349.000000
 Net Interconnect area: undefined (No wire load specified)

Total cell area: 2696.500000
 Total area: undefined

```

1
report_power
Loading           db          file
'/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25'
Warning: Main library 'tc240c' does not specify the following
unit required for power: 'Leakage Power'. (PWR-424)
Information: Propagating switching activity (low effort zero
delay simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-
415)
*****
```

```

Report : power
         -analysis_effort low
Design : CLA_64

```

Version: C-2009.06-SP5
Date : Thu Dec 3 01:28:46 2015

Library(s) Used:

tc240c (File:
/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25)

Operating Conditions: WCCOM25 Library: tc240c
Wire Load Model Mode: top

Global Operating Voltage = 2.3

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000ff

Time Units = 1ns

Dynamic Power Units = 1uW (derived from V,C,T units)

Leakage Power Units = Unitless

Cell Internal Power = 12.8623 mW (96%)

Net Switching Power = 537.8183 uW (4%)

Total Dynamic Power = 13.4001 mW (100%)

Cell Leakage Power = 0.0000

1

write -hierarchy -format verilog -output CLA_64_1_nl.v
Writing verilog file

'/home/pa/pand2610/Desktop/Project/CLA64/CLA_64_1_nl.v'.

Warning: Verilog 'assign' or 'tran' statements are written out.
(VO-4)

1

quit

Thank you...

Synthesis Report of CSAEQG

DC Professional (TM)

DC Expert (TM)
DC Ultra (TM)
FloorPlan Manager (TM)
HDL Compiler (TM)
VHDL Compiler (TM)
Library Compiler (TM)
DesignWare Developer (TM)
DFT Compiler (TM)
BSD Compiler
Power Compiler (TM)

Version C-2009.06-SP5 for linux -- Jan 15, 2010
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Initializing...
set link_library
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
/apps/synopsys/SYNTH/libraries/syn/dw02.sldb
/apps/synopsys/SYNTH/libraries/syn/dw01.sldb}
/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
/apps/synopsys/SYNTH/libraries/syn/dw02.sldb
/apps/synopsys/SYNTH/libraries/syn/dw01.sldb
set target_library
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}
/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
read_verilog {mux_carry.v,mux_sum.v,CSA64EQG.v}
Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25'
Loading db file '/apps/synopsys/SYNTH/libraries/syn/dw02.sldb'
Loading db file '/apps/synopsys/SYNTH/libraries/syn/dw01.sldb'
Loading db file '/apps/synopsys/SYNTH/libraries/syn/gtech.db'

```

Loading db file
' /apps/synopsys/SYNTH/libraries/syn/standard.sldb'
  Loading link library 'tc240c'
Warning: Function '=' leaked 1 allocations for 16 bytes. (EQN-
21)
  Loading link library 'gtech'
Loading verilog files:
' /home/pa/pand2610/Desktop/Project/CSA64EQG/mux_carry.v'
' /home/pa/pand2610/Desktop/Project/CSA64EQG/mux_sum.v'
' /home/pa/pand2610/Desktop/Project/CSA64EQG/CSA64EQG.v'
Detecting input file type automatically (-rtl or -netlist).
Running DC verilog reader
Reading with Presto HDL Compiler (equivalent to -rtl option).
Running PRESTO HDLC
Compiling source file
/ /home/pa/pand2610/Desktop/Project/CSA64EQG/mux_carry.v
Compiling source file
/ /home/pa/pand2610/Desktop/Project/CSA64EQG/mux_sum.v
Compiling source file
/ /home/pa/pand2610/Desktop/Project/CSA64EQG/CSA64EQG.v
Warning:
/ /home/pa/pand2610/Desktop/Project/CSA64EQG/CSA64EQG.v:56:      the
undeclared symbol 'CIN' assumed to have the default net type,
which is 'wire'. (VER-936)

Inferred memory devices in process
  in routine CSA64EQG line 75 in file

' /home/pa/pand2610/Desktop/Project/CSA64EQG/CSA64EQG.v'.
=====
=====
|   Register Name    |   Type     | Width | Bus | MB | AR | AS |
SR | SS | ST |
=====
=====
|   sum_reg          | Flip-flop | 64   | Y   | N  | Y  | N  |
N  | N  | N  |
|   crout_reg        | Flip-flop | 1    | N   | N  | Y  | N  |
N  | N  | N  |
|   op1f_reg         | Flip-flop | 64   | Y   | N  | Y  | N  |
N  | N  | N  |
|   op2f_reg         | Flip-flop | 64   | Y   | N  | Y  | N  |
N  | N  | N  |
=====
=====
Presto compilation completed successfully.

```

```

Current design is now
'/home/pa/pand2610/Desktop/Project/CSA64EQG/mux_carry.db:mux_carry'
Loaded 5 designs.
Current design is 'mux_carry'.
mux_carry mux_sum FA CSA4 CSA64EQG
current_design CSA64EQG
Current design is 'CSA64EQG'.
{CSA64EQG}
check_design
Warning: In design 'CSA64EQG', a pin on submodule 's1' is
connected to logic 1 or logic 0. (LINT-32)
    Pin 'cin_4' is connected to logic 0.
Warning: In design 'CSA4', a pin on submodule 'f1' is connected
to logic 1 or logic 0. (LINT-32)
    Pin 'cin' is connected to logic 0.
Warning: In design 'CSA4', a pin on submodule 'f5' is connected
to logic 1 or logic 0. (LINT-32)
    Pin 'cin' is connected to logic 1.
Information: Design 'CSA64EQG' has multiply instantiated
designs. Use the '-multiple_designs' switch for more
information. (LINT-78)
1
set_drive 0 clock
1
set_drive 0 reset
1
set_dont_touch_network clock
1
create_clock clock -name clock -period 8.00000
1
set_propagated_clock clock
Information: set_input_delay values are added to the propagated
clock skew. (TIM-113)
1
set_clock_uncertainty 0.25 clock
1
set_propagated_clock clock
Information: set_input_delay values are added to the propagated
clock skew. (TIM-113)
1
#set_output_delay 0.5 -clock clock [all_outputs]
#set      all_inputs_wo_rst_clk      [remove_from_collection
[remove_from_collection [all_inputs] [get_port clk]] [get_port
rst]]
#set_driving_cell -lib_cell CND2X1 $all_inputs_wo_rst_clk
#set_input_delay 0.5 -clock clk $all_inputs_wo_rst_clk

```

```
#set_max_delay 48.5 -to [all_outputs]
#set_max_delay 48.5 -from $all_inputs_wo_rst_clk
set_fix_hold [ get_clocks clock ]
1
compile -map_effort medium -incremental_mapping
Information: Evaluating DesignWare library utilization. (UISN-27)
```

```
=====
===== | DesignWare Building Block Library | Version |
Available | =====
===== | Basic DW Building Blocks | C-2009.06-DWBB_0912
| * | |
| Licensed DW Building Blocks | C-2009.06-DWBB_0912
| | |
=====
```

Information: There are 3 potential problems in your design.
Please run 'check_design' for more information. (LINT-99)

Warning: Operating condition WCCOM25 set on design CSA64EQG has different process,
voltage and temperatures parameters than the parameters at which target library
tc240c is characterized. Delays may be inaccurate as a result.
(OPT-998)

```
Beginning Pass 1 Mapping (Incremental)
-----
Processing 'mux_carry_0'
Processing 'mux_sum_0'
Processing 'FA_0'
Processing 'CSA64EQG'
```

Updating timing information
Information: Updating design information... (UID-85)
Information: Input delay ('fall') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)
Information: Input delay ('rise') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

Beginning	Mapping	Optimizations	(Medium	effort)
(Incremental)				

Beginning Incremental Implementation Selection

Information: Input delay ('fall') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

MIN DELAY ENDPOINT	ELAPSED		WORST SLACK	NEG SLACK	TOTAL RULE	NEG COST	DESIGN
	TIME	AREA					
		COST					
0.00	0:00:01	2416.0	2.92		46.5		1890.1
	0:00:03	2720.0	0.04		0.2		0.0
	sum_reg[61]/D		0.00				
	0:00:03	2712.5	0.00		0.0		0.0
	-84.89						

Beginning Design Rule Fixing (min_path)

MIN DELAY ENDPOINT	ELAPSED		WORST SLACK	NEG SLACK	TOTAL RULE	NEG COST	DESIGN
	TIME	AREA					
		COST					
	0:00:03	2712.5	0.00		0.0		0.0
-84.89	0:00:04	3288.5	0.00		0.0		0.0
	0.00						

```

Loading                               db                               file
'/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25'

Optimization Complete
-----
1
create_clock clk -name clock -period 21.000000
Warning: Can't find object 'clk' in design 'CSA64EQG'. (UID-95)
Error: Value for list 'source_objects' must have 1 elements.
(CMD-036)
0
set_propagated_clock clock
Information: set_input_delay values are added to the propagated
clock skew. (TIM-113)
1
set_clock_uncertainty 0.25 clock
1
set_propagated_clock clock
Information: set_input_delay values are added to the propagated
clock skew. (TIM-113)
1
update_timing
Information: Updating design information... (UID-85)
Information: Input delay ('fall') on clock port 'clock' will be
added to the clock's propagated skew. (TIM-112)
Information: Input delay ('rise') on clock port 'clock' will be
added to the clock's propagated skew. (TIM-112)
1
report -cell
report_cell

```

```
*****
Report : cell
Design : CSA64EQG
Version: C-2009.06-SP5
Date   : Thu Dec  3 10:07:32 2015
*****
```

Attributes:

- b - black box (unknown)
- h - hierarchical
- n - noncombinational
- r - removable
- u - contains unmapped logic

Cell	Area	Attributes	Reference	Library
------	------	------------	-----------	---------

U3	CIVX2	tc240c
1.000000		
U4	CDLY1XL	tc240c
3.500000		
U5	CNIVX1	tc240c
1.000000		
U6	CDLY1XL	tc240c
3.500000		
U7	CNIVX1	tc240c
1.000000		
U8	CDLY1XL	tc240c
3.500000		
U9	CNIVX1	tc240c
1.000000		
U10	CDLY1XL	tc240c
3.500000		
U11	CNIVX1	tc240c
1.000000		
U12	CDLY1XL	tc240c
3.500000		
U13	CNIVX1	tc240c
1.000000		
U14	CDLY1XL	tc240c
3.500000		
U15	CNIVX1	tc240c
1.000000		
U16	CDLY1XL	tc240c
3.500000		
U17	CNIVX1	tc240c
1.000000		
U18	CDLY1XL	tc240c
3.500000		
U19	CNIVX1	tc240c
1.000000		
U20	CDLY1XL	tc240c
3.500000		
U21	CNIVX1	tc240c
1.000000		
U22	CDLY1XL	tc240c
3.500000		
U23	CNIVX1	tc240c
1.000000		
U24	CDLY1XL	tc240c
3.500000		

U25	CNIVX1	tc240c
1.000000		
U26	CDLY1XL	tc240c
3.500000		
U27	CNIVX1	tc240c
1.000000		
U28	CDLY1XL	tc240c
3.500000		
U29	CNIVX1	tc240c
1.000000		
U30	CDLY1XL	tc240c
3.500000		
U31	CNIVX1	tc240c
1.000000		
U32	CDLY1XL	tc240c
3.500000		
U33	CNIVX1	tc240c
1.000000		
U34	CDLY1XL	tc240c
3.500000		
U35	CNIVX1	tc240c
1.000000		
U36	CDLY1XL	tc240c
3.500000		
U37	CNIVX1	tc240c
1.000000		
U38	CDLY1XL	tc240c
3.500000		
U39	CNIVX1	tc240c
1.000000		
U40	CDLY1XL	tc240c
3.500000		
U41	CNIVX1	tc240c
1.000000		
U42	CDLY1XL	tc240c
3.500000		
U43	CNIVX1	tc240c
1.000000		
U44	CDLY1XL	tc240c
3.500000		
U45	CNIVX1	tc240c
1.000000		
U46	CDLY1XL	tc240c
3.500000		
U47	CNIVX1	tc240c
1.000000		

U48	CDLY1XL	tc240c
3.500000		
U49	CNIVX1	tc240c
1.000000		
U50	CDLY1XL	tc240c
3.500000		
U51	CNIVX1	tc240c
1.000000		
U52	CDLY1XL	tc240c
3.500000		
U53	CNIVX1	tc240c
1.000000		
U54	CDLY1XL	tc240c
3.500000		
U55	CNIVX1	tc240c
1.000000		
U56	CDLY1XL	tc240c
3.500000		
U57	CNIVX1	tc240c
1.000000		
U58	CDLY1XL	tc240c
3.500000		
U59	CNIVX1	tc240c
1.000000		
U60	CDLY1XL	tc240c
3.500000		
U61	CNIVX1	tc240c
1.000000		
U62	CDLY1XL	tc240c
3.500000		
U63	CNIVX1	tc240c
1.000000		
U64	CDLY1XL	tc240c
3.500000		
U65	CNIVX1	tc240c
1.000000		
U66	CDLY1XL	tc240c
3.500000		
U67	CNIVX1	tc240c
1.000000		
U68	CDLY1XL	tc240c
3.500000		
U69	CNIVX1	tc240c
1.000000		
U70	CDLY1XL	tc240c
3.500000		

U71	CNIVX1	tc240c
1.000000		
U72	CDLY1XL	tc240c
3.500000		
U73	CNIVX1	tc240c
1.000000		
U74	CDLY1XL	tc240c
3.500000		
U75	CNIVX1	tc240c
1.000000		
U76	CDLY1XL	tc240c
3.500000		
U77	CNIVX1	tc240c
1.000000		
U78	CDLY1XL	tc240c
3.500000		
U79	CNIVX1	tc240c
1.000000		
U80	CDLY1XL	tc240c
3.500000		
U81	CNIVX1	tc240c
1.000000		
U82	CDLY1XL	tc240c
3.500000		
U83	CNIVX1	tc240c
1.000000		
U84	CDLY1XL	tc240c
3.500000		
U85	CNIVX1	tc240c
1.000000		
U86	CDLY1XL	tc240c
3.500000		
U87	CNIVX1	tc240c
1.000000		
U88	CDLY1XL	tc240c
3.500000		
U89	CNIVX1	tc240c
1.000000		
U90	CDLY1XL	tc240c
3.500000		
U91	CNIVX1	tc240c
1.000000		
U92	CDLY1XL	tc240c
3.500000		
U93	CNIVX1	tc240c
1.000000		

U94	CDLY1XL	tc240c
3.500000		
U95	CNIVX1	tc240c
1.000000		
U96	CDLY1XL	tc240c
3.500000		
U97	CNIVX1	tc240c
1.000000		
U98	CDLY1XL	tc240c
3.500000		
U99	CNIVX1	tc240c
1.000000		
U100	CDLY1XL	tc240c
3.500000		
U101	CNIVX1	tc240c
1.000000		
U102	CDLY1XL	tc240c
3.500000		
U103	CNIVX1	tc240c
1.000000		
U104	CDLY1XL	tc240c
3.500000		
U105	CNIVX1	tc240c
1.000000		
U106	CDLY1XL	tc240c
3.500000		
U107	CNIVX1	tc240c
1.000000		
U108	CDLY1XL	tc240c
3.500000		
U109	CNIVX1	tc240c
1.000000		
U110	CDLY1XL	tc240c
3.500000		
U111	CNIVX1	tc240c
1.000000		
U112	CDLY1XL	tc240c
3.500000		
U113	CNIVX1	tc240c
1.000000		
U114	CDLY1XL	tc240c
3.500000		
U115	CNIVX1	tc240c
1.000000		
U116	CDLY1XL	tc240c
3.500000		

U117	CNIVX1	tc240c
1.000000		
U118	CDLY1XL	tc240c
3.500000		
U119	CNIVX1	tc240c
1.000000		
U120	CDLY1XL	tc240c
3.500000		
U121	CNIVX1	tc240c
1.000000		
U122	CDLY1XL	tc240c
3.500000		
U123	CNIVX1	tc240c
1.000000		
U124	CDLY1XL	tc240c
3.500000		
U125	CNIVX1	tc240c
1.000000		
U126	CDLY1XL	tc240c
3.500000		
U127	CNIVX1	tc240c
1.000000		
U128	CDLY1XL	tc240c
3.500000		
U129	CNIVX1	tc240c
1.000000		
U130	CDLY1XL	tc240c
3.500000		
U131	CNIVX1	tc240c
1.000000		
U132	CDLY1XL	tc240c
3.500000		
U133	CNIVX1	tc240c
1.000000		
U134	CDLY1XL	tc240c
3.500000		
U135	CNIVX1	tc240c
1.000000		
U136	CDLY1XL	tc240c
3.500000		
U137	CNIVX1	tc240c
1.000000		
U138	CDLY1XL	tc240c
3.500000		
U139	CNIVX1	tc240c
1.000000		

U140	CDLY1XL	tc240c
3.500000		
U141	CNIVX1	tc240c
1.000000		
U142	CDLY1XL	tc240c
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U143	CNIVX1	tc240c
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U144	CDLY1XL	tc240c
3.500000		
U145	CNIVX1	tc240c
1.000000		
U146	CDLY1XL	tc240c
3.500000		
U147	CNIVX1	tc240c
1.000000		
U148	CDLY1XL	tc240c
3.500000		
U149	CNIVX1	tc240c
1.000000		
U150	CDLY1XL	tc240c
3.500000		
U151	CNIVX1	tc240c
1.000000		
U152	CDLY1XL	tc240c
3.500000		
U153	CNIVX1	tc240c
1.000000		
U154	CDLY1XL	tc240c
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U155	CNIVX1	tc240c
1.000000		
U156	CDLY1XL	tc240c
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U157	CNIVX1	tc240c
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U158	CDLY1XL	tc240c
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U159	CNIVX1	tc240c
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U160	CDLY1XL	tc240c
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U161	CNIVX1	tc240c
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U162	CDLY1XL	tc240c
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U163	CNIVX1	tc240c
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U164	CDLY1XL	tc240c
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U165	CNIVX1	tc240c
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U166	CDLY1XL	tc240c
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U167	CNIVX1	tc240c
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U168	CDLY1XL	tc240c
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U169	CNIVX1	tc240c
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U170	CDLY1XL	tc240c
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U171	CNIVX1	tc240c
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U172	CDLY1XL	tc240c
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U173	CNIVX1	tc240c
1.000000		
U174	CDLY1XL	tc240c
3.500000		
U175	CNIVX1	tc240c
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U176	CDLY1XL	tc240c
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1.000000		
U178	CDLY1XL	tc240c
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U182	CDLY1XL	tc240c
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U183	CNIVX1	tc240c
1.000000		
U184	CDLY1XL	tc240c
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U185	CNIVX1	tc240c
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U186	CDLY1XL	tc240c
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U187	CNIVX1	tc240c
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U188	CDLY1XL	tc240c
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U192	CDLY1XL	tc240c
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U193	CNIVX1	tc240c
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U194	CDLY1XL	tc240c
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U195	CNIVX1	tc240c
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U196	CDLY1XL	tc240c
3.500000		
U197	CNIVX1	tc240c
1.000000		
U198	CDLY1XL	tc240c
3.500000		
U199	CNIVX1	tc240c
1.000000		
U200	CDLY1XL	tc240c
3.500000		
U201	CNIVX1	tc240c
1.000000		
U202	CDLY1XL	tc240c
3.500000		
U203	CNIVX1	tc240c
1.000000		
U204	CDLY1XL	tc240c
3.500000		
U205	CNIVX1	tc240c
1.000000		
U206	CDLY1XL	tc240c
3.500000		
U207	CNIVX1	tc240c
1.000000		
U208	CDLY1XL	tc240c
3.500000		

U209	CNIVX1	tc240c
1.000000		
U210	CDLY1XL	tc240c
3.500000		
U211	CNIVX1	tc240c
1.000000		
U212	CDLY1XL	tc240c
3.500000		
U213	CNIVX1	tc240c
1.000000		
U214	CDLY1XL	tc240c
3.500000		
U215	CNIVX1	tc240c
1.000000		
U216	CDLY1XL	tc240c
3.500000		
U217	CNIVX1	tc240c
1.000000		
U218	CDLY1XL	tc240c
3.500000		
U219	CNIVX1	tc240c
1.000000		
U220	CDLY1XL	tc240c
3.500000		
U221	CNIVX1	tc240c
1.000000		
U222	CDLY1XL	tc240c
3.500000		
U223	CNIVX1	tc240c
1.000000		
U224	CDLY1XL	tc240c
3.500000		
U225	CNIVX1	tc240c
1.000000		
U226	CDLY1XL	tc240c
3.500000		
U227	CNIVX1	tc240c
1.000000		
U228	CDLY1XL	tc240c
3.500000		
U229	CNIVX1	tc240c
1.000000		
U230	CDLY1XL	tc240c
3.500000		
U231	CNIVX1	tc240c
1.000000		

U232	CDLY1XL	tc240c
3.500000		
U233	CNIVX1	tc240c
1.000000		
U234	CDLY1XL	tc240c
3.500000		
U235	CNIVX1	tc240c
1.000000		
U236	CDLY1XL	tc240c
3.500000		
U237	CNIVX1	tc240c
1.000000		
U238	CDLY1XL	tc240c
3.500000		
U239	CNIVX1	tc240c
1.000000		
U240	CDLY1XL	tc240c
3.500000		
U241	CNIVX1	tc240c
1.000000		
U242	CDLY1XL	tc240c
3.500000		
U243	CNIVX1	tc240c
1.000000		
U244	CDLY1XL	tc240c
3.500000		
U245	CNIVX1	tc240c
1.000000		
U246	CDLY1XL	tc240c
3.500000		
U247	CNIVX1	tc240c
1.000000		
U248	CDLY1XL	tc240c
3.500000		
U249	CNIVX1	tc240c
1.000000		
U250	CDLY1XL	tc240c
3.500000		
U251	CNIVX1	tc240c
1.000000		
U252	CDLY1XL	tc240c
3.500000		
U253	CNIVX1	tc240c
1.000000		
U254	CDLY1XL	tc240c
3.500000		

U255	CNIVX1	tc240c
1.000000		
U256	CDLY1XL	tc240c
3.500000		
U257	CNIVX1	tc240c
1.000000		
U258	CDLY1XL	tc240c
3.500000		
U259	CNIVX1	tc240c
1.000000		
U260	CDLY2X2	tc240c
7.000000		
U261	CDLY2X2	tc240c
7.000000		
U262	CDLY2X2	tc240c
7.000000		
U263	CDLY2X2	tc240c
7.000000		
U264	CDLY2X2	tc240c
7.000000		
U265	CDLY2X2	tc240c
7.000000		
U266	CDLY2X2	tc240c
7.000000		
U267	CDLY2X2	tc240c
7.000000		
U268	CDLY2X2	tc240c
7.000000		
U269	CDLY2X2	tc240c
7.000000		
U270	CDLY2X2	tc240c
7.000000		
U271	CDLY2X2	tc240c
7.000000		
U272	CDLY2X2	tc240c
7.000000		
U273	CDLY2X2	tc240c
7.000000		
U274	CDLY2X2	tc240c
7.000000		
U275	CDLY2X2	tc240c
7.000000		
U276	CDLY2X2	tc240c
7.000000		
crout_reg	CFD2QXL	tc240c
5.000000 n		

op1f_reg[0]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[1]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[2]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[3]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[4]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[5]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[6]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[7]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[8]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[9]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[10]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[11]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[12]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[13]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[14]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[15]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[16]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[17]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[18]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[19]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[20]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[21]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[22]	CFD2QX1	tc240c
7.000000 n		

op1f_reg[23]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[24]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[25]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[26]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[27]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[28]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[29]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[30]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[31]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[32]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[33]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[34]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[35]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[36]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[37]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[38]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[39]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[40]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[41]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[42]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[43]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[44]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[45]	CFD2QX1	tc240c
7.000000 n		

op1f_reg[46]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[47]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[48]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[49]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[50]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[51]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[52]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[53]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[54]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[55]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[56]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[57]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[58]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[59]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[60]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[61]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[62]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[63]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[0]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[1]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[2]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[3]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[4]	CFD2QX1	tc240c
7.000000 n		

op2f_reg[5]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[6]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[7]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[8]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[9]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[10]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[11]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[12]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[13]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[14]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[15]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[16]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[17]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[18]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[19]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[20]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[21]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[22]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[23]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[24]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[25]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[26]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[27]	CFD2QX1	tc240c
7.000000 n		

op2f_reg[28]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[29]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[30]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[31]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[32]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[33]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[34]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[35]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[36]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[37]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[38]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[39]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[40]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[41]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[42]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[43]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[44]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[45]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[46]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[47]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[48]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[49]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[50]	CFD2QX1	tc240c
7.000000 n		

op2f_reg[51]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[52]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[53]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[54]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[55]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[56]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[57]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[58]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[59]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[60]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[61]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[62]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[63]	CFD2QXL	tc240c
5.000000 n		
s1		CSA4_0
140.500000		
 h		
s2		CSA4_15
116.000000		
 h		
s3		CSA4_14
82.500000 h		
s4		CSA4_13
72.500000 h		
s5		CSA4_12
72.500000 h		
s6		CSA4_11
81.000000 h		
s7		CSA4_10
66.500000 h		
s8		CSA4_9
70.000000 h		

s9		CSA4_8
67.500000 h		
s10		CSA4_7
71.500000 h		
s11		CSA4_6
66.500000 h		
s12		CSA4_5
70.000000 h		
s13		CSA4_4
69.000000 h		
s14		CSA4_3
70.000000 h		
s15		CSA4_2
70.500000 h		
s16		CSA4_1
83.000000 h		
sum_reg[0]	CFD2QX1	tc240c
7.000000 n		
sum_reg[1]	CFD2QX1	tc240c
7.000000 n		
sum_reg[2]	CFD2QX1	tc240c
7.000000 n		
sum_reg[3]	CFD2QX1	tc240c
7.000000 n		
sum_reg[4]	CFD2QXL	tc240c
5.000000 n		
sum_reg[5]	CFD2QXL	tc240c
5.000000 n		
sum_reg[6]	CFD2QXL	tc240c
5.000000 n		
sum_reg[7]	CFD2QXL	tc240c
5.000000 n		
sum_reg[8]	CFD2QX1	tc240c
7.000000 n		
sum_reg[9]	CFD2QX1	tc240c
7.000000 n		
sum_reg[10]	CFD2QX1	tc240c
7.000000 n		
sum_reg[11]	CFD2QX1	tc240c
7.000000 n		
sum_reg[12]	CFD2QX1	tc240c
7.000000 n		
sum_reg[13]	CFD2QX1	tc240c
7.000000 n		
sum_reg[14]	CFD2QX1	tc240c
7.000000 n		

sum_reg[15]	CFD2QX1	tc240c
7.000000 n		
sum_reg[16]	CFD2QX1	tc240c
7.000000 n		
sum_reg[17]	CFD2QX1	tc240c
7.000000 n		
sum_reg[18]	CFD2QX1	tc240c
7.000000 n		
sum_reg[19]	CFD2QX1	tc240c
7.000000 n		
sum_reg[20]	CFD2QX1	tc240c
7.000000 n		
sum_reg[21]	CFD2QX1	tc240c
7.000000 n		
sum_reg[22]	CFD2QX1	tc240c
7.000000 n		
sum_reg[23]	CFD2QX1	tc240c
7.000000 n		
sum_reg[24]	CFD2QX1	tc240c
7.000000 n		
sum_reg[25]	CFD2QX1	tc240c
7.000000 n		
sum_reg[26]	CFD2QX1	tc240c
7.000000 n		
sum_reg[27]	CFD2QX1	tc240c
7.000000 n		
sum_reg[28]	CFD2QX1	tc240c
7.000000 n		
sum_reg[29]	CFD2QX1	tc240c
7.000000 n		
sum_reg[30]	CFD2QX1	tc240c
7.000000 n		
sum_reg[31]	CFD2QX1	tc240c
7.000000 n		
sum_reg[32]	CFD2QX1	tc240c
7.000000 n		
sum_reg[33]	CFD2QX1	tc240c
7.000000 n		
sum_reg[34]	CFD2QX1	tc240c
7.000000 n		
sum_reg[35]	CFD2QX1	tc240c
7.000000 n		
sum_reg[36]	CFD2QX1	tc240c
7.000000 n		
sum_reg[37]	CFD2QX1	tc240c
7.000000 n		

sum_reg[38]	CFD2QX1	tc240c
7.000000 n		
sum_reg[39]	CFD2QX1	tc240c
7.000000 n		
sum_reg[40]	CFD2QX1	tc240c
7.000000 n		
sum_reg[41]	CFD2QX1	tc240c
7.000000 n		
sum_reg[42]	CFD2QX1	tc240c
7.000000 n		
sum_reg[43]	CFD2QX1	tc240c
7.000000 n		
sum_reg[44]	CFD2QXL	tc240c
5.000000 n		
sum_reg[45]	CFD2QXL	tc240c
5.000000 n		
sum_reg[46]	CFD2QXL	tc240c
5.000000 n		
sum_reg[47]	CFD2QXL	tc240c
5.000000 n		
sum_reg[48]	CFD2QX1	tc240c
7.000000 n		
sum_reg[49]	CFD2QX1	tc240c
7.000000 n		
sum_reg[50]	CFD2QX1	tc240c
7.000000 n		
sum_reg[51]	CFD2QX1	tc240c
7.000000 n		
sum_reg[52]	CFD2QX1	tc240c
7.000000 n		
sum_reg[53]	CFD2QX1	tc240c
7.000000 n		
sum_reg[54]	CFD2QX1	tc240c
7.000000 n		
sum_reg[55]	CFD2QX1	tc240c
7.000000 n		
sum_reg[56]	CFD2QX1	tc240c
7.000000 n		
sum_reg[57]	CFD2QX1	tc240c
7.000000 n		
sum_reg[58]	CFD2QX1	tc240c
7.000000 n		
sum_reg[59]	CFD2QX1	tc240c
7.000000 n		
sum_reg[60]	CFD2QXL	tc240c
5.000000 n		

```

sum_reg[61]          CFD2QXL      tc240c
5.000000  n
sum_reg[62]          CFD2QXL      tc240c
5.000000  n
sum_reg[63]          CFD2QXL      tc240c
5.000000  n
-----
-----
Total                483          cells
3288.500000
1
report_timing -max_paths 5

```

```

*****
Report : timing
    -path full
    -delay max
    -max_paths 5
Design : CSA64EQG
Version: C-2009.06-SP5
Date   : Thu Dec  3 10:07:32 2015
*****

```

Operating Conditions: WCCOM25 Library: tc240c
Wire Load Model Mode: top

```

Startpoint: op1f_reg[0]
            (rising edge-triggered flip-flop clocked by clock)
Endpoint: sum_reg[61]
            (rising edge-triggered flip-flop clocked by clock)
Path Group: clock
Path Type: max

```

Point	Incr	Path
clock clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.00	0.00
op1f_reg[0]/CP (CFD2QX1)	0.00	0.00 r
op1f_reg[0]/Q (CFD2QX1)	0.48	0.48 r
s1/op1_4[0] (CSA4_0)	0.00	0.48 r
s1/f5/op1_fa (FA_124)	0.00	0.48 r
s1/f5/U2/Z (CENX1)	0.29	0.78 r
s1/f5/U4/Z (CND2X2)	0.14	0.91 f
s1/f5/U6/Z (CND2X2)	0.11	1.02 r
s1/f5/cout_fa (FA_124)	0.00	1.02 r
s1/f6/cin (FA_123)	0.00	1.02 r
s1/f6/U2/Z (CENX2)	0.20	1.23 r

s1/f6/U4/Z (CAOR2X1)	0.31	1.53	r
s1/f6/cout_fa (FA_123)	0.00	1.53	r
s1/f7/cin (FA_122)	0.00	1.53	r
s1/f7/U1/Z (CENX2)	0.24	1.78	r
s1/f7/U3/Z (CND2X2)	0.13	1.91	f
s1/f7/U5/Z (CND2X2)	0.11	2.02	r
s1/f7/cout_fa (FA_122)	0.00	2.02	r
s1/f8/cin (FA_121)	0.00	2.02	r
s1/f8/U2/Z (CENX2)	0.11	2.13	f
s1/f8/U5/Z (CAOR2X1)	0.28	2.41	f
s1/f8/cout_fa (FA_121)	0.00	2.41	f
s1/m2/cout1 (mux_carry_0)	0.00	2.41	f
s1/m2/U1/Z (CAOR2X1)	0.38	2.80	f
s1/m2/cout (mux_carry_0)	0.00	2.80	f
s1/cout_4 (CSA4_0)	0.00	2.80	f
s2/cin_4 (CSA4_15)	0.00	2.80	f
s2/m2/Cin (mux_carry_15)	0.00	2.80	f
s2/m2/U2/Z (CND2X1)	0.12	2.92	r
s2/m2/U3/Z (CND2X2)	0.12	3.04	f
s2/m2/cout (mux_carry_15)	0.00	3.04	f
s2/cout_4 (CSA4_15)	0.00	3.04	f
s3/cin_4 (CSA4_14)	0.00	3.04	f
s3/m2/Cin (mux_carry_14)	0.00	3.04	f
s3/m2/U4/Z (CIVX2)	0.07	3.11	r
s3/m2/U2/Z (CND2X2)	0.09	3.20	f
s3/m2/U3/Z (CND2X2)	0.08	3.28	r
s3/m2/cout (mux_carry_14)	0.00	3.28	r
s3/cout_4 (CSA4_14)	0.00	3.28	r
s4/cin_4 (CSA4_13)	0.00	3.28	r
s4/m2/Cin (mux_carry_13)	0.00	3.28	r
s4/m2/U4/Z (CIVX2)	0.07	3.35	f
s4/m2/U2/Z (CND2X2)	0.07	3.42	r
s4/m2/U3/Z (CND2X2)	0.11	3.53	f
s4/m2/cout (mux_carry_13)	0.00	3.53	f
s4/cout_4 (CSA4_13)	0.00	3.53	f
s5/cin_4 (CSA4_12)	0.00	3.53	f
s5/m2/Cin (mux_carry_12)	0.00	3.53	f
s5/m2/U1/Z (CND2X1)	0.12	3.65	r
s5/m2/U3/Z (CND2X2)	0.12	3.77	f
s5/m2/cout (mux_carry_12)	0.00	3.77	f
s5/cout_4 (CSA4_12)	0.00	3.77	f
s6/cin_4 (CSA4_11)	0.00	3.77	f
s6/m2/Cin (mux_carry_11)	0.00	3.77	f
s6/m2/U3/Z (CIVX2)	0.07	3.84	r
s6/m2/U4/Z (CND2X2)	0.09	3.93	f
s6/m2/U5/Z (CND2X2)	0.10	4.03	r
s6/m2/cout (mux_carry_11)	0.00	4.03	r

s6/cout_4 (CSA4_11)	0.00	4.03	r
s7/cin_4 (CSA4_10)	0.00	4.03	r
s7/m2/Cin (mux_carry_10)	0.00	4.03	r
s7/m2/U2/Z (CIVX2)	0.07	4.10	f
s7/m2/U1/Z (CAOR2X1)	0.31	4.40	f
s7/m2/cout (mux_carry_10)	0.00	4.40	f
s7/cout_4 (CSA4_10)	0.00	4.40	f
s8/cin_4 (CSA4_9)	0.00	4.40	f
s8/m2/Cin (mux_carry_9)	0.00	4.40	f
s8/m2/U2/Z (CIVX1)	0.07	4.47	r
s8/m2/U1/Z (CAOR2X1)	0.21	4.68	r
s8/m2/cout (mux_carry_9)	0.00	4.68	r
s8/cout_4 (CSA4_9)	0.00	4.68	r
s9/cin_4 (CSA4_8)	0.00	4.68	r
s9/m2/Cin (mux_carry_8)	0.00	4.68	r
s9/m2/U2/Z (CIVXL)	0.10	4.78	f
s9/m2/U1/Z (CAOR2X1)	0.32	5.10	f
s9/m2/cout (mux_carry_8)	0.00	5.10	f
s9/cout_4 (CSA4_8)	0.00	5.10	f
s10/cin_4 (CSA4_7)	0.00	5.10	f
s10/m2/Cin (mux_carry_7)	0.00	5.10	f
s10/m2/U4/Z (CIVXL)	0.11	5.21	r
s10/m2/U2/Z (CND2X1)	0.14	5.35	f
s10/m2/U3/Z (CND2X2)	0.12	5.47	r
s10/m2/cout (mux_carry_7)	0.00	5.47	r
s10/cout_4 (CSA4_7)	0.00	5.47	r
s11/cin_4 (CSA4_6)	0.00	5.47	r
s11/m2/Cin (mux_carry_6)	0.00	5.47	r
s11/m2/U2/Z (CIVX2)	0.07	5.54	f
s11/m2/U1/Z (CAOR2X1)	0.33	5.87	f
s11/m2/cout (mux_carry_6)	0.00	5.87	f
s11/cout_4 (CSA4_6)	0.00	5.87	f
s12/cin_4 (CSA4_5)	0.00	5.87	f
s12/m2/Cin (mux_carry_5)	0.00	5.87	f
s12/m2/U1/Z (CND2X1)	0.12	6.00	r
s12/m2/U3/Z (CND2X2)	0.15	6.14	f
s12/m2/cout (mux_carry_5)	0.00	6.14	f
s12/cout_4 (CSA4_5)	0.00	6.14	f
s13/cin_4 (CSA4_4)	0.00	6.14	f
s13/m2/Cin (mux_carry_4)	0.00	6.14	f
s13/m2/U4/Z (CIVX2)	0.07	6.22	r
s13/m2/U2/Z (CND2X2)	0.09	6.31	f
s13/m2/U3/Z (CND2X2)	0.10	6.41	r
s13/m2/cout (mux_carry_4)	0.00	6.41	r
s13/cout_4 (CSA4_4)	0.00	6.41	r
s14/cin_4 (CSA4_3)	0.00	6.41	r
s14/m2/Cin (mux_carry_3)	0.00	6.41	r

s14/m2/U4/Z (CIVX2)	0.08	6.48	f
s14/m2/U3/Z (CND2X2)	0.07	6.56	r
s14/m2/U1/Z (CND2X2)	0.13	6.69	f
s14/m2/cout (mux_carry_3)	0.00	6.69	f
s14/cout_4 (CSA4_3)	0.00	6.69	f
s15/cin_4 (CSA4_2)	0.00	6.69	f
s15/m2/Cin (mux_carry_2)	0.00	6.69	f
s15/m2/U2/Z (CIVX2)	0.07	6.76	r
s15/m2/U3/Z (CND2X2)	0.12	6.88	f
s15/m2/U4/Z (CND2X4)	0.11	6.98	r
s15/m2/cout (mux_carry_2)	0.00	6.98	r
s15/cout_4 (CSA4_2)	0.00	6.98	r
s16/cin_4 (CSA4_1)	0.00	6.98	r
s16/m1/Cin (mux_sum_1)	0.00	6.98	r
s16/m1/U5/Z (CIVX2)	0.08	7.06	f
s16/m1/U3/Z (CAOR2X1)	0.27	7.33	f
s16/m1/sum[1] (mux_sum_1)	0.00	7.33	f
s16/sum_4[1] (CSA4_1)	0.00	7.33	f
sum_reg[61]/D (CFD2QXL)	0.00	7.33	f
data arrival time		7.33	
clock clock (rise edge)	8.00	8.00	
clock network delay (propagated)	0.00	8.00	
clock uncertainty	-0.25	7.75	
sum_reg[61]/CP (CFD2QXL)	0.00	7.75	r
library setup time	-0.37	7.38	
data required time		7.38	

data required time		7.38	
data arrival time		-7.33	

slack (MET)		0.05	

Startpoint: op1f_reg[0]
 (rising edge-triggered flip-flop clocked by clock)
 Endpoint: sum_reg[62]
 (rising edge-triggered flip-flop clocked by clock)
 Path Group: clock
 Path Type: max

Point	Incr	Path
clock clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.00	0.00
op1f_reg[0]/CP (CFD2QX1)	0.00	0.00 r
op1f_reg[0]/Q (CFD2QX1)	0.48	0.48 r

s1/op1_4[0] (CSA4_0)	0.00	0.48	r
s1/f5/op1_fa (FA_124)	0.00	0.48	r
s1/f5/U2/Z (CENX1)	0.29	0.78	r
s1/f5/U4/Z (CND2X2)	0.14	0.91	f
s1/f5/U6/Z (CND2X2)	0.11	1.02	r
s1/f5/cout_fa (FA_124)	0.00	1.02	r
s1/f6/cin_fa (FA_123)	0.00	1.02	r
s1/f6/U2/Z (CENX2)	0.20	1.23	r
s1/f6/U4/Z (CAOR2X1)	0.31	1.53	r
s1/f6/cout_fa (FA_123)	0.00	1.53	r
s1/f7/cin_fa (FA_122)	0.00	1.53	r
s1/f7/U1/Z (CENX2)	0.24	1.78	r
s1/f7/U3/Z (CND2X2)	0.13	1.91	f
s1/f7/U5/Z (CND2X2)	0.11	2.02	r
s1/f7/cout_fa (FA_122)	0.00	2.02	r
s1/f8/cin_fa (FA_121)	0.00	2.02	r
s1/f8/U2/Z (CENX2)	0.11	2.13	f
s1/f8/U5/Z (CAOR2X1)	0.28	2.41	f
s1/f8/cout_fa (FA_121)	0.00	2.41	f
s1/m2/cout1 (mux_carry_0)	0.00	2.41	f
s1/m2/U1/Z (CAOR2X1)	0.38	2.80	f
s1/m2/cout (mux_carry_0)	0.00	2.80	f
s1/cout_4 (CSA4_0)	0.00	2.80	f
s2/cin_4 (CSA4_15)	0.00	2.80	f
s2/m2/Cin (mux_carry_15)	0.00	2.80	f
s2/m2/U2/Z (CND2X1)	0.12	2.92	r
s2/m2/U3/Z (CND2X2)	0.12	3.04	f
s2/m2/cout (mux_carry_15)	0.00	3.04	f
s2/cout_4 (CSA4_15)	0.00	3.04	f
s3/cin_4 (CSA4_14)	0.00	3.04	f
s3/m2/Cin (mux_carry_14)	0.00	3.04	f
s3/m2/U4/Z (CIVX2)	0.07	3.11	r
s3/m2/U2/Z (CND2X2)	0.09	3.20	f
s3/m2/U3/Z (CND2X2)	0.08	3.28	r
s3/m2/cout (mux_carry_14)	0.00	3.28	r
s3/cout_4 (CSA4_14)	0.00	3.28	r
s4/cin_4 (CSA4_13)	0.00	3.28	r
s4/m2/Cin (mux_carry_13)	0.00	3.28	r
s4/m2/U4/Z (CIVX2)	0.07	3.35	f
s4/m2/U2/Z (CND2X2)	0.07	3.42	r
s4/m2/U3/Z (CND2X2)	0.11	3.53	f
s4/m2/cout (mux_carry_13)	0.00	3.53	f
s4/cout_4 (CSA4_13)	0.00	3.53	f
s5/cin_4 (CSA4_12)	0.00	3.53	f
s5/m2/Cin (mux_carry_12)	0.00	3.53	f
s5/m2/U1/Z (CND2X1)	0.12	3.65	r
s5/m2/U3/Z (CND2X2)	0.12	3.77	f

s5/m2/cout (mux_carry_12)	0.00	3.77	f
s5/cout_4 (CSA4_12)	0.00	3.77	f
s6/cin_4 (CSA4_11)	0.00	3.77	f
s6/m2/Cin (mux_carry_11)	0.00	3.77	f
s6/m2/U3/Z (CIVX2)	0.07	3.84	r
s6/m2/U4/Z (CND2X2)	0.09	3.93	f
s6/m2/U5/Z (CND2X2)	0.10	4.03	r
s6/m2/cout (mux_carry_11)	0.00	4.03	r
s6/cout_4 (CSA4_11)	0.00	4.03	r
s7/cin_4 (CSA4_10)	0.00	4.03	r
s7/m2/Cin (mux_carry_10)	0.00	4.03	r
s7/m2/U2/Z (CIVX2)	0.07	4.10	f
s7/m2/U1/Z (CAOR2X1)	0.31	4.40	f
s7/m2/cout (mux_carry_10)	0.00	4.40	f
s7/cout_4 (CSA4_10)	0.00	4.40	f
s8/cin_4 (CSA4_9)	0.00	4.40	f
s8/m2/Cin (mux_carry_9)	0.00	4.40	f
s8/m2/U2/Z (CIVX1)	0.07	4.47	r
s8/m2/U1/Z (CAOR2X1)	0.21	4.68	r
s8/m2/cout (mux_carry_9)	0.00	4.68	r
s8/cout_4 (CSA4_9)	0.00	4.68	r
s9/cin_4 (CSA4_8)	0.00	4.68	r
s9/m2/Cin (mux_carry_8)	0.00	4.68	r
s9/m2/U2/Z (CIVXL)	0.10	4.78	f
s9/m2/U1/Z (CAOR2X1)	0.32	5.10	f
s9/m2/cout (mux_carry_8)	0.00	5.10	f
s9/cout_4 (CSA4_8)	0.00	5.10	f
s10/cin_4 (CSA4_7)	0.00	5.10	f
s10/m2/Cin (mux_carry_7)	0.00	5.10	f
s10/m2/U4/Z (CIVXL)	0.11	5.21	r
s10/m2/U2/Z (CND2X1)	0.14	5.35	f
s10/m2/U3/Z (CND2X2)	0.12	5.47	r
s10/m2/cout (mux_carry_7)	0.00	5.47	r
s10/cout_4 (CSA4_7)	0.00	5.47	r
s11/cin_4 (CSA4_6)	0.00	5.47	r
s11/m2/Cin (mux_carry_6)	0.00	5.47	r
s11/m2/U2/Z (CIVX2)	0.07	5.54	f
s11/m2/U1/Z (CAOR2X1)	0.33	5.87	f
s11/m2/cout (mux_carry_6)	0.00	5.87	f
s11/cout_4 (CSA4_6)	0.00	5.87	f
s12/cin_4 (CSA4_5)	0.00	5.87	f
s12/m2/Cin (mux_carry_5)	0.00	5.87	f
s12/m2/U1/Z (CND2X1)	0.12	6.00	r
s12/m2/U3/Z (CND2X2)	0.15	6.14	f
s12/m2/cout (mux_carry_5)	0.00	6.14	f
s12/cout_4 (CSA4_5)	0.00	6.14	f
s13/cin_4 (CSA4_4)	0.00	6.14	f

s13/m2/Cin (mux_carry_4)	0.00	6.14	f
s13/m2/U4/Z (CIVX2)	0.07	6.22	r
s13/m2/U2/Z (CND2X2)	0.09	6.31	f
s13/m2/U3/Z (CND2X2)	0.10	6.41	r
s13/m2/cout (mux_carry_4)	0.00	6.41	r
s13/cout_4 (CSA4_4)	0.00	6.41	r
s14/cin_4 (CSA4_3)	0.00	6.41	r
s14/m2/Cin (mux_carry_3)	0.00	6.41	r
s14/m2/U4/Z (CIVX2)	0.08	6.48	f
s14/m2/U3/Z (CND2X2)	0.07	6.56	r
s14/m2/U1/Z (CND2X2)	0.13	6.69	f
s14/m2/cout (mux_carry_3)	0.00	6.69	f
s14/cout_4 (CSA4_3)	0.00	6.69	f
s15/cin_4 (CSA4_2)	0.00	6.69	f
s15/m2/Cin (mux_carry_2)	0.00	6.69	f
s15/m2/U2/Z (CIVX2)	0.07	6.76	r
s15/m2/U3/Z (CND2X2)	0.12	6.88	f
s15/m2/U4/Z (CND2X4)	0.11	6.98	r
s15/m2/cout (mux_carry_2)	0.00	6.98	r
s15/cout_4 (CSA4_2)	0.00	6.98	r
s16/cin_4 (CSA4_1)	0.00	6.98	r
s16/m1/Cin (mux_sum_1)	0.00	6.98	r
s16/m1/U5/Z (CIVX2)	0.08	7.06	f
s16/m1/U2/Z (CAOR2X1)	0.27	7.33	f
s16/m1/sum[2] (mux_sum_1)	0.00	7.33	f
s16/sum_4[2] (CSA4_1)	0.00	7.33	f
sum_reg[62]/D (CFD2QXL)	0.00	7.33	f
data arrival time		7.33	
clock clock (rise edge)	8.00	8.00	
clock network delay (propagated)	0.00	8.00	
clock uncertainty	-0.25	7.75	
sum_reg[62]/CP (CFD2QXL)	0.00	7.75	r
library setup time	-0.37	7.38	
data required time		7.38	

data required time		7.38	
data arrival time		-7.33	

slack (MET)		0.05	

Startpoint: op1f_reg[0]
 (rising edge-triggered flip-flop clocked by clock)
 Endpoint: sum_reg[63]
 (rising edge-triggered flip-flop clocked by clock)
 Path Group: clock

Path Type: max

Point	Incr	Path
clock clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.00	0.00
op1f_reg[0]/CP (CFD2QX1)	0.00	0.00 r
op1f_reg[0]/Q (CFD2QX1)	0.48	0.48 r
s1/op1_4[0] (CSA4_0)	0.00	0.48 r
s1/f5/op1_fa (FA_124)	0.00	0.48 r
s1/f5/U2/Z (CENX1)	0.29	0.78 r
s1/f5/U4/Z (CND2X2)	0.14	0.91 f
s1/f5/U6/Z (CND2X2)	0.11	1.02 r
s1/f5/cout_fa (FA_124)	0.00	1.02 r
s1/f6/cin (FA_123)	0.00	1.02 r
s1/f6/U2/Z (CENX2)	0.20	1.23 r
s1/f6/U4/Z (CAOR2X1)	0.31	1.53 r
s1/f6/cout_fa (FA_123)	0.00	1.53 r
s1/f7/cin (FA_122)	0.00	1.53 r
s1/f7/U1/Z (CENX2)	0.24	1.78 r
s1/f7/U3/Z (CND2X2)	0.13	1.91 f
s1/f7/U5/Z (CND2X2)	0.11	2.02 r
s1/f7/cout_fa (FA_122)	0.00	2.02 r
s1/f8/cin (FA_121)	0.00	2.02 r
s1/f8/U2/Z (CENX2)	0.11	2.13 f
s1/f8/U5/Z (CAOR2X1)	0.28	2.41 f
s1/f8/cout_fa (FA_121)	0.00	2.41 f
s1/m2/cout1 (mux_carry_0)	0.00	2.41 f
s1/m2/U1/Z (CAOR2X1)	0.38	2.80 f
s1/m2/cout (mux_carry_0)	0.00	2.80 f
s1/cout_4 (CSA4_0)	0.00	2.80 f
s2/cin_4 (CSA4_15)	0.00	2.80 f
s2/m2/Cin (mux_carry_15)	0.00	2.80 f
s2/m2/U2/Z (CND2X1)	0.12	2.92 r
s2/m2/U3/Z (CND2X2)	0.12	3.04 f
s2/m2/cout (mux_carry_15)	0.00	3.04 f
s2/cout_4 (CSA4_15)	0.00	3.04 f
s3/cin_4 (CSA4_14)	0.00	3.04 f
s3/m2/Cin (mux_carry_14)	0.00	3.04 f
s3/m2/U4/Z (CIVX2)	0.07	3.11 r
s3/m2/U2/Z (CND2X2)	0.09	3.20 f
s3/m2/U3/Z (CND2X2)	0.08	3.28 r
s3/m2/cout (mux_carry_14)	0.00	3.28 r
s3/cout_4 (CSA4_14)	0.00	3.28 r
s4/cin_4 (CSA4_13)	0.00	3.28 r
s4/m2/Cin (mux_carry_13)	0.00	3.28 r
s4/m2/U4/Z (CIVX2)	0.07	3.35 f

s4/m2/U2/Z (CND2X2)	0.07	3.42	r
s4/m2/U3/Z (CND2X2)	0.11	3.53	f
s4/m2/cout (mux_carry_13)	0.00	3.53	f
s4/cout_4 (CSA4_13)	0.00	3.53	f
s5/cin_4 (CSA4_12)	0.00	3.53	f
s5/m2/Cin (mux_carry_12)	0.00	3.53	f
s5/m2/U1/Z (CND2X1)	0.12	3.65	r
s5/m2/U3/Z (CND2X2)	0.12	3.77	f
s5/m2/cout (mux_carry_12)	0.00	3.77	f
s5/cout_4 (CSA4_12)	0.00	3.77	f
s6/cin_4 (CSA4_11)	0.00	3.77	f
s6/m2/Cin (mux_carry_11)	0.00	3.77	f
s6/m2/U3/Z (CIVX2)	0.07	3.84	r
s6/m2/U4/Z (CND2X2)	0.09	3.93	f
s6/m2/U5/Z (CND2X2)	0.10	4.03	r
s6/m2/cout (mux_carry_11)	0.00	4.03	r
s6/cout_4 (CSA4_11)	0.00	4.03	r
s7/cin_4 (CSA4_10)	0.00	4.03	r
s7/m2/Cin (mux_carry_10)	0.00	4.03	r
s7/m2/U2/Z (CIVX2)	0.07	4.10	f
s7/m2/U1/Z (CAOR2X1)	0.31	4.40	f
s7/m2/cout (mux_carry_10)	0.00	4.40	f
s7/cout_4 (CSA4_10)	0.00	4.40	f
s8/cin_4 (CSA4_9)	0.00	4.40	f
s8/m2/Cin (mux_carry_9)	0.00	4.40	f
s8/m2/U2/Z (CIVX1)	0.07	4.47	r
s8/m2/U1/Z (CAOR2X1)	0.21	4.68	r
s8/m2/cout (mux_carry_9)	0.00	4.68	r
s8/cout_4 (CSA4_9)	0.00	4.68	r
s9/cin_4 (CSA4_8)	0.00	4.68	r
s9/m2/Cin (mux_carry_8)	0.00	4.68	r
s9/m2/U2/Z (CIVXL)	0.10	4.78	f
s9/m2/U1/Z (CAOR2X1)	0.32	5.10	f
s9/m2/cout (mux_carry_8)	0.00	5.10	f
s9/cout_4 (CSA4_8)	0.00	5.10	f
s10/cin_4 (CSA4_7)	0.00	5.10	f
s10/m2/Cin (mux_carry_7)	0.00	5.10	f
s10/m2/U4/Z (CIVXL)	0.11	5.21	r
s10/m2/U2/Z (CND2X1)	0.14	5.35	f
s10/m2/U3/Z (CND2X2)	0.12	5.47	r
s10/m2/cout (mux_carry_7)	0.00	5.47	r
s10/cout_4 (CSA4_7)	0.00	5.47	r
s11/cin_4 (CSA4_6)	0.00	5.47	r
s11/m2/Cin (mux_carry_6)	0.00	5.47	r
s11/m2/U2/Z (CIVX2)	0.07	5.54	f
s11/m2/U1/Z (CAOR2X1)	0.33	5.87	f
s11/m2/cout (mux_carry_6)	0.00	5.87	f

s11/cout_4 (CSA4_6)	0.00	5.87	f
s12/cin_4 (CSA4_5)	0.00	5.87	f
s12/m2/Cin (mux_carry_5)	0.00	5.87	f
s12/m2/U1/Z (CND2X1)	0.12	6.00	r
s12/m2/U3/Z (CND2X2)	0.15	6.14	f
s12/m2/cout (mux_carry_5)	0.00	6.14	f
s12/cout_4 (CSA4_5)	0.00	6.14	f
s13/cin_4 (CSA4_4)	0.00	6.14	f
s13/m2/Cin (mux_carry_4)	0.00	6.14	f
s13/m2/U4/Z (CIVX2)	0.07	6.22	r
s13/m2/U2/Z (CND2X2)	0.09	6.31	f
s13/m2/U3/Z (CND2X2)	0.10	6.41	r
s13/m2/cout (mux_carry_4)	0.00	6.41	r
s13/cout_4 (CSA4_4)	0.00	6.41	r
s14/cin_4 (CSA4_3)	0.00	6.41	r
s14/m2/Cin (mux_carry_3)	0.00	6.41	r
s14/m2/U4/Z (CIVX2)	0.08	6.48	f
s14/m2/U3/Z (CND2X2)	0.07	6.56	r
s14/m2/U1/Z (CND2X2)	0.13	6.69	f
s14/m2/cout (mux_carry_3)	0.00	6.69	f
s14/cout_4 (CSA4_3)	0.00	6.69	f
s15/cin_4 (CSA4_2)	0.00	6.69	f
s15/m2/Cin (mux_carry_2)	0.00	6.69	f
s15/m2/U2/Z (CIVX2)	0.07	6.76	r
s15/m2/U3/Z (CND2X2)	0.12	6.88	f
s15/m2/U4/Z (CND2X4)	0.11	6.98	r
s15/m2/cout (mux_carry_2)	0.00	6.98	r
s15/cout_4 (CSA4_2)	0.00	6.98	r
s16/cin_4 (CSA4_1)	0.00	6.98	r
s16/m1/Cin (mux_sum_1)	0.00	6.98	r
s16/m1/U5/Z (CIVX2)	0.08	7.06	f
s16/m1/U1/Z (CAOR2X1)	0.27	7.33	f
s16/m1/sum[3] (mux_sum_1)	0.00	7.33	f
s16/sum_4[3] (CSA4_1)	0.00	7.33	f
sum_reg[63]/D (CFD2QXL)	0.00	7.33	f
data arrival time		7.33	

clock clock (rise edge)	8.00	8.00	
clock network delay (propagated)	0.00	8.00	
clock uncertainty	-0.25	7.75	
sum_reg[63]/CP (CFD2QXL)	0.00	7.75	r
library setup time	-0.37	7.38	
data required time		7.38	

data required time		7.38	
data arrival time		-7.33	

slack (MET) 0.05

Startpoint: op1f_reg[0] (rising edge-triggered flip-flop clocked by clock)
 Endpoint: crout_reg (rising edge-triggered flip-flop clocked by clock)
 Path Group: clock
 Path Type: max

Point	Incr	Path
clock clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.00	0.00
op1f_reg[0]/CP (CFD2QX1)	0.00	0.00 r
op1f_reg[0]/Q (CFD2QX1)	0.48	0.48 r
s1/op1_4[0] (CSA4_0)	0.00	0.48 r
s1/f5/op1_fa (FA_124)	0.00	0.48 r
s1/f5/U2/Z (CENX1)	0.29	0.78 r
s1/f5/U4/Z (CND2X2)	0.14	0.91 f
s1/f5/U6/Z (CND2X2)	0.11	1.02 r
s1/f5/cout_fa (FA_124)	0.00	1.02 r
s1/f6/cin (FA_123)	0.00	1.02 r
s1/f6/U2/Z (CENX2)	0.20	1.23 r
s1/f6/U4/Z (CAOR2X1)	0.31	1.53 r
s1/f6/cout_fa (FA_123)	0.00	1.53 r
s1/f7/cin (FA_122)	0.00	1.53 r
s1/f7/U1/Z (CENX2)	0.24	1.78 r
s1/f7/U3/Z (CND2X2)	0.13	1.91 f
s1/f7/U5/Z (CND2X2)	0.11	2.02 r
s1/f7/cout_fa (FA_122)	0.00	2.02 r
s1/f8/cin (FA_121)	0.00	2.02 r
s1/f8/U2/Z (CENX2)	0.11	2.13 f
s1/f8/U5/Z (CAOR2X1)	0.28	2.41 f
s1/f8/cout_fa (FA_121)	0.00	2.41 f
s1/m2/cout1 (mux_carry_0)	0.00	2.41 f
s1/m2/U1/Z (CAOR2X1)	0.38	2.80 f
s1/m2/cout (mux_carry_0)	0.00	2.80 f
s1/cout_4 (CSA4_0)	0.00	2.80 f
s2/cin_4 (CSA4_15)	0.00	2.80 f
s2/m2/Cin (mux_carry_15)	0.00	2.80 f
s2/m2/U2/Z (CND2X1)	0.12	2.92 r
s2/m2/U3/Z (CND2X2)	0.12	3.04 f
s2/m2/cout (mux_carry_15)	0.00	3.04 f
s2/cout_4 (CSA4_15)	0.00	3.04 f
s3/cin_4 (CSA4_14)	0.00	3.04 f
s3/m2/Cin (mux_carry_14)	0.00	3.04 f

s3/m2/U4/Z (CIVX2)	0.07	3.11	r
s3/m2/U2/Z (CND2X2)	0.09	3.20	f
s3/m2/U3/Z (CND2X2)	0.08	3.28	r
s3/m2/cout (mux_carry_14)	0.00	3.28	r
s3/cout_4 (CSA4_14)	0.00	3.28	r
s4/cin_4 (CSA4_13)	0.00	3.28	r
s4/m2/Cin (mux_carry_13)	0.00	3.28	r
s4/m2/U4/Z (CIVX2)	0.07	3.35	f
s4/m2/U2/Z (CND2X2)	0.07	3.42	r
s4/m2/U3/Z (CND2X2)	0.11	3.53	f
s4/m2/cout (mux_carry_13)	0.00	3.53	f
s4/cout_4 (CSA4_13)	0.00	3.53	f
s5/cin_4 (CSA4_12)	0.00	3.53	f
s5/m2/Cin (mux_carry_12)	0.00	3.53	f
s5/m2/U1/Z (CND2X1)	0.12	3.65	r
s5/m2/U3/Z (CND2X2)	0.12	3.77	f
s5/m2/cout (mux_carry_12)	0.00	3.77	f
s5/cout_4 (CSA4_12)	0.00	3.77	f
s6/cin_4 (CSA4_11)	0.00	3.77	f
s6/m2/Cin (mux_carry_11)	0.00	3.77	f
s6/m2/U3/Z (CIVX2)	0.07	3.84	r
s6/m2/U4/Z (CND2X2)	0.09	3.93	f
s6/m2/U5/Z (CND2X2)	0.10	4.03	r
s6/m2/cout (mux_carry_11)	0.00	4.03	r
s6/cout_4 (CSA4_11)	0.00	4.03	r
s7/cin_4 (CSA4_10)	0.00	4.03	r
s7/m2/Cin (mux_carry_10)	0.00	4.03	r
s7/m2/U2/Z (CIVX2)	0.07	4.10	f
s7/m2/U1/Z (CAOR2X1)	0.31	4.40	f
s7/m2/cout (mux_carry_10)	0.00	4.40	f
s7/cout_4 (CSA4_10)	0.00	4.40	f
s8/cin_4 (CSA4_9)	0.00	4.40	f
s8/m2/Cin (mux_carry_9)	0.00	4.40	f
s8/m2/U2/Z (CIVX1)	0.07	4.47	r
s8/m2/U1/Z (CAOR2X1)	0.21	4.68	r
s8/m2/cout (mux_carry_9)	0.00	4.68	r
s8/cout_4 (CSA4_9)	0.00	4.68	r
s9/cin_4 (CSA4_8)	0.00	4.68	r
s9/m2/Cin (mux_carry_8)	0.00	4.68	r
s9/m2/U2/Z (CIVXL)	0.10	4.78	f
s9/m2/U1/Z (CAOR2X1)	0.32	5.10	f
s9/m2/cout (mux_carry_8)	0.00	5.10	f
s9/cout_4 (CSA4_8)	0.00	5.10	f
s10/cin_4 (CSA4_7)	0.00	5.10	f
s10/m2/Cin (mux_carry_7)	0.00	5.10	f
s10/m2/U4/Z (CIVXL)	0.11	5.21	r
s10/m2/U2/Z (CND2X1)	0.14	5.35	f

s10/m2/U3/Z (CND2X2)	0.12	5.47	r
s10/m2/cout (mux_carry_7)	0.00	5.47	r
s10/cout_4 (CSA4_7)	0.00	5.47	r
s11/cin_4 (CSA4_6)	0.00	5.47	r
s11/m2/Cin (mux_carry_6)	0.00	5.47	r
s11/m2/U2/Z (CIVX2)	0.07	5.54	f
s11/m2/U1/Z (CAOR2X1)	0.33	5.87	f
s11/m2/cout (mux_carry_6)	0.00	5.87	f
s11/cout_4 (CSA4_6)	0.00	5.87	f
s12/cin_4 (CSA4_5)	0.00	5.87	f
s12/m2/Cin (mux_carry_5)	0.00	5.87	f
s12/m2/U1/Z (CND2X1)	0.12	6.00	r
s12/m2/U3/Z (CND2X2)	0.15	6.14	f
s12/m2/cout (mux_carry_5)	0.00	6.14	f
s12/cout_4 (CSA4_5)	0.00	6.14	f
s13/cin_4 (CSA4_4)	0.00	6.14	f
s13/m2/Cin (mux_carry_4)	0.00	6.14	f
s13/m2/U4/Z (CIVX2)	0.07	6.22	r
s13/m2/U2/Z (CND2X2)	0.09	6.31	f
s13/m2/U3/Z (CND2X2)	0.10	6.41	r
s13/m2/cout (mux_carry_4)	0.00	6.41	r
s13/cout_4 (CSA4_4)	0.00	6.41	r
s14/cin_4 (CSA4_3)	0.00	6.41	r
s14/m2/Cin (mux_carry_3)	0.00	6.41	r
s14/m2/U4/Z (CIVX2)	0.08	6.48	f
s14/m2/U3/Z (CND2X2)	0.07	6.56	r
s14/m2/U1/Z (CND2X2)	0.13	6.69	f
s14/m2/cout (mux_carry_3)	0.00	6.69	f
s14/cout_4 (CSA4_3)	0.00	6.69	f
s15/cin_4 (CSA4_2)	0.00	6.69	f
s15/m2/Cin (mux_carry_2)	0.00	6.69	f
s15/m2/U2/Z (CIVX2)	0.07	6.76	r
s15/m2/U3/Z (CND2X2)	0.12	6.88	f
s15/m2/U4/Z (CND2X4)	0.11	6.98	r
s15/m2/cout (mux_carry_2)	0.00	6.98	r
s15/cout_4 (CSA4_2)	0.00	6.98	r
s16/cin_4 (CSA4_1)	0.00	6.98	r
s16/m2/Cin (mux_carry_1)	0.00	6.98	r
s16/m2/U2/Z (CIVX1)	0.08	7.06	f
s16/m2/U1/Z (CAOR2X1)	0.27	7.33	f
s16/m2/cout (mux_carry_1)	0.00	7.33	f
s16/cout_4 (CSA4_1)	0.00	7.33	f
crout_reg/D (CFD2QXL)	0.00	7.33	f
data arrival time		7.33	
 clock clock (rise edge)	8.00	8.00	
clock network delay (propagated)	0.00	8.00	

clock uncertainty	-0.25	7.75
crout_reg/CP (CFD2QXL)	0.00	7.75 r
library setup time	-0.37	7.38
data required time		7.38

data required time		7.38
data arrival time		-7.33

slack (MET)		0.05

Startpoint: op1f_reg[0]
 (rising edge-triggered flip-flop clocked by clock)
 Endpoint: sum_reg[60]
 (rising edge-triggered flip-flop clocked by clock)
 Path Group: clock
 Path Type: max

Point	Incr	Path
clock clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.00	0.00
op1f_reg[0]/CP (CFD2QX1)	0.00	0.00 r
op1f_reg[0]/Q (CFD2QX1)	0.48	0.48 r
s1/op1_4[0] (CSA4_0)	0.00	0.48 r
s1/f5/op1_fa (FA_124)	0.00	0.48 r
s1/f5/U2/Z (CENX1)	0.29	0.78 r
s1/f5/U4/Z (CND2X2)	0.14	0.91 f
s1/f5/U6/Z (CND2X2)	0.11	1.02 r
s1/f5/cout_fa (FA_124)	0.00	1.02 r
s1/f6/cin (FA_123)	0.00	1.02 r
s1/f6/U2/Z (CENX2)	0.20	1.23 r
s1/f6/U4/Z (CAOR2X1)	0.31	1.53 r
s1/f6/cout_fa (FA_123)	0.00	1.53 r
s1/f7/cin (FA_122)	0.00	1.53 r
s1/f7/U1/Z (CENX2)	0.24	1.78 r
s1/f7/U3/Z (CND2X2)	0.13	1.91 f
s1/f7/U5/Z (CND2X2)	0.11	2.02 r
s1/f7/cout_fa (FA_122)	0.00	2.02 r
s1/f8/cin (FA_121)	0.00	2.02 r
s1/f8/U2/Z (CENX2)	0.11	2.13 f
s1/f8/U5/Z (CAOR2X1)	0.28	2.41 f
s1/f8/cout_fa (FA_121)	0.00	2.41 f
s1/m2/cout1 (mux_carry_0)	0.00	2.41 f
s1/m2/U1/Z (CAOR2X1)	0.38	2.80 f
s1/m2/cout (mux_carry_0)	0.00	2.80 f
s1/cout_4 (CSA4_0)	0.00	2.80 f

s2/cin_4 (CSA4_15)	0.00	2.80	f
s2/m2/Cin (mux_carry_15)	0.00	2.80	f
s2/m2/U2/Z (CND2X1)	0.12	2.92	r
s2/m2/U3/Z (CND2X2)	0.12	3.04	f
s2/m2/cout (mux_carry_15)	0.00	3.04	f
s2/cout_4 (CSA4_15)	0.00	3.04	f
s3/cin_4 (CSA4_14)	0.00	3.04	f
s3/m2/Cin (mux_carry_14)	0.00	3.04	f
s3/m2/U4/Z (CIVX2)	0.07	3.11	r
s3/m2/U2/Z (CND2X2)	0.09	3.20	f
s3/m2/U3/Z (CND2X2)	0.08	3.28	r
s3/m2/cout (mux_carry_14)	0.00	3.28	r
s3/cout_4 (CSA4_14)	0.00	3.28	r
s4/cin_4 (CSA4_13)	0.00	3.28	r
s4/m2/Cin (mux_carry_13)	0.00	3.28	r
s4/m2/U4/Z (CIVX2)	0.07	3.35	f
s4/m2/U2/Z (CND2X2)	0.07	3.42	r
s4/m2/U3/Z (CND2X2)	0.11	3.53	f
s4/m2/cout (mux_carry_13)	0.00	3.53	f
s4/cout_4 (CSA4_13)	0.00	3.53	f
s5/cin_4 (CSA4_12)	0.00	3.53	f
s5/m2/Cin (mux_carry_12)	0.00	3.53	f
s5/m2/U1/Z (CND2X1)	0.12	3.65	r
s5/m2/U3/Z (CND2X2)	0.12	3.77	f
s5/m2/cout (mux_carry_12)	0.00	3.77	f
s5/cout_4 (CSA4_12)	0.00	3.77	f
s6/cin_4 (CSA4_11)	0.00	3.77	f
s6/m2/Cin (mux_carry_11)	0.00	3.77	f
s6/m2/U3/Z (CIVX2)	0.07	3.84	r
s6/m2/U4/Z (CND2X2)	0.09	3.93	f
s6/m2/U5/Z (CND2X2)	0.10	4.03	r
s6/m2/cout (mux_carry_11)	0.00	4.03	r
s6/cout_4 (CSA4_11)	0.00	4.03	r
s7/cin_4 (CSA4_10)	0.00	4.03	r
s7/m2/Cin (mux_carry_10)	0.00	4.03	r
s7/m2/U2/Z (CIVX2)	0.07	4.10	f
s7/m2/U1/Z (CAOR2X1)	0.31	4.40	f
s7/m2/cout (mux_carry_10)	0.00	4.40	f
s7/cout_4 (CSA4_10)	0.00	4.40	f
s8/cin_4 (CSA4_9)	0.00	4.40	f
s8/m2/Cin (mux_carry_9)	0.00	4.40	f
s8/m2/U2/Z (CIVX1)	0.07	4.47	r
s8/m2/U1/Z (CAOR2X1)	0.21	4.68	r
s8/m2/cout (mux_carry_9)	0.00	4.68	r
s8/cout_4 (CSA4_9)	0.00	4.68	r
s9/cin_4 (CSA4_8)	0.00	4.68	r
s9/m2/Cin (mux_carry_8)	0.00	4.68	r

s9/m2/U2/Z (CIVXL)	0.10	4.78	f
s9/m2/U1/Z (CAOR2X1)	0.32	5.10	f
s9/m2/cout (mux_carry_8)	0.00	5.10	f
s9/cout_4 (CSA4_8)	0.00	5.10	f
s10/cin_4 (CSA4_7)	0.00	5.10	f
s10/m2/Cin (mux_carry_7)	0.00	5.10	f
s10/m2/U4/Z (CIVXL)	0.11	5.21	r
s10/m2/U2/Z (CND2X1)	0.14	5.35	f
s10/m2/U3/Z (CND2X2)	0.12	5.47	r
s10/m2/cout (mux_carry_7)	0.00	5.47	r
s10/cout_4 (CSA4_7)	0.00	5.47	r
s11/cin_4 (CSA4_6)	0.00	5.47	r
s11/m2/Cin (mux_carry_6)	0.00	5.47	r
s11/m2/U2/Z (CIVX2)	0.07	5.54	f
s11/m2/U1/Z (CAOR2X1)	0.33	5.87	f
s11/m2/cout (mux_carry_6)	0.00	5.87	f
s11/cout_4 (CSA4_6)	0.00	5.87	f
s12/cin_4 (CSA4_5)	0.00	5.87	f
s12/m2/Cin (mux_carry_5)	0.00	5.87	f
s12/m2/U1/Z (CND2X1)	0.12	6.00	r
s12/m2/U3/Z (CND2X2)	0.15	6.14	f
s12/m2/cout (mux_carry_5)	0.00	6.14	f
s12/cout_4 (CSA4_5)	0.00	6.14	f
s13/cin_4 (CSA4_4)	0.00	6.14	f
s13/m2/Cin (mux_carry_4)	0.00	6.14	f
s13/m2/U4/Z (CIVX2)	0.07	6.22	r
s13/m2/U2/Z (CND2X2)	0.09	6.31	f
s13/m2/U3/Z (CND2X2)	0.10	6.41	r
s13/m2/cout (mux_carry_4)	0.00	6.41	r
s13/cout_4 (CSA4_4)	0.00	6.41	r
s14/cin_4 (CSA4_3)	0.00	6.41	r
s14/m2/Cin (mux_carry_3)	0.00	6.41	r
s14/m2/U4/Z (CIVX2)	0.08	6.48	f
s14/m2/U3/Z (CND2X2)	0.07	6.56	r
s14/m2/U1/Z (CND2X2)	0.13	6.69	f
s14/m2/cout (mux_carry_3)	0.00	6.69	f
s14/cout_4 (CSA4_3)	0.00	6.69	f
s15/cin_4 (CSA4_2)	0.00	6.69	f
s15/m2/Cin (mux_carry_2)	0.00	6.69	f
s15/m2/U2/Z (CIVX2)	0.07	6.76	r
s15/m2/U3/Z (CND2X2)	0.12	6.88	f
s15/m2/U4/Z (CND2X4)	0.11	6.98	r
s15/m2/cout (mux_carry_2)	0.00	6.98	r
s15/cout_4 (CSA4_2)	0.00	6.98	r
s16/cin_4 (CSA4_1)	0.00	6.98	r
s16/m1/Cin (mux_sum_1)	0.00	6.98	r
s16/m1/U4/Z (CIVXL)	0.09	7.08	f

s16/m1/U6/Z (COND2XL)	0.16	7.24	r
s16/m1/sum[0] (mux_sum_1)	0.00	7.24	r
s16/sum_4[0] (CSA4_1)	0.00	7.24	r
sum_reg[60]/D (CFD2QXL)	0.00	7.24	r
data arrival time		7.24	
clock clock (rise edge)	8.00	8.00	
clock network delay (propagated)	0.00	8.00	
clock uncertainty	-0.25	7.75	
sum_reg[60]/CP (CFD2QXL)	0.00	7.75	r
library setup time	-0.39	7.36	
data required time		7.36	

data required time		7.36	
data arrival time		-7.24	

slack (MET)		0.12	

1
report_area

```
*****
Report : area
Design : CSA64EQG
Version: C-2009.06-SP5
Date   : Thu Dec  3 10:07:32 2015
*****
```

Library(s) Used:

tc240c (File:
/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25)

Number of ports: 195
Number of nets: 678
Number of cells: 483
Number of references: 22

Combinational area: 1965.500000
Noncombinational area: 1323.000000
Net Interconnect area: undefined (No wire load specified)

Total cell area: 3288.500000
Total area: undefined

1
report_power

```

Loading db file
'/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25'
Warning: Main library 'tc240c' does not specify the following
unit required for power: 'Leakage Power'. (PWR-424)
Information: Propagating switching activity (low effort zero
delay simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-
415)

```

```

*****
Report : power
      -analysis_effort low
Design : CSA64EQG
Version: C-2009.06-SP5
Date   : Thu Dec  3 10:07:33 2015
*****

```

Library(s) Used:

```

tc240c                               (File:
/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25)

```

Operating Conditions: WCCOM25 Library: tc240c
Wire Load Model Mode: top

Global Operating Voltage = 2.3
Power-specific unit information :
 Voltage Units = 1V
 Capacitance Units = 1.000000ff
 Time Units = 1ns
 Dynamic Power Units = 1uW (derived from V,C,T units)
 Leakage Power Units = Unitless

Cell Internal Power	=	12.9995 mW	(94%)
Net Switching Power	=	772.8808 uW	(6%)
<hr/>			
Total Dynamic Power	=	13.7724 mW	(100%)
Cell Leakage Power	=	0.0000	

```

1
write -hierarchy -format verilog -output CSA64EQG_1_nl.v

```

```
Writing verilog file
'/home/pa/pand2610/Desktop/Project/CSA64EQG/CSA64EQG_1_nl.v'.
1
quit
```

Thank you...

Synthesis Report of CSAUEQG

```
DC Professional (TM)
DC Expert (TM)
DC Ultra (TM)
FloorPlan Manager (TM)
HDL Compiler (TM)
VHDL Compiler (TM)
Library Compiler (TM)
DesignWare Developer (TM)
DFT Compiler (TM)
BSD Compiler
Power Compiler (TM)
```

```
Version C-2009.06-SP5 for linux -- Jan 15, 2010
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```

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```
Initializing...
set link_library
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
/apps/synopsys/SYNTH/libraries/syn/dw02.sldb
/apps/synopsys/SYNTH/libraries/syn/dw01.sldb}
```

```

/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
/apps/synopsys/SYNTH/libraries/syn/dw02.sldb
/apps/synopsys/SYNTH/libraries/syn/dw01.sldb
set                                         target_library
{/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}
/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
read_verilog
{FA.v,CSA2.v,CSA3.v,CSA4.v,CSA5.v,CSA6.v,CSA7.v,CSA8.v,CSA9.v,CSA10.v,CSA11.v,CSA64UEQG.v}
Loading                      db                  file
'/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25'
Loading db file '/apps/synopsys/SYNTH/libraries/syn/dw02.sldb'
Loading db file '/apps/synopsys/SYNTH/libraries/syn/dw01.sldb'
Loading db file '/apps/synopsys/SYNTH/libraries/syn/gtech.db'
Loading                      db                  file
'/apps/synopsys/SYNTH/libraries/syn/standard.sldb'
    Loading link library 'tc240c'
Warning: Function '=' leaked 1 allocations for 16 bytes. (EQN-21)
    Loading link library 'gtech'
Loading verilog files: '/home/pa/pand2610/Desktop/samvid/FA.v'
'/home/pa/pand2610/Desktop/samvid/CSA2.v'
'/home/pa/pand2610/Desktop/samvid/CSA3.v'
'/home/pa/pand2610/Desktop/samvid/CSA4.v'
'/home/pa/pand2610/Desktop/samvid/CSA5.v'
'/home/pa/pand2610/Desktop/samvid/CSA6.v'
'/home/pa/pand2610/Desktop/samvid/CSA7.v'
'/home/pa/pand2610/Desktop/samvid/CSA8.v'
'/home/pa/pand2610/Desktop/samvid/CSA9.v'
'/home/pa/pand2610/Desktop/samvid/CSA10.v'
'/home/pa/pand2610/Desktop/samvid/CSA11.v'
'/home/pa/pand2610/Desktop/samvid/CSA64UEQG.v'
Detecting input file type automatically (-rtl or -netlist).
Running DC verilog reader
Reading with Presto HDL Compiler (equivalent to -rtl option).
Running PRESTO HDLC
Compiling source file /home/pa/pand2610/Desktop/samvid/FA.v
Compiling source file /home/pa/pand2610/Desktop/samvid/CSA2.v
Compiling source file /home/pa/pand2610/Desktop/samvid/CSA3.v
Compiling source file /home/pa/pand2610/Desktop/samvid/CSA4.v
Compiling source file /home/pa/pand2610/Desktop/samvid/CSA5.v
Compiling source file /home/pa/pand2610/Desktop/samvid/CSA6.v
Compiling source file /home/pa/pand2610/Desktop/samvid/CSA7.v
Compiling source file /home/pa/pand2610/Desktop/samvid/CSA8.v
Compiling source file /home/pa/pand2610/Desktop/samvid/CSA9.v
Compiling source file /home/pa/pand2610/Desktop/samvid/CSA10.v
Compiling source file /home/pa/pand2610/Desktop/samvid/CSA11.v

```

```

Compiling source file
/home/pa/pand2610/Desktop/samvid/CSA64UEQG.v
Warning: /home/pa/pand2610/Desktop/samvid/CSA64UEQG.v:19: the
undeclared symbol 'Cin' assumed to have the default net type,
which is 'wire'. (VER-936)
Warning: /home/pa/pand2610/Desktop/samvid/CSA64UEQG.v:31: the
undeclared symbol 'C7' assumed to have the default net type,
which is 'wire'. (VER-936)
Warning: /home/pa/pand2610/Desktop/samvid/CSA64UEQG.v:33: the
undeclared symbol 'C8' assumed to have the default net type,
which is 'wire'. (VER-936)

```

```

Inferred memory devices in process
in routine CSA64UEQG line 37 in file
'/home/pa/pand2610/Desktop/samvid/CSA64UEQG.v'.
=====
```

	Register Name	Type	Width	Bus	MB	AR	AS
SR	SS	ST					
<hr/>							
N	sum_reg	Flip-flop	64		Y		N
N	crount_reg	Flip-flop	1		N		Y
N	op1f_reg	Flip-flop	64		Y		N
N	op2f_reg	Flip-flop	64		Y		N
<hr/>							

```
Presto compilation completed successfully.
```

```
Current design is now
'/home/pa/pand2610/Desktop/samvid/FA.db:FA'
```

```
Loaded 12 designs.
```

```
Current design is 'FA'.
```

```
FA CSA2 CSA3 CSA4 CSA5 CSA6 CSA7 CSA8 CSA9 CSA10 CSA11 CSA64UEQG
current_design CSA64UEQG
```

```
Current design is 'CSA64UEQG'.
```

```
{CSA64UEQG}
```

```
check_design
```

```
Warning: In design 'CSA64UEQG', a pin on submodule 'P1' is
connected to logic 1 or logic 0. (LINT-32)
```

```
    Pin 'cin_4' is connected to logic 0.
```

```
Warning: In design 'CSA4', a pin on submodule 'f1' is connected
to logic 1 or logic 0. (LINT-32)
```

```
    Pin 'cin' is connected to logic 0.
```

```
Warning: In design 'CSA4', a pin on submodule 'f5' is connected  
to logic 1 or logic 0. (LINT-32)  
    Pin 'cin' is connected to logic 1.  
Warning: In design 'CSA2', a pin on submodule 'f1' is connected  
to logic 1 or logic 0. (LINT-32)  
    Pin 'cin' is connected to logic 0.  
Warning: In design 'CSA2', a pin on submodule 'f3' is connected  
to logic 1 or logic 0. (LINT-32)  
    Pin 'cin' is connected to logic 1.  
Warning: In design 'CSA3', a pin on submodule 's1' is connected  
to logic 1 or logic 0. (LINT-32)  
    Pin 'cin' is connected to logic 0.  
Warning: In design 'CSA3', a pin on submodule 's4' is connected  
to logic 1 or logic 0. (LINT-32)  
    Pin 'cin' is connected to logic 1.  
Information: Design 'CSA64UEQG' has multiply instantiated  
designs. Use the '-multiple_designs' switch for more  
information. (LINT-78)  
1  
set_drive 0 clock  
1  
set_drive 0 reset  
1  
set_dont_touch_network clock  
1  
create_clock clock -name clock -period 8.00000  
1  
set_propagated_clock clock  
Information: set_input_delay values are added to the propagated  
clock skew. (TIM-113)  
1  
set_clock_uncertainty 0.25 clock  
1  
set_propagated_clock clock  
Information: set_input_delay values are added to the propagated  
clock skew. (TIM-113)  
1  
#set_output_delay 0.5 -clock clock [all_outputs]  
#set_all_inputs_wo_rst_clk [remove_from_collection  
[remove_from_collection [all_inputs] [get_port clk]] [get_port  
rst]]  
#set_driving_cell -lib_cell CND2X1 $all_inputs_wo_rst_clk  
#set_input_delay 0.5 -clock clk $all_inputs_wo_rst_clk  
#set_max_delay 48.5 -to [all_outputs]  
#set_max_delay 48.5 -from $all_inputs_wo_rst_clk  
set_fix_hold [ get_clocks clock ]  
1
```

```
compile -map_effort medium -incremental_mapping
Information: Evaluating DesignWare library utilization. (UISN-27)
```

```
=====
=====
| DesignWare Building Block Library | Version |
Available |
=====
=====
| Basic DW Building Blocks | C-2009.06-DWBB_0912
| * | 
| Licensed DW Building Blocks | C-2009.06-DWBB_0912
| | 
=====
=====
```

```
Information: There are 7 potential problems in your design.
Please run 'check_design' for more information. (LINT-99)
```

```
Warning: Operating condition WCCOM25 set on design CSA64UEQG has
different process,
voltage and temperatures parameters than the parameters at which
target library
tc240c is characterized. Delays may be inaccurate as a result.
(OPT-998)
```

```
Beginning Pass 1 Mapping (Incremental)
-----
Processing 'FA_0'
Processing 'CSA4_0'
Processing 'CSA3_0'
Processing 'CSA2_0'
Processing 'CSA64UEQG'
```

```
Updating timing information
Information: Updating design information... (UID-85)
Information: Input delay ('fall') on clock port 'clock' will be
added to the clock's propagated skew. (TIM-112)
Information: Input delay ('rise') on clock port 'clock' will be
added to the clock's propagated skew. (TIM-112)
Information: Input delay ('fall') on clock port 'clock' will be
added to the clock's propagated skew. (TIM-112)
Information: Input delay ('rise') on clock port 'clock' will be
added to the clock's propagated skew. (TIM-112)
```

Beginning Mapping Optimizations (Medium effort)
 (Incremental)

 Beginning Incremental Implementation Selection

Information: Input delay ('fall') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clock' will be added to the clock's propagated skew. (TIM-112)

 Beginning Delay Optimization Phase

ELAPSED MIN DELAY		WORST	NEG	TOTAL	NEG	DESIGN
TIME ENDPOINT	AREA COST	SLACK		SLACK	RULE	COST
0:00:01 0.00	2410.5	4.61		89.7		1890.1
0:00:03 sum_reg[60]/D	2653.5	2.15 0.00		31.4		0.0
0:00:04 sum_reg[60]/D	2754.0	1.05 0.00		11.5		0.0
0:00:04 sum_reg[60]/D	2830.0	0.31 0.00		1.6		0.0
0:00:05 sum_reg[60]/D	2891.0	0.11 0.00		0.5		0.0
0:00:05 -84.99	2891.5	0.00		0.0		0.0

 Beginning Design Rule Fixing (min_path)

ELAPSED MIN DELAY		WORST	NEG	TOTAL	NEG	DESIGN
TIME ENDPOINT	AREA COST	SLACK		SLACK	RULE	COST
0:00:05 -84.99	2891.5	0.00		0.0		0.0

```

0:00:06      3467.5      0.00      0.0      0.0
0.00
Loading          db
'/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25'

Optimization Complete
-----
1
create_clock clk -name clock -period 21.000000
Warning: Can't find object 'clk' in design 'CSA64UEQG'. (UID-95)
Error: Value for list 'source_objects' must have 1 elements.
(CMD-036)
0
set_propagated_clock clock
Information: set_input_delay values are added to the propagated
clock skew. (TIM-113)
1
set_clock_uncertainty 0.25 clock
1
set_propagated_clock clock
Information: set_input_delay values are added to the propagated
clock skew. (TIM-113)
1
update_timing
Information: Updating design information... (UID-85)
Information: Input delay ('fall') on clock port 'clock' will be
added to the clock's propagated skew. (TIM-112)
Information: Input delay ('rise') on clock port 'clock' will be
added to the clock's propagated skew. (TIM-112)
1
report -cell
report_cell

*****
Report : cell
Design : CSA64UEQG
Version: C-2009.06-SP5
Date   : Thu Dec  3 13:10:02 2015
*****

```

Attributes:

- b - black box (unknown)
- h - hierarchical
- n - noncombinational
- r - removable
- u - contains unmapped logic

Cell Area	Attributes	Reference	Library
P1 181.500000	h	CSA4_0	
P2 134.500000	h	CSA4_8	
P3 102.500000	h	CSA5	
P4 129.500000	h	CSA6	
P5 160.000000	h	CSA7	
P6 166.500000	h	CSA8	
P7 194.500000	h	CSA9	
P8 214.500000	h	CSA10	
P9 218.000000	h	CSA11	
U3 1.000000	CIVX2	tc240c	
U4 3.500000	CDLY1XL	tc240c	
U5 1.000000	CNIVX1	tc240c	

U6	CDLY1XL	tc240c
3.500000		
U7	CNIVX1	tc240c
1.000000		
U8	CDLY1XL	tc240c
3.500000		
U9	CNIVX1	tc240c
1.000000		
U10	CDLY1XL	tc240c
3.500000		
U11	CNIVX1	tc240c
1.000000		
U12	CDLY1XL	tc240c
3.500000		
U13	CNIVX1	tc240c
1.000000		
U14	CDLY1XL	tc240c
3.500000		
U15	CNIVX1	tc240c
1.000000		
U16	CDLY1XL	tc240c
3.500000		
U17	CNIVX1	tc240c
1.000000		
U18	CDLY1XL	tc240c
3.500000		
U19	CNIVX1	tc240c
1.000000		
U20	CDLY1XL	tc240c
3.500000		
U21	CNIVX1	tc240c
1.000000		
U22	CDLY1XL	tc240c
3.500000		
U23	CNIVX1	tc240c
1.000000		
U24	CDLY1XL	tc240c
3.500000		
U25	CNIVX1	tc240c
1.000000		
U26	CDLY1XL	tc240c
3.500000		
U27	CNIVX1	tc240c
1.000000		
U28	CDLY1XL	tc240c
3.500000		

U29	CNIVX1	tc240c
1.000000		
U30	CDLY1XL	tc240c
3.500000		
U31	CNIVX1	tc240c
1.000000		
U32	CDLY1XL	tc240c
3.500000		
U33	CNIVX1	tc240c
1.000000		
U34	CDLY1XL	tc240c
3.500000		
U35	CNIVX1	tc240c
1.000000		
U36	CDLY1XL	tc240c
3.500000		
U37	CNIVX1	tc240c
1.000000		
U38	CDLY1XL	tc240c
3.500000		
U39	CNIVX1	tc240c
1.000000		
U40	CDLY1XL	tc240c
3.500000		
U41	CNIVX1	tc240c
1.000000		
U42	CDLY1XL	tc240c
3.500000		
U43	CNIVX1	tc240c
1.000000		
U44	CDLY1XL	tc240c
3.500000		
U45	CNIVX1	tc240c
1.000000		
U46	CDLY1XL	tc240c
3.500000		
U47	CNIVX1	tc240c
1.000000		
U48	CDLY1XL	tc240c
3.500000		
U49	CNIVX1	tc240c
1.000000		
U50	CDLY1XL	tc240c
3.500000		
U51	CNIVX1	tc240c
1.000000		

U52	CDLY1XL	tc240c
3.500000		
U53	CNIVX1	tc240c
1.000000		
U54	CDLY1XL	tc240c
3.500000		
U55	CNIVX1	tc240c
1.000000		
U56	CDLY1XL	tc240c
3.500000		
U57	CNIVX1	tc240c
1.000000		
U58	CDLY1XL	tc240c
3.500000		
U59	CNIVX1	tc240c
1.000000		
U60	CDLY1XL	tc240c
3.500000		
U61	CNIVX1	tc240c
1.000000		
U62	CDLY1XL	tc240c
3.500000		
U63	CNIVX1	tc240c
1.000000		
U64	CDLY1XL	tc240c
3.500000		
U65	CNIVX1	tc240c
1.000000		
U66	CDLY1XL	tc240c
3.500000		
U67	CNIVX1	tc240c
1.000000		
U68	CDLY1XL	tc240c
3.500000		
U69	CNIVX1	tc240c
1.000000		
U70	CDLY1XL	tc240c
3.500000		
U71	CNIVX1	tc240c
1.000000		
U72	CDLY1XL	tc240c
3.500000		
U73	CNIVX1	tc240c
1.000000		
U74	CDLY1XL	tc240c
3.500000		

U75	CNIVX1	tc240c
1.000000		
U76	CDLY1XL	tc240c
3.500000		
U77	CNIVX1	tc240c
1.000000		
U78	CDLY1XL	tc240c
3.500000		
U79	CNIVX1	tc240c
1.000000		
U80	CDLY1XL	tc240c
3.500000		
U81	CNIVX1	tc240c
1.000000		
U82	CDLY1XL	tc240c
3.500000		
U83	CNIVX1	tc240c
1.000000		
U84	CDLY1XL	tc240c
3.500000		
U85	CNIVX1	tc240c
1.000000		
U86	CDLY1XL	tc240c
3.500000		
U87	CNIVX1	tc240c
1.000000		
U88	CDLY1XL	tc240c
3.500000		
U89	CNIVX1	tc240c
1.000000		
U90	CDLY1XL	tc240c
3.500000		
U91	CNIVX1	tc240c
1.000000		
U92	CDLY1XL	tc240c
3.500000		
U93	CNIVX1	tc240c
1.000000		
U94	CDLY1XL	tc240c
3.500000		
U95	CNIVX1	tc240c
1.000000		
U96	CDLY1XL	tc240c
3.500000		
U97	CNIVX1	tc240c
1.000000		

U98	CDLY1XL	tc240c
3.500000		
U99	CNIVX1	tc240c
1.000000		
U100	CDLY1XL	tc240c
3.500000		
U101	CNIVX1	tc240c
1.000000		
U102	CDLY1XL	tc240c
3.500000		
U103	CNIVX1	tc240c
1.000000		
U104	CDLY1XL	tc240c
3.500000		
U105	CNIVX1	tc240c
1.000000		
U106	CDLY1XL	tc240c
3.500000		
U107	CNIVX1	tc240c
1.000000		
U108	CDLY1XL	tc240c
3.500000		
U109	CNIVX1	tc240c
1.000000		
U110	CDLY1XL	tc240c
3.500000		
U111	CNIVX1	tc240c
1.000000		
U112	CDLY1XL	tc240c
3.500000		
U113	CNIVX1	tc240c
1.000000		
U114	CDLY1XL	tc240c
3.500000		
U115	CNIVX1	tc240c
1.000000		
U116	CDLY1XL	tc240c
3.500000		
U117	CNIVX1	tc240c
1.000000		
U118	CDLY1XL	tc240c
3.500000		
U119	CNIVX1	tc240c
1.000000		
U120	CDLY1XL	tc240c
3.500000		

U121	CNIVX1	tc240c
1.000000		
U122	CDLY1XL	tc240c
3.500000		
U123	CNIVX1	tc240c
1.000000		
U124	CDLY1XL	tc240c
3.500000		
U125	CNIVX1	tc240c
1.000000		
U126	CDLY1XL	tc240c
3.500000		
U127	CNIVX1	tc240c
1.000000		
U128	CDLY1XL	tc240c
3.500000		
U129	CNIVX1	tc240c
1.000000		
U130	CDLY1XL	tc240c
3.500000		
U131	CNIVX1	tc240c
1.000000		
U132	CDLY1XL	tc240c
3.500000		
U133	CNIVX1	tc240c
1.000000		
U134	CDLY1XL	tc240c
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U135	CNIVX1	tc240c
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U136	CDLY1XL	tc240c
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U137	CNIVX1	tc240c
1.000000		
U138	CDLY1XL	tc240c
3.500000		
U139	CNIVX1	tc240c
1.000000		
U140	CDLY1XL	tc240c
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U141	CNIVX1	tc240c
1.000000		
U142	CDLY1XL	tc240c
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U143	CNIVX1	tc240c
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U144	CDLY1XL	tc240c
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U145	CNIVX1	tc240c
1.000000		
U146	CDLY1XL	tc240c
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U147	CNIVX1	tc240c
1.000000		
U148	CDLY1XL	tc240c
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U149	CNIVX1	tc240c
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U150	CDLY1XL	tc240c
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U151	CNIVX1	tc240c
1.000000		
U152	CDLY1XL	tc240c
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U153	CNIVX1	tc240c
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U154	CDLY1XL	tc240c
3.500000		
U155	CNIVX1	tc240c
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U156	CDLY1XL	tc240c
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U157	CNIVX1	tc240c
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U158	CDLY1XL	tc240c
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U159	CNIVX1	tc240c
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U160	CDLY1XL	tc240c
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U161	CNIVX1	tc240c
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U162	CDLY1XL	tc240c
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U163	CNIVX1	tc240c
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U164	CDLY1XL	tc240c
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U165	CNIVX1	tc240c
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U166	CDLY1XL	tc240c
3.500000		

U167	CNIVX1	tc240c
1.000000		
U168	CDLY1XL	tc240c
3.500000		
U169	CNIVX1	tc240c
1.000000		
U170	CDLY1XL	tc240c
3.500000		
U171	CNIVX1	tc240c
1.000000		
U172	CDLY1XL	tc240c
3.500000		
U173	CNIVX1	tc240c
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U174	CDLY1XL	tc240c
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U175	CNIVX1	tc240c
1.000000		
U176	CDLY1XL	tc240c
3.500000		
U177	CNIVX1	tc240c
1.000000		
U178	CDLY1XL	tc240c
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U179	CNIVX1	tc240c
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U180	CDLY1XL	tc240c
3.500000		
U181	CNIVX1	tc240c
1.000000		
U182	CDLY1XL	tc240c
3.500000		
U183	CNIVX1	tc240c
1.000000		
U184	CDLY1XL	tc240c
3.500000		
U185	CNIVX1	tc240c
1.000000		
U186	CDLY1XL	tc240c
3.500000		
U187	CNIVX1	tc240c
1.000000		
U188	CDLY1XL	tc240c
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U189	CNIVX1	tc240c
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U190	CDLY1XL	tc240c
3.500000		
U191	CNIVX1	tc240c
1.000000		
U192	CDLY1XL	tc240c
3.500000		
U193	CNIVX1	tc240c
1.000000		
U194	CDLY1XL	tc240c
3.500000		
U195	CNIVX1	tc240c
1.000000		
U196	CDLY1XL	tc240c
3.500000		
U197	CNIVX1	tc240c
1.000000		
U198	CDLY1XL	tc240c
3.500000		
U199	CNIVX1	tc240c
1.000000		
U200	CDLY1XL	tc240c
3.500000		
U201	CNIVX1	tc240c
1.000000		
U202	CDLY1XL	tc240c
3.500000		
U203	CNIVX1	tc240c
1.000000		
U204	CDLY1XL	tc240c
3.500000		
U205	CNIVX1	tc240c
1.000000		
U206	CDLY1XL	tc240c
3.500000		
U207	CNIVX1	tc240c
1.000000		
U208	CDLY1XL	tc240c
3.500000		
U209	CNIVX1	tc240c
1.000000		
U210	CDLY1XL	tc240c
3.500000		
U211	CNIVX1	tc240c
1.000000		
U212	CDLY1XL	tc240c
3.500000		

U213	CNIVX1	tc240c
1.000000		
U214	CDLY1XL	tc240c
3.500000		
U215	CNIVX1	tc240c
1.000000		
U216	CDLY1XL	tc240c
3.500000		
U217	CNIVX1	tc240c
1.000000		
U218	CDLY1XL	tc240c
3.500000		
U219	CNIVX1	tc240c
1.000000		
U220	CDLY1XL	tc240c
3.500000		
U221	CNIVX1	tc240c
1.000000		
U222	CDLY1XL	tc240c
3.500000		
U223	CNIVX1	tc240c
1.000000		
U224	CDLY1XL	tc240c
3.500000		
U225	CNIVX1	tc240c
1.000000		
U226	CDLY1XL	tc240c
3.500000		
U227	CNIVX1	tc240c
1.000000		
U228	CDLY1XL	tc240c
3.500000		
U229	CNIVX1	tc240c
1.000000		
U230	CDLY1XL	tc240c
3.500000		
U231	CNIVX1	tc240c
1.000000		
U232	CDLY1XL	tc240c
3.500000		
U233	CNIVX1	tc240c
1.000000		
U234	CDLY1XL	tc240c
3.500000		
U235	CNIVX1	tc240c
1.000000		

U236	CDLY1XL	tc240c
3.500000		
U237	CNIVX1	tc240c
1.000000		
U238	CDLY1XL	tc240c
3.500000		
U239	CNIVX1	tc240c
1.000000		
U240	CDLY1XL	tc240c
3.500000		
U241	CNIVX1	tc240c
1.000000		
U242	CDLY1XL	tc240c
3.500000		
U243	CNIVX1	tc240c
1.000000		
U244	CDLY1XL	tc240c
3.500000		
U245	CNIVX1	tc240c
1.000000		
U246	CDLY1XL	tc240c
3.500000		
U247	CNIVX1	tc240c
1.000000		
U248	CDLY1XL	tc240c
3.500000		
U249	CNIVX1	tc240c
1.000000		
U250	CDLY1XL	tc240c
3.500000		
U251	CNIVX1	tc240c
1.000000		
U252	CDLY1XL	tc240c
3.500000		
U253	CNIVX1	tc240c
1.000000		
U254	CDLY1XL	tc240c
3.500000		
U255	CNIVX1	tc240c
1.000000		
U256	CDLY1XL	tc240c
3.500000		
U257	CNIVX1	tc240c
1.000000		
U258	CDLY1XL	tc240c
3.500000		

U259	CNIVX1	tc240c
1.000000		
U260	CDLY2X2	tc240c
7.000000		
U261	CDLY2X2	tc240c
7.000000		
U262	CDLY2X2	tc240c
7.000000		
U263	CDLY2X2	tc240c
7.000000		
U264	CDLY2X2	tc240c
7.000000		
U265	CDLY2X2	tc240c
7.000000		
U266	CDLY2X2	tc240c
7.000000		
U267	CDLY2X2	tc240c
7.000000		
U268	CDLY2X2	tc240c
7.000000		
U269	CDLY2X2	tc240c
7.000000		
U270	CDLY2X2	tc240c
7.000000		
U271	CDLY2X2	tc240c
7.000000		
U272	CDLY2X2	tc240c
7.000000		
U273	CDLY2X2	tc240c
7.000000		
U274	CDLY2X2	tc240c
7.000000		
U275	CDLY2X2	tc240c
7.000000		
U276	CDLY2X2	tc240c
7.000000		
crout_reg	CFD2QXL	tc240c
5.000000 n		
op1f_reg[0]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[1]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[2]	CFD2QXL	tc240c
5.000000 n		
op1f_reg[3]	CFD2QX1	tc240c
7.000000 n		

op1f_reg[4]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[5]	CFD2QX4	tc240c
8.000000 n		
op1f_reg[6]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[7]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[8]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[9]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[10]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[11]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[12]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[13]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[14]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[15]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[16]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[17]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[18]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[19]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[20]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[21]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[22]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[23]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[24]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[25]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[26]	CFD2QX1	tc240c
7.000000 n		

op1f_reg[27]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[28]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[29]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[30]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[31]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[32]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[33]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[34]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[35]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[36]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[37]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[38]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[39]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[40]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[41]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[42]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[43]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[44]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[45]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[46]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[47]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[48]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[49]	CFD2QX1	tc240c
7.000000 n		

op1f_reg[50]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[51]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[52]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[53]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[54]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[55]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[56]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[57]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[58]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[59]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[60]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[61]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[62]	CFD2QX1	tc240c
7.000000 n		
op1f_reg[63]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[0]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[1]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[2]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[3]	CFD2QXL	tc240c
5.000000 n		
op2f_reg[4]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[5]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[6]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[7]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[8]	CFD2QX1	tc240c
7.000000 n		

op2f_reg[9]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[10]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[11]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[12]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[13]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[14]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[15]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[16]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[17]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[18]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[19]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[20]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[21]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[22]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[23]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[24]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[25]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[26]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[27]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[28]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[29]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[30]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[31]	CFD2QX1	tc240c
7.000000 n		

op2f_reg[32]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[33]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[34]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[35]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[36]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[37]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[38]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[39]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[40]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[41]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[42]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[43]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[44]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[45]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[46]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[47]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[48]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[49]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[50]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[51]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[52]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[53]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[54]	CFD2QX1	tc240c
7.000000 n		

op2f_reg[55]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[56]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[57]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[58]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[59]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[60]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[61]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[62]	CFD2QX1	tc240c
7.000000 n		
op2f_reg[63]	CFD2QX1	tc240c
7.000000 n		
sum_reg[0]	CFD2QX1	tc240c
7.000000 n		
sum_reg[1]	CFD2QX1	tc240c
7.000000 n		
sum_reg[2]	CFD2QX1	tc240c
7.000000 n		
sum_reg[3]	CFD2QX1	tc240c
7.000000 n		
sum_reg[4]	CFD2QXL	tc240c
5.000000 n		
sum_reg[5]	CFD2QXL	tc240c
5.000000 n		
sum_reg[6]	CFD2QXL	tc240c
5.000000 n		
sum_reg[7]	CFD2QXL	tc240c
5.000000 n		
sum_reg[8]	CFD2QXL	tc240c
5.000000 n		
sum_reg[9]	CFD2QXL	tc240c
5.000000 n		
sum_reg[10]	CFD2QXL	tc240c
5.000000 n		
sum_reg[11]	CFD2QXL	tc240c
5.000000 n		
sum_reg[12]	CFD2QXL	tc240c
5.000000 n		
sum_reg[13]	CFD2QXL	tc240c
5.000000 n		

sum_reg[14]	CFD2QXL	tc240c
5.000000 n		
sum_reg[15]	CFD2QXL	tc240c
5.000000 n		
sum_reg[16]	CFD2QXL	tc240c
5.000000 n		
sum_reg[17]	CFD2QXL	tc240c
5.000000 n		
sum_reg[18]	CFD2QXL	tc240c
5.000000 n		
sum_reg[19]	CFD2QXL	tc240c
5.000000 n		
sum_reg[20]	CFD2QXL	tc240c
5.000000 n		
sum_reg[21]	CFD2QXL	tc240c
5.000000 n		
sum_reg[22]	CFD2QX1	tc240c
7.000000 n		
sum_reg[23]	CFD2QX1	tc240c
7.000000 n		
sum_reg[24]	CFD2QX1	tc240c
7.000000 n		
sum_reg[25]	CFD2QX1	tc240c
7.000000 n		
sum_reg[26]	CFD2QX1	tc240c
7.000000 n		
sum_reg[27]	CFD2QX1	tc240c
7.000000 n		
sum_reg[28]	CFD2QX1	tc240c
7.000000 n		
sum_reg[29]	CFD2QX1	tc240c
7.000000 n		
sum_reg[30]	CFD2QX1	tc240c
7.000000 n		
sum_reg[31]	CFD2QX1	tc240c
7.000000 n		
sum_reg[32]	CFD2QX1	tc240c
7.000000 n		
sum_reg[33]	CFD2QX1	tc240c
7.000000 n		
sum_reg[34]	CFD2QXL	tc240c
5.000000 n		
sum_reg[35]	CFD2QXL	tc240c
5.000000 n		
sum_reg[36]	CFD2QXL	tc240c
5.000000 n		

sum_reg[37]	CFD2QXL	tc240c
5.000000 n		
sum_reg[38]	CFD2QXL	tc240c
5.000000 n		
sum_reg[39]	CFD2QXL	tc240c
5.000000 n		
sum_reg[40]	CFD2QXL	tc240c
5.000000 n		
sum_reg[41]	CFD2QXL	tc240c
5.000000 n		
sum_reg[42]	CFD2QXL	tc240c
5.000000 n		
sum_reg[43]	CFD2QXL	tc240c
5.000000 n		
sum_reg[44]	CFD2QXL	tc240c
5.000000 n		
sum_reg[45]	CFD2QXL	tc240c
5.000000 n		
sum_reg[46]	CFD2QXL	tc240c
5.000000 n		
sum_reg[47]	CFD2QXL	tc240c
5.000000 n		
sum_reg[48]	CFD2QXL	tc240c
5.000000 n		
sum_reg[49]	CFD2QX1	tc240c
7.000000 n		
sum_reg[50]	CFD2QX1	tc240c
7.000000 n		
sum_reg[51]	CFD2QX1	tc240c
7.000000 n		
sum_reg[52]	CFD2QX1	tc240c
7.000000 n		
sum_reg[53]	CFD2QXL	tc240c
5.000000 n		
sum_reg[54]	CFD2QXL	tc240c
5.000000 n		
sum_reg[55]	CFD2QXL	tc240c
5.000000 n		
sum_reg[56]	CFD2QXL	tc240c
5.000000 n		
sum_reg[57]	CFD2QXL	tc240c
5.000000 n		
sum_reg[58]	CFD2QXL	tc240c
5.000000 n		
sum_reg[59]	CFD2QXL	tc240c
5.000000 n		

```

sum_reg[60]                                CFD2X2          tc240c
8.000000  n
sum_reg[61]                                CFD2X2          tc240c
8.000000  n
sum_reg[62]                                CFD2X2          tc240c
8.000000  n
sum_reg[63]                                CFD2QX4        tc240c
8.000000  n
-----
-----
Total                                     476           cells
3467.500000
1
report_timing -max_paths 5

*****
Report : timing
    -path full
    -delay max
    -max_paths 5
Design : CSA64UEQG
Version: C-2009.06-SP5
Date   : Thu Dec  3 13:10:02 2015
*****

```

Operating Conditions: WCCOM25 Library: tc240c
Wire Load Model Mode: top

```

Startpoint: op1f_reg[4]
            (rising edge-triggered flip-flop clocked by clock)
Endpoint: sum_reg[60]
            (rising edge-triggered flip-flop clocked by clock)
Path Group: clock
Path Type: max

```

Point	Incr	Path
clock clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.00	0.00
op1f_reg[4]/CP (CFD2QX1)	0.00	0.00 r
op1f_reg[4]/Q (CFD2QX1)	0.48	0.48 f
P2/op1_4[0] (CSA4_8)	0.00	0.48 f
P2/f1/op1_fa (FA_120)	0.00	0.48 f
P2/f1/U1/Z (CENX1)	0.26	0.74 f
P2/f1/U4/Z (CND2X2)	0.08	0.82 r
P2/f1/U6/Z (CND2X2)	0.12	0.95 f
P2/f1/cout_fa (FA_120)	0.00	0.95 f

P2/f2/cin (FA_119)	0.00	0.95	f
P2/f2/U3/Z (CEOX2)	0.24	1.19	f
P2/f2/U2/Z (CAOR2X1)	0.32	1.50	f
P2/f2/cout_fa (FA_119)	0.00	1.50	f
P2/f3/cin (FA_118)	0.00	1.50	f
P2/f3/U1/Z (CENX1)	0.25	1.75	f
P2/f3/U2/Z (CAOR2X1)	0.32	2.08	f
P2/f3/cout_fa (FA_118)	0.00	2.08	f
P2/f4/cin (FA_117)	0.00	2.08	f
P2/f4/U1/Z (CENX1)	0.22	2.29	f
P2/f4/U4/Z (CAOR2X1)	0.31	2.60	f
P2/f4/cout_fa (FA_117)	0.00	2.60	f
P2/U8/Z (CND2X2)	0.07	2.67	r
P2/U9/Z (CND2X2)	0.10	2.77	f
P2/cout_4 (CSA4_8)	0.00	2.77	f
P3/in (CSA5)	0.00	2.77	f
P3/D1/cin_2 (CSA2_0)	0.00	2.77	f
P3/D1/U3/Z (CIVX2)	0.07	2.84	r
P3/D1/U5/Z (CND2X2)	0.09	2.94	f
P3/D1/U6/Z (CND2X2)	0.10	3.03	r
P3/D1/cout_2 (CSA2_0)	0.00	3.03	r
P3/D2/cin_3 (CSA3_0)	0.00	3.03	r
P3/D2/U6/Z (CIVX2)	0.07	3.11	f
P3/D2/U10/Z (CND2X2)	0.07	3.18	r
P3/D2/U8/Z (CND2X2)	0.09	3.27	f
P3/D2/cout_3 (CSA3_0)	0.00	3.27	f
P3/co (CSA5)	0.00	3.27	f
P4/in6 (CSA6)	0.00	3.27	f
P4/E1/cin_3 (CSA3_7)	0.00	3.27	f
P4/E1/U4/Z (COND2X1)	0.25	3.52	r
P4/E1/cout_3 (CSA3_7)	0.00	3.52	r
P4/E2/cin_3 (CSA3_6)	0.00	3.52	r
P4/E2/U3/Z (CIVX1)	0.14	3.66	f
P4/E2/U7/Z (CND2IX2)	0.07	3.73	r
P4/E2/U9/Z (CND2X2)	0.10	3.83	f
P4/E2/cout_3 (CSA3_6)	0.00	3.83	f
P4/co6 (CSA6)	0.00	3.83	f
P5/in7 (CSA7)	0.00	3.83	f
P5/J1/cin_3 (CSA3_5)	0.00	3.83	f
P5/J1/U7/Z (CIVX2)	0.07	3.91	r
P5/J1/U9/Z (CND2X2)	0.09	4.00	f
P5/J1/U10/Z (CND2X2)	0.08	4.08	r
P5/J1/cout_3 (CSA3_5)	0.00	4.08	r
P5/J2/cin_4 (CSA4_7)	0.00	4.08	r
P5/J2/U3/Z (CND2IX1)	0.13	4.20	f
P5/J2/U10/Z (CND2X2)	0.10	4.30	r
P5/J2/cout_4 (CSA4_7)	0.00	4.30	r

P5/co7 (CSA7)	0.00	4.30	r
P6/in8 (CSA8)	0.00	4.30	r
P6/T1/cin_4 (CSA4_6)	0.00	4.30	r
P6/T1/U4/Z (CIVX2)	0.07	4.38	f
P6/T1/U9/Z (CND2IX2)	0.07	4.45	r
P6/T1/U13/Z (CND2X2)	0.10	4.55	f
P6/T1/cout_4 (CSA4_6)	0.00	4.55	f
P6/T2/cin_4 (CSA4_5)	0.00	4.55	f
P6/T2/U6/Z (CIVX2)	0.07	4.62	r
P6/T2/U4/Z (CND2X2)	0.09	4.71	f
P6/T2/U5/Z (CND2X2)	0.10	4.81	r
P6/T2/cout_4 (CSA4_5)	0.00	4.81	r
P6/co8 (CSA8)	0.00	4.81	r
P7/in9 (CSA9)	0.00	4.81	r
P7/V1/cin_3 (CSA3_4)	0.00	4.81	r
P7/V1/U6/Z (CIVX2)	0.07	4.88	f
P7/V1/U9/Z (CND2X2)	0.07	4.95	r
P7/V1/U10/Z (CND2X2)	0.10	5.05	f
P7/V1/cout_3 (CSA3_4)	0.00	5.05	f
P7/V2/cin_3 (CSA3_3)	0.00	5.05	f
P7/V2/U6/Z (CIVX2)	0.07	5.12	r
P7/V2/U4/Z (CND2X2)	0.09	5.22	f
P7/V2/U5/Z (CND2X2)	0.09	5.31	r
P7/V2/cout_3 (CSA3_3)	0.00	5.31	r
P7/V3/cin_3 (CSA3_2)	0.00	5.31	r
P7/V3/U7/Z (CIVX2)	0.08	5.39	f
P7/V3/U9/Z (CND2X2)	0.07	5.46	r
P7/V3/U10/Z (CND2X2)	0.10	5.56	f
P7/V3/cout_3 (CSA3_2)	0.00	5.56	f
P7/co9 (CSA9)	0.00	5.56	f
P8/in10 (CSA10)	0.00	5.56	f
P8/J1/cin_2 (CSA2_1)	0.00	5.56	f
P8/J1/U3/Z (CIVX2)	0.07	5.63	r
P8/J1/U7/Z (CND2X2)	0.09	5.72	f
P8/J1/U8/Z (CND2X2)	0.08	5.80	r
P8/J1/cout_2 (CSA2_1)	0.00	5.80	r
P8/J2/cin_4 (CSA4_4)	0.00	5.80	r
P8/J2/U5/Z (CIVX2)	0.07	5.87	f
P8/J2/U7/Z (CND2IX2)	0.07	5.94	r
P8/J2/U10/Z (CND2X2)	0.12	6.06	f
P8/J2/cout_4 (CSA4_4)	0.00	6.06	f
P8/J3/cin_4 (CSA4_3)	0.00	6.06	f
P8/J3/U3/Z (COND2X1)	0.25	6.31	r
P8/J3/cout_4 (CSA4_3)	0.00	6.31	r
P8/co10 (CSA10)	0.00	6.31	r
P9/in11 (CSA11)	0.00	6.31	r
P9/R1/cin_3 (CSA3_1)	0.00	6.31	r

P9/R1/U8/Z (CIVX1)	0.14	6.46	f
P9/R1/U5/Z (CND2X2)	0.07	6.53	r
P9/R1/U7/Z (CND2X2)	0.12	6.65	f
P9/R1/cout_3 (CSA3_1)	0.00	6.65	f
P9/R2/cin_4 (CSA4_2)	0.00	6.65	f
P9/R2/U7/Z (CIVX2)	0.08	6.73	r
P9/R2/U4/Z (CND2X1)	0.10	6.83	f
P9/R2/U5/Z (CND2X1)	0.18	7.01	r
P9/R2/cout_4 (CSA4_2)	0.00	7.01	r
P9/R3/cin_4 (CSA4_1)	0.00	7.01	r
P9/R3/U3/Z (CIVX2)	0.11	7.12	f
P9/R3/U6/Z (CAOR2X1)	0.28	7.40	f
P9/R3/sum_4[0] (CSA4_1)	0.00	7.40	f
P9/s11[7] (CSA11)	0.00	7.40	f
sum_reg[60]/D (CFD2X2)	0.00	7.40	f
data arrival time		7.40	
clock clock (rise edge)	8.00	8.00	
clock network delay (propagated)	0.00	8.00	
clock uncertainty	-0.25	7.75	
sum_reg[60]/CP (CFD2X2)	0.00	7.75	r
library setup time	-0.34	7.41	
data required time		7.41	

data required time		7.41	
data arrival time		-7.40	

slack (MET)	0.01		

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Startpoint: op1f_reg[4]
             (rising edge-triggered flip-flop clocked by clock)
Endpoint: sum_reg[61]
             (rising edge-triggered flip-flop clocked by clock)
Path Group: clock
Path Type: max
```

Point	Incr	Path
clock clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.00	0.00
op1f_reg[4]/CP (CFD2QX1)	0.00	0.00 r
op1f_reg[4]/Q (CFD2QX1)	0.48	0.48 f
P2/op1_4[0] (CSA4_8)	0.00	0.48 f
P2/f1/op1_fa (FA_120)	0.00	0.48 f
P2/f1/U1/Z (CENX1)	0.26	0.74 f
P2/f1/U4/Z (CND2X2)	0.08	0.82 r

P2/f1/U6/Z (CND2X2)	0.12	0.95	f
P2/f1/cout_fa (FA_120)	0.00	0.95	f
P2/f2/cin (FA_119)	0.00	0.95	f
P2/f2/U3/Z (CEOX2)	0.24	1.19	f
P2/f2/U2/Z (CAOR2X1)	0.32	1.50	f
P2/f2/cout_fa (FA_119)	0.00	1.50	f
P2/f3/cin (FA_118)	0.00	1.50	f
P2/f3/U1/Z (CENX1)	0.25	1.75	f
P2/f3/U2/Z (CAOR2X1)	0.32	2.08	f
P2/f3/cout_fa (FA_118)	0.00	2.08	f
P2/f4/cin (FA_117)	0.00	2.08	f
P2/f4/U1/Z (CENX1)	0.22	2.29	f
P2/f4/U4/Z (CAOR2X1)	0.31	2.60	f
P2/f4/cout_fa (FA_117)	0.00	2.60	f
P2/U8/Z (CND2X2)	0.07	2.67	r
P2/U9/Z (CND2X2)	0.10	2.77	f
P2/cout_4 (CSA4_8)	0.00	2.77	f
P3/in (CSA5)	0.00	2.77	f
P3/D1/cin_2 (CSA2_0)	0.00	2.77	f
P3/D1/U3/Z (CIVX2)	0.07	2.84	r
P3/D1/U5/Z (CND2X2)	0.09	2.94	f
P3/D1/U6/Z (CND2X2)	0.10	3.03	r
P3/D1/cout_2 (CSA2_0)	0.00	3.03	r
P3/D2/cin_3 (CSA3_0)	0.00	3.03	r
P3/D2/U6/Z (CIVX2)	0.07	3.11	f
P3/D2/U10/Z (CND2X2)	0.07	3.18	r
P3/D2/U8/Z (CND2X2)	0.09	3.27	f
P3/D2/cout_3 (CSA3_0)	0.00	3.27	f
P3/co (CSA5)	0.00	3.27	f
P4/in6 (CSA6)	0.00	3.27	f
P4/E1/cin_3 (CSA3_7)	0.00	3.27	f
P4/E1/U4/Z (COND2X1)	0.25	3.52	r
P4/E1/cout_3 (CSA3_7)	0.00	3.52	r
P4/E2/cin_3 (CSA3_6)	0.00	3.52	r
P4/E2/U3/Z (CIVX1)	0.14	3.66	f
P4/E2/U7/Z (CND2IX2)	0.07	3.73	r
P4/E2/U9/Z (CND2X2)	0.10	3.83	f
P4/E2/cout_3 (CSA3_6)	0.00	3.83	f
P4/co6 (CSA6)	0.00	3.83	f
P5/in7 (CSA7)	0.00	3.83	f
P5/J1/cin_3 (CSA3_5)	0.00	3.83	f
P5/J1/U7/Z (CIVX2)	0.07	3.91	r
P5/J1/U9/Z (CND2X2)	0.09	4.00	f
P5/J1/U10/Z (CND2X2)	0.08	4.08	r
P5/J1/cout_3 (CSA3_5)	0.00	4.08	r
P5/J2/cin_4 (CSA4_7)	0.00	4.08	r
P5/J2/U3/Z (CND2IX1)	0.13	4.20	f

P5/J2/U10/Z (CND2X2)	0.10	4.30	r
P5/J2/cout_4 (CSA4_7)	0.00	4.30	r
P5/co7 (CSA7)	0.00	4.30	r
P6/in8 (CSA8)	0.00	4.30	r
P6/T1/cin_4 (CSA4_6)	0.00	4.30	r
P6/T1/U4/Z (CIVX2)	0.07	4.38	f
P6/T1/U9/Z (CND2IX2)	0.07	4.45	r
P6/T1/U13/Z (CND2X2)	0.10	4.55	f
P6/T1/cout_4 (CSA4_6)	0.00	4.55	f
P6/T2/cin_4 (CSA4_5)	0.00	4.55	f
P6/T2/U6/Z (CIVX2)	0.07	4.62	r
P6/T2/U4/Z (CND2X2)	0.09	4.71	f
P6/T2/U5/Z (CND2X2)	0.10	4.81	r
P6/T2/cout_4 (CSA4_5)	0.00	4.81	r
P6/co8 (CSA8)	0.00	4.81	r
P7/in9 (CSA9)	0.00	4.81	r
P7/V1/cin_3 (CSA3_4)	0.00	4.81	r
P7/V1/U6/Z (CIVX2)	0.07	4.88	f
P7/V1/U9/Z (CND2X2)	0.07	4.95	r
P7/V1/U10/Z (CND2X2)	0.10	5.05	f
P7/V1/cout_3 (CSA3_4)	0.00	5.05	f
P7/V2/cin_3 (CSA3_3)	0.00	5.05	f
P7/V2/U6/Z (CIVX2)	0.07	5.12	r
P7/V2/U4/Z (CND2X2)	0.09	5.22	f
P7/V2/U5/Z (CND2X2)	0.09	5.31	r
P7/V2/cout_3 (CSA3_3)	0.00	5.31	r
P7/V3/cin_3 (CSA3_2)	0.00	5.31	r
P7/V3/U7/Z (CIVX2)	0.08	5.39	f
P7/V3/U9/Z (CND2X2)	0.07	5.46	r
P7/V3/U10/Z (CND2X2)	0.10	5.56	f
P7/V3/cout_3 (CSA3_2)	0.00	5.56	f
P7/co9 (CSA9)	0.00	5.56	f
P8/in10 (CSA10)	0.00	5.56	f
P8/J1/cin_2 (CSA2_1)	0.00	5.56	f
P8/J1/U3/Z (CIVX2)	0.07	5.63	r
P8/J1/U7/Z (CND2X2)	0.09	5.72	f
P8/J1/U8/Z (CND2X2)	0.08	5.80	r
P8/J1/cout_2 (CSA2_1)	0.00	5.80	r
P8/J2/cin_4 (CSA4_4)	0.00	5.80	r
P8/J2/U5/Z (CIVX2)	0.07	5.87	f
P8/J2/U7/Z (CND2IX2)	0.07	5.94	r
P8/J2/U10/Z (CND2X2)	0.12	6.06	f
P8/J2/cout_4 (CSA4_4)	0.00	6.06	f
P8/J3/cin_4 (CSA4_3)	0.00	6.06	f
P8/J3/U3/Z (COND2X1)	0.25	6.31	r
P8/J3/cout_4 (CSA4_3)	0.00	6.31	r
P8/co10 (CSA10)	0.00	6.31	r

P9/in11 (CSA11)	0.00	6.31	r
P9/R1/cin_3 (CSA3_1)	0.00	6.31	r
P9/R1/U8/Z (CIVX1)	0.14	6.46	f
P9/R1/U5/Z (CND2X2)	0.07	6.53	r
P9/R1/U7/Z (CND2X2)	0.12	6.65	f
P9/R1/cout_3 (CSA3_1)	0.00	6.65	f
P9/R2/cin_4 (CSA4_2)	0.00	6.65	f
P9/R2/U7/Z (CIVX2)	0.08	6.73	r
P9/R2/U4/Z (CND2X1)	0.10	6.83	f
P9/R2/U5/Z (CND2X1)	0.18	7.01	r
P9/R2/cout_4 (CSA4_2)	0.00	7.01	r
P9/R3/cin_4 (CSA4_1)	0.00	7.01	r
P9/R3/U3/Z (CIVX2)	0.11	7.12	f
P9/R3/U5/Z (CAOR2X1)	0.28	7.40	f
P9/R3/sum_4[1] (CSA4_1)	0.00	7.40	f
P9/s11[8] (CSA11)	0.00	7.40	f
sum_reg[61]/D (CFD2X2)	0.00	7.40	f
data arrival time		7.40	
clock clock (rise edge)	8.00	8.00	
clock network delay (propagated)	0.00	8.00	
clock uncertainty	-0.25	7.75	
sum_reg[61]/CP (CFD2X2)	0.00	7.75	r
library setup time	-0.34	7.41	
data required time		7.41	

data required time		7.41	
data arrival time		-7.40	
slack (MET)		0.01	

Startpoint: op1f_reg[4]
 (rising edge-triggered flip-flop clocked by clock)
Endpoint: sum_reg[62]
 (rising edge-triggered flip-flop clocked by clock)
Path Group: clock
Path Type: max

Point	Incr	Path
clock clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.00	0.00
op1f_reg[4]/CP (CFD2QX1)	0.00	0.00 r
op1f_reg[4]/Q (CFD2QX1)	0.48	0.48 f
P2/op1_4[0] (CSA4_8)	0.00	0.48 f
P2/f1/op1_fa (FA_120)	0.00	0.48 f

P2/f1/U1/Z (CENX1)	0.26	0.74	f
P2/f1/U4/Z (CND2X2)	0.08	0.82	r
P2/f1/U6/Z (CND2X2)	0.12	0.95	f
P2/f1/cout_fa (FA_120)	0.00	0.95	f
P2/f2/cin (FA_119)	0.00	0.95	f
P2/f2/U3/Z (CEOX2)	0.24	1.19	f
P2/f2/U2/Z (CAOR2X1)	0.32	1.50	f
P2/f2/cout_fa (FA_119)	0.00	1.50	f
P2/f3/cin (FA_118)	0.00	1.50	f
P2/f3/U1/Z (CENX1)	0.25	1.75	f
P2/f3/U2/Z (CAOR2X1)	0.32	2.08	f
P2/f3/cout_fa (FA_118)	0.00	2.08	f
P2/f4/cin (FA_117)	0.00	2.08	f
P2/f4/U1/Z (CENX1)	0.22	2.29	f
P2/f4/U4/Z (CAOR2X1)	0.31	2.60	f
P2/f4/cout_fa (FA_117)	0.00	2.60	f
P2/U8/Z (CND2X2)	0.07	2.67	r
P2/U9/Z (CND2X2)	0.10	2.77	f
P2/cout_4 (CSA4_8)	0.00	2.77	f
P3/in (CSA5)	0.00	2.77	f
P3/D1/cin_2 (CSA2_0)	0.00	2.77	f
P3/D1/U3/Z (CIVX2)	0.07	2.84	r
P3/D1/U5/Z (CND2X2)	0.09	2.94	f
P3/D1/U6/Z (CND2X2)	0.10	3.03	r
P3/D1/cout_2 (CSA2_0)	0.00	3.03	r
P3/D2/cin_3 (CSA3_0)	0.00	3.03	r
P3/D2/U6/Z (CIVX2)	0.07	3.11	f
P3/D2/U10/Z (CND2X2)	0.07	3.18	r
P3/D2/U8/Z (CND2X2)	0.09	3.27	f
P3/D2/cout_3 (CSA3_0)	0.00	3.27	f
P3/co (CSA5)	0.00	3.27	f
P4/in6 (CSA6)	0.00	3.27	f
P4/E1/cin_3 (CSA3_7)	0.00	3.27	f
P4/E1/U4/Z (COND2X1)	0.25	3.52	r
P4/E1/cout_3 (CSA3_7)	0.00	3.52	r
P4/E2/cin_3 (CSA3_6)	0.00	3.52	r
P4/E2/U3/Z (CIVX1)	0.14	3.66	f
P4/E2/U7/Z (CND2IX2)	0.07	3.73	r
P4/E2/U9/Z (CND2X2)	0.10	3.83	f
P4/E2/cout_3 (CSA3_6)	0.00	3.83	f
P4/co6 (CSA6)	0.00	3.83	f
P5/in7 (CSA7)	0.00	3.83	f
P5/J1/cin_3 (CSA3_5)	0.00	3.83	f
P5/J1/U7/Z (CIVX2)	0.07	3.91	r
P5/J1/U9/Z (CND2X2)	0.09	4.00	f
P5/J1/U10/Z (CND2X2)	0.08	4.08	r
P5/J1/cout_3 (CSA3_5)	0.00	4.08	r

P5/J2/cin_4 (CSA4_7)	0.00	4.08	r
P5/J2/U3/Z (CND2IX1)	0.13	4.20	f
P5/J2/U10/Z (CND2X2)	0.10	4.30	r
P5/J2/cout_4 (CSA4_7)	0.00	4.30	r
P5/co7 (CSA7)	0.00	4.30	r
P6/in8 (CSA8)	0.00	4.30	r
P6/T1/cin_4 (CSA4_6)	0.00	4.30	r
P6/T1/U4/Z (CIVX2)	0.07	4.38	f
P6/T1/U9/Z (CND2IX2)	0.07	4.45	r
P6/T1/U13/Z (CND2X2)	0.10	4.55	f
P6/T1/cout_4 (CSA4_6)	0.00	4.55	f
P6/T2/cin_4 (CSA4_5)	0.00	4.55	f
P6/T2/U6/Z (CIVX2)	0.07	4.62	r
P6/T2/U4/Z (CND2X2)	0.09	4.71	f
P6/T2/U5/Z (CND2X2)	0.10	4.81	r
P6/T2/cout_4 (CSA4_5)	0.00	4.81	r
P6/co8 (CSA8)	0.00	4.81	r
P7/in9 (CSA9)	0.00	4.81	r
P7/V1/cin_3 (CSA3_4)	0.00	4.81	r
P7/V1/U6/Z (CIVX2)	0.07	4.88	f
P7/V1/U9/Z (CND2X2)	0.07	4.95	r
P7/V1/U10/Z (CND2X2)	0.10	5.05	f
P7/V1/cout_3 (CSA3_4)	0.00	5.05	f
P7/V2/cin_3 (CSA3_3)	0.00	5.05	f
P7/V2/U6/Z (CIVX2)	0.07	5.12	r
P7/V2/U4/Z (CND2X2)	0.09	5.22	f
P7/V2/U5/Z (CND2X2)	0.09	5.31	r
P7/V2/cout_3 (CSA3_3)	0.00	5.31	r
P7/V3/cin_3 (CSA3_2)	0.00	5.31	r
P7/V3/U7/Z (CIVX2)	0.08	5.39	f
P7/V3/U9/Z (CND2X2)	0.07	5.46	r
P7/V3/U10/Z (CND2X2)	0.10	5.56	f
P7/V3/cout_3 (CSA3_2)	0.00	5.56	f
P7/co9 (CSA9)	0.00	5.56	f
P8/in10 (CSA10)	0.00	5.56	f
P8/J1/cin_2 (CSA2_1)	0.00	5.56	f
P8/J1/U3/Z (CIVX2)	0.07	5.63	r
P8/J1/U7/Z (CND2X2)	0.09	5.72	f
P8/J1/U8/Z (CND2X2)	0.08	5.80	r
P8/J1/cout_2 (CSA2_1)	0.00	5.80	r
P8/J2/cin_4 (CSA4_4)	0.00	5.80	r
P8/J2/U5/Z (CIVX2)	0.07	5.87	f
P8/J2/U7/Z (CND2IX2)	0.07	5.94	r
P8/J2/U10/Z (CND2X2)	0.12	6.06	f
P8/J2/cout_4 (CSA4_4)	0.00	6.06	f
P8/J3/cin_4 (CSA4_3)	0.00	6.06	f
P8/J3/U3/Z (COND2X1)	0.25	6.31	r

P8/J3/cout_4 (CSA4_3)	0.00	6.31	r
P8/co10 (CSA10)	0.00	6.31	r
P9/in11 (CSA11)	0.00	6.31	r
P9/R1/cin_3 (CSA3_1)	0.00	6.31	r
P9/R1/U8/Z (CIVX1)	0.14	6.46	f
P9/R1/U5/Z (CND2X2)	0.07	6.53	r
P9/R1/U7/Z (CND2X2)	0.12	6.65	f
P9/R1/cout_3 (CSA3_1)	0.00	6.65	f
P9/R2/cin_4 (CSA4_2)	0.00	6.65	f
P9/R2/U7/Z (CIVX2)	0.08	6.73	r
P9/R2/U4/Z (CND2X1)	0.10	6.83	f
P9/R2/U5/Z (CND2X1)	0.18	7.01	r
P9/R2/cout_4 (CSA4_2)	0.00	7.01	r
P9/R3/cin_4 (CSA4_1)	0.00	7.01	r
P9/R3/U3/Z (CIVX2)	0.11	7.12	f
P9/R3/U4/Z (CAOR2X1)	0.28	7.40	f
P9/R3/sum_4[2] (CSA4_1)	0.00	7.40	f
P9/s11[9] (CSA11)	0.00	7.40	f
sum_reg[62]/D (CFD2X2)	0.00	7.40	f
data arrival time		7.40	
clock clock (rise edge)	8.00	8.00	
clock network delay (propagated)	0.00	8.00	
clock uncertainty	-0.25	7.75	
sum_reg[62]/CP (CFD2X2)	0.00	7.75	r
library setup time	-0.34	7.41	
data required time		7.41	

data required time		7.41	
data arrival time		-7.40	

slack (MET)	0.01		

Startpoint: op1f_reg[4]
 (rising edge-triggered flip-flop clocked by clock)
 Endpoint: sum_reg[63]
 (rising edge-triggered flip-flop clocked by clock)
 Path Group: clock
 Path Type: max

Point	Incr	Path
clock clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.00	0.00
op1f_reg[4]/CP (CFD2QX1)	0.00	0.00 r
op1f_reg[4]/Q (CFD2QX1)	0.48	0.48 f

P2/op1_4[0] (CSA4_8)	0.00	0.48	f
P2/f1/op1_fa (FA_120)	0.00	0.48	f
P2/f1/U1/Z (CENX1)	0.26	0.74	f
P2/f1/U4/Z (CND2X2)	0.08	0.82	r
P2/f1/U6/Z (CND2X2)	0.12	0.95	f
P2/f1/cout_fa (FA_120)	0.00	0.95	f
P2/f2/cin (FA_119)	0.00	0.95	f
P2/f2/U3/Z (CEOX2)	0.24	1.19	f
P2/f2/U2/Z (CAOR2X1)	0.32	1.50	f
P2/f2/cout_fa (FA_119)	0.00	1.50	f
P2/f3/cin (FA_118)	0.00	1.50	f
P2/f3/U1/Z (CENX1)	0.25	1.75	f
P2/f3/U2/Z (CAOR2X1)	0.32	2.08	f
P2/f3/cout_fa (FA_118)	0.00	2.08	f
P2/f4/cin (FA_117)	0.00	2.08	f
P2/f4/U1/Z (CENX1)	0.22	2.29	f
P2/f4/U4/Z (CAOR2X1)	0.31	2.60	f
P2/f4/cout_fa (FA_117)	0.00	2.60	f
P2/U8/Z (CND2X2)	0.07	2.67	r
P2/U9/Z (CND2X2)	0.10	2.77	f
P2/cout_4 (CSA4_8)	0.00	2.77	f
P3/in (CSA5)	0.00	2.77	f
P3/D1/cin_2 (CSA2_0)	0.00	2.77	f
P3/D1/U3/Z (CIVX2)	0.07	2.84	r
P3/D1/U5/Z (CND2X2)	0.09	2.94	f
P3/D1/U6/Z (CND2X2)	0.10	3.03	r
P3/D1/cout_2 (CSA2_0)	0.00	3.03	r
P3/D2/cin_3 (CSA3_0)	0.00	3.03	r
P3/D2/U6/Z (CIVX2)	0.07	3.11	f
P3/D2/U10/Z (CND2X2)	0.07	3.18	r
P3/D2/U8/Z (CND2X2)	0.09	3.27	f
P3/D2/cout_3 (CSA3_0)	0.00	3.27	f
P3/co (CSA5)	0.00	3.27	f
P4/in6 (CSA6)	0.00	3.27	f
P4/E1/cin_3 (CSA3_7)	0.00	3.27	f
P4/E1/U4/Z (COND2X1)	0.25	3.52	r
P4/E1/cout_3 (CSA3_7)	0.00	3.52	r
P4/E2/cin_3 (CSA3_6)	0.00	3.52	r
P4/E2/U3/Z (CIVX1)	0.14	3.66	f
P4/E2/U7/Z (CND2IX2)	0.07	3.73	r
P4/E2/U9/Z (CND2X2)	0.10	3.83	f
P4/E2/cout_3 (CSA3_6)	0.00	3.83	f
P4/co6 (CSA6)	0.00	3.83	f
P5/in7 (CSA7)	0.00	3.83	f
P5/J1/cin_3 (CSA3_5)	0.00	3.83	f
P5/J1/U7/Z (CIVX2)	0.07	3.91	r
P5/J1/U9/Z (CND2X2)	0.09	4.00	f

P5/J1/U10/Z (CND2X2)	0.08	4.08	r
P5/J1/cout_3 (CSA3_5)	0.00	4.08	r
P5/J2/cin_4 (CSA4_7)	0.00	4.08	r
P5/J2/U3/Z (CND2IX1)	0.13	4.20	f
P5/J2/U10/Z (CND2X2)	0.10	4.30	r
P5/J2/cout_4 (CSA4_7)	0.00	4.30	r
P5/co7 (CSA7)	0.00	4.30	r
P6/in8 (CSA8)	0.00	4.30	r
P6/T1/cin_4 (CSA4_6)	0.00	4.30	r
P6/T1/U4/Z (CIVX2)	0.07	4.38	f
P6/T1/U9/Z (CND2IX2)	0.07	4.45	r
P6/T1/U13/Z (CND2X2)	0.10	4.55	f
P6/T1/cout_4 (CSA4_6)	0.00	4.55	f
P6/T2/cin_4 (CSA4_5)	0.00	4.55	f
P6/T2/U6/Z (CIVX2)	0.07	4.62	r
P6/T2/U4/Z (CND2X2)	0.09	4.71	f
P6/T2/U5/Z (CND2X2)	0.10	4.81	r
P6/T2/cout_4 (CSA4_5)	0.00	4.81	r
P6/co8 (CSA8)	0.00	4.81	r
P7/in9 (CSA9)	0.00	4.81	r
P7/V1/cin_3 (CSA3_4)	0.00	4.81	r
P7/V1/U6/Z (CIVX2)	0.07	4.88	f
P7/V1/U9/Z (CND2X2)	0.07	4.95	r
P7/V1/U10/Z (CND2X2)	0.10	5.05	f
P7/V1/cout_3 (CSA3_4)	0.00	5.05	f
P7/V2/cin_3 (CSA3_3)	0.00	5.05	f
P7/V2/U6/Z (CIVX2)	0.07	5.12	r
P7/V2/U4/Z (CND2X2)	0.09	5.22	f
P7/V2/U5/Z (CND2X2)	0.09	5.31	r
P7/V2/cout_3 (CSA3_3)	0.00	5.31	r
P7/V3/cin_3 (CSA3_2)	0.00	5.31	r
P7/V3/U7/Z (CIVX2)	0.08	5.39	f
P7/V3/U9/Z (CND2X2)	0.07	5.46	r
P7/V3/U10/Z (CND2X2)	0.10	5.56	f
P7/V3/cout_3 (CSA3_2)	0.00	5.56	f
P7/co9 (CSA9)	0.00	5.56	f
P8/in10 (CSA10)	0.00	5.56	f
P8/J1/cin_2 (CSA2_1)	0.00	5.56	f
P8/J1/U3/Z (CIVX2)	0.07	5.63	r
P8/J1/U7/Z (CND2X2)	0.09	5.72	f
P8/J1/U8/Z (CND2X2)	0.08	5.80	r
P8/J1/cout_2 (CSA2_1)	0.00	5.80	r
P8/J2/cin_4 (CSA4_4)	0.00	5.80	r
P8/J2/U5/Z (CIVX2)	0.07	5.87	f
P8/J2/U7/Z (CND2IX2)	0.07	5.94	r
P8/J2/U10/Z (CND2X2)	0.12	6.06	f
P8/J2/cout_4 (CSA4_4)	0.00	6.06	f

P8/J3/cin_4 (CSA4_3)	0.00	6.06	f
P8/J3/U3/Z (COND2X1)	0.25	6.31	r
P8/J3/cout_4 (CSA4_3)	0.00	6.31	r
P8/co10 (CSA10)	0.00	6.31	r
P9/in11 (CSA11)	0.00	6.31	r
P9/R1/cin_3 (CSA3_1)	0.00	6.31	r
P9/R1/U8/Z (CIVX1)	0.14	6.46	f
P9/R1/U5/Z (CND2X2)	0.07	6.53	r
P9/R1/U7/Z (CND2X2)	0.12	6.65	f
P9/R1/cout_3 (CSA3_1)	0.00	6.65	f
P9/R2/cin_4 (CSA4_2)	0.00	6.65	f
P9/R2/U7/Z (CIVX2)	0.08	6.73	r
P9/R2/U4/Z (CND2X1)	0.10	6.83	f
P9/R2/U5/Z (CND2X1)	0.18	7.01	r
P9/R2/cout_4 (CSA4_2)	0.00	7.01	r
P9/R3/cin_4 (CSA4_1)	0.00	7.01	r
P9/R3/U3/Z (CIVX2)	0.11	7.12	f
P9/R3/U10/Z (COND2XL)	0.22	7.35	r
P9/R3/sum_4[3] (CSA4_1)	0.00	7.35	r
P9/s11[10] (CSA11)	0.00	7.35	r
sum_reg[63]/D (CFD2QX4)	0.00	7.35	r
data arrival time		7.35	
clock clock (rise edge)	8.00	8.00	
clock network delay (propagated)	0.00	8.00	
clock uncertainty	-0.25	7.75	
sum_reg[63]/CP (CFD2QX4)	0.00	7.75	r
library setup time	-0.34	7.41	
data required time		7.41	

data required time		7.41	
data arrival time		-7.35	

slack (MET)		0.07	

```
Startpoint: op1f_reg[4]
             (rising edge-triggered flip-flop clocked by clock)
  Endpoint: crout_reg (rising edge-triggered flip-flop clocked
by clock)
  Path Group: clock
  Path Type: max
```

Point	Incr	Path
clock clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.00	0.00

op1f_reg[4]/CP (CFD2QX1)	0.00	0.00	r
op1f_reg[4]/Q (CFD2QX1)	0.48	0.48	f
P2/op1_4[0] (CSA4_8)	0.00	0.48	f
P2/f1/op1_fa (FA_120)	0.00	0.48	f
P2/f1/U1/Z (CENX1)	0.26	0.74	f
P2/f1/U4/Z (CND2X2)	0.08	0.82	r
P2/f1/U6/Z (CND2X2)	0.12	0.95	f
P2/f1/cout_fa (FA_120)	0.00	0.95	f
P2/f2/cin_(FA_119)	0.00	0.95	f
P2/f2/U3/Z (CEOX2)	0.24	1.19	f
P2/f2/U2/Z (CAOR2X1)	0.32	1.50	f
P2/f2/cout_fa (FA_119)	0.00	1.50	f
P2/f3/cin_(FA_118)	0.00	1.50	f
P2/f3/U1/Z (CENX1)	0.25	1.75	f
P2/f3/U2/Z (CAOR2X1)	0.32	2.08	f
P2/f3/cout_fa (FA_118)	0.00	2.08	f
P2/f4/cin_(FA_117)	0.00	2.08	f
P2/f4/U1/Z (CENX1)	0.22	2.29	f
P2/f4/U4/Z (CAOR2X1)	0.31	2.60	f
P2/f4/cout_fa (FA_117)	0.00	2.60	f
P2/U8/Z (CND2X2)	0.07	2.67	r
P2/U9/Z (CND2X2)	0.10	2.77	f
P2/cout_4 (CSA4_8)	0.00	2.77	f
P3/in_(CSA5)	0.00	2.77	f
P3/D1/cin_2 (CSA2_0)	0.00	2.77	f
P3/D1/U3/Z (CIVX2)	0.07	2.84	r
P3/D1/U5/Z (CND2X2)	0.09	2.94	f
P3/D1/U6/Z (CND2X2)	0.10	3.03	r
P3/D1/cout_2 (CSA2_0)	0.00	3.03	r
P3/D2/cin_3 (CSA3_0)	0.00	3.03	r
P3/D2/U6/Z (CIVX2)	0.07	3.11	f
P3/D2/U10/Z (CND2X2)	0.07	3.18	r
P3/D2/U8/Z (CND2X2)	0.09	3.27	f
P3/D2/cout_3 (CSA3_0)	0.00	3.27	f
P3/co_(CSA5)	0.00	3.27	f
P4/in6_(CSA6)	0.00	3.27	f
P4/E1/cin_3 (CSA3_7)	0.00	3.27	f
P4/E1/U4/Z (COND2X1)	0.25	3.52	r
P4/E1/cout_3 (CSA3_7)	0.00	3.52	r
P4/E2/cin_3 (CSA3_6)	0.00	3.52	r
P4/E2/U3/Z (CIVX1)	0.14	3.66	f
P4/E2/U7/Z (CND2IX2)	0.07	3.73	r
P4/E2/U9/Z (CND2X2)	0.10	3.83	f
P4/E2/cout_3 (CSA3_6)	0.00	3.83	f
P4/co6_(CSA6)	0.00	3.83	f
P5/in7_(CSA7)	0.00	3.83	f
P5/J1/cin_3 (CSA3_5)	0.00	3.83	f

P5/J1/U7/Z (CIVX2)	0.07	3.91	r
P5/J1/U9/Z (CND2X2)	0.09	4.00	f
P5/J1/U10/Z (CND2X2)	0.08	4.08	r
P5/J1/cout_3 (CSA3_5)	0.00	4.08	r
P5/J2/cin_4 (CSA4_7)	0.00	4.08	r
P5/J2/U3/Z (CND2IX1)	0.13	4.20	f
P5/J2/U10/Z (CND2X2)	0.10	4.30	r
P5/J2/cout_4 (CSA4_7)	0.00	4.30	r
P5/co7 (CSA7)	0.00	4.30	r
P6/in8 (CSA8)	0.00	4.30	r
P6/T1/cin_4 (CSA4_6)	0.00	4.30	r
P6/T1/U4/Z (CIVX2)	0.07	4.38	f
P6/T1/U9/Z (CND2IX2)	0.07	4.45	r
P6/T1/U13/Z (CND2X2)	0.10	4.55	f
P6/T1/cout_4 (CSA4_6)	0.00	4.55	f
P6/T2/cin_4 (CSA4_5)	0.00	4.55	f
P6/T2/U6/Z (CIVX2)	0.07	4.62	r
P6/T2/U4/Z (CND2X2)	0.09	4.71	f
P6/T2/U5/Z (CND2X2)	0.10	4.81	r
P6/T2/cout_4 (CSA4_5)	0.00	4.81	r
P6/co8 (CSA8)	0.00	4.81	r
P7/in9 (CSA9)	0.00	4.81	r
P7/V1/cin_3 (CSA3_4)	0.00	4.81	r
P7/V1/U6/Z (CIVX2)	0.07	4.88	f
P7/V1/U9/Z (CND2X2)	0.07	4.95	r
P7/V1/U10/Z (CND2X2)	0.10	5.05	f
P7/V1/cout_3 (CSA3_4)	0.00	5.05	f
P7/V2/cin_3 (CSA3_3)	0.00	5.05	f
P7/V2/U6/Z (CIVX2)	0.07	5.12	r
P7/V2/U4/Z (CND2X2)	0.09	5.22	f
P7/V2/U5/Z (CND2X2)	0.09	5.31	r
P7/V2/cout_3 (CSA3_3)	0.00	5.31	r
P7/V3/cin_3 (CSA3_2)	0.00	5.31	r
P7/V3/U7/Z (CIVX2)	0.08	5.39	f
P7/V3/U9/Z (CND2X2)	0.07	5.46	r
P7/V3/U10/Z (CND2X2)	0.10	5.56	f
P7/V3/cout_3 (CSA3_2)	0.00	5.56	f
P7/co9 (CSA9)	0.00	5.56	f
P8/in10 (CSA10)	0.00	5.56	f
P8/J1/cin_2 (CSA2_1)	0.00	5.56	f
P8/J1/U3/Z (CIVX2)	0.07	5.63	r
P8/J1/U7/Z (CND2X2)	0.09	5.72	f
P8/J1/U8/Z (CND2X2)	0.08	5.80	r
P8/J1/cout_2 (CSA2_1)	0.00	5.80	r
P8/J2/cin_4 (CSA4_4)	0.00	5.80	r
P8/J2/U5/Z (CIVX2)	0.07	5.87	f
P8/J2/U7/Z (CND2IX2)	0.07	5.94	r

P8/J2/U10/Z (CND2X2)	0.12	6.06	f
P8/J2/cout_4 (CSA4_4)	0.00	6.06	f
P8/J3/cin_4 (CSA4_3)	0.00	6.06	f
P8/J3/U3/Z (COND2X1)	0.25	6.31	r
P8/J3/cout_4 (CSA4_3)	0.00	6.31	r
P8/co10 (CSA10)	0.00	6.31	r
P9/in11 (CSA11)	0.00	6.31	r
P9/R1/cin_3 (CSA3_1)	0.00	6.31	r
P9/R1/U8/Z (CIVX1)	0.14	6.46	f
P9/R1/U5/Z (CND2X2)	0.07	6.53	r
P9/R1/U7/Z (CND2X2)	0.12	6.65	f
P9/R1/cout_3 (CSA3_1)	0.00	6.65	f
P9/R2/cin_4 (CSA4_2)	0.00	6.65	f
P9/R2/U7/Z (CIVX2)	0.08	6.73	r
P9/R2/U4/Z (CND2X1)	0.10	6.83	f
P9/R2/U5/Z (CND2X1)	0.18	7.01	r
P9/R2/cout_4 (CSA4_2)	0.00	7.01	r
P9/R3/cin_4 (CSA4_1)	0.00	7.01	r
P9/R3/U3/Z (CIVX2)	0.11	7.12	f
P9/R3/U7/Z (COND2XL)	0.16	7.29	r
P9/R3/cout_4 (CSA4_1)	0.00	7.29	r
P9/co11 (CSA11)	0.00	7.29	r
crout_reg/D (CFD2QXL)	0.00	7.29	r
data arrival time		7.29	
clock clock (rise edge)	8.00	8.00	
clock network delay (propagated)	0.00	8.00	
clock uncertainty	-0.25	7.75	
crout_reg/CP (CFD2QXL)	0.00	7.75	r
library setup time	-0.39	7.36	
data required time		7.36	

data required time		7.36	
data arrival time		-7.29	

slack (MET)		0.07	

1
report_area

```
*****
Report : area
Design : CSA64UEQG
Version: C-2009.06-SP5
Date   : Thu Dec  3 13:10:02 2015
*****
```

Library(s) Used:

tc240c (File:
 /apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25)

Number of ports:	195
Number of nets:	671
Number of cells:	476
Number of references:	17
Combinational area:	2197.500000
Noncombinational area:	1270.000000
Net Interconnect area:	undefined (No wire load specified)

Total cell area:	3467.500000	
Total area:	undefined	
1		
report_power		
Loading	db	file
'/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25'		
Warning:	Main library 'tc240c' does not specify the following unit required for power: 'Leakage Power'. (PWR-424)	
Information:	Propagating switching activity (low effort zero delay simulation). (PWR-6)	
Warning:	Design has unannotated primary inputs. (PWR-414)	
Warning:	Design has unannotated sequential cell outputs. (PWR-415)	

Report : power	
-analysis_effort	low
Design : CSA64UEQG	
Version: C-2009.06-SP5	
Date : Thu Dec 3 13:10:03 2015	

Library(s) Used:

tc240c (File:
 /apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25)

Operating Conditions: WCCOM25 Library: tc240c
 Wire Load Model Mode: top

Global Operating Voltage = 2.3

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000ff

Time Units = 1ns

Dynamic Power Units = 1uW (derived from V,C,T units)

Leakage Power Units = Unitless

Cell Internal Power = 12.4141 mW (93%)

Net Switching Power = 912.2189 uW (7%)

Total Dynamic Power = 13.3263 mW (100%)

Cell Leakage Power = 0.0000

1

write -hierarchy -format verilog -output CSA64UEQG_nl.v
Writing verilog file

'/home/pa/pand2610/Desktop/Project/CSA64UEQG/CSA64UEQG_nl.v'.

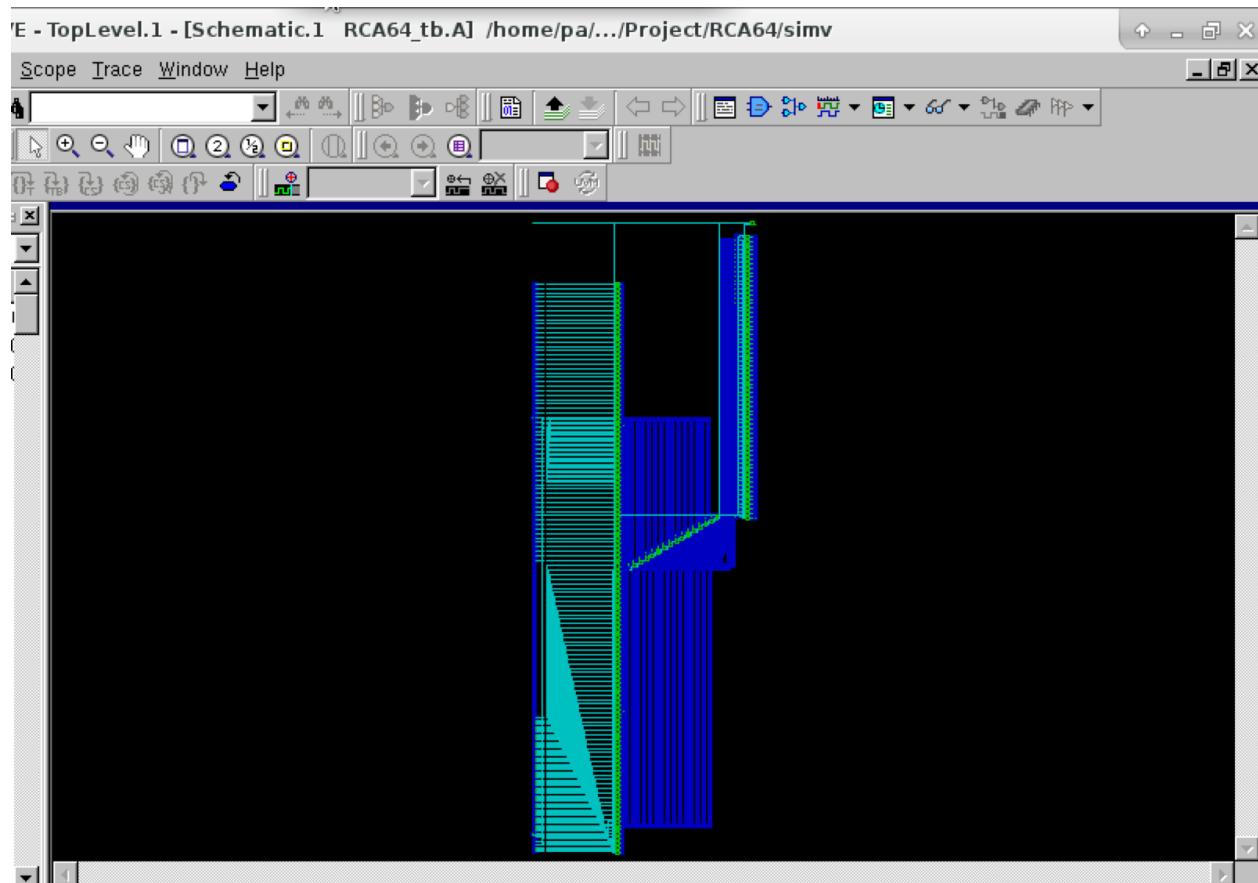
1

quit

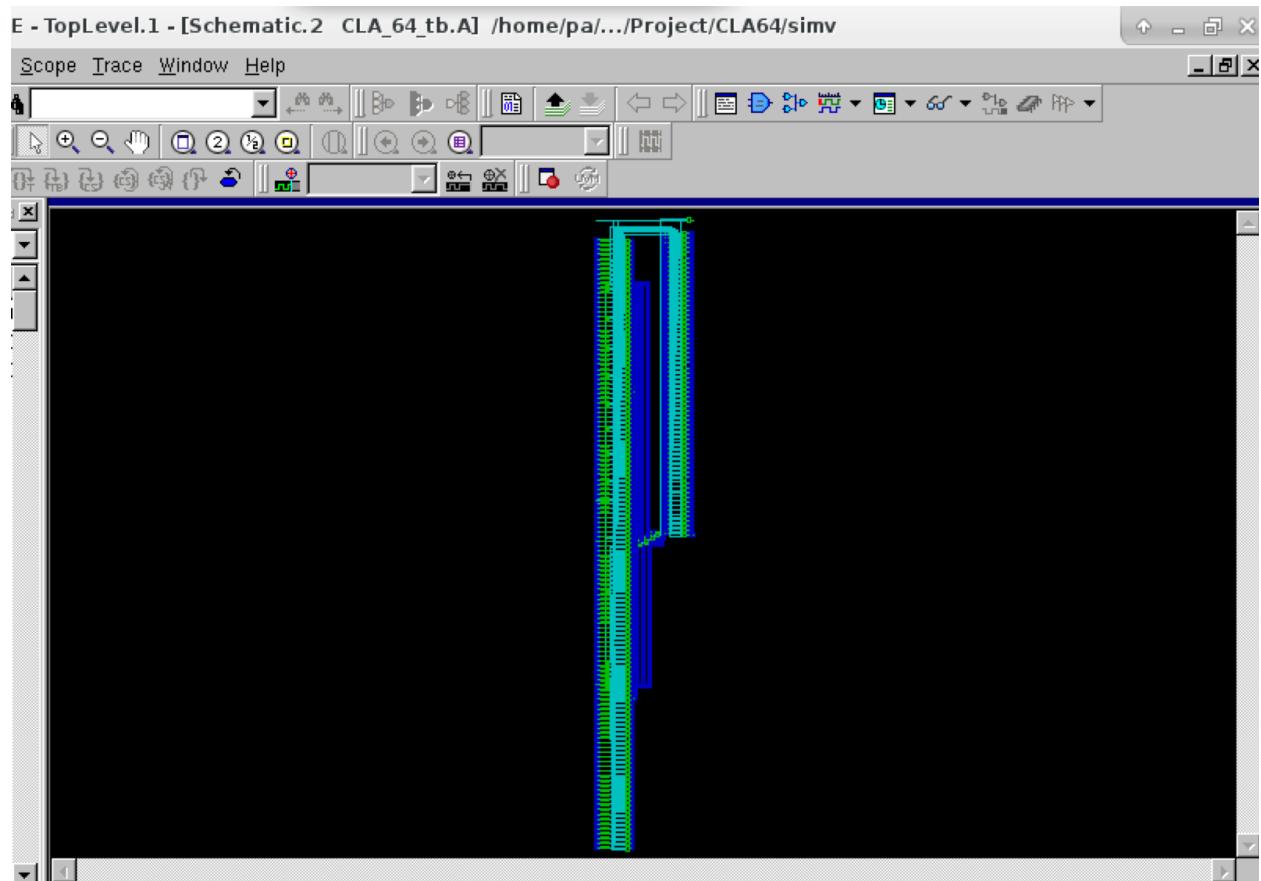
Thank you...

C.4 Screenshot Circuits from Synthesis (Design Compiler)

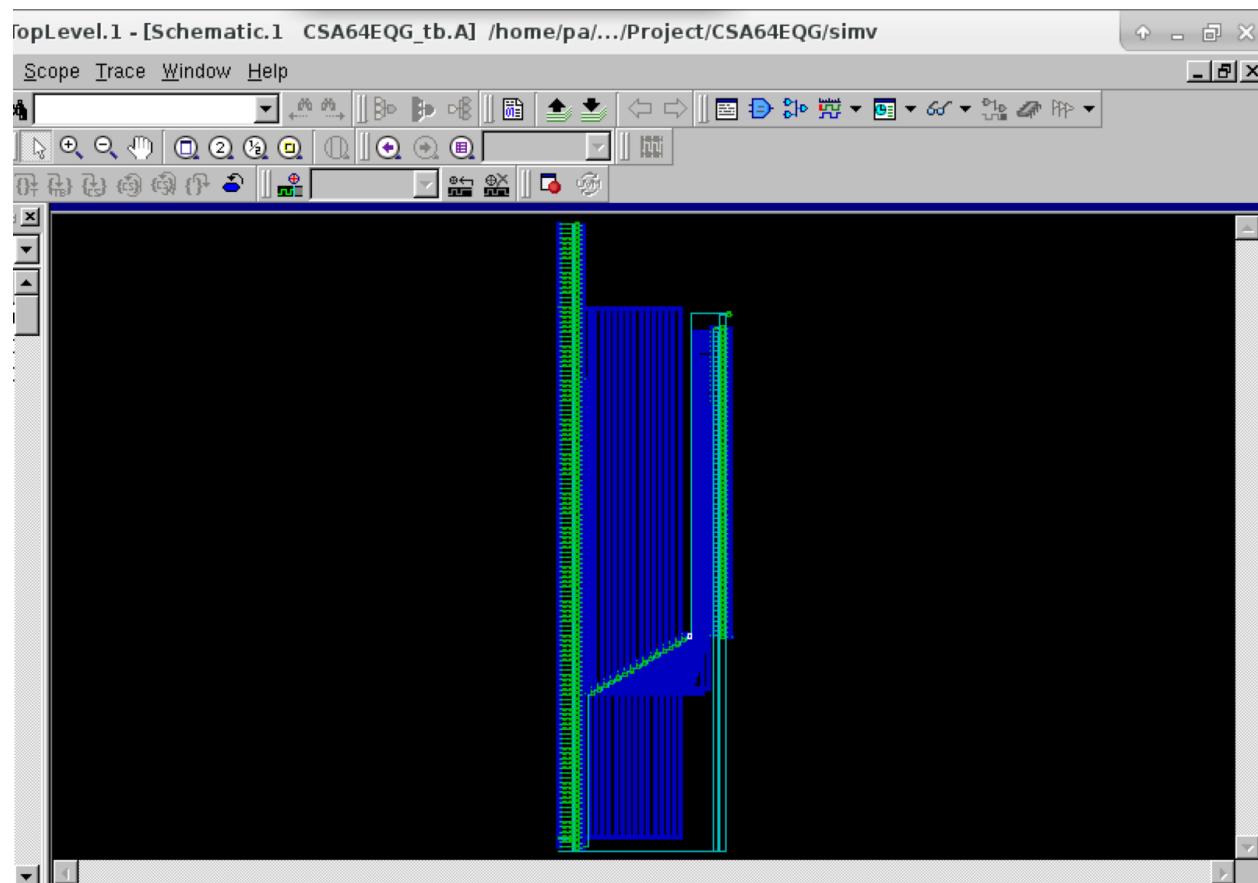
Ripple Carry Adder



Carry Look Ahead Adder



Carry Select Adder Equal Group



Carry Select Adder Unequal Group

