MAXVY's MIPI – I3C Basic Master Controller IP

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RELEASE INFORMATION

Date	Issue	Confidentiality	change
11.06.2019	version-0.5	confidential	-
18.09.2019	version-0.51	confidential	Updated with register controller in AHB_TOP/APB_TOP
21.9.2019	version-0.6	confidential	Updated with IBI and timing registers
06.11.2019	Version-0.61	confidential	Updated with address arbitration support
05.12.2019	Version-0.62	confidential	Updated with Hot Join feature
01.01.2020	Version-0.63	confidential	Updated with removing unused registers
04.01.2020	Version-0.64	confidential	Updating with manufacture register
07.01.2020	Version-0.64	confidential	Updating with debug register
10.01.2020	Version-0.64	confidential	Updating with Bit - Bang register
21.01.2020	Version-0.64	confidential	Updating with Reset register
27.01.2020	Version-0.65	confidential	Updated with clock architecture and drive logic changes

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1 INTRODUCTION:

The MIPI I3C interface has been developed to ease sensor system design architectures in mobile wireless products by providing a fast, low cost, low power, two-wire digital interface for sensors.

1.1 FEATURES:

- Compliance as per MIPI-I3C Basic version 1.0
- Dynamic address assignment
- I3C Host controller compliance as per version 1.0
- SDA arbitration
- Backward compatibility with I2C
- Data transfer with and without broadcast
- All basic CCC command features
- Both push-pull and open drain mode transaction
- Private write and read operations
- In-band Interrupt
- Hot-Join Mechanism
- Secondary Mastership(optional)

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2 BLOCK DIAGRAM:

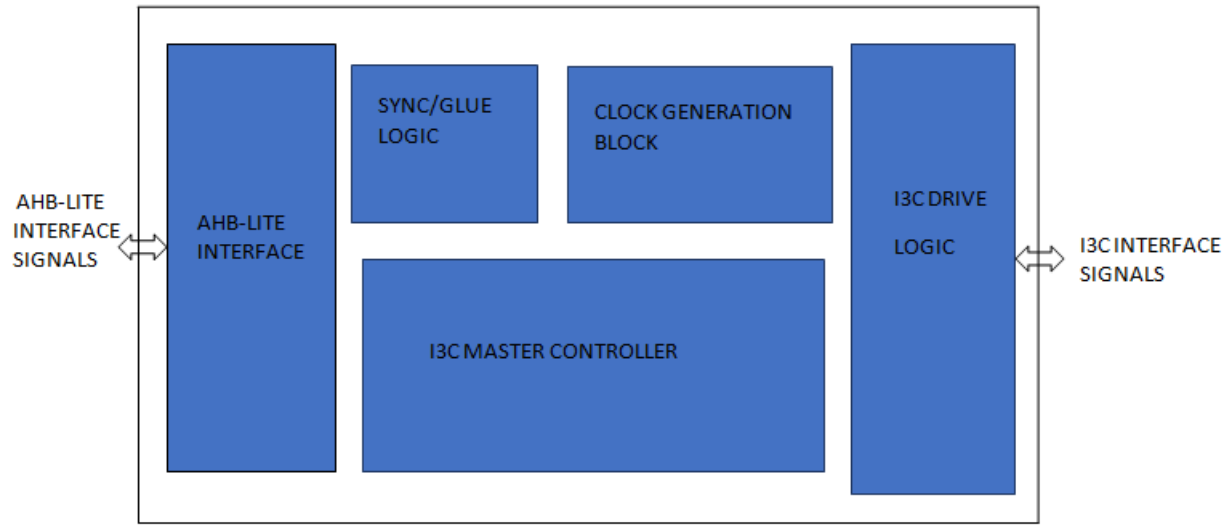

Figure 1: Block Diagram with AHB-LITE INTERFACE

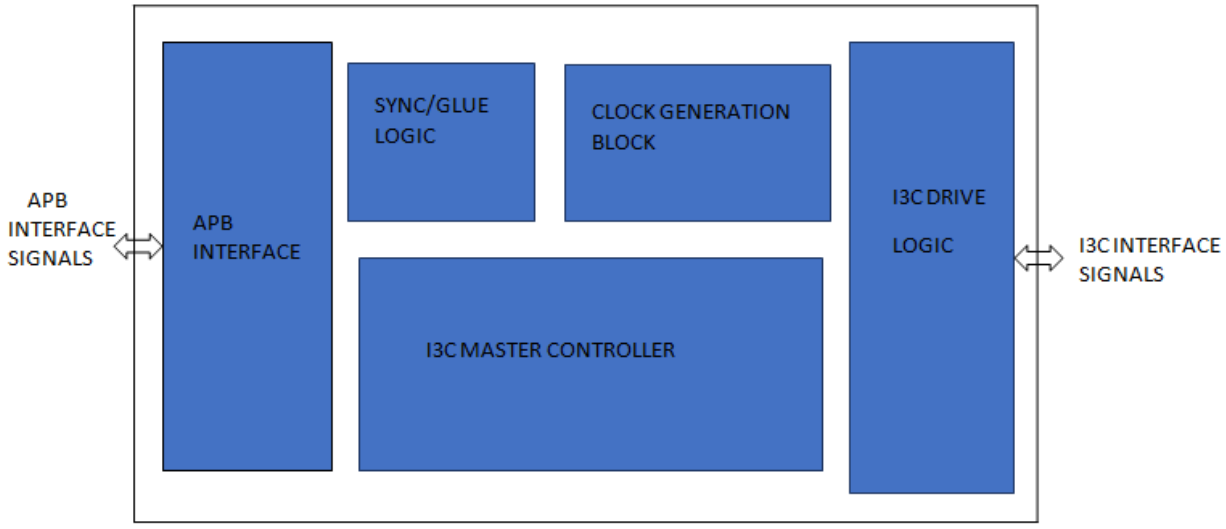

Figure 2: Block Diagram with APB-INTERFACE

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2.1 MAXVY's MIPI-I3C BASIC MASTER CONTROLLER IP WITH RISC-V SUB-SYSTEM

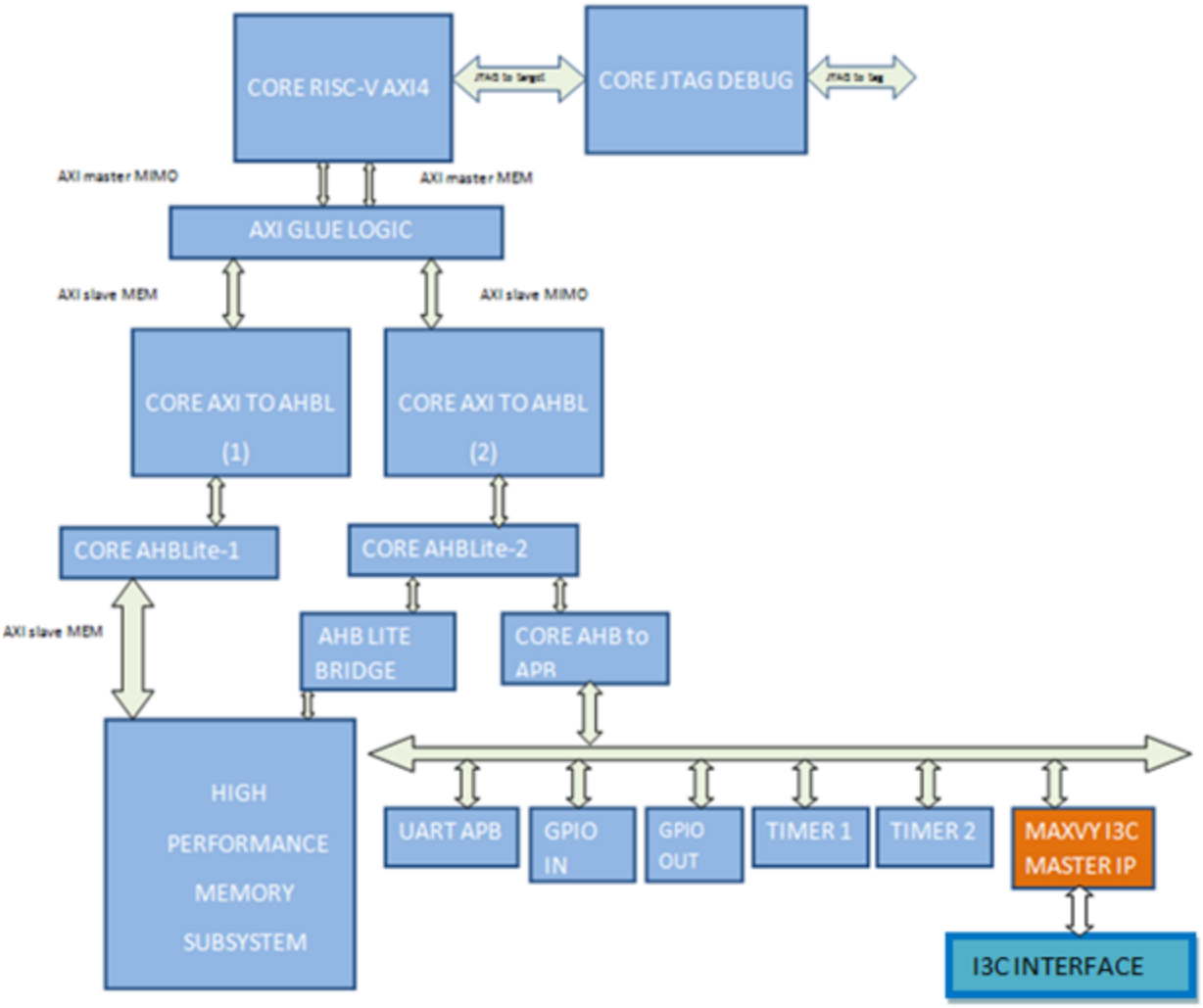

Figure 3: MAXVY 'S MIPI-I3C Basic Master Controller IP with RISC-V Subsystem

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3 BLOCK DESCRIPTION:

This section gives the detailed description about every block.

3.1 AHB-LITE INTERFACE:

The AHB-LITE interface communicates with the I3C Master for the command transfer that includes Address Assignment Command, Immediate Data Transfer, Internal Control Command and Regular Data Transfer.

3.2 SYNC LOGIC:

The Sync/Glue Logic is used to select AHB/APB interface to communicate with I3C.

3.3 CLOCK GENERATION BLOCK:

Clock Generation Block generates the clock for push-pull mode and open-drain mode.

3.4 I3C MASTER CONTROLLER:

I3C Master Controller controls the functions of I3C master through FSM by the control enable signals and also drives and sample the data on SDA line.

3.5 I3C DRIVE LOGIC:

I3C Drive Logic contains all the enable signals and controls the data on SDA line.

3.6 APB INTERFACE:

The APB interface communicates with the I3C Master for the command transfer that includes Address Assignment Command, Immediate Data Transfer, Internal Control Command and Regular Data Transfer. APB interface is used along with RISCV Subsystem for verification using FPGA.

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4 SIGNAL INTERFACES:

Signal interfaces for top-level block and low-level block are described in this section.

4.1 I3C DRIVE LOGIC:

4.1.1 SYSTEM INTERFACE:

Signal Name	Bits	Direction	Description
sys_clk_i	1 bit	Input	System clock input
sys_reset_i	1 bit	Input	System reset input
sys_interrupt_o	1 bit	Output	System Interrupt output

Table 1 System Interface signals

4.1.2 I3C INTERFACE:

Signal Name	Bits	Direction	Description
sda_in_i	1 bit	Input	SDA signal used as input
scl_in_i	1 bit	Input	SCL signal used as input
scl_out_o	1 bit	Output	SCL signal used as output
scl_out_en_o	1 bit	Output	SCL output enable signal
sda_out_o	1 bit	Output	SDA used as output
sda_out_en_o	1 bit	Output	SDA output enable signal

Table 2 I3C Interface Signals

4.1.3 AHB_LITE INTERFACE:

Signal Name	Bits	Direction	Description
hclk_i	1 bit	Input	AHB clock signal
hreset_i	1 bit	Input	AHB reset signal
haddr_i	32 bits	Input	The 32-bit address bus.
hburst_i	3 bits	Input	The burst type indicates if the transfer is a single transfer or forms part of a burst. Fixed length bursts of 4, 8, and 16 beats are supported. The burst can be incrementing or wrapping. Incrementing bursts of undefined length are also supported.
hmastlock_i	1 bit	Input	Not supported. Reserved for Future implementation
hprot_i	1 bit	Input	Not supported. Reserved for Future implementation
hsize_i	3 bits	Input	Indicates the size of the transfer, that

			is typically byte, half word (16 bits), or word (32 bits).
htrans_i	2 bits	Input	Indicates the transfer type of the current transfer. This can be: 2'b00 for IDLE 2'b01 for BUSY 2'b10 for NONSEQUENTIAL 2'b11 for SEQUENTIAL.
hwdata_i	32 bits	Input	The write data bus transfers data from the master to the slaves during write operations.
hwrite_i	1 bit	Input	Indicates the transfer direction. 1 for Write 0 for Read
hsel_i	1 bit	Input	Slave select signal, which indicates current transfer is intended for this slave.
hrdata_o	32 bits	Output	The read data bus stores the data from the slaves during read operation.
hready_o	1 bit	Output	When HIGH, the HREADY signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend a transfer.
hresp_o	1 bit	Output	Provide the status of a transfer. When LOW, the HRESP signal indicates that the transfer status is OKAY. When HIGH, the HRESP signal indicates that the transfer status is ERROR.

Table 3 AHB-Lite Interface Signals

4.1.4 APB INTERFACE:

Signal Name	Bits	Direction	Description
PRESETN_i	1 bit	Input	Reset. The APB reset signal is active LOW. This signal is normally connected directly to the system bus reset signal.
PCLK_i	1 bit	Input	Clock. The rising edge of PCLK times all transfers on the APB
PADDR_i	8 bits	Input	Address. This is the APB address bus. It can be up to 32 bits wide and is

			driven by the peripheral bus bridge unit.
PWDATA_i	32 bits	Input	Write data. This bus is driven by the peripheral bus bridge unit during write cycles when PWRITE is HIGH. This bus can be up to 32 bits wide.
PWRITE_i	1 bit	Input	This signal indicates an APB write access when HIGH and an APB read access when LOW.
PSEL_i	1 bit	Input	Select. The APB bridge unit generates this signal to each peripheral bus slave. It indicates that the slave device is selected and that a data transfer is required.
PENABLE_i	1 bit	Input	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
PRDATA_o	32 bits	Output	Read Data. The selected slave drives this bus during read cycles when PWRITE is LOW. This bus can be up to 32-bits wide.
PREADY_o	1 bit	Output	Ready. The slave uses this signal to extend an APB transfer.
PSLVERR_o	1 bit	Output	This signal indicates a transfer failure.

Table 4 APB Interface Signals

5 REGISTER MAP:

5.1EXTERNALLY DEFINED REGISTERS: (FOR APB INTERFACE)

All registers are 32-bit wide.

Register name	**Address Offset**	**Memory access**	**Reset value**	**Description**
Ideal time register	0x0000	W	0x0	Ideal count time value which has to be maintained during I3C transaction
Clock port register	0x0004	W	0x0	Clock port register give the values of push pull and open drain mode clock divisions

				[7:0]->push pull clock division value *2 for division by 4 [15:8]->open drain clock division value *16 for division by 32 *Note: Give value as 1002 in hex value*
Broadcast address register	0x0008	W	0x0	The Broadcast address register contains 7'h7E broadcast address value.
Command transfer register0	0x000C	W	0x0	The command transfer register0 indicates the lower 32 bits of command transfer values which is totally 64 bits, Immediate command, Regular command, Address assignment command, Internal control command. *Note*
Command transfer register1	0x0010	W	0x0	The command transfer register1 indicates the upper 32 bits of command transfer values such as Immediate command, Regular command, Address assignment command, Internal control command. *Note:*
Write data port register	0x0014	W	0x0	DATA write register which has the data to be sent from I3C transaction
Read data port register	0x0018	R	0x0	DATA read register which has the value read by I3C during read transaction.
Reserved	0x001C	NA	NA	Reserved for future implementation
Reserved	0x0020	NA	NA	Reserved for future implementation
Reserved	0x0024	NA	NA	Reserved for future implementation
Reserved	0x0028	NA	NA	Reserved for future implementation
Reserved	0x002C	NA	NA	Reserved for future implementation
Reserved	0x0030	NA	NA	Reserved for future implementation
Reserved	0x0034	NA	NA	Reserved for future implementation
Interrupt status register	0x0038	R/W	0x0	The Interrupt Status register reflects the status of outstanding interrupt(s). Bit 0:ahb_wr_almost_empty Bit 1:ahb_wr_empty Bit 2:ahb_wr_almost_full Bit 3:ahb_wr_full Bit 4:comm_fifo_empty

				Bit 5:comm_fifo_full Bit 6:ahb_rd_full Bit 7:ahb_rd_empty Bit 15:8:ahb_wr_fifo Bit 23:16:ahb_rd_fifo Bit24:apb_idal_time_finish Bit 25:Overwrite_idle_en Bit 26:res_wr_full Bit 27:res_wr_empty Bit 28:ibi_interrupt Bit 29:hot-join interrupt Bit 30:cmd_complete_interrupt Bit 31:bus_idle_condition
Interrupt signal enable register	0x0040	R/W	0x0	The Interrupt Signal enable register reflects the status of interrupt(s). Bit 0: enable signal for ahb_wr_almost_empty Bit 1: enable signal for ahb_wr_empty Bit 2: enable signal for ahb_wr_almost_full Bit 3: enable signal for ahb_wr_full Bit 4: enable signal for comm_fifo_empty Bit 5: enable signal for comm_fifo_full Bit 6: enable signal for ahb_rd_full Bit 7: enable signal for ahb_rd_empty Bit 15:8: enable signal for ahb_wr_fifo Bit 23:16: enable signal for ahb_rd_fifo Bit24: enable signal for apb_idal_time_finish Bit 25: enable signal for Overwrite_idle_en Bit 26: enable signal for res_wr_full Bit 27: enable signal for res_wr_empty Bit 28: enable signal for ibi_interrupt Bit 29: enable signal for hot-join interrupt Bit 30: enable signal for cmd_complete_interrupt Bit 31: enable signal for bus_idle_condition
Debug read register_0	0x0044	R	0x0	Debug data read register indicates lower 32 bits of 64 bits debug read

				data, which has the functional and FSM signal informations for debug purpose.
Debug read register_1	0x0048	R	0x0	Debug data read register indicates upper 32 bits of 64 bits debug read data, which has the functional and FSM signal informations for debug purpose.
Device address table_0	0x004C	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 0 *Note: on 64 bit, only least 32 bit are taken*
Device address table_1	0x0050	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 1
Debug control enable register	0x0054	W	0x0	The Debug control enable register is to enable the debug modes during I3C transaction
Hj_feature_reg	0x0058	NA	NA	This register is used for setting the hot join acknowledgement from the interface Bit 0: hot_join ack Bit 1:ibi ack enable Bit 2:ibi read byte
Ibi_status_register	0x005c	R	0x0	This register is to read the status during IBI transition Bit 31:IBI received status 1:NACK 0:ACK Bit 24:Last IBI status Bit 15:8:IBI received ID
Device address table_2 to Device address table_31	-	NA	NA	Reserved for future implementation
Device characteristics table_0	0x0070	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*

Device characteristics table_1	0x0074	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_2	0x0078	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_3	0x007C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_4 to Device characteristics table_63	-	NA	NA	Reserved for future implementation
Response Read Register	0x0080	R/W	0x0	Response Read Register will show the status of transaction id, remaining data length and error status
Debug register	0x0084	R/W	0x0	Register for debug purpose
Reserved	0x0088-0x009c	NA	NA	Reserved for future implementation
Pio_interrupt_signal_enable_reg	0x00A0	R/W	0x0	This register is used for setting the in-band interrupt request from the interface
Reserved	0x00A4-0x00D0	NA	NA	Reserved for future implementation
Reset_register	0x00d4	R/W	0x0	Bit[0]: Soft_reset Bit[1]: Wr_FIFO_reset Bit[2]:Rd_FIFO_reset Bit[3]:cmd_FIFO_reset
Hot_join_command_addr0_reg	0x00D8	R/W	0X0	This register is used for the hot-join command to be processed during hot

				join interrupt.
Hot_join_command_addr1_reg	0x00DC	R	0X0	This register is used for the hot-join command to be processed during hot join interrupt.
timing_reg	0x00E0	R/W	0x0	Reserved for future implementation
watch_dog_timer_reg	0x00E4	R/W	0x0	Reserved for future implementation
Sdr_error_reg	0x00E8	R/W	0x0	Reserved for future implementation
Configuration_reg	0X00EC	R/W	0x0	Reserved for future implementation
Maxvy versionid	0x00F0	R/W	0x0	Reserved for future implementation
Maxvy register	0x00F4	R/W	0x0	Reserved for future implementation
Bit-bang register	0x00F8	R/W	NA	Reserved for future implementation
Mas_sla_reg	0x00FC	R/W	0x0	Reserved for future implementation

Table 5 APB Interface Signals

5.1.1 COMMAND TRANSFER REGISTER 0:

Bits	Field name	Memory access	Reset value	Description
31	TOC	W	0x0	if **bit[2:0]=0x0 ,0x1 and 0x2** then bit[31] is Terminate on Completion · 1'b0-repeated start after data transfer · 1'b1- stop after data transfer If **bit[2:0]=0x7** then bit[31] =MIPI Reserved
30	ROC	W	0x0	if **bit[2:0]=0x0 ,0x1 and 0x2** then bit[31] is Response on Completion · 1'b0-not required · 1'b1-required If **bit[2:0]=0x7** then bit[31] =MIPI Reserved

29:26	DEV_COUNT/RNW/ MODE	W	0x0	If **bit[2:0]=0x0** then
				bit[29]=RNW
				• 0-Write
				• 1-Read
				If **bit[2:0]=0x1**then
				bit[29]=RNW(should always be write only)
				• 0-Write
				bit[28:26]=MODE
				• 0x0-sdr0-12.5MHZ
				• 0x1-sdr1-8MHZ
				• 0x2-sdr2-6MHZ
				• 0x3-sdr3-4MHZ
				• 0x4-sdr4-2MHZ
				• 0x5-HDR_TS
				• 0x6-HDR_DDR
				If **bit[2:0]=0x2** then
				bit[29:26] = Device count
				if **bit[2:0]=0x7** then
				bit[29:26] =MIPI Reserved

25:21	BYTE_COUNT	-	-	If **bit[2:0]=0x0** then
				bit[25:21] = RESERVED
				if **bit[2:0]=0x1** then
				bit[25:23]=BYTE_COUNT
				• 0:No Payload
				• 1-4:N bytes are valid
				• 5-7:Reserved values, do not use
				bit[23:21]=RESERVED
				if **bit[2:0]=0x2** then
				bit[25:21]=RESERVED
				if **bit[2:0]=0x7** then
				bit[25:21]=RESERVED

20:16	DEV_INDEX	W	0x0	If **bit[2:0]=0x0,0x1,0x2** then
				bit[20:16]=Device index. Static and device addressing related information will be stored to this index in the DAT.
				If **bit[2:0]=0x7** then
				bit[20:16]=MIPI Reserved

15	CP	W	0x0	If **bit[2:0]=0x0 and 0x1** then bit[15]=command present • 0-SDR transfer • 1-HDR transfer If **bit[2:0]=0x2** then bit[15]=RESERVED If **bit[2:0]=0x7** then bit[15]=MIPI Reserved
14:7	CMD	W	0x0	If **bit[2:0]=0x0 and 0x1** then bit[14:7]=CMD indicates whether CCC is valid for CCC or HDR • For CCC:8bits • For HDR:7 bits If **bit[2:0]=0x2** then bit[14:7]=Transfer Command CCC Value indicate whether address assignment uses ENTDAA or SETDASA commands. If **bit[2:0]=0x7** then bit[14:13]=MIPI Reserved bit[12]=ON-OFF • 0-IBA-off • 1-IBA-on bit[11:8]=MIPI_CMD • 0-Reserved • 1-Reserved • 2-Include 7E(IBA) • 3-Reserved bit[7]=Vendor info
6:3	TID	W	0x0	Transaction ID
2:0	CMD_ATTR	W	0x0	**Command Attributes** Command Type, defining the format of the other fields. **Values:** • 0x0: XFER: Regular Transfer • 0x1: IMMED_DATA_XFER: Immediate Data Transfer • 0x2: ADDR_ASSGN_CMD: Address Assignment Command • 0x3: WWR_COMBO_XFER: Write + Write/Read Combo

				Transfer • 0x4–0x6: Reserved, do not use • 0x7: INTERNAL_CONTROL: Internal Control command

5.1.2 COMMAND TRANSFER REGISTERS 1:

Bits	Field name	Memory access	Reset value	Description
(32+)31:24	DATA_BYTE_4	W	0x0	If **bit[2:0]=0x0** then bit[63:56]=Data Transfer Length. If **bit[2:0]=0x1** then bit[63:56]= Data Byte4 If **bit[2:0]=0x2** then bit[63:56]=RESERVED If **bit[2:0]=0x7** then bit[63:56]= Vendor Specific
(32+)23:16	DATA_BYTE_3	W	0x0	If **bit[2:0]=0x0** then bit[55:48]=Data Transfer Length. If **bit[2:0]=0x1** then bit[55:48]=Data Byte3 If **bit[2:0]=0x2** then bit[55:48]=RESERVED If **bit[2:0]=0x7** then bit[55:48]=Vendor Specific
(32+)15:8	DATA_BYTE_2	W	0x0	If **bit[2:0]=0x0** then bit[47:40]= RESERVED. If **bit[2:0]=0x1** then bit[47:40]=Data Byte2 If **bit[2:0]=0x2** then bit[47:40]=RESERVED If **bit[2:0]=0x7** then bit[47:40]=Vendor Specific
(32+)7:0	DATA_BYTE_1	W	0x0	If **bit[2:0]=0x0** then bit[39:32]= RESERVED. If **bit[2:0]=0x1** then bit[39:32]= Data Byte1

				If **bit[2:0]=0x2** then
				bit[39:32]= RESERVED
				If **bit[2:0]=0x7** then
				bit[39:32]= Vendor Specific

5.1.3 DEVICE ADDRESS TABLE_0:

Bits	Field name	Memory access	Reset value	Description
31	device	R/W	0x0	Device type values 0x0 i3c device 0x1 i2c device
30:29	Dev_nack_retry_cnt	R/W	0x0	Reserved for future implementation
28:26	Ring_id	R/W	0x0	Reserved for future implementation
25:24	reserved	R/W	0x0	-
23:16	Dynamic address	R/W	0x0	Device i3c dynamic address
15	TS	R/W	0x0	Reserved for future implementation
14	MR reject	R/W	0x0	Reserved for future implementation
13	SIR reject	R/W	0x0	Reserved for future implementation
12	IBI payload	R/W	0x0	Reserved for future implementation
11:7	reserved	R/W	0x0	-
6:0	Static address	R/W	0x0	Device static address i3c/i2c static address

5.1.3 DEVICE ADDRESS TABLE_1:

Bits	Field name	Memory access	Reset value	Description
(32+) 31:0	reserved	R/W	0x0	Reserved for future implementation

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5.1.4 DEVICE CHARACTERISTICS TABLE_0:

Bits	Field name	Memory access	Reset value	Description
31:0	PID	R	0x0	Device provisional id High which contains PID data of bit[48:16]

5.1.5 DEVICE CHARACTERISTICS TABLE_1:

Bits	Field name	Memory access	Reset value	Description
(32+)31:16	Reserved	-	-	-
(32+)15:0	PID	R	0x0	Device provisional id High which contains PID data of bit[15:0]

5.1.6 DEVICE CHARACTERISTICS TABLE_2:

Bits	Field name	Memory access	Reset value	Description
(64+)31:16	Reserved	-	-	-
(64+)15:8	BCR	R	0x0	Device bus characteristic register
(64+)7:0	DCR	R	0x0	Device i3c device characteristic register

5.1.7 DEVICE CHARACTERISTICS TABLE_3:

Bits	Field name	Memory access	Reset value	Description
(96+)31:8	Reserved	-	-	-
(96+)7:0	Dynamic address	R	0x0	Device i3c dynamic address include parity bit

5.1.8 RESPONSE READ PORT REGISTER:

Bits	Field Name	Memory Access	Rest Value	Descriptor
31:28	ERR_STATUS	R	0x0	Response Error Status • 0x0: SUCESS: Transfer successful no error • 0x1: CRC: CRC Error • 0x2: PARITY: Parity error • 0x3: FRAME: Frame Error • 0x4: ADDR_HEADER: Address Header Error • 0x5: NACK: Address Nack ed or Dynamic address Nacked • 0x6: OVL: Receive overflow or underflow error • 0x7:RESERVED • 0x8: ABORTED: Aborted • 0x9: I2C_WR_DATA_NACK: Nack received for I2C write data transfer • 0xA:NOT_SUPPORTED • 0xB: RESERVED
27:24	TID	R	0x0	Identification tag for the command. This value match one of the command sent on the Bus • 0x0-0x7: Valid Transaction Ids • 0x8-0xF: Reserved
23:16	RESERVED	-	-	-
15:0	DATA_LENGTH	R	0x0	Data length/Device Count • For write transfer: Remaining data length(in bytes) • For Read transfer: Received data length(in bytes) • For address assignment: Remaining Device count

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5.1.9 PIO_INTERRUPT_SIGNAL_ENABLE_REG:(Not used)

Bits	Field Name	Memory Access	Rest Value	Descriptor
31:10	Reserved	-	-	-
9	TRANSFER_ ERR_SIGNAL_ EN	R/W	0X0	When set to 1'b1 & field TRANSFER_ERR_STAT is set, asserts interrupt to host.
8:6	Reserved	-	-	-
5	TRANSFER_ ABORT_ SIGNAL_EN	R/W	0X0	When set to 1'b1 & field TRANSFER_ABORT_SIGNAL_ENi s set, asserts interrupt to host.
4	RESP_READY_SIG NAL_EN	R/W	0X0	When set to 1'b1 & field RESP_READY_SIGNAL_ENis set, asserts interrupt to host.
3	CMD_QUEUE_RE ADY_ SIGNAL_EN	R/W	0X0	When set to 1'b1 & field CMD_QUEUE_READY_SIGNAL_E Nis set, asserts interrupt to host.
2	IBI_THLD_ SIGNAL_EN	R/W	0X0	When set to 1'b1 & field IBI_THLD_SIGNAL_ENis set, asserts interrupt to host.
1	RX_THLD_ SIGNAL_EN	R/W	0X0	When set to 1'b1 & field RX_THLD_SIGNAL_ENis set, asserts interrupt to host.
0	TX_THLD_ SIGNAL_EN	R/W	0X0	When set to 1'b1 & field TX_THLD_SIGNAL_ENis set, asserts interrupt to host.

5.2.0 IBI_STATUS_REG: (IBI_ID only used. Other field is Not Used)

Bits	Field Name	Memory Access	Rest Value	Descriptor
31	IBI_STS	R	0X0	1:nack 0:ack
30:29	RESERVED	R	0X0	-
28:26	HW_CONTEXT	R	0X0	Hardware specific context for IBI processing
25	TS	R	0X0	1:on 0:off
24	LAST_STATUS	R	0X0	Last IBI status for IBI transaction
23:16	CHUNKS	R	0X0	IBI valid chunks count
15:8	IBI_ID	R	0X0	IBI received ID **For slave interrupt or Master Request**: bits 15:9 contains slave device address and bit 8 contains r/w'

				bit **For Hot-Join IBI:** Bits 15:8 contain the hot-join ID for the IBI
7:0	DATA_LENGTH	R	0X0	IBI Data Length **For PIO Mode:** Number of data bytes in IBI Data **For DMA Mode:** Number of data bytes in the last data chunk

5.2.1 TIMING REGISTER:

Bits	Field Name	Memory Access	Rest Value	Descriptor
32:24	RESERVED	-	0x0	Reserved for future implementation
23:16	RESERVED	-	0x0	Reserved for future implementation
15:12	TCOUNT_REPEATEDSTART	R/W	0x0	Timing to be maintained after repeated start
11:9	TCOUNT_PUSHPULL	R/W	0x0	Timing to be maintained during push-pull mode
8:6	TCOUNT_OD	R/W	0x0	Timing to be maintained during open drain mode
5:3	TCOUNT_STOP	R/W	0x0	Timing to be maintained during stop state
2:0	TCOUNT_START	R/W	0x0	Timing to be maintained during start state

6 EXTERNALLY DEFINED REGISTERS: (FOR AHB INTERFACE)

All registers are 32-bit wide.

MAXVY's MIPI – I3C Basic Master Controller IP

Register name	Address Offset	Memory access	Reset value	Description
Ideal time register	0x0000	W	0x0	Ideal count time value which has to be maintained during I3C transaction
Clock port register	0x0004	W	0x0	Clock port register give the values of push pull and open drain mode clock divisions [7:0]->push pull clock division value *2 for division by 4 [15:8]->open drain clock division value *16 for division by 32 *Note: Give value as 1002 in hex value*
Reserved	0x0008	NA	0x0	Reserved for future implementation
Command transfer register0	0x000C	W	0x0	The command transfer register0 indicates the lower 32 bits of command transfer values which is totally 64 bits, Immediate command, Regular command, Address assignment command, Internal control command. *Note*
Command transfer register1	0x0010	W	0x0	The command transfer register1 indicates the upper 32 bits of command transfer values such as Immediate command, Regular command, Address assignment command, Internal control command. *Note:*
Write data port register	0x0014	W	0x0	DATA write register which has the data to be sent from I3C transaction
Read data port register	0x0018	R	0x0	DATA read register which has the value read by I3C during read transaction.
Reserved	0x001C-0x0034	NA	0x0	Reserved for future implementation

Interrupt status register	0x0038	R/W	0x0	The Interrupt Status register reflects the status of outstanding interrupt(s). Bit 0:ahb_wr_almost_empty Bit 1:ahb_wr_empty Bit 2:ahb_wr_almost_full Bit 3:ahb_wr_full Bit 4:comm_fifo_empty Bit 5:comm_fifo_full Bit 6:ahb_rd_full Bit 7:ahb_rd_empty Bit 15:8:ahb_wr_fifo Bit 23:16:ahb_rd_fifo Bit24:apb_idal_time_finish Bit 25:Overwrite_idle_en Bit 26:res_wr_full Bit 27:res_wr_empty Bit 28:ibi_interrupt Bit 29:hot-join interrupt Bit 30:cmd_complete_interrupt Bit 31:bus_idle_condition(not implemented)
Interrupt signal enable register	0x0040	R/W	0x0	The Interrupt Signal enable register reflects the status of interrupt(s). Bit 0: enable signal for ahb_wr_almost_empty Bit 1: enable signal for ahb_wr_empty Bit 2: enable signal for ahb_wr_almost_full Bit 3: enable signal for ahb_wr_full Bit 4: enable signal for comm_fifo_empty Bit 5: enable signal for comm_fifo_full Bit 6: enable signal for ahb_rd_full Bit 7: enable signal for ahb_rd_empty Bit 15:8: enable signal for ahb_wr_fifo Bit 23:16: enable signal for ahb_rd_fifo Bit24: enable signal for apb_idal_time_finish Bit 25: enable signal for Overwrite_idle_en Bit 26: enable signal for res_wr_full Bit 27: enable signal for res_wr_empty

				Bit 28: enable signal for ibi_interrupt Bit 29: enable signal for hot-join interrupt Bit 30: enable signal for cmd_complete_interrupt Bit 31: enable signal for bus_idle_condition
Reserved	0x0044-0x0048	NA	NA	Reserved for future implementation
Device address table_0	0x004C	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 0 *Note: on 64 bit, only least 32 bit are taken*
Device address table_1	0x0050	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 1 *Note: on 64 bit, only least 32 bit are taken*
Device address table_2	0x014C	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 2 *Note: on 64 bit, only least 32 bit are taken*
Device address table_3	0x0150	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 3 *Note: on 64 bit, only least 32 bit are taken*
Device address table_4	0x024C	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 4 *Note: on 64 bit, only least 32 bit are taken*
Device address table_5	0x0250	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 5 *Note: on 64 bit, only least 32 bit are taken*
Device address table_6	0x034C	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 6 *Note: on 64 bit, only least 32 bit are*

				taken
Device address table_7	0x0350	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 7 *Note: on 64 bit, only least 32 bit are taken*
Device address table_8	0x044C	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 8 *Note: on 64 bit, only least 32 bit are taken*
Device address table_9	0x0450	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 9 *Note: on 64 bit, only least 32 bit are taken*
Device address table_10	0x054C	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 10 *Note: on 64 bit, only least 32 bit are taken*
Device address table_11	0x0550	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 11 *Note: on 64 bit, only least 32 bit are taken*
Device address table_12	0x064C	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 12 *Note: on 64 bit, only least 32 bit are taken*
Device address table_13	0x0650	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 13 *Note: on 64 bit, only least 32 bit are taken*
Device address table_14	0x074C	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 14 *Note: on 64 bit, only least 32 bit are taken*

Device address table_15	0x0750	R/W	0x0	DAT table stores the address, information and control fields of device attached to I3C bus for slave 15 *Note: on 64 bit, only least 32 bit are taken*
Reserved	-	R/W	0x0	Reserved for future implementation
Hj_feature_reg	0x0058	NA	NA	This register is used for setting the hot join acknowledgement from the interface Bit 0: hot_join ack Bit 1:ibi ack enable Bit 2:ibi read byte
Ibi_status_register	0x005c	R	0x0	This register is to read the status during IBI transition Bit 31:IBI received status 1:NACK 0:ACK Bit 24:Last IBI status Bit 15:8:IBI received ID
Reserved	0x0064-0x006c	NA	NA	Reserved for future implementation
Device characteristics table_0	0x0070	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_1	0x0074	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_2	0x0078	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*

Device characteristics table_3	0x007C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_4	0x0170	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_5	0x0174	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_6	0x0178	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_7	0x017C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_8	0x0270	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_9	0x0274	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*

Device characteristics table_10	0x0278	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_11	0x027C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_12	0x0370	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_13	0x0374	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_14	0x0378	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_15	0x037C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_16	0x0470	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*

Device characteristics table_17	0x0474	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_18	0x0478	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_19	0x047C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_20	0x0570	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_21	0x0574	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_22	0x0578	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_23	0x057C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*

Device characteristics table_24	0x0670	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_25	0x0674	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_26	0x0678	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_27	0x067C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_28	0x0770	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_29	0x0774	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_30	0x0778	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*

Device characteristics table_31	0x077C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_32	0x0870	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_33	0x0874	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_34	0x0878	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_35	0x087C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_36	0x0970	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_37	0x0974	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*

Device characteristics table_38	0x0978	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_39	0x097C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_40	0x0A70	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_41	0x0A74	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_42	0x0A78	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_43	0x0A7C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_44	0x0B70	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*

Device characteristics table_45	0x0B74	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_46	0x0B78	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_47	0x0B7C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_48	0x0C70	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_49	0x0C74	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_50	0x0C78	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_51	0x0C7C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*

Device characteristics table_52	0x0D70	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_53	0x0D74	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_54	0x0D78	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_55	0x0D7C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_56	0x0E70	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_57	0x0E74	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_58	0x0E78	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*

Device characteristics table_59	0x0E7C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_60	0x0F70	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_61	0x0F74	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_62	0x0F78	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Device characteristics table_63	0x0F7C	R/W	0x0	DCT table captures the device characteristics (PID, BCR, DCR) and assigned dynamic address for the device attached to I3C. *Note: Each device contains 4 DCT table.*
Response Read Register	0x0080	R/W	0x0	Response Read Register will show the status of transaction id, remaining data length and error status
Debug register	0x0084	R/W	0x0	Reserved for future implementation
Reserved	0x0088-0x009C	R/W	0x0	Reserved for future implementation
Pio_interrupt_signal_enable_reg	0x00A0	R/W	0x0	This register is used for setting the in-band interrupt request from the interface

Reset_register	0x00d4	R/W	0x0	Bit[0]: Soft_reset Bit[1]: Wr_FIFO_reset Bit[2]:Rd_FIFO_reset Bit[3]:cmd_FIFO_reset
Hot_join_command_addr0_reg	0X00D8	R/W	0X0	This register is used for the hot-join command to be processed during hot join interrupt.
Hot_join_command_addr1_reg	0X00DC	R	0X0	This register is used for the hot-join command to be processed during hot join interrupt.
Timing_Reg	0x00E0	R/W	0x0	Reserved for future implementation
Watch_Dog_Timer_Reg	0x00E4	R/W	0x0	Reserved for future implementation
Sdr_Error_Reg	0x00E8	R/W	0x0	Reserved for future implementation
Configuration_Reg	0x00EC	R/W	0x0	Reserved for future implementation
Maxvy version	0x00F0	R/W	0x0	Reserved for future implementation
Maxvy register	0x00F4	R/W	0x0	Reserved for future implementation
Bit-Bang register	0x00F8	R/W	0x0	Reserved for future implementation
Master_slave_reg	0x00FC	R/W	0x0	Reserved for future implementation

Table 6 AHB Interface Signals

7 CONTACT INFORMATION:

Email:

MAXVY's MIPI – I3C Basic Master Controller IP

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Web:

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