BENNETT UNIVERSITY
THE TIMES GROUP

Enrolment No: _____

Name of Student: _____

Department/ School: _____

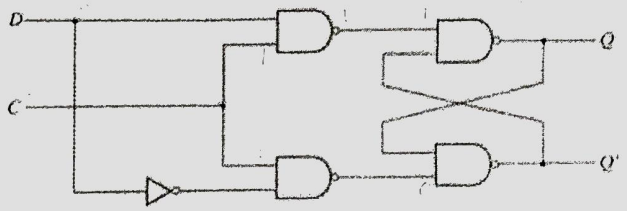
END TERM EXAMINATION EVEN SEMESTER 2021-22

COURSE CODE	**CSET105**	**MAX. DURATION**	**2 HRS**
COURSE TITLE	**Digital Design**		
COURSE CREDIT	**3-0-2**	**TOTAL MARKS**	**35**

GENERAL INSTRUCTIONS: -

1. Do not write anything on the question paper except **name, enrolment number** and **department/school.**
2. Carrying mobile phone, smart watch and any other non-permissible materials in the examination hall is an act of **UFM.**

Q1. (a). Construct truth table of the given logic diagram. Where (D- Input, C- Clock, Q and Q'- Outputs). **[3]**

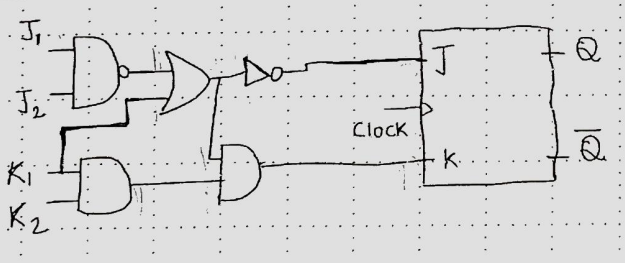


(b). Explain in one sentence.

1. Drawback with S-R Flipflop.
2. Drawback with J-K Flipflop.

Q2. The Following serial data are applied to FF shown in Figure. Determine the resulting serial data that appears at Q output. There is one clock pulse for each bit time. Assume initially Q=0. **[4]**

CLOCK	J1	J2	~~J3~~ K1	~~J4~~ K2	Q	$\bar{Q}$
1st	1	1	1	1	?	?
2nd	0	1	0	1	?	?
3rd	1	0	0	0	?	?



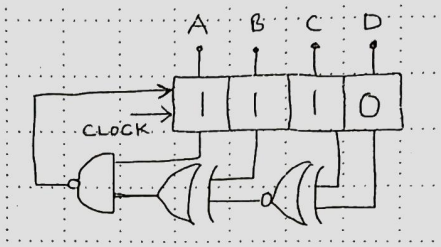
Q3. A new Flip Flop (XY) is designed with the following Truth table. The previous state of XY Flip Flop is Q_n and the Next State Denoted by Q_{n+1}. For the New Flip Flop create the Characteristic Table and Excitation Table also Find the Characteristic Equation for Given Flip Flop. **[4]**

	Input	Input	Output
Clock	**X**	**Y**	Q_{n+1}
0	Don't care	Don't care	Q_n
1	0	0	1
1	0	1	Q_n
1	1	0	$\overline{Q_n}$
1	1	1	0

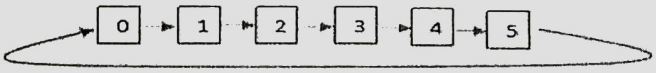
Truth Table of XY Flip Flop

Q4. Design a 2-bit Synchronous Down Counter with detailed diagram. (Use T Flip Flop). **[4]**

Q5. In SIPO Register (Given in the Diagram), Find the output (A, B, C, D) ~~after 1st~~ clock, 2nd clock, 3rd clock, and 4th clock. **[4]**



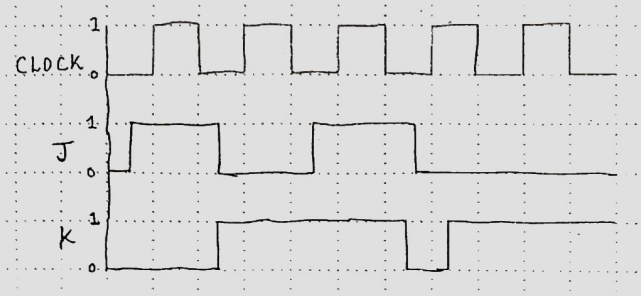
Q6. Design an asynchronous counter using T flipflop for the following sequence. **[4]**



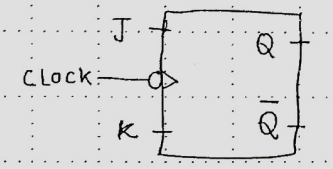
Q7. Convert the S R Flip Flop to T Flip Flop with suitable tables and Logic expression and Logic Diagram. **[4]**

Q8. Design a counter which has no. of states double of no. of Flip Flop used in that counter circuit with the suitable diagram. **[4]**

Q9. Draw the Output wave form (Q) of the given JK Flip Flop for given Input waveform. Assume previous state is '1' **[4]**



Input Waveform



Logic Symbol

ALL THE BEST