BENNETT UNIVERSITY

Enrollment No.: _____ Name: _____

Department/School: _____

End Semester Examination, Even Semester 2022-23

Course Code: CSET-105

Course Name: Digital Design

Max. Time Duration: 2 hour

Max. Marks: 35

WRITE YOUR BATCH NUMBER ON THE TOP OF FRONT PAGE OF YOUR ANSWERSHEET

Instructions:

1. Do not write anything on the question paper except name, enrolment number and school.
2. Carrying mobile phone, smart watch and any other non-permissible materials in the examination hall is an act of UFM.

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1. Attempt all the questions. **(1 * 5 = 5 Marks)**

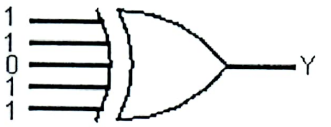
a. Write the truth table of 4:2 Priority Encoder.

b. Draw D flip flop in toggle mode.

c. Draw a circuit that removes Race around condition in JK flip flops.

d. What is the difference between Mealy and Moore state machines?

e. Calculate the output Y in the below circuit



2. Attempt all the questions. **(3*5 = 15 Marks)**

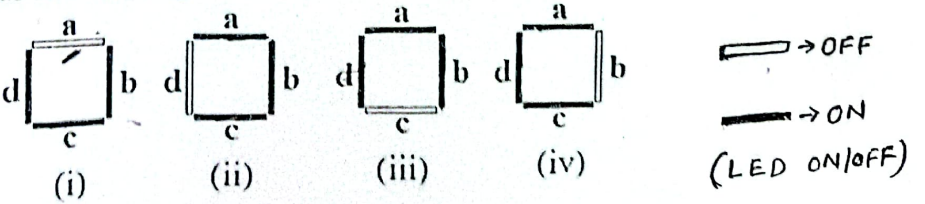
a. Adi needs JK flip-flips in order to make an application specific circuit. By fault, he bought D-Flip Flops from the market. Help Adi to use D-Flip Flops as JK.

b. Adi wants to code a three-bit binary number into its corresponding Gray code. Help Adi in forming the truth table of the conversion and then in implementing the circuit.

c. Can more than one decoder output be activated at one time? Justify your answer with an example circuit using 2:4 Decoders.

d. Design Mod-8 asynchronous UP counter using T-Flip Flops. Also explain its working using truth table and timing diagram.

e. Four rectangular LEDs a, b, c and d are arranged in square pattern on a board. Consider an anonymous 2:4 decoding in which the four outputs correspond to four different states of LEDs (i), (ii), (iii) and (iv) as shown in figure below. Realize this circuit using fundamental gates.



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3. **Attempt all the questions.** **(5*3 = 15 Marks)**

a. What are Shift Registers. List the various types of Shift Registers. Draw and explain the working of Universal Shift Register.

b. What is a PLD and how a PAL differs from PLA? Realize the following Boolean expressions in its minimized form using a single PLA.
F_1 (A, B, C) = (1, 2, 4, 6, 7) and
F_2 (A, B, C) = (3, 5, 6, 7)

c. Design the counter that goes through below state diagram using T-flip-flops. Also explain its working using truth table and timing diagram.