POSSESSION OF MOBILE IN EXAMINATION IS UFM PRACTICE

Name of Student ---------- Enrolment No. ----------

Department ----------

BENNETT UNIVERSITY, GREATER NOIDA

Final Examination, SPRING SEMESTER 2018-19

COURSE CODE: **ECSE104L** MAX. DURATION: **Two HOUR**

COURSE NAME: **DIGITAL DESIGN**

COURSE CREDIT: **5** MAX. MARKS: **60**

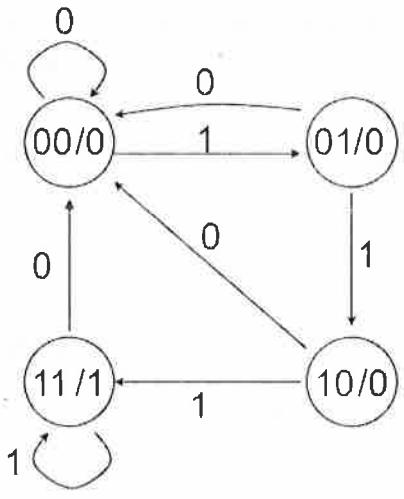
Note: All the questions are compulsory.

- Please write precisely and neatly. Please make clear diagram wherever required.

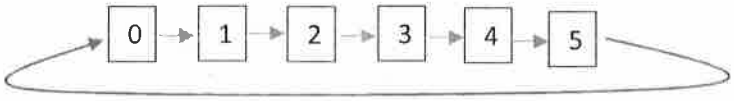
Q 1. You are in the process of designing an application where you need a full adder, so you went to a shop and requested for full adder, unfortunately full adder was out of stock, but shopkeeper has 3-8 decoder basic gates (AND, OR, NOT). How you will utilize available 3-8 decoder and basic gates to make full adder? Draw the design. **5 Marks**

Q 2. Analyze the following state diagram and derive state table. Design circuit diagram using d flip flop. **10 Marks**

a. Make state table
b. Excitation table of D flip flop
c. Find input equation using K map
d. Design circuit diagram



Q 3. Design an asynchronous counter using T flipflop for the following sequence. **5 Marks**



Q4. Suppose you want to design a circuit which can toggle the output, if input is High and no change in output at low input, but you have only D flip flop, AND, OR and Inverter in the stock then how to do it? **5 Marks**

Q 5. Explain in one sentence. **3 Marks**

a. Problem with S-R latch, solved by S - R Flipflop.
b. Problem with S-R Flipflop, solved by J-K Flipflop.
c. Problem with J-K Flipflop, solved by master slave Flipflop.

Q 6. Write Verilog code for 4 bit asynchronous counter using T flip flop. **10 Marks**

```
module TFF(T, clk, Q)

input T, clk;
output wire Q;

// write your code here

endmodule

module counter(clk, Q)
input clk;
output wire [3:0]Q;

//write your code here

endmodule
```

Q 7. Design a combined register which have capability of serial in serial out (SISO) and parallel in and serial out (PISO) together. **6 Marks**

Q 8. Design a circuit which can convert BCD to excess-3. **10 Marks**

a. Make truth table
b. Derive equations using K-map.
c. Draw the circuit diagram

Q.9 Write short Notes **6 Marks**

a. Edge trigger and level trigger
b. Number representation using sign number, one's complement, two's complement
c. Racing condition