BENNETT UNIVERSITY

POSSESSION OF MOBILE IN EXAMINATION IS UFM PRACTICE

Name of Student ---------- Enrolment No. ----------
Department ----------

BENNETT UNIVERSITY, GREATER NOIDA
End-Term Examination, SPRING SEMESTER 2017-18

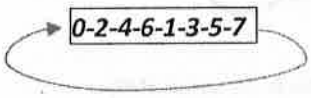
COURSE CODE: **ECSE104L** MAX. DURATION: **TWO HOURS**
COURSE NAME: **DIGITAL DESIGN**
COURSE CREDIT: **5** MAX. MARKS: **60**

Note:

- All the questions are compulsory.
- Please write precisely and neatly. Please make clear diagram wherever required.

Q1. Design a 4-to-16-line decoder with 2-to-4-line decoders with enable bit. (6 Marks)

Q2. Design the synchronous counter using T flip flop which counts numbers as follows: (10 Marks)



Explain following steps in detail:

a. Develop state diagram
b. Create excitation table
c. Identify function using k maps
d. Design counter circuit

Q3. Design a combined register which have capability of both serial in serial out (SISO) and parallel in and serial out (PISO) registers. (8 Marks)

Q4. Write a short notes on: (5 X 2=10 Marks)

a. You're going to a sweet shop and 8 sweets are available in that shop. You select one of the sweet. This is an example of decoder, encoder, Mux or Demux. Justify your answer.

b. In the same sweet shop, eight customers are present and shop-owner is giving sweets to one of the customers. This is an example of decoder, encoder, Mux or Demux. Justify your answer.

c. Seven Segment Display is an example of encoder, decoder, Mux or Demux. Justify your answer.

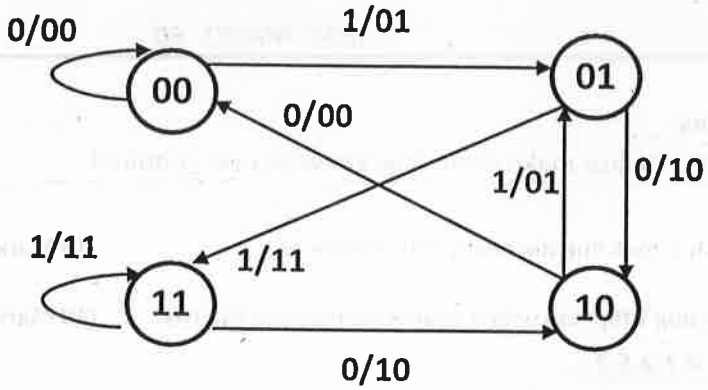
d. In what kind of situation (in terms of the number of min-terms or number of elements in each min-term) circuits designed using PLA, PAL, and ROM are exactly equivalent.

e. A 3-bit asynchronous counter can count from 0 to 7 and counting is done based on outputs of three flip-flops (Q_A, Q_B, and Q_C). What are the outputs of these three flip-flops in 66^{th} clock cycle? Justify your answer.

Q5. Design circuits for the following functions using PLA, PAL and ROM. (8 Marks)

F0 (A, B, C, D) = A
F1(A, B, C, D) = AB+AC+ABC+AD
F3(A, B, C, D) = AB+B+ABCD

Q6. Analyse the given state diagram, derive excitation table, and design circuit. (12 Marks)



Input/output
X1/Y1Y2

Note- Each output has two bits therefore deal each bit separately.

Q7. Multiple choice questions. Write explanation along with your answer. (4 X 1.5 = 6 Marks)

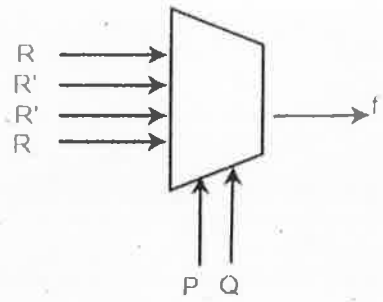
I. The min-term expansion of ***f(P, Q, R) = PQ + QR' + PR'*** is

(A) m2 + m4 + m6 + m7
(B) m0 + m1 + m3 + m5
(C) m0 + m1 + m6 + m7
(D) m2 + m3 + m4 + m5

II. Consider the following Boolean function of four variables:
f(w,x,y,z) = ∑(1,3,4,6,9,11,12,14)
The function is:
(A) independent of one variables.
(B) independent of two variables.
(C) independent of three variables.
(D) dependent on all the variables.

III. Consider the following Boolean expression for F:
F(P, Q, R, S) = PQ + P'QR + P'QR'S
The minimal sum-of-products form of F is
(A) PQ + QR + QS
(B) P + Q + R + S
(C) P' + Q' + R' + S'
(D) P'R + P'R'S + P

IV. The Boolean expression for the output 'f' of the multiplexer shown below is



(A) (P(XOR)Q(XOR)R)'
(B) P(XOR)Q(XOR)R
(C) (P+Q+R)'
(D) P+Q+R