BENNETT UNIVERSITY

POSSESSION OF MOBILE IN EXAMINATION IS UFM PRACTICE

Name of Student ---------- Enrolment No. ----------
Department ----------

BENNETT UNIVERSITY, GREATER NOIDA
Minor-2 Examination, SPRING SEMESTER 2017-18

COURSE CODE: **ECSE104L** MAX. DURATION: **ONE HOUR**
COURSE NAME: **DIGITAL DESIGN**
COURSE CREDIT: **5** MAX. MARKS: **50**

Note:

- All the questions are compulsory.
- Please write precisely and neatly. Please make clear diagram wherever required.

Q1. Design a 2-bit magnitude comparator to check whether the given first binary number is greater or lesser or equal to the second binary number. (10 Marks)

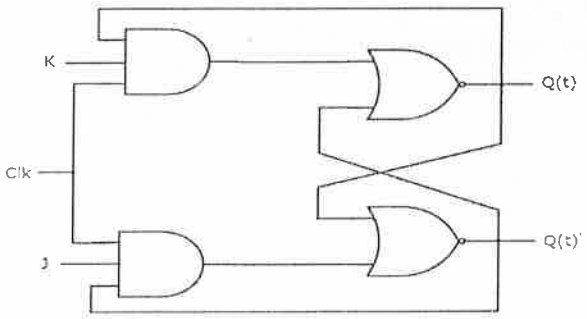
Q2. Design an adder and 1's complement subtractor in a single unit. The beauty of the unit is that same unit has the capability to perform addition and subtraction based on the given input. (10 Marks)

Q3. Develop a Verilog code for the D flip-flop. (7 Marks)

```
module DFF (Q, Qb, D);
    input D;
    output Q, Qb;

    // write your code
endmodule
```

Q4. Develop the characteristic table for J-K flip-flop and then derive a Boolean expression for next state output. (circuit and state table for J-K flip-flop are given below) (10 Marks)



J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q(t)'

Characteristic Table:

Present Inputs		Present State	Next State
J	K	Q(t)	Q(t+1)

Q5. Write a short note: (3*3=9 Marks)

a. Issues in SR latch.
b. The advantage of D flip-flop over S-R flip-flop.
c. Difference between edge trigger and level trigger

Q6. Multiple choice questions. Write explanation along with your answer. (4*1 = 4 Marks)

I. In an SR latch made by cross-coupling two NAND gates, if both S and R inputs are set to 1, then it will result in

(a) Q = 0, Q' = 1
(b) Q = 1, Q' = 0
(c) Memory
(d) Not allowed

II. Equation of carry in full adder is (a, b are inputs, and c is carry input).

(a) carry = ab + bc +ca
(b) carry = ab + (a $\oplus$ b) c
(c) Both a and b
(d) None of the above

III. Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?

(a) Multiplexer
(b) Demultiplexer
(c) Both a and b
(d) None of the above

IV. Why a demultiplexer is called as a data distributor?

(a) The input will be distributed to one of the outputs
(b) One of the inputs will be selected for the output
(c) The output will be distributed to one of the inputs
(d) None of the Mentioned