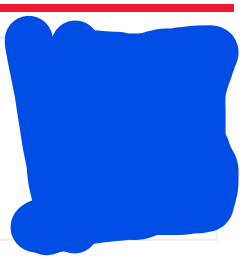


Started on	Monday, 7 June 2021, 1:02 PM
State	Finished
Completed on	Monday, 7 June 2021, 1:47 PM
Time taken	45 mins 1 sec
Marks	24.00/35.00
Grade	**6.86** out of 10.00 (**69**%)

Question 1

Correct

Mark 1.00 out of 1.00

A half adder has

Select one:

- a. 3 inputs and 2 outputs
- b. 2 inputs and 1 outputs
- c. 2 inputs and 2 outputs ✓
- d. 2 inputs and 3 outputs

The correct answer is: 2 inputs and 2 outputs

Question 2

Correct

Mark 1.00 out of 1.00

Each term in SOP form is called min term

Select one:

- True ✓
- False

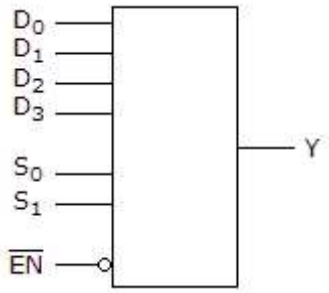
The correct answer is 'True'.

Question 3

Correct

Mark 1.50 out of 1.50

For the MUX shown here, let all D inputs be 0110, both S inputs be HIGH, and the EN input be HIGH. What will be the status of the Y output?



Select one:

- a. Don't care
- b. Low ✓
- c. High Impedance
- d. HIGH

The correct answer is: Low

Question 4

Not answered

Marked out of 2.00

For 4 bit parallel addition, we need minimum _____ half adder(s) and _____ full adder(s). Assume no previous carrry

Select one:

- a. 2 HA and 2 FA
- b. 0 HA and 3 FA
- c. 4 HA and 0 FA
- d. 1 HA and 3 FA

The correct answer is: 1 HA and 3 FA

Question 5

Correct

Mark 1.00 out of 1.00

In reference to the truth table of SR latch, how many valid entries are there?

Select one:

- a. 3 ✓
- b. 2
- c. 4
- d. 0
- e. 1

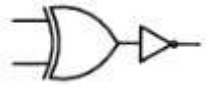
The correct answer is: 3

Question 6

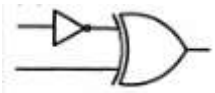
Correct

Mark 2.00 out of 2.00

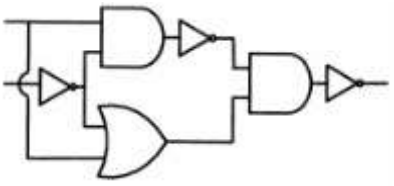
Match The following



XNOR ✓

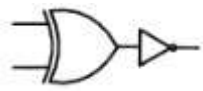
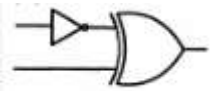


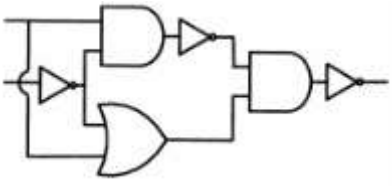
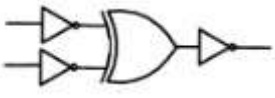
XNOR ✓



XOR ✓

XNOR ✓

The correct answer is:  → XNOR,  → XNOR,

 → XOR,  → XNOR

Question 7

Correct

Mark 1.00 out of 1.00

An n variable K-map can have.

Select one:

- a. 2*n cell
- b. n pow n cell
- c. 2 pow n cell ✓
- d. n pow 2 cell

The correct answer is: 2 pow n cell

Question 8

Incorrect

Mark 0.00 out of 1.50

The equivalent minimum expression for the expression f(X, Y, Z) = XY + YZ' + XZ' is:

Select one:

- a. m2+ m4+ m6+m7
- b. m0 +m1 +m3+ m5
- c. m2 +m3 + m4 +m5 ✗
- d. m0+ m1 +m6 +m7

The correct answer is: m2+ m4+ m6+m7

Question 9

Correct

Mark 2.00 out of 2.00

In a look-ahead carry generator, the carry generate function G_i and the carry propagate function P_i for inputs A_i and B_i are given by:

$P_i = A_i \oplus B_i$ and $G_i = A_iB_i$

The expressions for the sum bit S_i and the carry bit C_{i+1} of the look-ahead carry adder are given by:

$S_i = P_i \oplus C_i$ and $C_{i+1} = G_i + P_iC_i$, where C_0 is the input carry.

Consider a two-level logic implementation of the look-ahead carry generator. Assume that all P_i and G_i are available for the carry generator circuit and you can choose AND and OR gates with **any number of inputs.** The minimum number of AND gates and OR gates needed for carry generator for a 4-bit adder to gerenate C4, C3, C2, C1 as its outputs.

Select one:

- a. 6 AND , 3 OR
- b. 15 AND , 10 OR
- c. 6 AND , 4 OR
- d. 10 AND , 4 OR ✓

The correct answer is: 10 AND , 4 OR

Question 10

Incorrect

Mark 0.00 out of 2.00

11001, 1001, and 111001 correspondings to the 2's complement representation of the following set of numbers. Assume the first bit represents the sign

Select one:

- a. -7, -7 and -7 respectively
- b. -25, -9 and -57 respectively
- c. 25, 9 and 57 respectively ✗
- d. -7, -6 and -7 respectively

The correct answer is: -7, -7 and -7 respectively

Question 11

Correct

Mark 1.50 out of 1.50

Latches constructed with NOR and NAND gates tend to remain in latched condition due to which configuration feature?

Select one:

- a. Synchronous operation
- b. Gate impedance
- c. Cross Coupling ✓
- d. Low Input Voltage

The correct answer is: Cross Coupling

Question 12

Correct

Mark 1.50 out of 1.50

What would happen to the output if the Q=0 in S-R flip-flop?

Select one:

- a. RESET ✓
- b. Current state
- c. SET
- d. Previous State

The correct answer is: RESET

Question 13

Correct

Mark 1.00 out of 1.00

A combinational logic circuit does not have feedback from output to input.

Select one:

- True ✓
- False

The correct answer is 'True'.

Question 14

Correct

Mark 1.50 out of 1.50

What is one of the major issue in the ripple-carry adder?

Select one:

- a. None of the given
- b. The interconnections are more complex
- c. It is slow due to propagation time ✓
- d. Extra stages are required to a full adder

The correct answer is: It is slow due to propagation time

Question 15

Correct

Mark 1.50 out of 1.50

Which Boolean function can be represented by following truth table?

A	B	F(A,B)
0	0	0
0	1	0
1	1	1
1	0	1

Select one:

- a. A XOR B
- b. B
- c. A ✓
- d. A and B

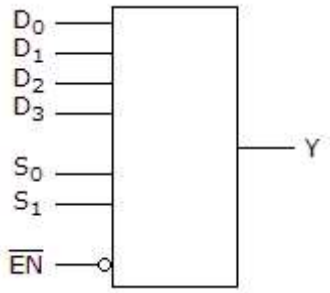
The correct answer is: A

Question 16

Incorrect

Mark 0.00 out of 1.50

For the MUX shown here, let all D inputs be 1001, both S inputs be HIGH, and the EN input be HIGH. What will be the status of the Y output?



Select one:

- a. LOW ✗
- b. Don't care
- c. High Impedance
- d. HIGH

The correct answer is: HIGH

Question 17

Correct

Mark 1.00 out of 1.00

Which gate will generate the high output when one input is high and other is low?

Select one:

- a. Only OR gate
- b. Only NAND Gate
- c. Only AND GATE
- d. Both OR and NAND ✓

The correct answer is: Both OR and NAND

Question 18

Incorrect

Mark 0.00 out of 1.50

If in a base number system, 5+3=12, what is the base of the number is?

Select one:

- a. 6
- b. 8 ✗
- c. 4
- d. 10

The correct answer is: 6

Question 19

Correct

Mark 1.00 out of 1.00

What will be the Boolean expression for the Half adder for input X and Y?

Select one:

- a. Sum = x AND y ; carry = x OR y
- b. Sum = x NOR y ; carry = x NOT y
- c. Sum = x AND y ; carry = x AND y
- d. Sum = x XOR y ; carry = x AND y ✓

The correct answer is: Sum = x XOR y ; carry = x AND y

Question 20

Correct

Mark 1.50 out of 1.50

Which logic gates can be used to construct a basic S-R flip-flop?

Select one:

- a. AND or NOR gates
- b. AND or OR gates
- c. NOR or NAND gates ✓
- d. XOR or XNOR gates

The correct answer is: NOR or NAND gates

Question 21

Incorrect

Mark 0.00 out of 1.00

In Karnaugh map an octet eliminates _____variables.

Select one:

- a. Two
- b. None
- c. one ✗
- d. Three

The correct answer is: Three

Question 22

Correct

Mark 1.00 out of 1.00

Which gate used for even parity check?

Select one:

- a. NAND
- b. XOR ✓
- c. None of the given
- d. OR
- e. NOR

The correct answer is: XOR

Question 23

Correct

Mark 2.00 out of 2.00

Which of the following logic expressions is incorrect?

Select one:

- a. 1 ⊕ 0 ⊕ 1 ⊕ 0 ⊕1 ⊕ 0 ⊕1⊕1= 1
- b. 1 ⊕ 0 ⊕ 1 ⊕ 0 ⊕1 ⊕ 0 ⊕1⊕0= 0
- c. 1 ⊕ 0 ⊕ 1 ⊕ 0 ⊕1 ⊕ 0 ⊕1⊕0= 1 ✓
- d. 0 ⊕ 0 ⊕ 1 ⊕ 0 ⊕1 ⊕ 0 ⊕1⊕1= 0

The correct answer is: 1 ⊕ 0 ⊕ 1 ⊕ 0 ⊕1 ⊕ 0 ⊕1⊕0= 1

Question 24

Correct

Mark 1.00 out of 1.00

Which mapping is related to a Demultiplexer?

Select one:

- a. one to one
- b. None of the mentioned
- c. many to one
- d. one to many ✓

The correct answer is: one to many

Question 25

Incorrect

Mark 0.00 out of 1.50

A multiplexers is a combinational logic circuit need to perform the operations_____

Select one:

- a. XOR-NAND
- b. OR-OR
- c. NOR-OR ✗
- d. AND-OR

The correct answer is: AND-OR