Course- B.Tech

Type- Core

Course Code-CSET-105

Course Name- Digital Design

Session-2022-23

Semester-Even

Date- 3-7 April 2023

Batch- ALL

Lab Assignment 12_Tuesday

Practical title: Shift-Registers

Name	CO1	CO2	CO3
	✓	-	✓

In this Lab, we will work on Logisim. It is an educational tool for designing and simulating digital logic circuits, featuring a simple-to-learn interface, hierarchical circuits, wire bundles, and a large component library. The drawing interface is based on an intuitive toolbar. Color-coded wires aid in simulating and debugging a circuit. The wiring tool draws horizontal and vertical wires, automatically connecting to components and to other wires. In this lab we will implement various shift registers using flipflops in LOGISIM.

1. What are Shift registers. What are different types of Shift-registers. Discuss about the various applications of Registers.
2. What are timing diagrams in shift registers? Design Serial in Serial out shift register using D flip flop in LOGISIM.
3. Explain the concept of Serial in Parallel out data analysis. Design Serial in Parallel out shift register using D flip flop in LOGISIM.
4. Design a parallel in serial out shift register using D flip flops in LOGISIM.
5. What are universal shift registers. Design a 4-bit universal shift register in LOGISIM.

Submission Instructions:

• Prepare the submission file according to the following process:

1. "Export image" from file menu option of the designed logic circuit and save it in local drive.

2. Insert the logic circuit image into the word file.

3. Repeat Step 1 and 2 for all the programs which depends on Logisim.

4. Convert the word file into pdf file, name it as RollNo _Assignment.

(Example: E20CSE001_Assignment2.pdf).

5. Submit your file on LMS within the deadline.

• Write your Name and Roll No. in textbox above the logic circuit. Keep in mind that this is Mandatory. Failing which you may lose your marks.

• Each student will submit their assignment on their corresponding group slot only.

• Late submission will lead to penalty.

• Any form of plagiarism/copying from peer or internet sources will lead penalty.

• Above mentioned instructions at submission time are mandatory. Missing of any instructions at submission time will lead penalty.