EESM6000C SOC Design

Lab4-2 Caravel FIR report

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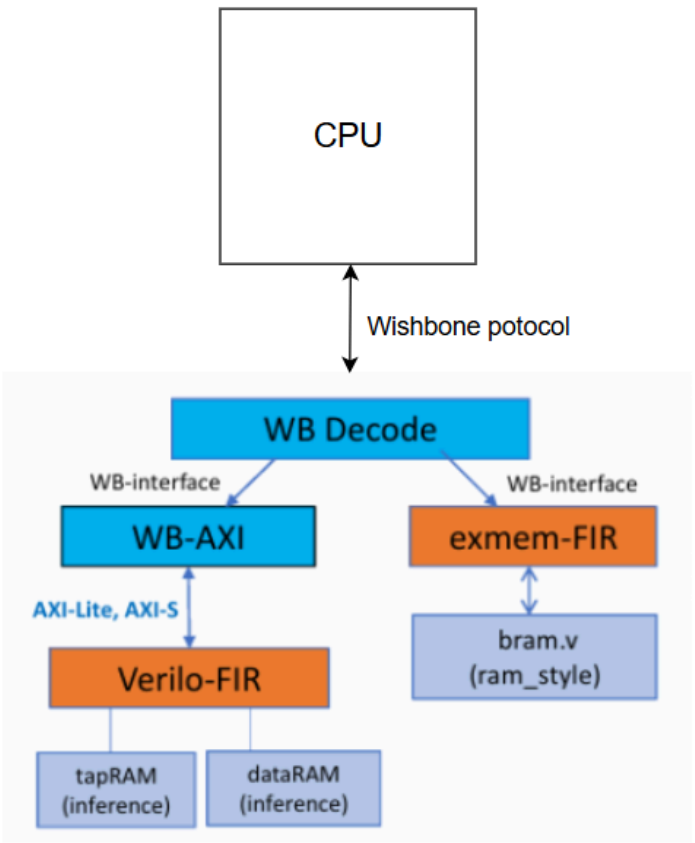
Block Diagram



The interface protocol

- MPRJ pins are used between firmware and testbench
  - MPRJ[23:16] are used
  - When mprj[23:16] == 0x00A5, it indicates that the FIR starts running
  - When mprj[23:16] == 0x005A, it indicates that the FIR stops running
  - The pins also used to indicated the start and the end of the test case
  - The calculation result from FIR is obtained by CPU first and the output from these pins for checking.

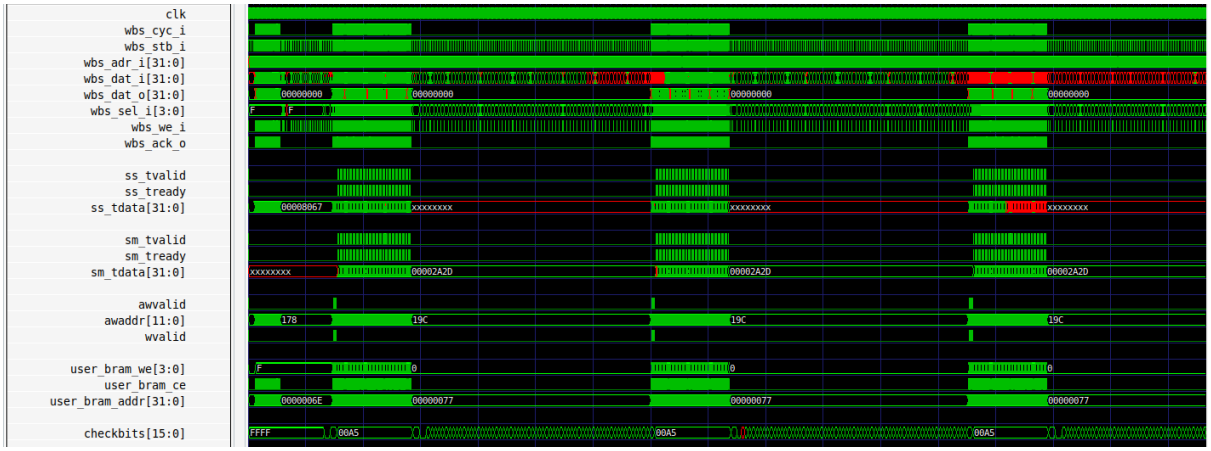
- Wishbone interface is used between firmware and user project.
  - Writing instruction to user memory from SPI flash interface

    - Getting instruction from user memory to CPU
    - Sending X input to FIR from CPU
    - Receiving Y input from FIR to CPU

- Interface translation between AXI and Wishbone
    - FIR is using AXI-lite and AXI steam for data inputting, while data is received from CPU by Wishbone. Thus, a Wishbone decoder is used for translation between these two interface protocols.
    - Specific memory addresses are assigned to some AXI input and output, such as memory address 0x00000000 representing the AP register in FIR.
    - The Wishbone interface is used to access user memory and FIR at the same time, so the decoder helps to identify which module the Wishbone interface is requesting.

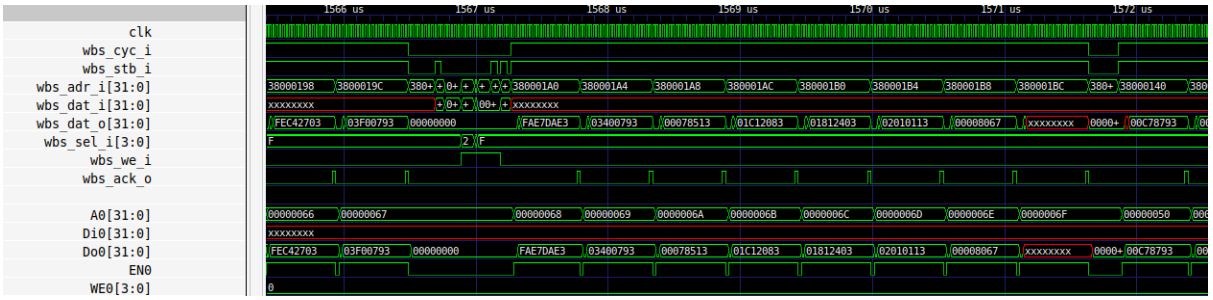
Waveform and analysis of the hardware/software behavior

- Overall simulation result

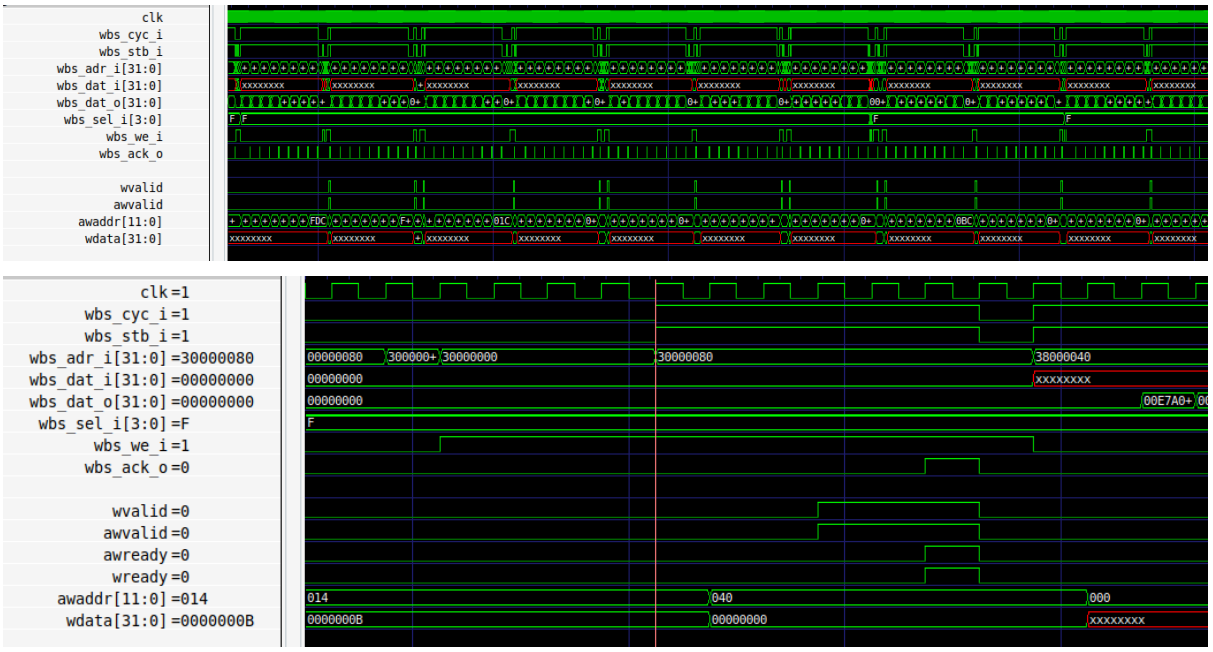


- Allocating instruction from SPI flash to user memory

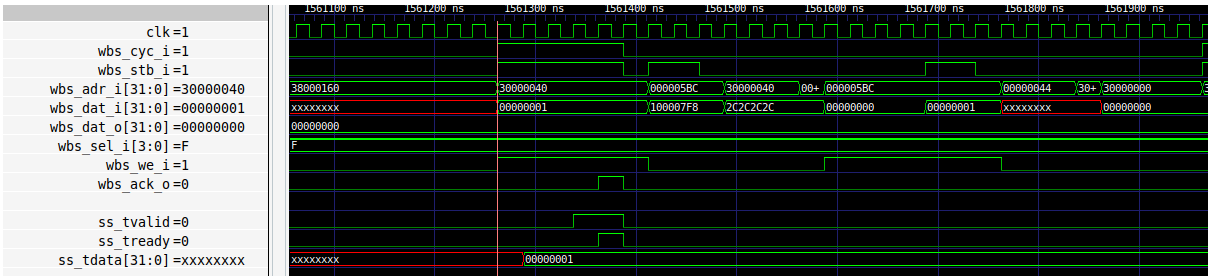
- Obtaining instruction from user memory to CPU



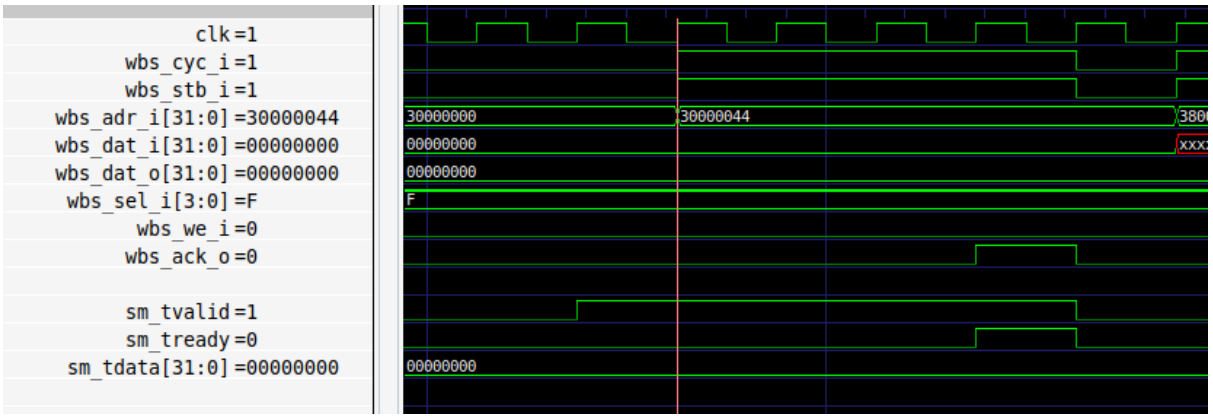
- Writing parameter and TAP value to FIR from CPU



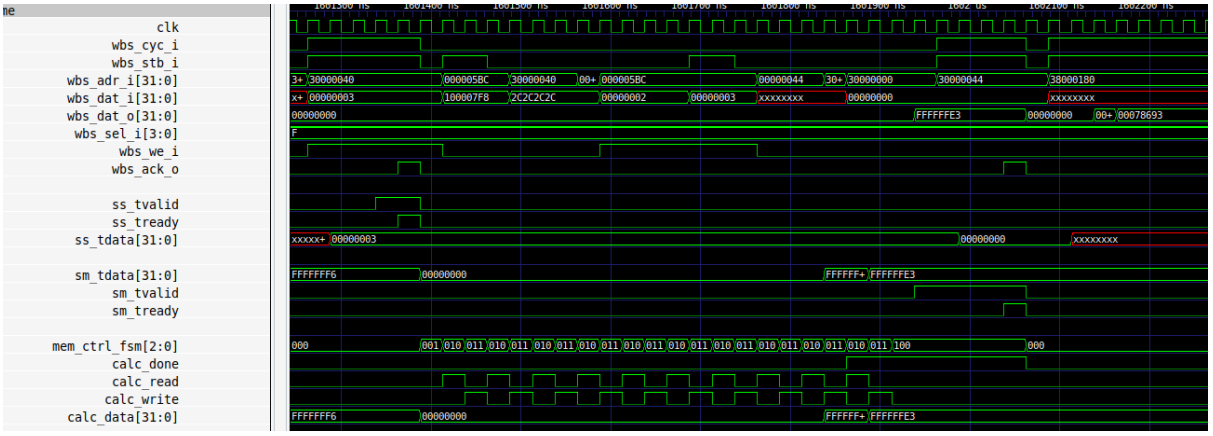
- Writing X input to FIR from CPU



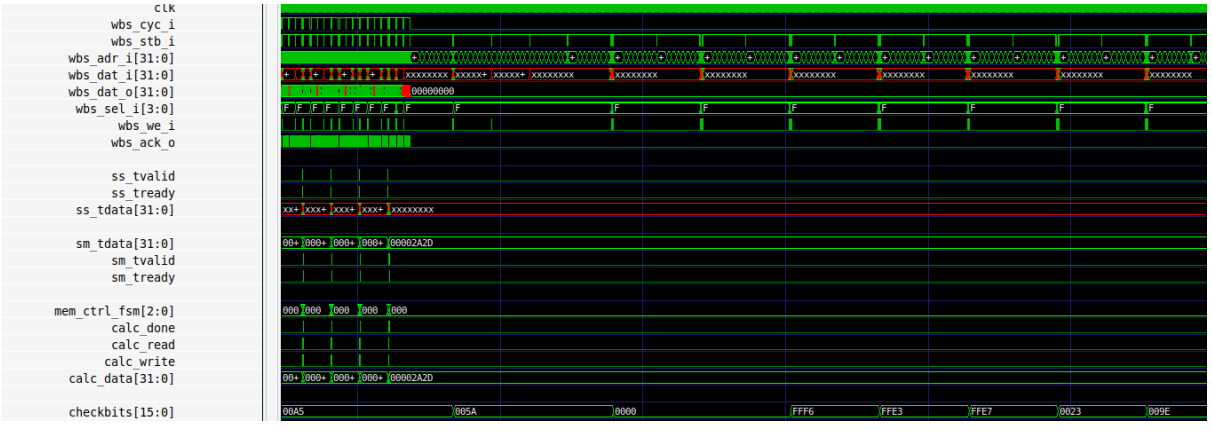
- Getting Y output from FIR to CPU



- FIR calculation



- MPRJ output to test bench



- Simulation Log

```
tbench/counter_la_fir$ source run_sim
Reading counter_la_fir.hex
counter_la_fir.hex loaded into memory
Memory 5 bytes = 0x6f 0x00 0x00 0x0b 0x13
VCD info: dumpfile counter_la_fir.vcd opened for output.
Test 1 started
test1 starts @       4806
test1 ends @      57800
test2 starts @     225892
Test 2 started
test2 ends @     278886
test3 starts @     446978
Test 3 started
test3 ends @     499972
ALL Test passed
```

What is the FIR engine theoretical throughput?

Assumed the adding and multiplication are done in different stage, so at least 11 cycles for adding and 11 cycles for multiplication.

Assumed the memory can only execute 1 write or 1 read in the same cycle, so at least 11 cycles for write and 10 cycles for read.

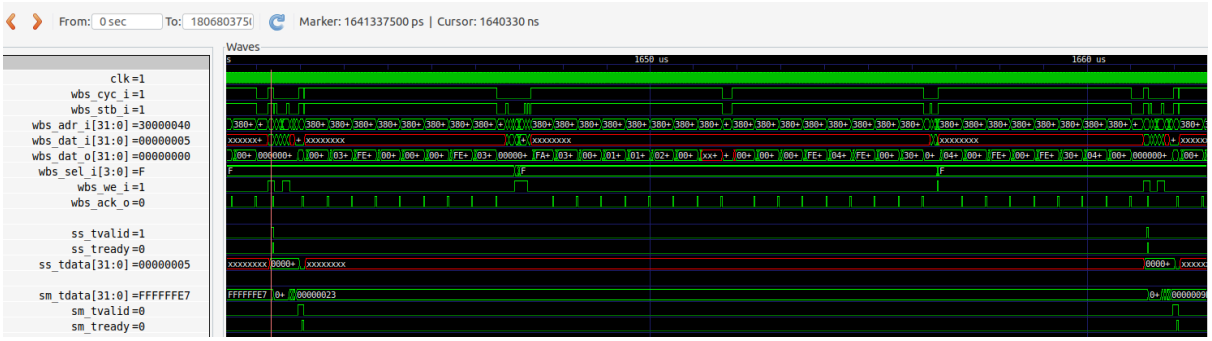
Therefore, at least 22 cycles for operation, adding 1 more cycle for input signal sampling, as a result, the theoretical throughput is 23 cycle per 1 output.

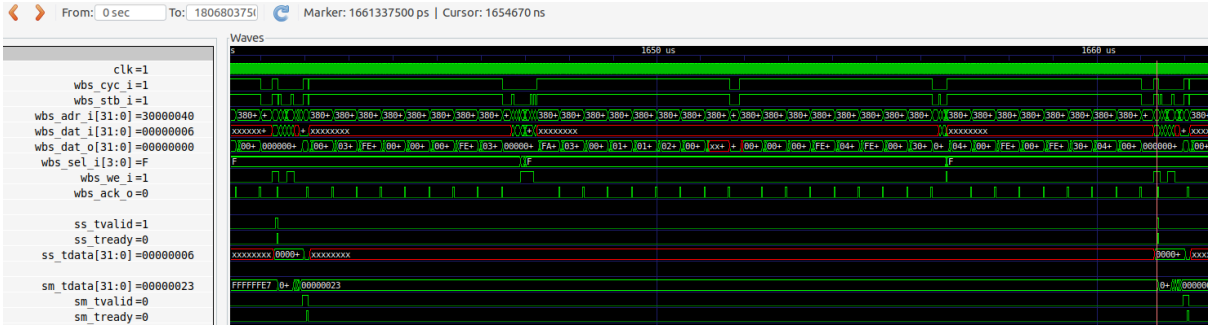
By waveform, the Y output is ready in the 23 cycles after receiving X input, and this matches with the theoretical throughput.

By simulation log, the average cycles to complete the calculation for 64*3 input
= ((57800 - 4806) + (278886 - 225892) + (499972 - 446978)) / (64*3)
= 828.03125 cycles per 1 output

The average cycle is longer than expected, which is affected by software.

What is the latency for firmware to feed data?





Cycle period = 25000 ps
The latency = 1661337500 ps - 1641337500 ps = 20000000 ps = 800 cycles

Ten cycles are assigned for memory read latency in lab 4-1.

What techniques are used to improve the throughput?

Increasing the cache size in CPU helps to reduce the number of instructions fetching from user memory, thus the firmware feed data latency could be reduced.

Reducing the memory read latency in user memory can speed up the instruction fetching, thus reducing the firmware feed data latency.

Simplifying the firmware code helps reduce the number of instructions in CPU, thus speed up the execution and reduce firmware feed data latency.

Replacing the memory in FIR with a memory with 1 read port and 1 write port, so the calculation in FIR could be shortened into 12 cycles theoretically.

Allowing adding and multiplication be executed in the same stage can speed up the calculation in FIR.

Synthesis result: