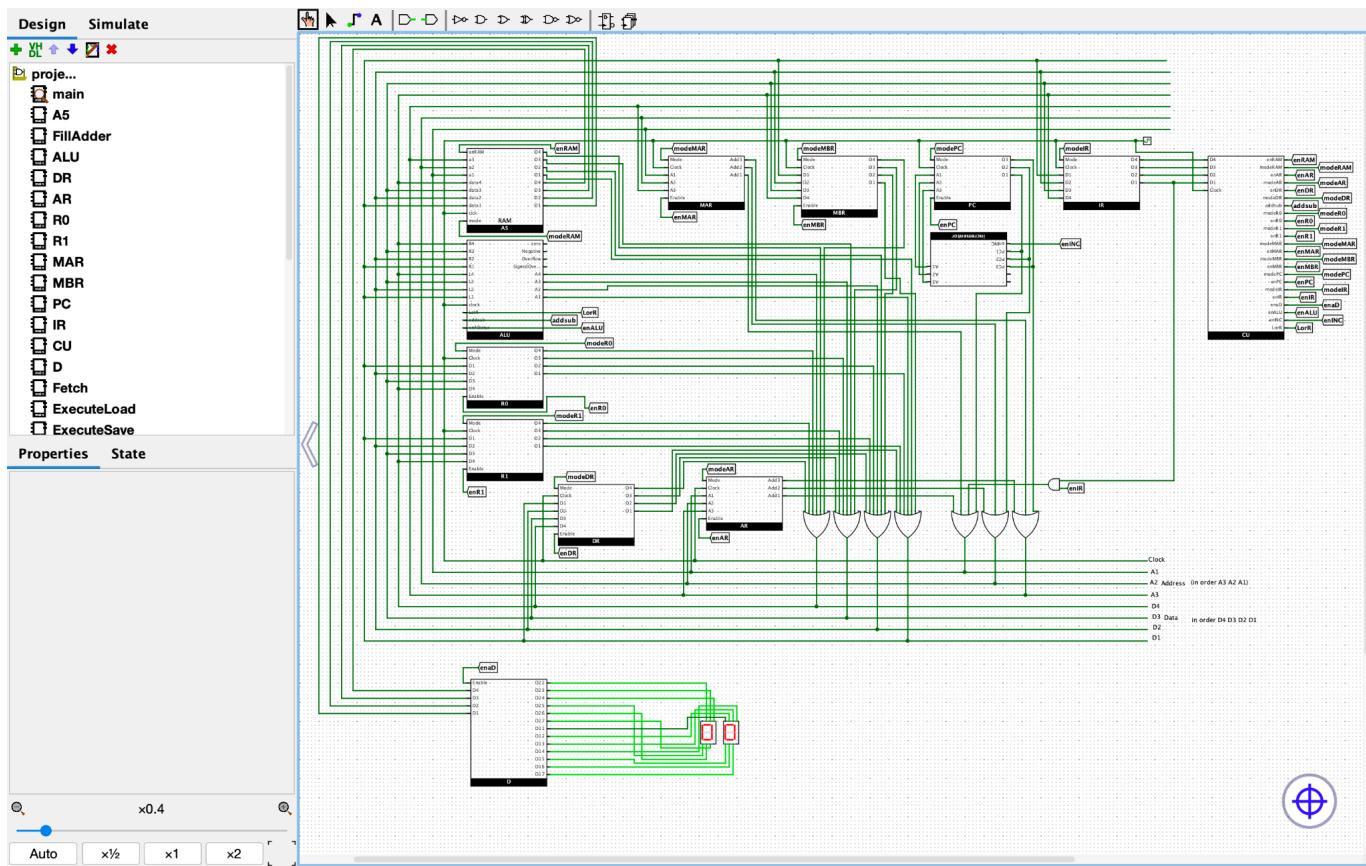


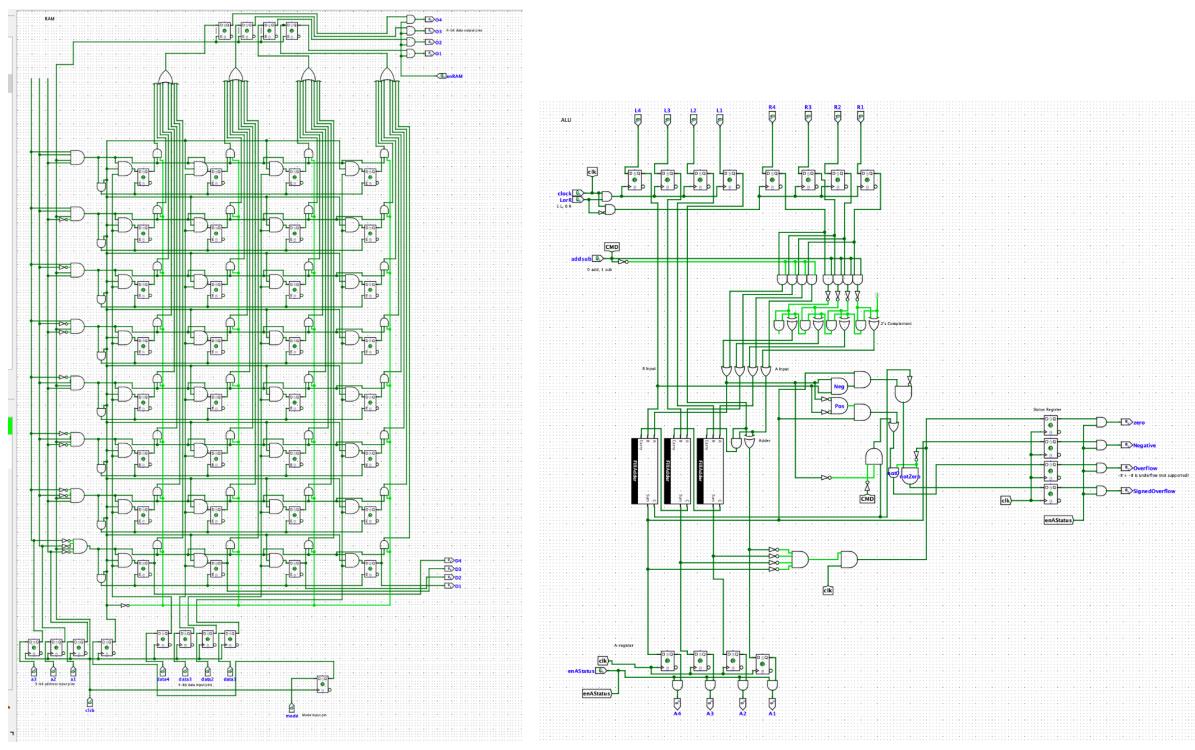
CPU in Logisim Evolution

Sana Cheval



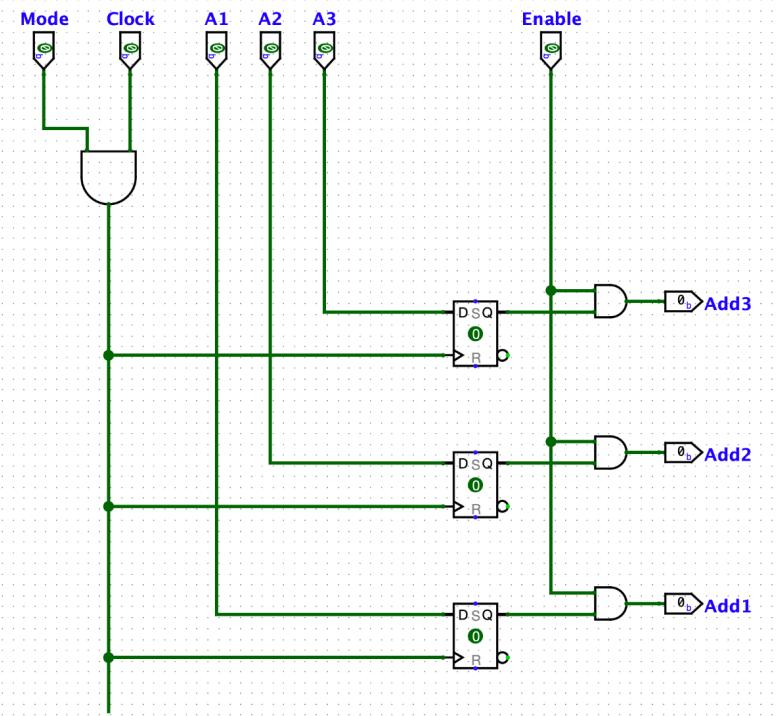
Above: A screenshot of the main circuit for the CPU which connects each component together.

Below: Screenshots from each individual component of the CPU

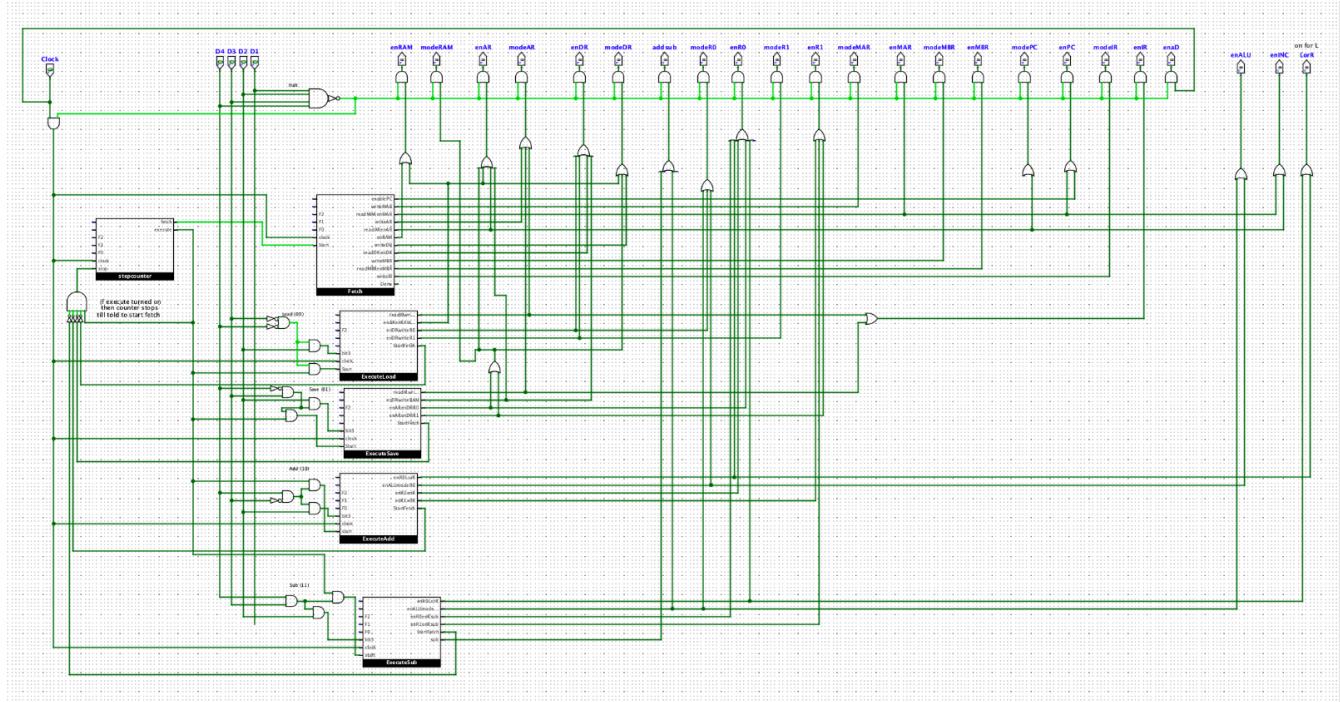


RAM

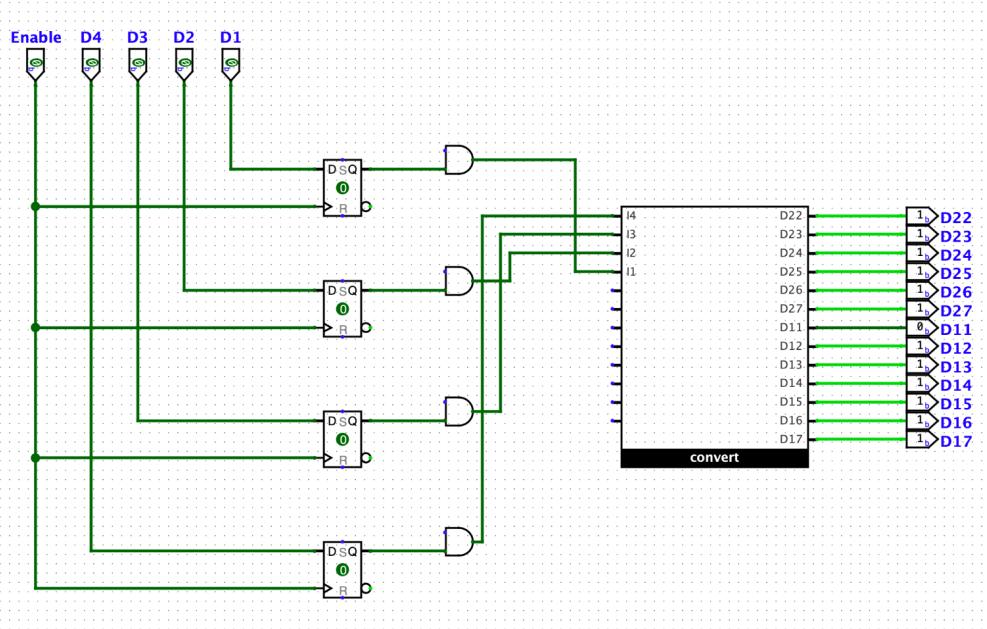
ALU



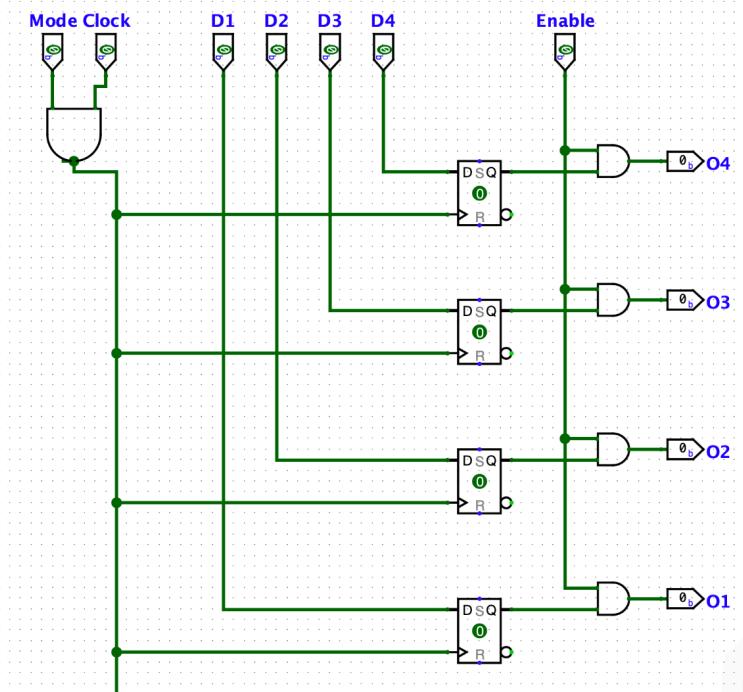
Address Register (AR)



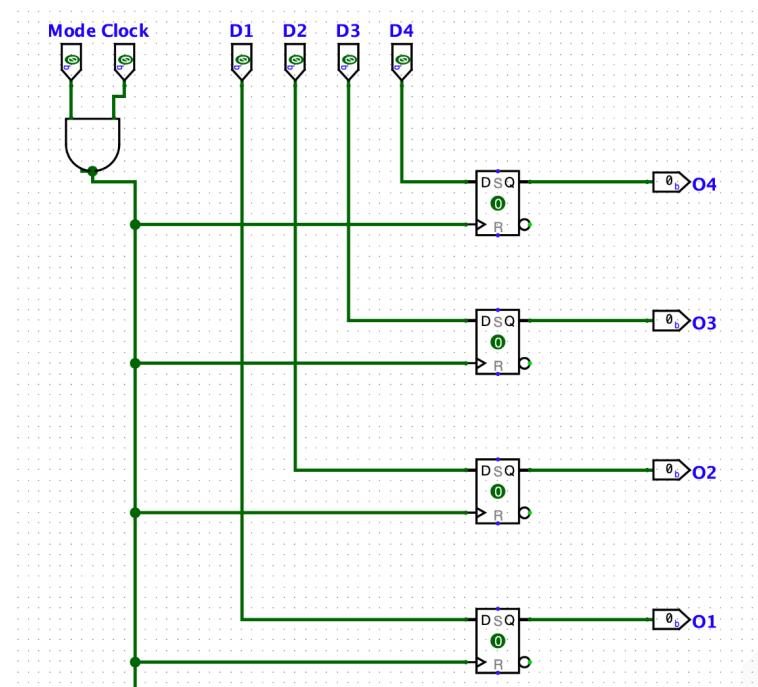
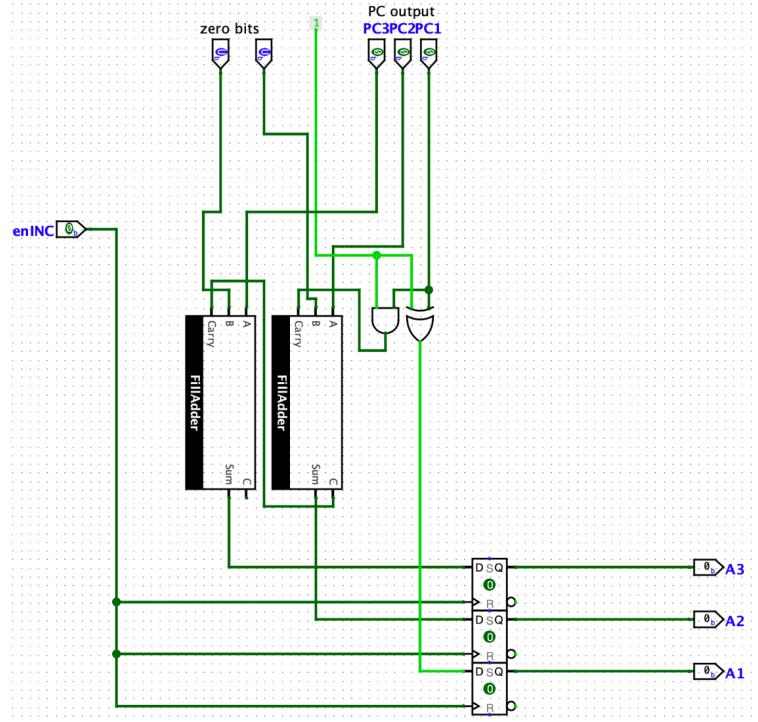
Control Unit (CU)

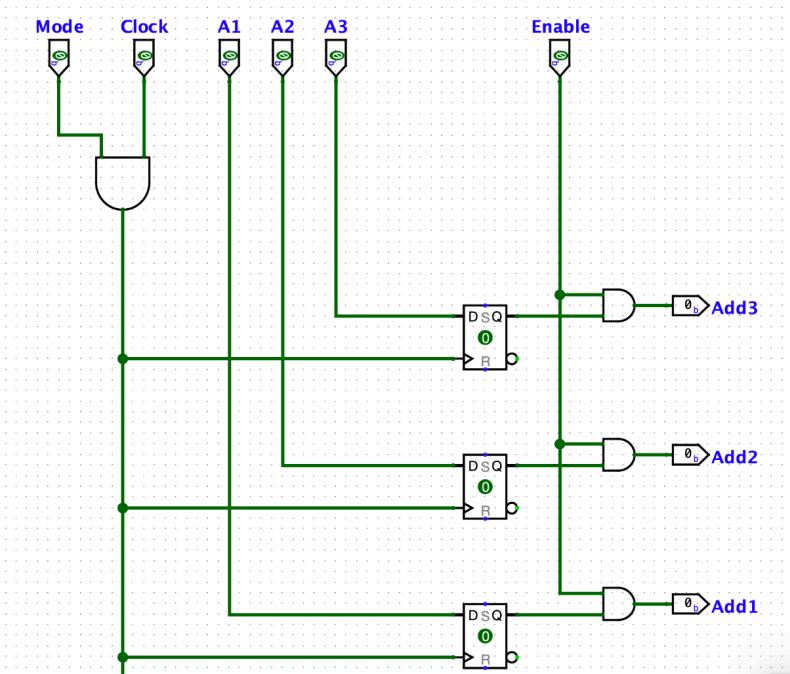


D (for the digital display)

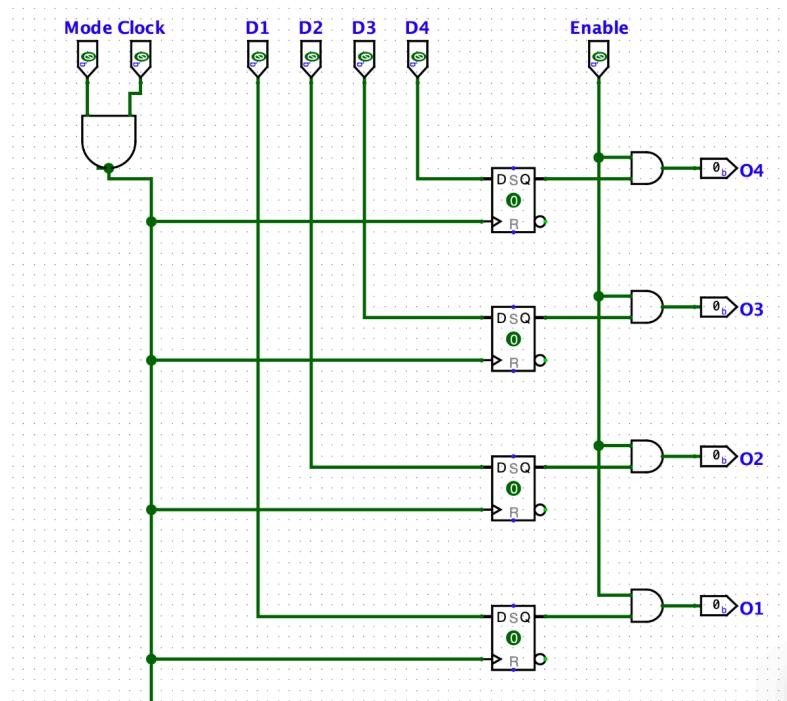


Data Register (DR)

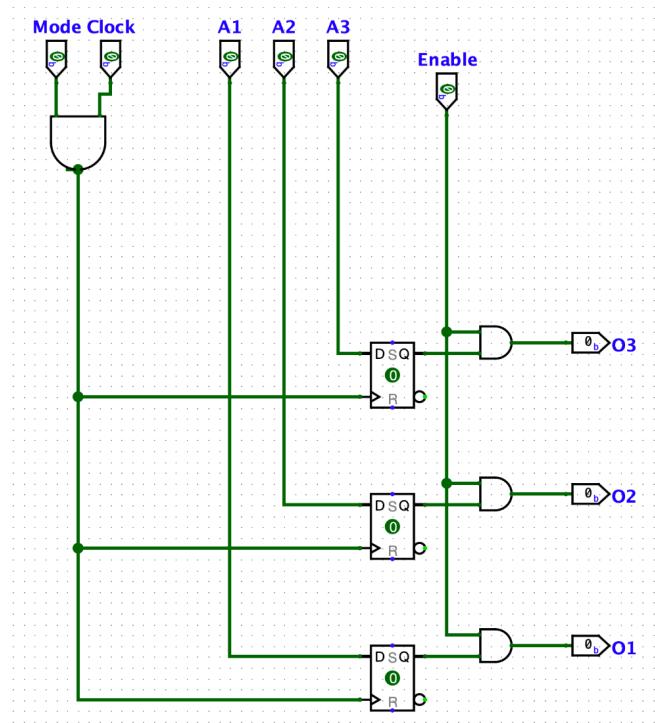




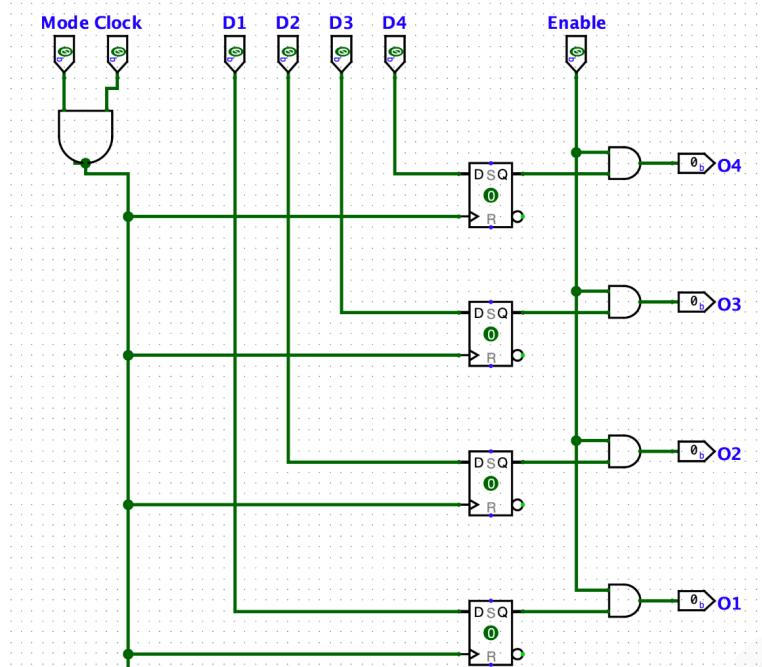
Memory Address Register (MAR)



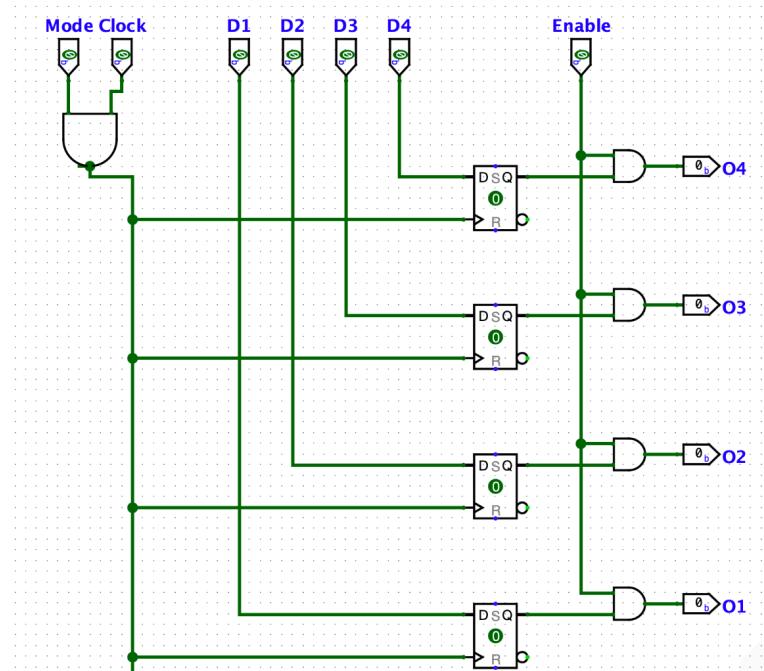
Memory Buffer Register (MBR)



Program Counter (PC)



Register 0 (R0)



Register 1 (R1)