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Microcontroller based overcurrent relay and directional overcurrent relay with ground fault protection

Zhijun Gan, S. Elangovan, A.C. Liew

Department of Electrical Engineering, National University of Singapore, 10 Kent Ridge Crescent, Singapore 119260, Singapore

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Abstract

This paper presents the design and construction of overcurrent and directional overcurrent relays with ground fault protection for the protection of three-phase subtransmission and distribution systems, using a 16-bit microprocessor, the Intel 8096BH. The relay obtains the system currents at the rate of 12 samples per cycle and estimates the fundamental-frequency components of the current signals using discrete Fourier transform techniques. In the case of the directional overcurrent relay, the direction of the current flow is identified to determine whether the fault current is flowing into its protected zone. For this purpose, several internally stored voltage vectors, corresponding to the different directional element settings, are synchronized accurately with the system voltage and used to determine the direction of the power flow. Facilities to change relay characteristics, the time dial and plug settings are provided. The user can also set the relay as an instantaneous overcurrent relay. The desired operating characteristics are achieved by direct curve data storage in the memory.

Keywords: Overcurrent relays; Directional overcurrent relays; Relay protection; Ground fault protection

1. Introduction

Overcurrent relays (OCRs) and directional overcurrent relays (DOCRs) are widely used for the protection of radial and ring subtransmission systems and distribution systems. They are also used as backup protection in transmission systems. The DOCRs slightly differ from OCRs in the sense that they have to determine the fault current direction in addition to its magnitude. DOCRs are mainly used for the protection of ring distribution systems as the same magnitude of fault current can flow in either direction.

Electric power utilities all over the world, perhaps with a few exceptions, are still using electromechanical OCRs and DOCRs for the protection of their distribution networks. Microprocessor based relays are preferable because several types of characteristics can be implemented in the same hardware or with a minimum change of hardware [1,2]. For example, the hardware of digital OCRs and DOCRs is identical, whereas the hardware for conventional OCRs is quite different from that of conventional DOCRs. Moreover, with the development of VLSI technology and the advent of power microprocessors, the implementation of digital protection will be cost effective.

This paper presents the design and construction of OCRs and DOCRs with ground fault protection. A general equation is used to represent different types of time–current characteristics. The voltage phasors of the directional unit are obtained by tracing the system voltage phase and using stored voltage vectors to reduce the computational burden and hardware cost. The hardware and software of the relay are described and the relay laboratory test results are included.

2. Relay algorithms

An overcurrent relay algorithm normally includes a digital filter to extract the fundamental-frequency components, fault detection, representation of time–current characteristics and trip time emulation. This section presents these developments in some detail. The directional element and ground fault protection are also described here.

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2.1. Representation of relay time–current characteristics

The time–current characteristics of overcurrent relays are usually represented by a family of curves which are originally developed from time–current device experimental tests. A time dial setting is used to achieve a desired relay operating time and coordinate with upstream and/or downstream relays.

Several equations have been suggested for representing the time–current characteristics of overcurrent relays [3]. Warrington [4] proposed an exponential equation for calculating the relay contact closing time. Sachdev et al. investigated the use of polynomial equations, suggested in Ref. [5].

Elmore [6] presented a pair of general equations for representing the characteristics of a series of ABB CO type relays, and they are also used in the proposed relay described here. These curves are stored in the program by their coefficients and constants. When the relay initiates, it generates the direct curve data according to the relay type and time dial setting (TDS). Hence the required memory block is saved dynamically and the truncation error due to the TDS is also reduced.

Elmore's equations [6] are

$$T = \left[T_0 + \frac{K}{(M-C)^p} \right] \frac{D}{24000} \quad \text{for} \quad M \geq 1.5 \tag{1}$$

$$T = \frac{R}{M-1} \frac{D}{24000} \quad \text{for} \quad M < 1.5 \tag{2}$$

where T is the trip time in seconds, D is the TDS from 1 to 63, M is the operating current in terms of the plug setting multiple (PSM), T_0 is a defined time period, K is the scale factor for the basic inverse time, and p is an exponent determining inverseness. T_0, K, C, p and R are constants and are shown in Table 1.

2.2. Digital filter to extract the fundamental-frequency current phasor

The current waveform of a practical power system during a fault departs from a sinusoidal pattern because of the presence of DC offset and higher harmonic components. It becomes necessary to introduce a band-pass filter to reduce the constant-frequency and high-frequency components. For this purpose a digital filter [7] is used for extraction of the fundamental-frequency components from the distorted current signal. This digital filter is based on a discrete Fourier transform, where the sine and cosine waves of the fundamental frequency are cross-correlated with a distorted signal I to get the real (I_c) and imaginary (I_s) parts of the fundamental-frequency component of the signal:

$$I_c = \frac{2}{N} \sum_{r=0}^{N-1} I_{k-r} \cos\left(\frac{2\pi}{N} r\right) \tag{3}$$

$$I_s = \frac{2}{N} \sum_{r=0}^{N-1} I_{k-r} \sin\left(\frac{2\pi}{N} r\right) \tag{4}$$

The relay obtains the system currents at the rate of 12 samples per cycle and estimates the fundamental-frequency components of the current signals using discrete Fourier transform techniques. It has already been established that the use of the above filter greatly reduces the DC components and higher harmonics [7].

Table 1
Constants in Eqs. (1) and (2)

Curve no.	T_0	K	C	p	R
CO-2	111.99	735.00	0.675	1	501
CO-5	8196.67	13768.94	1.130	1	22705
CO-6	784.52	671.01	1.190	1	1475
CO-7	524.84	3120.56	0.800	1	2491
CO-8	477.84	4122.08	1.270	1	9200
CO-9	310.01	2756.06	1.350	1	9342
CO-11	110.00	17640.00	0.500	2	8875

2.3. Current r.m.s. value estimation

In the numerical implementation of an overcurrent relay, there are several schemes to store the time–current curves, namely, time–PSM^2, time–PSM and time–log(PSM). It is known that the time–current curves are quite sharp at the low values of PSM and become smooth with large values of PSM, and the memory space of a numerical relay normally has certain limitations. Considering the trade-off between the accuracy of curve representation and the required memory space, the time–PSM curve storage scheme was adopted in the proposed relay. The r.m.s. value of the fundamental component of the current signal is given by

$$I = \frac{I_c^2 + I_s^2}{2} \tag{5}$$

and is obtained iteratively using Newton's method in the proposed relay.

2.4. Relay trip time emulation

After estimating the r.m.s. value of the fundamental-frequency components of the current signals, the relay program compares each phase and/or zero-sequence currents with the respective plug setting. If any of these currents exceeds the plug setting(s), then the overcurrent algorithm is invoked. Since the fault current may be changing as time passes, direct application of Eqs. (1) and (2) may result in an erroneous trip time or even false tripping. The integral of the actuating current is commonly used to determine the instant when a trip signal should be issued.

The integration process begins immediately after the r.m.s. value of any phase and/or zero-sequence current is found to be equal to or greater than the plug setting. In the digital implementation, numerical integration is performed using the following equation, as in Ref. [8]:

$$\sum_{i=1}^{N} X_i > T_{\text{tar}} \tag{6}$$

where

$$X_i = 0 \tag{7}$$

when the current is less than the plug setting,

$$X_i = \frac{T_{\text{tar}}\,\Delta T}{T_i} \tag{8}$$

when the current is equal to or greater than the plug setting.

T_{tar} is the relay trip time target. The selection of this target number is also mentioned in Ref. [8]. However, in the proposed relay a fixed target number of 65 535 (FFFFH) is chosen for different time–current characteristics, and the accuracy of the relay operating time is still satisfactory, as shown in a later section.

In these equations, i represents the ith sample after the inception of a fault, T_i is the relay operating time, corresponding to the current r.m.s. value estimated on receiving the ith sample, which can be obtained by applying Eq. (1) or Eq. (2), and ΔT is the sampling interval. Substituting Eq. (1) or Eq. (2) in Eq. (8), X-values can be calculated for values of PSM from 1 to 20 with respect to a uniform sampling frequency of 600 Hz. In the proposed relay design, the table of X for a selected relay characteristic is generated in steps of 1/40 PSM and stored in memory when the relay initiates. In the numerical implementation, the relay algorithms are programmed with fixed-point arithmetic and the internal representation of the PSM is constructed to coincide with the stored X table, i.e. also in steps of 1/40 PSM. Thus, no interpolation is required. The program simply executes a table look-up to obtain X_i, modifies X_i according to the current sampling interval, and performs the integration and comparison as shown in Eq. (6).

As soon as the current in the protected circuit is interrupted or falls below the plug setting, the relay will be reset according to user defined resetting characteristics or default characteristics.

2.5. Directional element and ground fault protection

In the case of the DOCR, the direction of the power flow has to be determined using the following equation:

$$P = I_c V_c + I_s V_s \tag{9}$$

where V_c and V_s are the particular internally stored voltage vectors depending on the directional element connection setting (as compared with the maximum torque angle for electromechanical relays) [9]. There are five directional element settings available in the proposed relay: 0°, 30°, 45°, 60° and 90°.

The zero-sequence current phasor can be obtained either from the primary zero-sequence CT or by adding the three phase currents. This also provides a hardware self-check method for the current signal input circuit and the CT connection itself.

3. Hardware implementation

The overall hardware block diagram of the relay is shown in Fig. 1, which is comprised of the following modules: 1, current and voltage scaling module; 2, isolation amplifier and low-pass filter module; 3, analog-to-digital interface module, including zero-crossing detector; 4, central processing module; 5, operator interface module; 6, digital input and isolation module; 7, digital output module; 8, trip logic and relay module; 9, DC/DC power supply module.

The current and voltage signals are supplied by the primary CTs and the PT. The currents go directly through low-resistance shunts to be converted to voltage signals as the analog-to-digital converter only accepts voltage signals as input. Instead of using auxiliary CTs and PTs, a low-cost linear isolation amplifier is adopted in the hardware design to avoid the additional error introduced by auxiliary transducers.

The low-pass filter, isolation amplifier and the digital input and isolation module will not be discussed in this paper as these circuits are of standard form.

3.1. Analog-to-digital interface module

This module converts the output of the isolation amplifier to an equivalent numerical value. It comprises four sample-and-hold ICs, an eight-channel multiplexer and a 12-bit successive approximation A/D converter. A sensitive and accurate zero-crossing detector is included in this module to trace the system frequency and voltage phase.

3.2. Central processing module

The processor is the heart of the digital relay. An Intel 8096BH microcontroller was chosen for its power control capability and low cost. In the hardware design of this module, all memory space is implemented and the processor is upgradable to the latest Intel MCS-96 product. The external bus for accessing other modules is controlled by the processor, i.e., when the external modules are not accessed, the external bus is shut down to minimize the probability of interference.

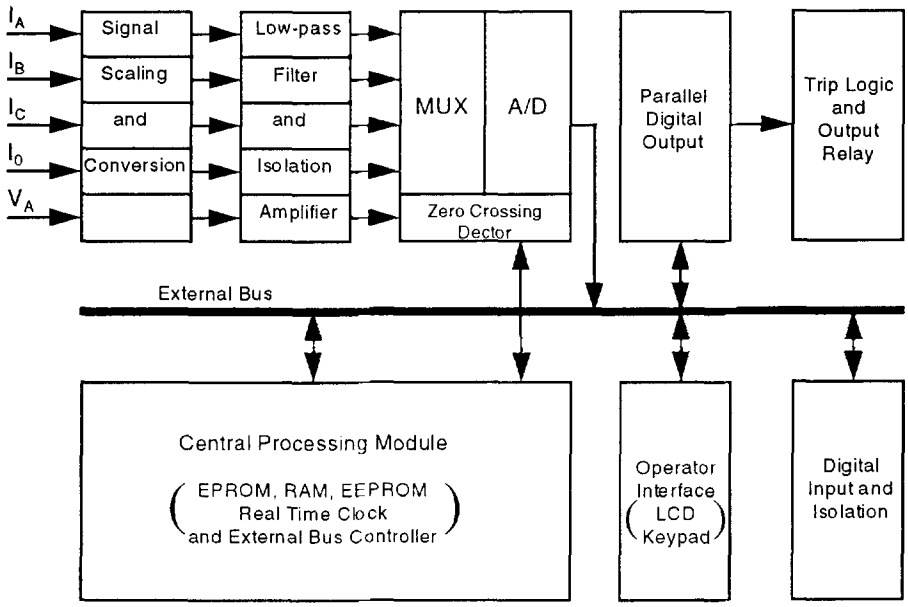

Fig. 1. Block diagram of the proposed relay hardware.

3.3. Operator interface and digital output module

The operator interface module consists of a LCD dot matrix display, a 4 × 4 multifunction keypad and some LEDs for operation status indication. The RS-232 port, also provided, can be used in a SCADA system and device maintenance.

The output and trip logic circuit is designed very carefully based on relay security considerations. Several self-monitoring and relay hardware fault blocking methods are provided in this module which can effectively detect any hardware failure except in the trip relay coils and prevent relay false tripping. High-speed mercury reed relays are selected for initiating the trip signal.

4. The digital relay functions

The relay obtains the current samples at regular intervals to determine the magnitude of the current flow in the system. As the sampling period is made frequency dependent, less error is introduced in the filtered samples when the system frequency deviates from its nominal value. The software implementation of the directional element in the case of a DOCR to find whether the fault current is flowing into its protected zone requires both the current and voltage samples. Further, if a close fault occurs, the voltage at the relay location will be almost zero and hence the relay may not be able to determine the direction of the fault current correctly. Moreover, for successful operation of the DOCR, it is necessary to find only the direction of the power flow at the relay point. For this purpose, several internally stored vectors corresponding to different directional element settings are used. In order to synchronize the phase of these voltage vectors with that of the system voltage signals, an external signal at intervals corresponding to the period of the system frequency is generated by a carefully designed zero-crossing detecting circuit which has the ability to ignore multiple zero-crossings during system distortion.

The advantages of this scheme are as follows:

(1) Voltage samples need not be obtained and hence there is no need to use a digital filter to extract the fundamental-frequency component of the voltage signal. This considerably reduces the computational burden on the processor.

(2) A counter is used to keep track of the number of machine cycles between two external zero-crossing signals of the voltage signal from a PT. As the content of this counter is a measure of the system frequency, the sampling interval can be modified accordingly. When the content of the counter exceeds the possible range with respect to the system frequency, this measure will be ignored.

(3) The sampling period for any frequency is so chosen that after the 12th sample the zero-crossing signal will occur before the next sampling timer interrupt. Even when the system frequency is continuously changing, it can make sure that the zero-crossing signal occurs just before the sampling timer interrupt for the 13th sample.

(4) When a fault has occurred very close to the relay, the system voltage may become zero; but the system frequency would not change much over the next few cycles. So, when the zero-crossing signal is not generated, the sampling interval is based on the latest value

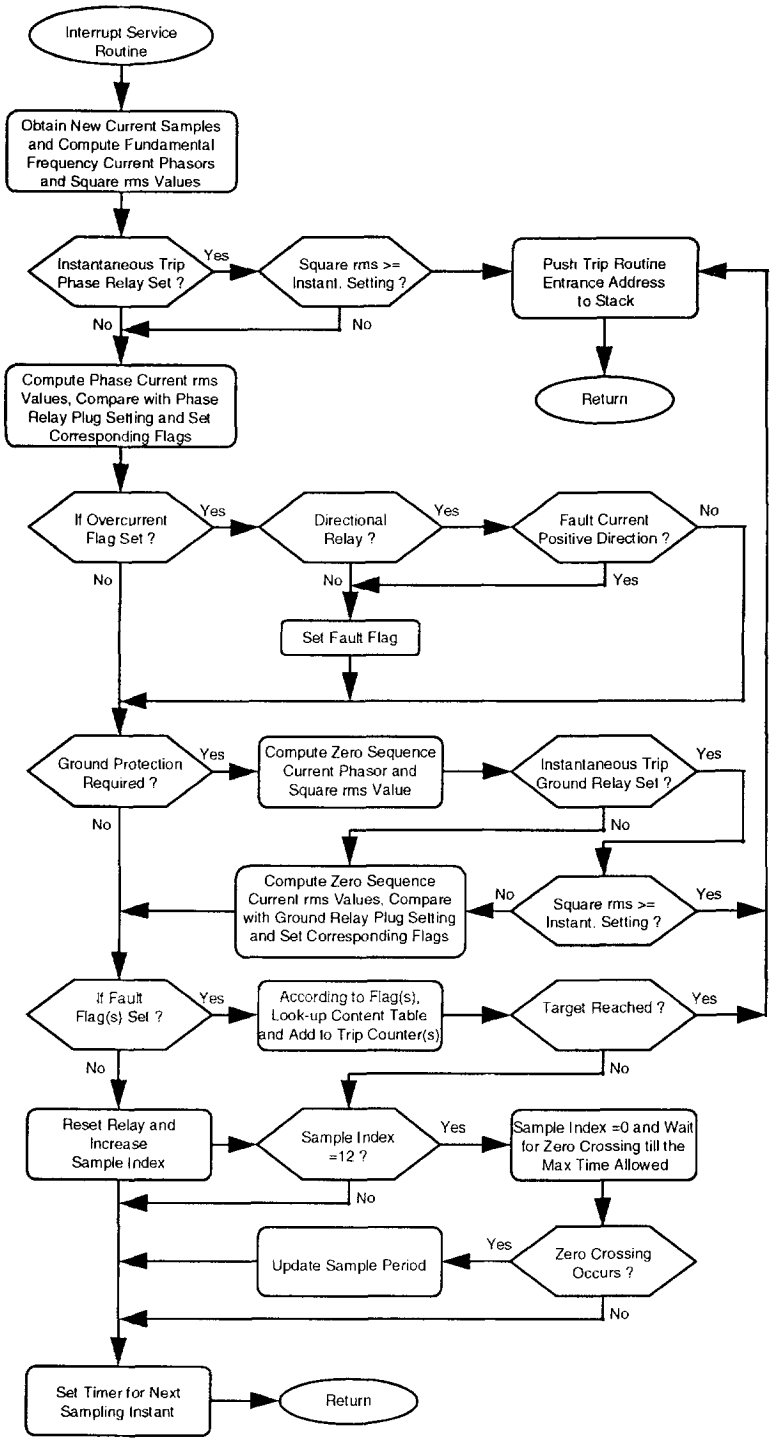

Fig. 2. Flowchart of the interrupt service routine.

of the system frequency recorded and the phase of the internally stored voltage vectors will automatically synchronize with the current samples.

The software can be divided into three segments: power-on overall hardware self-test, menu-driven operator interface and online operation.

4.1. Overall hardware self-test

When the power supply is switched on, the protection system will do an overall self-diagnosis first. If these tests fail, it will inform the operators with the error displayed. If and only if the protection system

Table 2
Test result for 1.4 × plug setting and TDS at 4

Relay type	T_{calc} (s)	T_{test} (s)	Error (%)
CO-6	0.615	0.62	0.81
CO-7	1.038	1.04	0.19
CO-8	3.833	3.84	0.18
CO-9	3.893	3.90	0.18
CO-11	3.698	3.72	0.59

Table 3
Test result for 1.5 × plug setting and TDS at 6

Relay type	T_{calc} (s)	T_{test} (s)	Error (%)
CO-6	0.737	0.74	0.41
CO-7	1.246	1.26	1.12
CO-8	4.600	4.62	0.43
CO-9	4.670	4.68	0.21
CO-11	4.375	4.44	0.57

Table 4
Test result for 2.5 × plug setting and TDS at 6

Relay type	T_{calc} (s)	T_{test} (s)	Error (%)
CO-6	0.324	0.34	4.94
CO-7	0.590	0.60	1.69
CO-8	0.957	0.96	0.31
CO-9	0.677	0.68	0.44
CO-11	1.077	1.12	3.99

passes these tests twice will it enter the protection function execution loop.

4.2. Menu-driven operation interface and relay initiation

This part of the software is the firmware of the relay. It prompts the operator to select the relay function, enter settings or do online debugging and maintenance. It is a user friendly interface.

If the operator puts the relay into commission, the relay begins initiation. It gets settings from the memory and generates the table(s) of constants. Then the relay waits for the zero-crossing signal. After determination of the sampling interval, it enters into online operation.

4.3. Online operation

The online operation includes a main routine which is actually an online self-check loop, a sampling timer interrupt routine and a fault trip routine. The interrupt service routine is for obtaining the new samples, computing current magnitude and current flow direction if necessary, fault detection and trip accumulator operation. When the trip target is reached, the fault trip routine entrance address is pushed into the processor stack, then the program goes to the fault trip routine. This routine is for issuing the trip command and detecting the line current after a certain delay of circuit breaker operation time. If the line still has current, the circuit break failure signal is issued. The flowchart of the interrupt service routine is shown in Fig. 2.

5. Laboratory performance assessment

The proposed relay was successfully constructed in the laboratory. It is housed in an industrial standard subrack system. The analog input and analog-to-digital interface modules are carefully calibrated. The accuracy of the relay to correctly emulate several CO series relay characteristics was tested. For laboratory test purposes, the relay is programmed to record the sample number from fault inception to trip command issued. The test results are compared with the theoretical calculation results and ABB published data [6]. These results are tabulated in Tables 2–7. It is found that the maximum error of the proposed relay is within 43 ms or 4.94%.

The program execution time for any online control device is very critical. If the timing of the system is not controlled properly, the relay will not function as de-

Table 5
Test result for 2.5 × plug setting and TDS at 8

Relay type	T_{calc} (s)	T_{test} (s)	Error (%)
CO-6	0.432	0.44	1.85
CO-7	0.787	0.80	1.65
CO-8	1.276	1.28	0.31
CO-9	0.902	0.90	0.22
CO-11	1.507	1.50	0.46

Table 6
Test result for 4 × plug setting and TDS at 7

Relay type	T_{calc} (s)	T_{test} (s)	Error (%)
CO-6	0.298	0.30	0.67
CO-7	0.438	0.44	0.46
CO-8	0.580	0.58	0
CO-9	0.398	0.40	0.50
CO-11	0.452	0.46	1.77

Table 7
Test result for 4 × plug setting and TDS at 11

Relay type	T_{cal} (s)	T_{test} (s)	Error (%)
CO-6	0.469	0.48	2.34
CO-7	0.688	0.70	0.29
CO-8	0.911	0.92	0.99
CO-9	0.619	0.62	0.16
CO-11	0.710	0.72	1.41

sired. Since the relay employs an iteration algorithm, the program execution time of the interrupt service routine was carefully investigated theoretically and practically. The system clock of the central processing module is 12 MHz. The internal operation of the microprocessor is based on the state time. For the 8096BH microcontroller, the state time is equal to three times the clock period. Timer 1 of the microcontroller, which is a free-running timer and is clocked once every eighth state time, is introduced to measure the program execution time. As the proposed relay samples at a frequency of 600 Hz nominally, the available time between two samples is 1666 μs or 341H with respect to timer 1. Considering the worst case of 52 Hz system frequency, the actually available time for execution of the interrupt service routine is 1602 μs or 321H. The theoretical maximum execution time to get the square root of a 32-bit long word is 236 μs. If ground protection is activated, the total maximum execution time is 944 μs or 1D8H for getting the four square roots. By properly scaling the analog input signal and carefully choosing the initial value for the square root iteration, the execution time can be reduced considerably. As well as the square root computation, other operations in the interrupt service routine are data transfer, table look-up, comparison and a very few multiplications and divisions. The practical test found that the maximum execution time is 1204 μs or 25AH.

6. Conclusion

Prototype digital overcurrent and directional overcurrent relays based on a 16-bit Intel 8096 microcontroller have been designed, constructed and tested successfully. Each unit is capable of clearing a fault according to the given characteristics. In the case of the DOCR, the direction of the fault current was identified correctly.

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