Sub: Digital Logic

1. **Which one of the following logic expression is incorrect?**
   1. $1 \oplus 1 \oplus 0 = 1$ 3. $1 \oplus 0 = 1$
   2 $1 \oplus 1 = 0$ 4. $1 \oplus 1 \oplus 1 = 1$

   Option:4

2.The time required for a gate or inverter to change its state is called

1. Decay time
2. Rise time
3. Charging time
4. Propagation time

Option:4

3.The number of canonical expressions that can be developed over a 3-valued Boolean algebra is

1. 16
2. 8
3. 64
4. 32

Option:3

4. What is the minimum number of two-input NAND gates used to perform the function of two input OR gate ?

1. two
2. one
3. four
4. three

Option:4

5. How many 1\'s are present in the binary representation of 15 x 256 5 x 16 3 is

1. 9
2. 8
3. 11
4. 7

Option:2

6. The time required for a pulse to change from 10 to 90 percent of its maximum value is called

1. Decay time
2. Rise time
3. Charging time
4. Propagation time

Option:2

7.The output of NOR gate is

1. Low if all of its inputs are low
2. High if all of its inputs are high
3. High if only of its inputs is low
4. High if all of its inputs are low

Option:4

8.Which of the following adders can add three or more numbers at a time ?

1. Carry-look-ahead adder
2. Parallel adder
3. Full adder
4. Carry-save-adder

Option:4

9.The output of NOR gate is

1. Low if all of its inputs are low
2. High if all of its inputs are high
3. High if only of its inputs is low
4. High if all of its inputs are low

Option: 4

10.Which of the following adders can add three or more numbers at a time ?

1. Carry-look-ahead adder
2. Parallel adder
3. Full adder
4. Carry-save-adder

Option:4

11. In a digital counter circuit feedback loop is introduced to

A.Improve distortion
B.Improve stability
C.Reduce the number of input pulses to reset the counter
D.Asynchronous input and output pulses

Option: C

12..Select the statement that best describes the parity method of error detection:

A. Parity checking is best suited for detecting double-bit errors that occur during the transmission of codes from one location to another.

B. Parity checking is not suitable for detecting single-bit errors in transmitted codes.

C. Parity checking is best suited for detecting single-bit errors in transmitted codes.

D. Parity checking is capable of detecting and correcting errors in transmitted codes.

Option C

13. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is a(n):

A.Ex-NOR gate

B.OR gate

C.Ex-OR gate

D.NAND gate

Option A

14.A logic circuit that provides a HIGH output if one input or the other input, but not both, is HIGH, is a(n):

A.Ex-NOR gate

B.OR gate

C.Ex-OR gate

D.NAND gate

Option C

15.Identify the type of gate below from the equation $X = A \oplus B = \bar{A}B + A\bar{B}$

A.Ex-NOR gate

B.OR gate

C.Ex-OR gate

D.NAND gate

Option C

16.How is odd parity generated differently from even parity?

A.The first output is inverted.

B.The last output is inverted.

Option B

17.How many 3-line-to-8-line decoders are required for a 1-of-32 decoder?

A.1

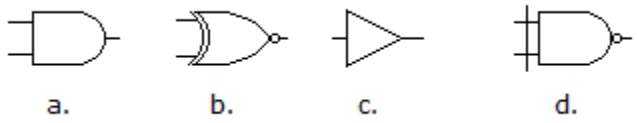
B.

C.4

D.8

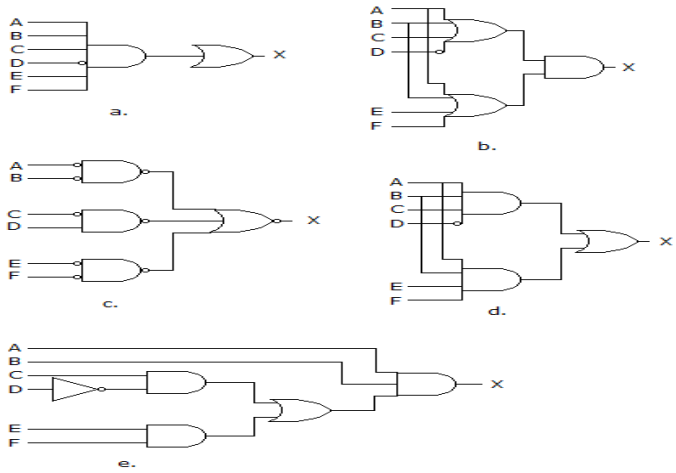
Option C

18.Which of the figures shown below represents the exclusive-NOR gate?



Answer: Option B

19.Which of the circuits in figure (a to d) is the sum-of-products implementation of figure (e)?



Option D

20.Which statement BEST describes the operation of a negative-edge-triggered D flip-flop?

A.The logic level at the *D* input is transferred to *Q* on NGT of *CLK*.

B.The *Q* output is ALWAYS identical to the *CLK* input if the *D* input is HIGH.

C.The *Q* output is ALWAYS identical to the *D* input when *CLK* = PGT.

D.The *Q* output is ALWAYS identical to the *D* input.

Option A

21.How is a *J-K* flip-flop made to toggle?

A. $J = 0, K = 0$

B. $J = 1, K = 0$

C. $J = 0, K = 1$

D. $J = 1, K = 1$

Option D

22.How many flip-flops are in the 7475 IC?

A.1

B.2

C.4

D.8

Option C

23.How many flip-flops are required to produce a divide-by-128 device?

A.1

B.4

C.6

D.7

Option D

24.How many flip-flops are required to make a MOD-32 binary counter?

A.3

B.45

C.5

D.6

Option C

25.How can a digital one-shot be implemented using HDL?

A.By using a resistor and a capacitor

B.By applying the concept of a counter

C.By using a library function

D.By applying a level trigger

Option B

26.The output of an exclusive-NOR gate is 1. Which input combination is correct?

A.A = 1, B = 0

B.A = 0, B = 1

C.A = 0, B = 0

D.none of the above

Option C

27.If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a HIGH output?

A.1

B.2

C.7

D.8

Option A

28.If a signal passing through a gate is inhibited by sending a LOW into one of the inputs, and the output is HIGH, the gate is a(n):

A.AND

B.NAND

C.NOR

D.OR

Option B

29. What is the minimum number of two-input NAND gates used to perform the function of two input OR gate ?

A. one
B. two
C. three
D. four
Option: C

30. The schmitt trigger may be used to?
[A] change voltage to corresponding frequency
[B] Change frequency to voltage
[C] Square slowly varying input
[D] None of above
Option:C
2. Which of the following is minimum error code?
[A] Octal code
[B] Grey code
[C] Binary code
[D] Excess 3 code
Option:B
31. Popular application flip-flop are ?
[A] Counters
[B] Shift registers
[C] Transfer registers
[D] All of above
Option:D

32. SR Flip flop can be converted to T-type flip-flop if ?

[A] S is connected to Q

[B] R is connected to Q

[C] Both S and R are shortend

[D] S and R are connected to Q and Q' respectively

Option: D

33. Register is a ?
[A] Set of capacitor used to register input instructions in a digital computer
[B] Set of paper tapes and cards put in a file
[C] Temporary storage unit within the CPU having dedicated or general purpose use
[D] Part of the auxiliary memory
Option:C

34. For which of the following flip-flop the output clearly defined for all combinations of two inputs?
[A] Q type flip-flop
[B] R S type flip-flop
[C] J K flip-flop
[D] T flip-flop

Option:C

35. A simple flip-flop
[A] is 2 bit memory
[B] is 1 bit memory
[C] is a four state device
[D] has nothing to do with memory

Option:B

36. An SR flip flop cannot accept the following input entry
[A] Both input zero
[B] zero at R and one at S
[C] zero at S and one at R
[D] Both inputs one

Option:D

37. The main difference between JK and RS flip-flop is that?
[A] JK flip-flop does not need a clock pulse
[B] there is feedback in JK flip-flop
[C] JK flip-flop accepts both inputs as 1
[D] JK flip-flop is acronym of junction cathode multivibrator

Option:C

38. Radix of binary number system is _____?
[A] 0
[B] 1
[C] 2
[D] A & B

Option:C

39.What is the minimum number of two-input NAND gates used to perform the function of two input OR gate?

A) 2 B) 1 C) 4 D) 3

Option:D

40 . If A ⊕ B = C, then

A) B ⊕C = A C) A ⊕C = B
B) A ⊕B ⊕C =0 D) All of these

Option: A

41. How many truth tables can be made from one function table ?

A) Two B) One

C) Any numbers D) Three

Option:A

42 which of the following is fastest Logic family

A) TTl C) ECL
B) DTL D) CMOS

Option:C

43 CMOS stands for

A. Complementary metal oxide semiconductors B. Compulsory metal oxide semiconductors

C. Complementary metal oxygen semiconductors D. NONE

Answer **Complementary metal oxide semiconductors**

44 The digital logic family which has minimum power dissipation is

A. TTL B. RTL

C. DTL D. CMOS

Answer CMOS

4 5 .The logic 0 level of a CMOS logic device is approximately

A. 1.2 volts B. 0.4 volts

C. 5 volts D. 0 volts

Answer 0 volts

46. CMOS circuits consume power

A. Equal to TTL B. Less than TTL

C. Twice of TTL D. Thrice of TTL

Answer Less than TTL

47. Which of the following logic families has the shortest propagation delay?

A. CMOS B. TTL

C. ECL D. 74SXX

Answer ECL

48. The output stage of most TTL logic is

A. To-tem pole B. adder

C. push-pull D. none

AnswerTo-tem pole

49. The following logic families have their propagation delay. Arrange them from lowest propagation delay to highest propagation delay. 1. TTL (Standard) 2. ECL 3. Low power CMOS 4. DTL

A. 2, 1, 4, 3 B. 2,4,1,3

C. 4,2,3,1 D. 1,2,3,4

Answer 2, 1, 4, 3

50. If the various logic families are arranged in the ascending order of their fan-out capabilities, the sequence will be

A. TTL, DTL, ECL, MOS

B. DTL, TTL, MOS, ECL

C. MOS, DTL, TTL, ECL

D. ECL, TTL, DTL, MOS

Answer MOS, DTL, TTL, ECL

51. Consider the following logic families & correct sequence of the logic families in the order of their increasing noise margin. 1. MOS 2. TTL 3. RTL 4. ECL

A. 3, 4, 1, 2

B. 3, 4, 2, 1

C. 4, 3, 2, 1

D. 4, 3, 1, 2

Answer 3, 4, 1, 2

52. Which is not a bipolar logic family?

A. TTL

B. ECL

C. IIL

D. NMOS

Answer NMOS

53.Which logic family dissipates the minimum power?

A. DTL

B. TTL

C. ECL

D. CMOS

Answer: Option

54.Combinational logic circuit which is used to send data coming from a single source to two or more separate destinations is called as

A. decoder

B. encoder

C. multiplexer

D. de-multiplexer

Answer: Option D

55. What logic function is obtained by adding an inverter to the inputs of an AND gate?

A. OR

B. NAND

C. XOR

D. NOR

Answer: Option D

56.An OR gate has 6 inputs. How many input words are in its truth table?

A. 64

B. 32

C. 16

D. 128

Answer: Option A

57.Which of the following Boolean algebra statements represent commutative law

A. (A+B)+CA+(B+C)

B. A.(B+C)(A.B)+(A.C)

C. A+BB+A

D. A+AA

E. None of the above

Answer: Option C

58. A multiplexer is also known as

A. coder

B. decoder

C. data selector

D. multivibrator

E. None of the above

Answer: Option C

59. An AND gate has 7 inputs, what is the only input word that produces a 1 output?

A. 0

B. 1111

C. 1110000

D. 1111111

Answer: Option D

60. The Gray code for decimal 7 is

A. 111

B. 1011

C. 100

D. 101

Answer: Option C

61. Select the statement that best describes the parity method of error detection:

A. Parity checking is best suited for detecting double-bit errors that occur during the transmission of codes from one location to another.

B. Parity checking is not suitable for detecting single-bit errors in transmitted codes.

C. Parity checking is best suited for detecting single-bit errors in transmitted codes.

D. Parity checking is capable of detecting and correcting errors in transmitted codes.

Answer: Option C

62. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is a(n):

A. Ex-NOR gate

B. OR gate

C. Ex-OR gate

D. NAND gate

Answer: Option A

63. A logic circuit that provides a HIGH output if one input or the other input, but not both, is HIGH, is a(n):

A. Ex-NOR gate

B. OR gate

C. Ex-OR gate

D. NAND gate

Answer: Option C

64. Identify the type of gate below from the equation $X = A \oplus B = \bar{A}B + A\bar{B}$

A.Ex-NOR gate

B.OR gate

C.Ex-OR gate

D.NAND gate

Answer: Option C

65. How is odd parity generated differently from even parity?

A.The first output is inverted.

B.The last output is inverted.

Answer: Option B

A. Propagation delay in TTL is due to slow switching speeds.

A. True B. False

Answer False

B. In TTL the noise margin is between 0.8 V and 0.4 V.

A. True B. False

AnswerTrue

C. CMOS has High speed as compared to TTL

A. True B. False

Answer False

D. When using TTL logic to drive CMOS logic the high level voltage of the TTL output must be increased with a pull-up resistor.

A. True B. False

Answer True

E.When the two logic families being interfaced have different power supplies then special circuits called level shifters or translators must be used.

A. True B. False

Answer True

F. The CMOS family has high input impedance and very high power consumption.

A. True B. False

Answer False

G. ECL IC technology is faster than TTL technology

A. True B. False

Answer True

H. There are four different logic levels in TTL and CMOS: V IH, V IL, V OL, V OH

A. True B. False

AnswerTrue