CISC vs RISC

Lesson 3

CISC (Complex Instruction Set Computer)

- CISC was developed to make compiler development easier and simpler.
- They are chips that are easy to program that makes efficient use of memory.
- CISC eliminates the need for generating machine instructions to the processor.
- For example, instead of having to make a compiler, write lengthy machine instructions to calculate a square-root distance, a CISC processor offers a built-in ability to do this.
- Many of the early computing machines were programmed in assembly language. Computer memory was slow and expensive.
- CISC was commonly implemented in such large computers
- Examples of CISC processors are the System/360, VAX, PDP-11, Motorola 68000 family, AMD, and Intel x86 CPUs.

CISC:

Characteristics of CISC

- A large number of instructions.
- Instruction-decoding logic will be complex.
- Instructions for special tasks used infrequently.
- A large variety of addressing modes
- It offers variable-length instruction formats.
- Instruction are larger than one-word size.
- Instruction may take more than a single clock cycle to get executed.
- Less number of general-purpose registers as operation get performed in memory itself.
- Various CISC designs are set up with two special registers for the stack pointer for managing interrupts

RISC(Reduced Instruction Set Computer)

- It is a microprocessor that is designed to perform smaller number of computer instruction so that it can operate at a higher speed.
- RISC instruction sets hold less than 100 instructions and use a fixed instruction format.
- This method uses a few simple addressing modes that use a register-based instruction.
- In this compiler development mechanism, LOAD/STORE is the only individual instructions for accessing memory.
- Examples of processors with the RISC architecture include MIPS, PowerPC, Atmel's AVR, the Microchip PIC processors, Arm processors, RISC-V.

RISC:

Characteristics of RISC

- Simpler instruction decoding
- A number of general-purpose registers.
- Simple Addressing Modes
- Fewer Data types.
- A pipeline can be achieved
- One instruction per cycle
- Register-to-register operations
- Simple instruction format
- Instruction execution would be faster
- Smaller Programs

CISC	RISC
It has a microprogramming unit.	It has a hard-wired unit of programming.
The instruction set has various different instructions that can be used for complex operations.	The instruction set is reduced, and most of these instructions are very primitive.
Performance is optimized with emphasis on hardware.	Performance is optimized which emphasis on software
Only single register set	Multiple register sets are present
They are mostly less or not pipelined	This type of processors are highly pipelined
Execution time is very high	Execution time is very less
Code expansion is not a problem.	Code expansion may create a problem.
Decoding of instructions is complex.	The decoding of instructions is simple.
It requires external memory for calculations	It doesn’t require external memory for calculations
Examples of CISC processors are the System/360, VAX, AMD, and Intel x86 CPUs.	Common RISC microprocessors are ARC, Alpha, ARC, ARM, AVR, PA-RISC, and SPARC.

CISC	RISC
More efficient use of RAM than RISC	Heavy use of RAM (can cause bottlenecks if RAM is limited)
Simple, standardized instructions	Complex and variable-length instructions
A small number of fixed-length instructions	A large number of instructions
Limited addressing modes	Compound addressing modes
Important applications are Security systems, Home automation.	Important applications are : Smartphones, PDAs.
Varying formats (16-64 bits for each instruction).	fixed (32-bit) format
Unified cache for instructions and data.	Separate data and instruction cache.
Instructions can take several clock cycles	Single-cycle for each instruction