A-D Converters

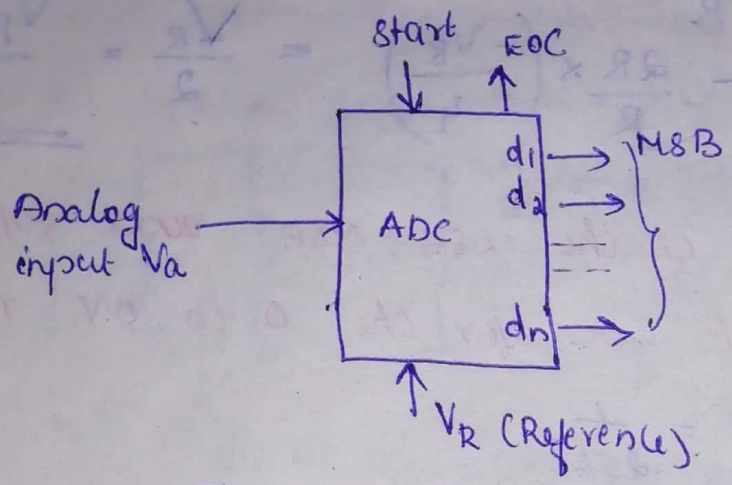

Fig: Functional diagram of ADC.

It provides the function just opposite to that of a DAC. It accepts an analog input voltage V_a and produces an output binary word $d_1, d_2, \ldots d_n$ of functional value D, so that

$$D = d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}$$

$d_1 \rightarrow$ MSB

$d_n \rightarrow$ LSB

ADC has two additional control lines: the START input to tell the ADC when to start the conversion and the EOC [End of Conversion] output to announce when the conversion is complete.

ADCs are classified broadly into two groups according to their conversion technique.

(a) Direct type ADCs

(b) Integrating type ADCs

Direct type ADCs compare a given analog signal with the internally generated equivalent signal. This group includes:

Flash (comparator) type converter.

Counter type converter.

Tracking or servo converter

Successive approximation type converter.

Integrating type ADCs perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code. This group includes:

charge balancing ADC

Dual slope ADC.

* Most commonly used ADCs are successive approximation and the integrator type.

Successive Approximation Converter

It uses very efficient code search strategy to complete n-bit conversion in just n-clock periods. An eight bit converter would require eight clock pulses to obtain a digital output.

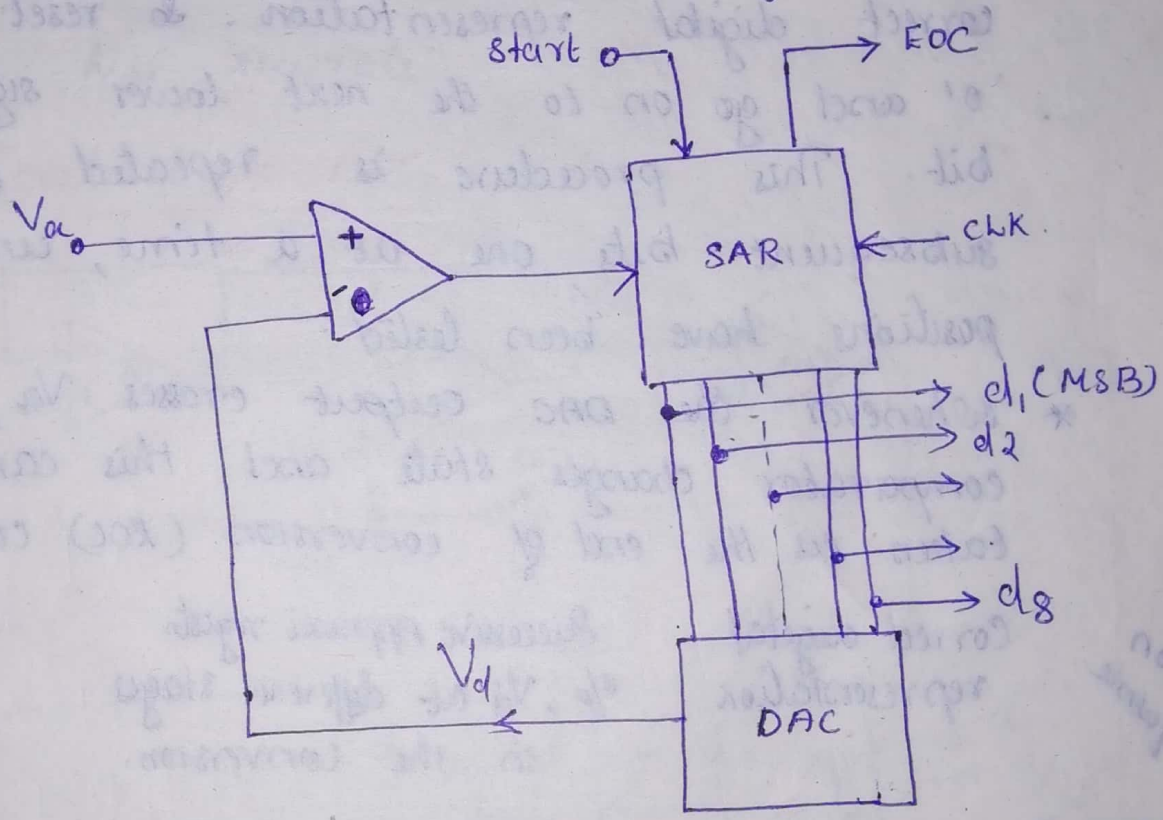

Fig: Functional diagram of the successive approximation ADC.

The figure shows an 8-bit converter. It uses a successive approximation register (SAR) to find the required value of each bit by trial and error. With the arrival of the START command, the SAR sets the MSB $d_1 = 1$ with all other bits to zero so that

the trial code is 10000000.

* The o/p of the DAC, V_d is now compared with analog input V_a.
* If $V_a > V_d$, then 10000000 is less than the correct digital representation. The MSB is left at '1' and the next lower significant bit is made '1' and further tested.
* If $V_a < V_d$, then 10000000 is greater than the correct digital representation. So reset MSB to '0' and go on to the next lower significant bit. This procedure is repeated for all subsequent bits one at a time, until all bit positions have been tested.
* Whenever the DAC output crosses V_a, the comparator changes state and this can be taken as the end of conversion (EOC) command.

Conversion sequence

Correct digital representation	Successive Approxi register o/p, V_d at different stages in the conversion.	Comparator o/p
11010100	10000000	1
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	—

It require eight pulses to establish the accurate output regardless of the value of the analog input.

Advantages

* The most commonly used ADCs are successive approximation and the integrator type.
* Successive approximation converter is faster.

Applns: → * used in applications such as data loggers and instrumentation where conversion speed is imp.

Disadvantage: → less accurate.

The parallel Comparator [Flash] A/D converter

* This is the simplest possible A/D converter.
* This is the fastest and most expensive technique.

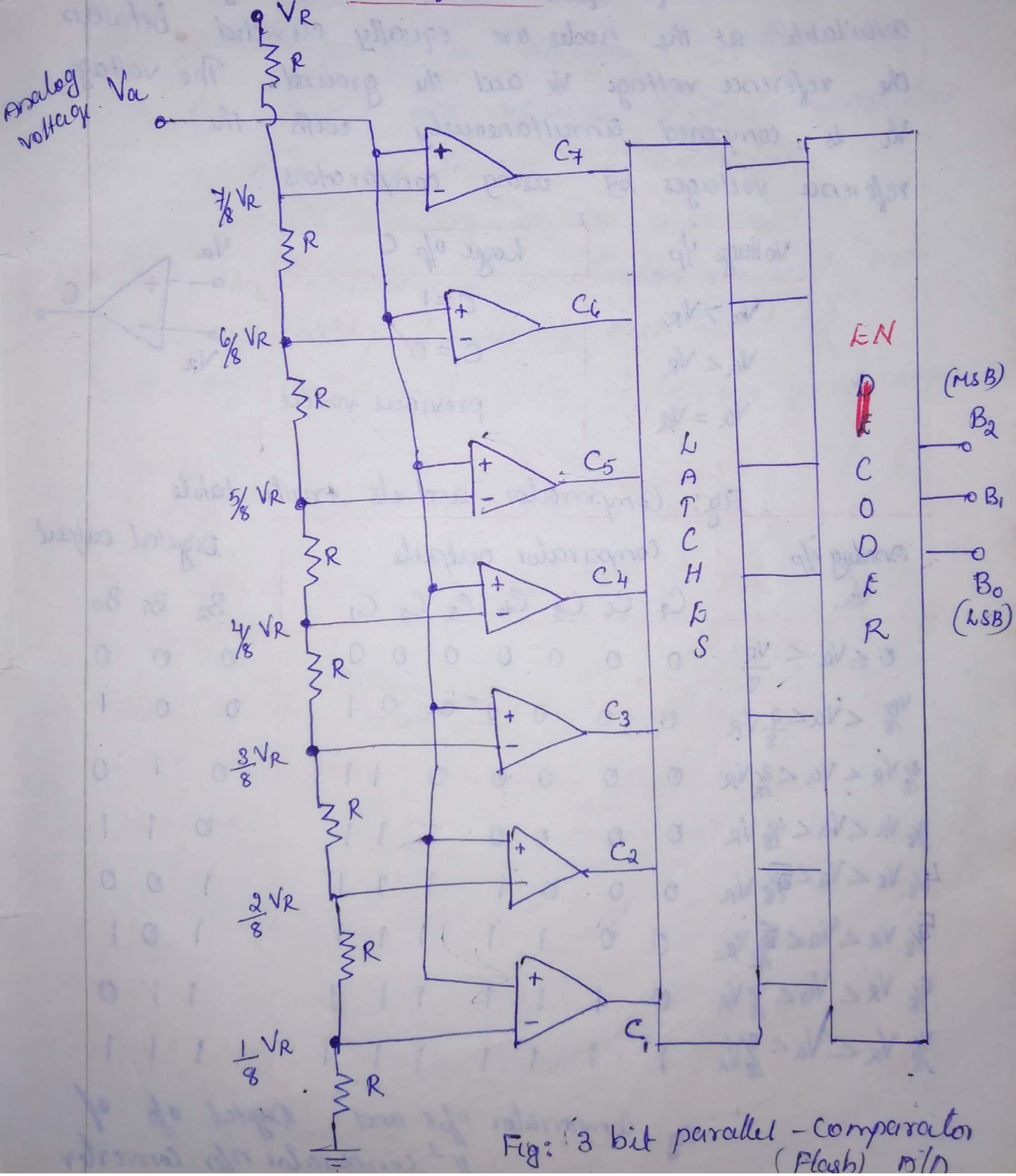

Fig: 3 bit parallel - Comparator (Flash) A/D

The circuit consists of a resistive divider network. At each node of the resistive divider, a comparison voltage is available. Since all resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage V_R and the ground. The voltage V_a is compared simultaneously with the reference voltages by using comparators.

Voltage i/p	Logic o/p C
$V_a > V_R$	C = 1
$V_a < V_R$	C = 0
$V_a = V_R$	previous value

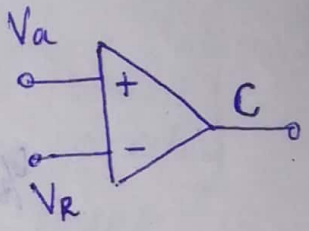

Fig: Comparator and its truth table

Analog i/p	Comparator outputs							Digital output		
V_a	C_7	C_6	C_5	C_4	C_3	C_2	C_1	B_2	B_1	B_0
$0 \le V_a < \frac{V_R}{8}$	0	0	0	0	0	0	0	0	0	0
$\frac{V_R}{8} < V_a < \frac{2}{8}V_R$	0	0	0	0	0	0	1	0	0	1
$\frac{2}{8}V_R < V_a < \frac{3}{8}V_R$	0	0	0	0	0	1	1	0	1	0
$\frac{3}{8}V_R < V_a < \frac{4}{8}V_R$	0	0	0	0	1	1	1	0	1	1
$\frac{4}{8}V_R < V_a < \frac{5}{8}V_R$	0	0	0	1	1	1	1	1	0	0
$\frac{5}{8}V_R < V_a < \frac{6}{8}V_R$	0	0	1	1	1	1	1	1	0	1
$\frac{6}{8}V_R < V_a < \frac{7}{8}V_R$	0	1	1	1	1	1	1	1	1	0
$\frac{7}{8}V_R < V_a < \frac{8}{8}V_R$	1	1	1	1	1	1	1	1	1	1

Fig: Comparator o/ps and Digital o/p of 11 comparator A/D converter

advant.

A 7-bit output is obtained from the comparators which is stored in latches. This 7-bit digital signal is converted to a 3-bit output by using an ~~decoder~~ encoder circuit. Here the conversion take place simultaneously so this is the fastest one.

* An n-bit ADC requires $2^n - 1$ comparators
  ie 2-bit ADC requires 3 comparators
  3-bit ADC requires 7 comparators.

Disadva →

* The number of comperators required are approximately doubles for each added bit.
* Larger the value of n, then it becomes more complex.