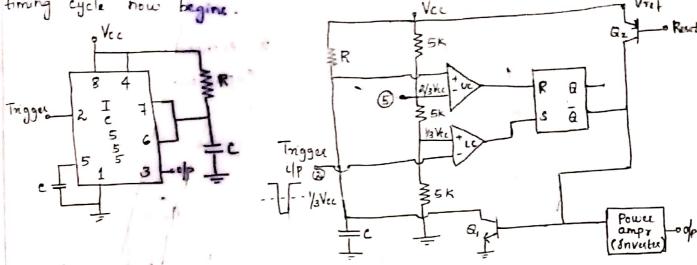
passes through 1/3 Vec at -ve 1/p of LC, the LC comparator of p is one and the FF is set is \$2:0. This makes \$0.0 FF and short linewet across C is released. As \$\tilde{a}\$ is Low, of p goes HIGH. The timing cycle now begins.

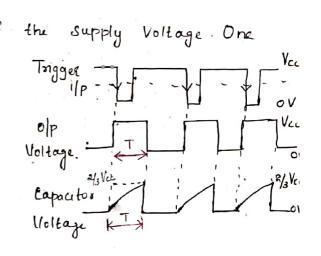


Since [in unclamped, the Voltage across it vises exponentially through R towards Vec with a time const RC. After a time period T the Capacitor Voltage is just greater than 2/3 Vec and the UC resets the FF. This makes \$\overline{L}=1\$, \$\overline{A}\$, turns on there by discharging the Capacitor C rapidly to 3nd potential. The olp is kero is returns to a Stand by State.

The Voltage across the Capacitor $V_c = V_f + (V_i - V_f)e^{-t/Rc}$ $V_f = V_{cc} \quad \text{S} \quad V_i = 0 \quad \text{i.} \quad V_c = V_{cc} \left[i - e^{-t/Rc}\right]$ at $t = T^2$ $V_c = \frac{2}{3} V_{cc}$

$$\frac{1}{3} \text{ Vec} = \text{ Vec} \left[1 - e^{-T/RC} \right]$$
 $\frac{2}{3} = 1 - e^{-T/RC} \implies e^{-T/RC} = \frac{1}{3}$
 $\frac{7}{16} = \frac{1}{16} = \frac$

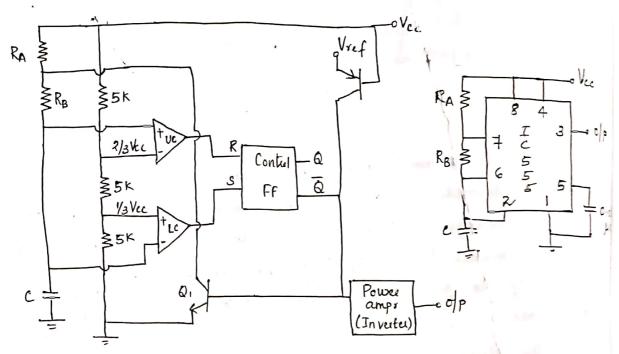
The timing interval is independent of triggered, of remains high until the time T elapses, which depends on R and c. Any additional trigger coming during this time will not change the olp state. But if a reset signal is applied the \$55 circuit will be in reset condition and olp is Zero.



ASTABLE MULTIVIBRATOR USING IC 555

An astable Multivibrator often called a free nenning multiple Tt does not require an exteenal trigger to change the state the olp, hence the name free minning.

The time during which the olp is either high or low is determined by two resistors and a Capacitor which are externally connected to the \$55 times.



Working:

When the power supply V_{cc} is connected the external timing Capacitor C Charges toward V_{cc} with time Const $(R_A+R_B)c$. During this time the olp is equal to HIGH (i. initially the capacitor Voltage is Xero and olp of UC is LOW and olp of CC is HIGH in R=0 and S=1, FF Sets in $\bar{Q}=0$ and O|P=1).

When the Capacitor Voltage is just greater than $\frac{2}{3}$ Vec the Vetriggers and R=1 which resets the FF and $\bar{\alpha}=1$. Hence Op is Zero. This in turn make $\bar{\alpha}_1$ ON and the Capacitor starts discharge towards ground through RB and $\bar{\alpha}_1$ with a time Censt RBC

During the discharge the Capacitor Voltage is just less than 1/3 Vcc, the LC is inggered is S=1 and R=0 which turn R=0 and O[P=1 The Capacitor C is thus periodically charged and discharged between 2/3 Vcc and 1/3 Vcc respectively. The length of time that the OIP remains HIGH is the time for the Capacitor Charge from 1/3 Vcc to 2/3 Vcc