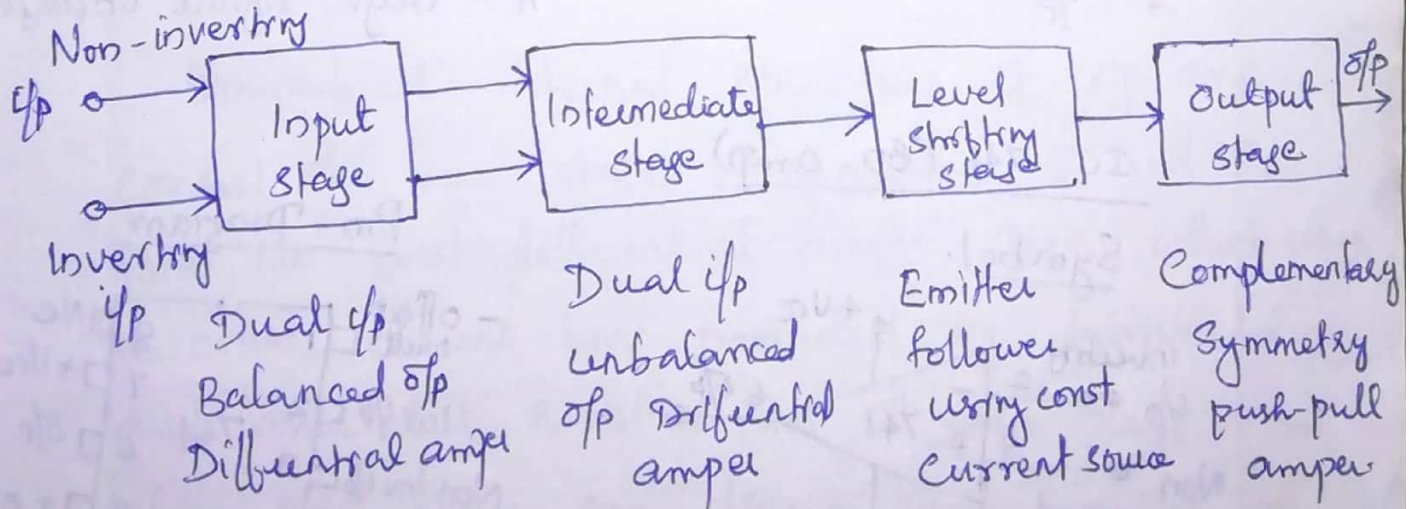
Analog Circuits II

Operational Amplifiers

An operational amplifier is a direct coupled high gain amplifier usually consisting of one or more differential amps and usually followed by a level translator and an output stage.

The operational amp is a versatile device that can be used to amplify dc as well as ac i/p signals and was originally designed for performing mathematical operations such as addition, subtraction, multiplication and integration. Op-amp can be used for variety of another applications like active filters, oscillators, comparators, regulators etc ..

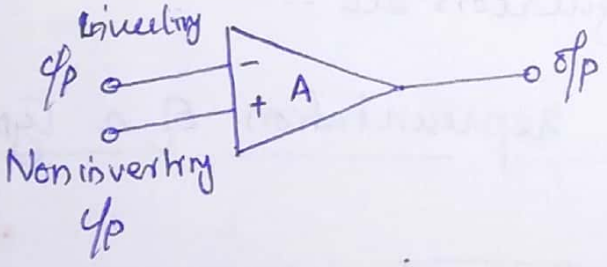
Block diagram representation of a typical Op-amp



i/p stage generally provides most of the voltage gain of the amper and also establishes the i/p resistance of op-amp. Intermediate stage is driven by the o/p of the first stage. It is a dual i/p unbalanced o/p differential amper.

A level translator is used to shift the d.c level at the o/p of intermediate stage to zero with respect to gnd (Because direct coupling is used, the dc voltage at the o/p of intermediate stage is above gnd potential). The o/p stage increases the o/p voltage swing and raises the current supplying capability of the Op-amp.

Schematic Symbol

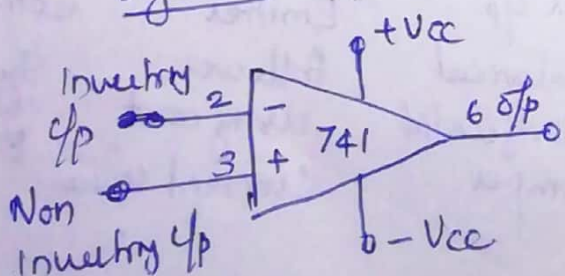


In the fig., for simplicity power supply and other pin connections are omitted.

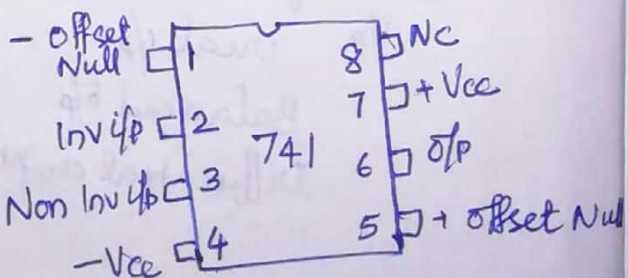
A - Large signal voltage gain

IC 741 (Op-amp)

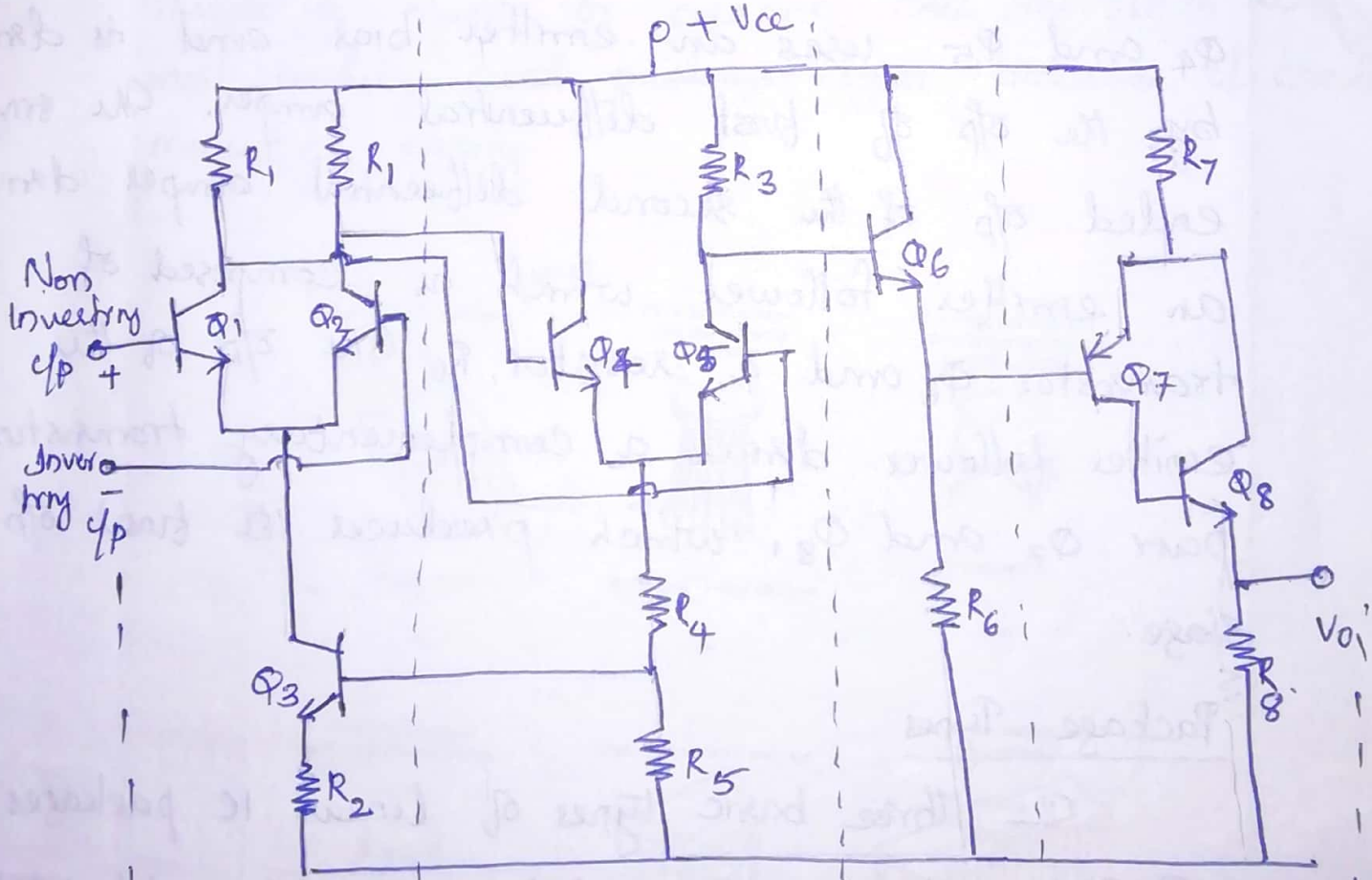
Symbol.



Pin-Diagram



Simplified Internal Circuit of Op-amp (MC 1435)

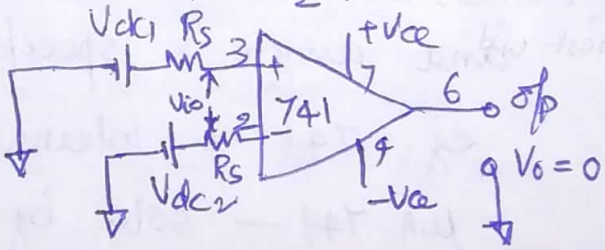


Electrical Parameters (Non-ideal characteristics)

Input offset voltage (V_{io})

I/p offset voltage is the voltage that must be applied between the two I/p terminals of an op-amp to null the o/p. force the o/p volt to zero. The o/p offset voltage

$V_{io} = V_{dc_1} - V_{dc_2}$.



I/p offset voltage V_{io} could be +ve or -ve. ∴ absolute value as listed in the data sheet.

e.g. 741C precision op-amp V_{io} = 150μ

For a 741C max. value of V_{io} is 6mV.

The smaller the value of V_{io} better the I/p terminals

are matched.

Input offset current (I_{io})

The algebraic difference between the currents into the inverting and non-inverting terminals is referred to as i/p offset current I_{io}.

$$I_{io} = |I_{B1} - I_{B2}|$$

I_{B1} → current into + terminal
I_{B2} → " into − terminal

i/p offset current for 741 C is 200nA max.

As the matching between two i/p terminals are improved, the difference between I_{B1} and I_{B2} becomes smaller.

741C precision op-amp – I_{io} – 6nA.

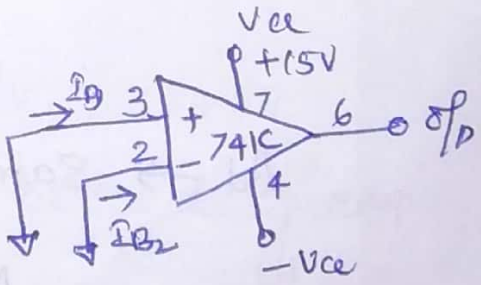
Input Bias Current

Input bias current I_B is the avg. of the currents that flow into the inverting and non inverting i/p terminals of the op-amp.

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

For 741C I_B = 500nA. max.

For precision 741C $I_B = \pm 7$nA.



I_{B1}, I_{B2} are the base currents of the first differential amplifier stage.

→ Total o/p offset v.g (p.t.o a/c ideal chara)

Differential Input Resistance

Differential i/p resistance R_i is the equivalent resistance that can be measured at

either the inverting or non inverting i/p terminal with other terminal connected to gnd.

For 741c – i/p R – 2MΩ

For FET op-amp R_i^o is large, μAF 771 FET $R^o = 10^{12}\Omega$

Input Capacitance

i/p capacitance C_i^o is the equivalent capacitance that can be measured at either the inverting or non inverting terminal with other terminal connected to gnd.

For 741C C_i^o – 1.4PF

Common Mode Rejection Ratio (CMRR)

CMRR is defined as the ratio of the differential voltage gain Ad to the common mode voltage gain Acm.

$$CMRR = \frac{A_d}{A_{cm}}$$

Ad → Same as the large signal voltage gain A.

$A_d = \frac{V_o}{V_{id}}$ $\quad A_{cm} = \frac{V_{ocm}}{V_{icm}}$

V_{ocm} – o/p common mode voltage

V_{cm} – i/p common mode voltage

Acm is very small.

CMRR is very large – so it is expressed in dB.

For 741C – CMRR is 90 dB.

The higher the value of CMRR, the better is the matching between two i/p terminals, and smaller is the o/p common mode voltage.

For 741C – precision op-amp CMRR – 120dB.

Supply Voltage Rejection Ratio (SVRR)

The change in an op-amp's input offset voltage Vio caused by variations in supply voltages is called the supply voltage rejection ratio (SVRR).

It is also termed as power supply rejection ratio (PSRR) and power supply sensitivity (PSS).

If the change in supply voltage is ΔV and the corresponding change in i/p offset voltage is ΔV_{io},

$$SVRR = \frac{\Delta V_{io}}{\Delta V}$$

For 741C SVRR = ~~max~~ 150 μV/V / 104 dB

Lower the value of SVRR, better the op-amp performance.

Large Signal Voltage Gain

$$\text{Voltage gain} = \frac{\text{o/p voltage}}{\text{Differential i/p voltage.}}$$

$$A_d = \frac{V_o}{V_{id}}$$

Output Resistance (R_o)

O/p resistance R_o is the equivalent resistance that can be measured between the o/p terminal of the Op-amp and the gnd.

For 741C — $R_o \rightarrow 75\Omega$.

Slew Rate (SR)

Slew rate is defined as the maximum rate of change of o/p voltage per unit time.

It is expressed in volts per microseconds.

$$SR = \frac{dV_o}{dt} \quad V/\mu s$$

Slew rate indicates how rapidly the o/p of an op-amp can change in response to changes in i/p frequency. The slew rate changes with change in voltage gain and is normally specified at unity gain. Slew rate of an op-amp is fixed.

The slew rate is one of the important factors in selecting the op-amp for ac applications particularly at relatively high frequencies.

For 741C slew rate 0.5V/μs [Low value disadvantage]

LM 318 → high speed op-amp slew rate 70V/μs.

Gain Bandwidth Product

The gain band width product (GB) is the band width of the op-amp when the voltage gain is 1.

For 741C GB is 1MHz.

The Ideal Op-amp

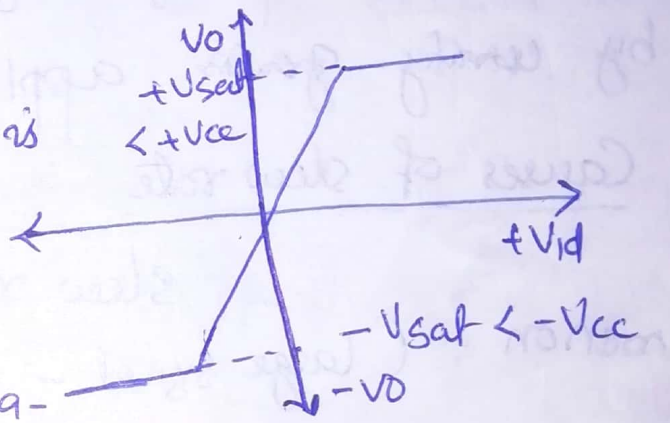
An ideal op-amp would exhibit the following electrical characteristics.

1. Infinite voltage gain A (Non ideal – 2×10^5)
2. Infinit i/p R so that almost any signal source can drive it and there is no loading of the preceding stage (non ideal – 2MΩ)
3. Zero o/p R, so that the o/p can drive an infinite number of other devices. (Non ideal 75Ω)
4. Zero o/p voltage when i/p voltage is zero (Non ideal)
5. Infinite B.W so that any freq. signal from 0 to ∞Hz can be amplified without attenuation. (Non ideal 1MHz)
6. Infinite CMRR so that the o/p common mode noise voltage is zero (non ideal 90 dB)
7. Infinite slew rate so that o/p voltage changes

Ideal voltage transfer curve.

o/p voltage Vo is plotted against Vid, keeping gain A is const.

o/p v is proportional to i/p voltage only until it reaches saturation.



values for the 741C are given in Table 29.2.

TABLE 29.2. *Ideal and Typical Characteristics of a Monolithic Op-amp IC*

Particulars	Ideal	Typical Values For 741C
Voltage gain (open-loop)	∞	2×10^5
Output impedance	0	75 Ω
Input impedance	∞	2 MΩ
Offset voltage	0	2 mV
Offset current	0	20 nA
Bandwidth (BW)	∞	1 MHz