Expression for Capacitor Voltage

$$V_c = V_f + (V_i - V_f)\, e^{-t/RC}$$

$V_i = 1/3\, V_{cc}$ & $V_f = V_{cc}$

$$V_c = V_{cc} + \left[\frac{1}{3}V_{cc} - V_{cc}\right] e^{-t/RC}$$

At time $t = T_{HIGH}$ $\quad V_c = 2/3\, V_{cc}$

$$\frac{2}{3}V_{cc} = V_{cc} + \left[\frac{1}{3}V_{cc} - V_{cc}\right] e^{-T_{HIGH}/RC}$$

$$\frac{2}{3} = 1 + \left(\frac{1}{3} - 1\right) e^{-T_{HIGH}/RC}$$

$$\frac{2}{3}\, e^{-T_{HIGH}/RC} = 1/3$$

$$T_{HIGH} = 0.69\, RC$$

Capacitor charges through R_A & R_B $\therefore T_{HIGH} = 0.69\,(R_A + R_B)\,C$

The o/p is low while the capacitor discharges from $2/3\, V_{cc}$ to $1/3\, V_{cc}$.)

Voltage across capacitor $V_c = V_f + (V_i - V_f)\, e^{-t/RC}$

$V_f = 0$ & $V_i = 2/3\, V_{cc} \Rightarrow V_c = 0 + (2/3\, V_{cc} - 0)\, e^{-t/RC}$

At $t = T_{Low}$, $V_c = 1/3\, V_{cc}$

$$\therefore \frac{1}{3}V_{cc} = \frac{2}{3}V_{cc}\, e^{-T_{Low}/RC}$$

$$T_{Low} = 0.69RC$$

Capacitor discharges through R_B $\therefore T_{Low} = 0.69\, R_B\, C$

Total Time $= T_{HIGH} + T_{Low}$

$$T = 0.69\,(R_A + 2R_B)\,C$$

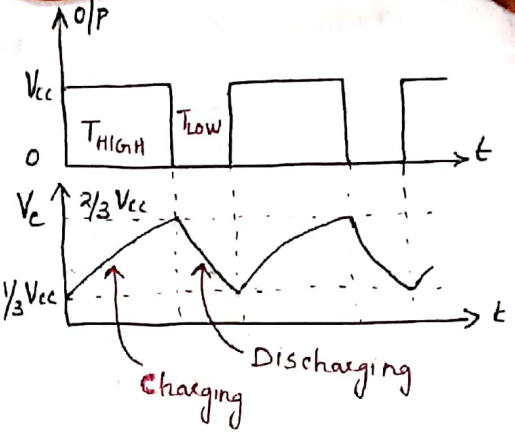
$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)\,C}$$

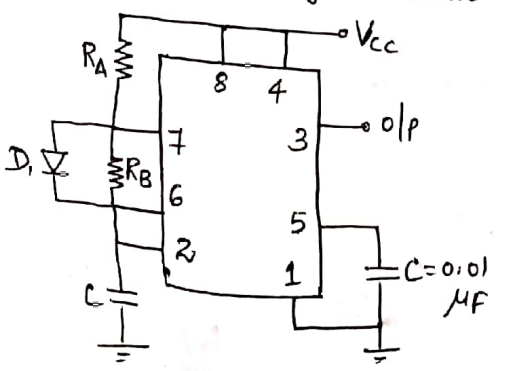
$$\% \text{ Duty cycle} = \frac{T_{HIGH}}{T} \times 100 = \frac{0.69\,(R_A + R_B)\,C}{0.69\,(R_A + R_B)\,C + 0.69\,R_B\,C}$$

To get 50% Duty cycle R_A must be reduced to zero. It is not practically possible because high current will flow through Q_1 & damage Q_1.

An alternative circuit to set duty cycle 50% is shown in fig.

During charging D_1 is forward biased effectively short circuiting R_B so that $T_{HIGH} = 0.69\, R_A\, C$





During discharging portion Q_1 ON and grounding pin 7, hence D_1 is in reverse biased condition. So $T_{LOW} = 0.69 R_B C$

$$T = T_{HIGH} + T_{LOW} = 0.69 (R_A + R_B) C$$

$$f = \frac{1}{T} = \frac{1.45}{(R_A + R_B) C}$$

$$\text{Duty cycle} = \frac{R_B}{R_A + R_B}$$

If $R_A = R_B$, % Duty cycle = 50 %.

PHASE LOCKED LOOP (PLL)

A Phase Locked loop (PLL) is basically a closed loop feedback system. The action of the PLL is to Lock the o/p frequency and Phase to the frequency and phase of i/p signal.

Operating Principles of PLL

The PLL is a circuit which causes a particular system to track with another one ie PLL Synchronizes an o/p with an i/p signal in frequency as well as phase. In Synchronized State or locked state the phase error between the oscillators o/p and the i/p signal is zero or very small.

If the phase error builds up, a control mechanism acts on the oscillator in such a way that the phase error is again reduced to a minimum ie phase of o/p signal is actually locked to the phase of the i/p signal. That is why it is referred to as phase locked loop

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