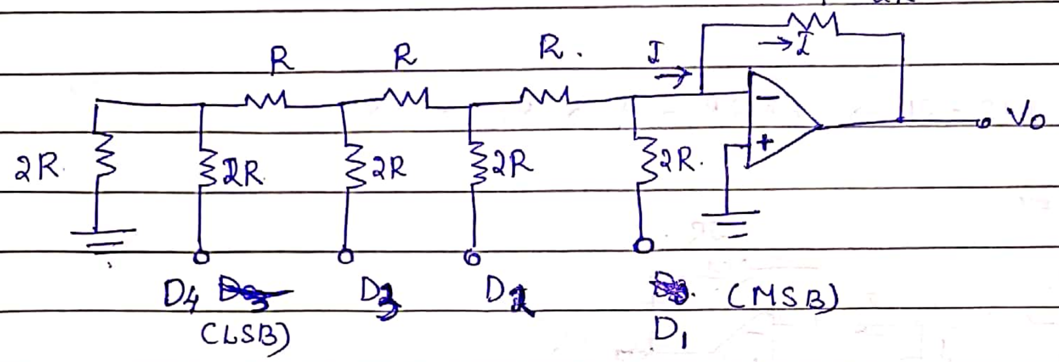
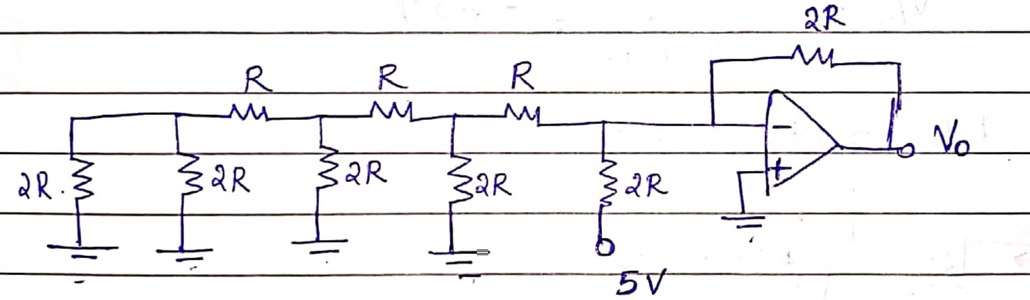
R-2R DAC

Wide range of resistors used in binary weighted type DAC. It can be avoided by using R-2R ladder type DAC where only two values of resistors are required. The typical value of R ranges from 2.5 kΩ to 10 kΩ

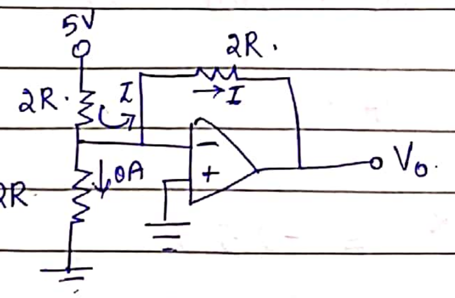


Consider a 4-bit DAC where the switch position $D_1 D_2 D_3 D_4$ corresponds to the binary word 1000. ie $D_1 = 1$ and other i/ps = 0.



ie $\frac{2R \times 2R}{2R+2R} = R \rightarrow R+R = 2R \rightarrow \frac{2R \times 2R}{2R+2R} = R \rightarrow R+R = 2R. \rightarrow \frac{2R \times 2R}{2R+2R} = R. \rightarrow R+R = 2R$

ie



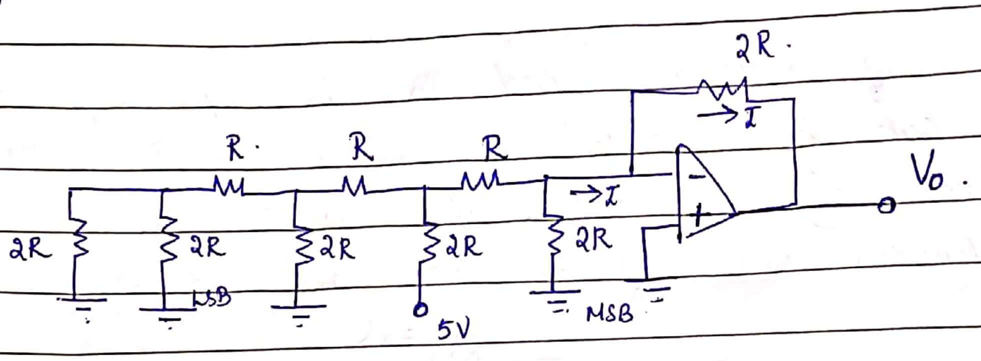
$R_{eq} = 2R$

ie $R_{eq} = \left(\left\{\left[(2R \| 2R) + R \| 2R\right] + R\right\} \| 2R\right) + R = 2R$

There is essentially no current through 2R equivalent resistance. Thus all the current $I = \frac{5V}{2R}$ goes through R_f

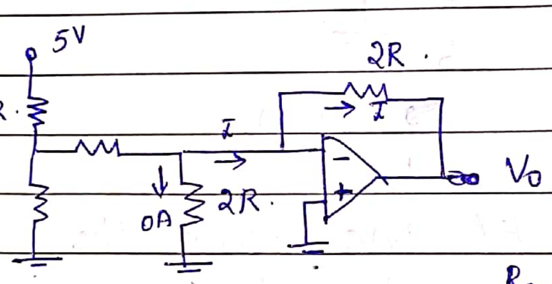
$$\therefore V_o = -I R_f = \frac{-5V \times 2R}{2R} = -5V$$

☆ Consider the input 0100. ie $D_2 = 1$ & all others $= 0$



$$\frac{2R \times 2R}{2R + 2R} = R \rightarrow R + R = 2R \rightarrow \frac{2R \times 2R}{2R + 2R} = R \rightarrow R + R = 2R.$$

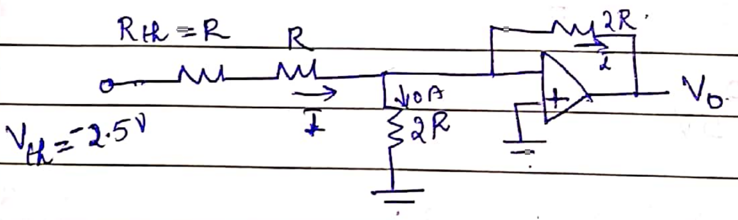
$R_{eq} = 2R.$



$$R_{eq} = \{[(2R // 2R) + R] // 2R\} + R = 2R.$$

$$V_{th} = \frac{-5 \times 2R}{2R + 2R} = -2.5\,V$$

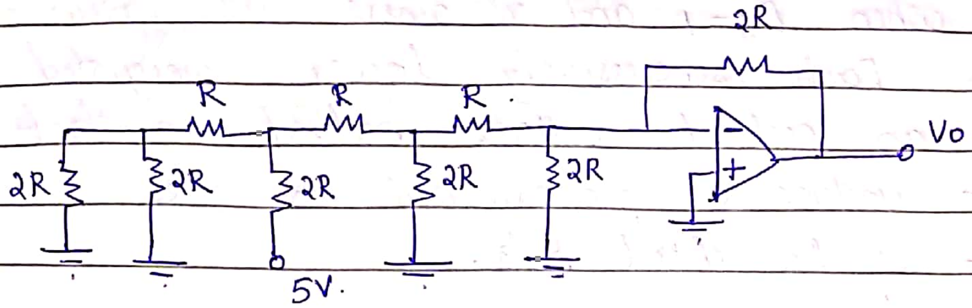
$$R_{th} = 2R // 2R = R.$$



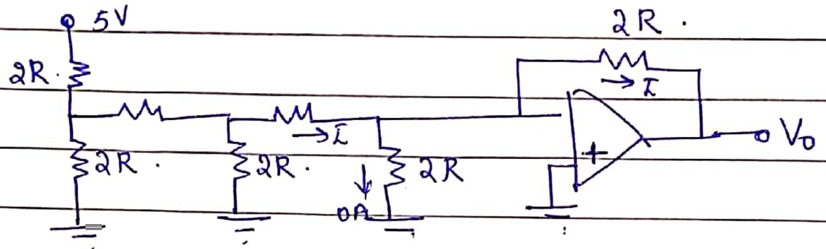
No current flows through 2R. Thus all current $I = \frac{2.5}{2R}$ goes through R_f.

$$\therefore V_o = -I R_f = \frac{-2.5}{2R} \times 2R = -2.5\,V$$

★ Consider the input 0010. ie $D_3 = 1$ and all other grnded.

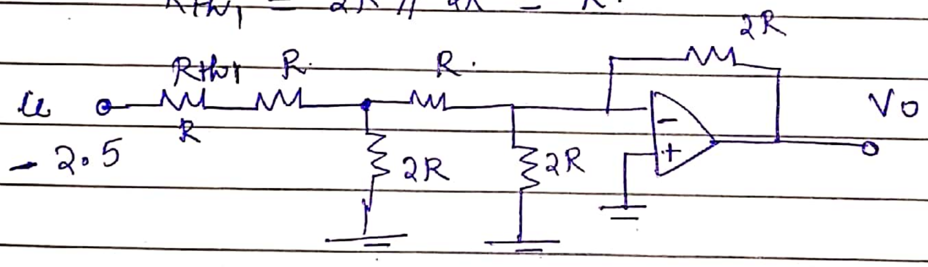


$$\frac{2R \times 2R}{2R + 2R} = R \rightarrow R + R = 2R.$$



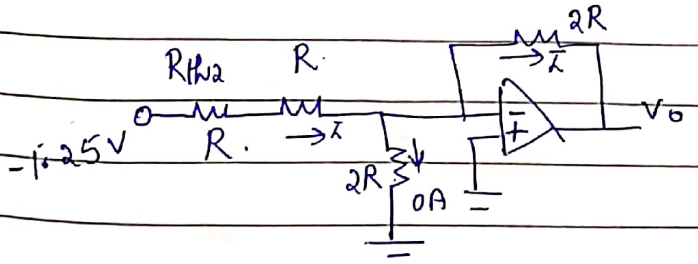
$$V_{th_1} = \frac{-5 \times 2R}{2R + 2R} = -2.5V.$$

$$R_{th_1} = 2R \,//\, 2R = R.$$



Again $$V_{th_2} = \frac{-2.5 \times 2R}{2R + 2R} = -1.25$$

$$R_{th_2} = 2R \,//\, 2R = R.$$



No current flows through 2R.

Thus all current $I = \frac{-1.25}{2R}$ goes through R_f.

$$\therefore V_o = \frac{-1.25 \times 2R}{2R} = -1.25V$$

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Similarly when $D_4 = 1$ and all others are grounded. $V_0 = -0.625V$. Each successively lower weighted i/p produces an output voltage halved, so that the output voltage is proportional to the binary weight of the input bits.