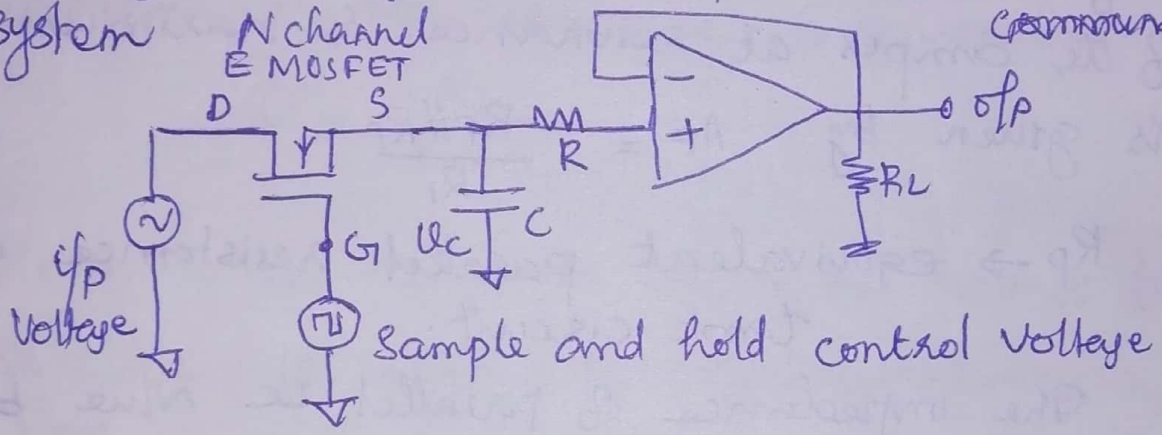
# Sample and hold Circuit

A sample and hold circuit samples an i/p signal and holds on to its last sampled value until the i/p is sampled again. This type of ckt is very useful in digital interfacing and analog to digital and pulse code modulation system




In the above circuit E-MOSFET works as a switch that is controlled by the sample and hold control voltage $V_s$ and capacitor C serves as storage element.

The analog signal $V_{in}$ to be sampled is applied to the drain and sample and hold control voltage $V_s$ applied to the gate of E MOSFET. During the true portion of $V_s$, the EMOSFET conducts and acts as a closed switch. This allows the i/p voltage to charge capacitor C and appears at the o/p.

When $V_s$ is zero, the EMOSFET is off and acts as an open switch. There is no discharge path for C

and the voltage across C is retained.

The time period $T_S$ of $V_S$ during which o/p voltage equals i/p voltage is are called sample periods. The time period $T_H$ of $V_S$ during which the voltage across the capacitor const (or const voltage at the o/p) are called hold periods.

Sample and hold IC LF 398.

To obtain close approximation of o/p waveform freq. of $V_S$ must be significantly higher than that of i/p.