Oriole

Graphic

LCD

Module

OGM-24064S

OGM-24011S

OGM - Series

USER'S

MANUAL

Oriole ELECTRONICS

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1. GENERAL SPECIFICATION

1.1 General

Oriole Graphic LCD Module consists of LCD panel with CMOS LSIs for LCD driving.
Since these modules have a full dot matrix graphic display, it is possible to display graphics as well as characters.

LCD Module 24064S has 240 x 64 dots.
LCD Module 24011S has 240 x 128 dots.

1.2 Features

1. CMOS LSIs specifically designed to drive LCDs.
2. Large Capacity Graphics type capable of displaying numerics, alphabets, special characters, graphs, charts and patterns.
3. Super twisted nematic LCD.
4. High contrast, wide viewing range.

2. Mechanical Data

OGM-24064S

1. Number of Dots..... 240 x 64 dots
2. View Area ..... 132.0W x 39.0 Ht mm
3. Dot Size ..... 0.49 x 0.49 mm
4. Dot Pitch ..... 0.53 x 0.53 mm
5. Outline Dimension ..... See brochure.

OGM-24011S

1. Number of Dots..... 240 x 128 dots
2. View Area ..... 114.0W x 64.0 Ht mm
3. Dot Size ..... 0.4 x 0.4 mm
4. Dot Pitch ..... 0.45 x 0.45 mm
5. Outline Dimension ..... See brochure.

3. Absolute Maximum Ratings

3.1 Electrical Absolute Maximum Ratings

V_{SS} = 0 V, T_a = 25°C

ITEM	SYMBOL	MIN	MAX	UNIT
Logic Circuit Power Supply Voltage	V_{DD}	0	7.0	V
Supply Voltage	V_{EE}	-15	-20	V
Input Voltage	V_I	V_{SS}	V_{DD}	V
Operating Temperature	T_{OP}	−20	+ 70	°C
Storage Temperature	T_{ST}	−30	+ 80	°C
Supply for LCD	V_{DD}-V_O	0	Note (1)	V

Note (1) : V_{DD}-V_O (Max) = 16V for 24064S LCD Modules.
V_{DD}-V_O (Max) =25 V for 24011S LCD Modules.

3.2 Environmental Absolute Maximum Ratings

ITEM	OPERATING		STORAGE		COMMENT
	MIN	MAX	MIN	MAX	
Ambient Temp.	-20 °C	+70 °C	−30 C	+80 °C	-
Humidity	Note (2)		Note (2)		Without Condenstation
Vibration	-	4.9m/S²	-	19.6m/S²	XYZ Directions
Shock	-	29.4m/S²	-	470.0m/S²	XYZ Directions

Note (2) T_a < 40 °C : 90% RH Max.
T_a > 40 °C : Absolute Humidity must be lower than the humidity of 90% at 40 °C

4. Operational Characteristics

4.1 Electrical Characteristics

V_{SS} = 0 V, T_a = 25°C

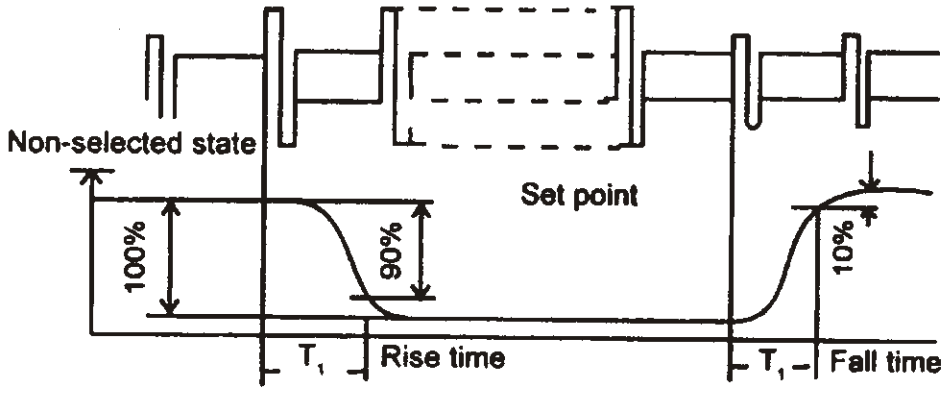
ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Logic Circuit Power Supply	V_{DD}	-	4.75	5.0	5.25	V
Supply Voltage	V_{EE}	-	Note (1)			V
Input Voltage	V_{IH}	V_{DD} = 5	3	-	V_{DD}	V
	V_{IL}	± 0.25	0	-	0.8	
Power Supply Current	I_{DD}	V_{DD} = 5V	-	Note(2)	-	mA
	I_{EE}	V_{EE} = -15 V	-	1	-	

Note (1) V_{EE} = -10V ± 0.25V for 24064S
V_{EE} = -15V ± 0.25V for 24011S

Note (2) I_{DD} (typ) 30 mA for 24064S LCD Modules.
I_{DD} (typ) 15 mA for 24011S LCD Modules.

4.2 Optical Characteristics

Definition of Optical Response Time



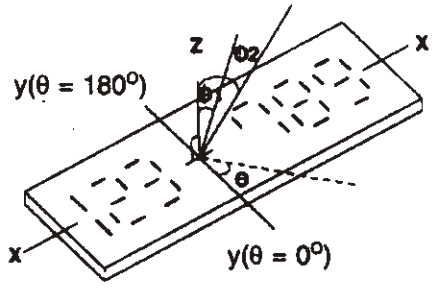
T_a = 25°C

ITEM	SYMBOL	CONDITION	MIN	TYPE	MAX	UNIT	NOTE
Viewing angle	$\phi 2 - \phi 1$	K = 1.4	20	-	-	deg.	1,2
Constrast ratio	K	ϕ = 25° θ = 0°	-	3	-	-	3

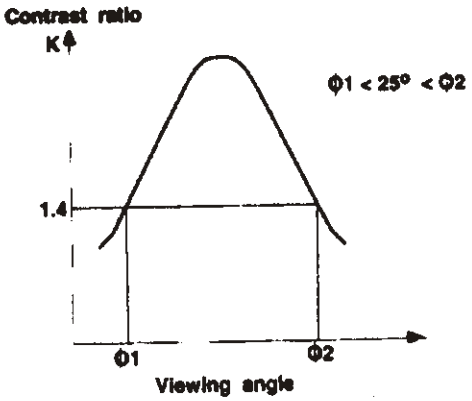
Note (1) Defination of ϕ and θ

θ is in the XY plane

ϕ is in the YZ plane

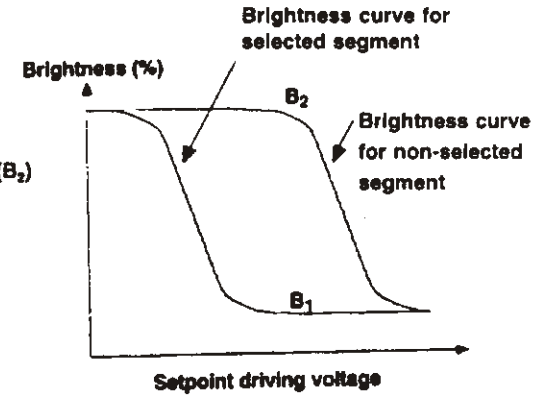


Note (2) : Definition of viewing angle q1 and θ2



Note (3) : Definition of contrast 'K'

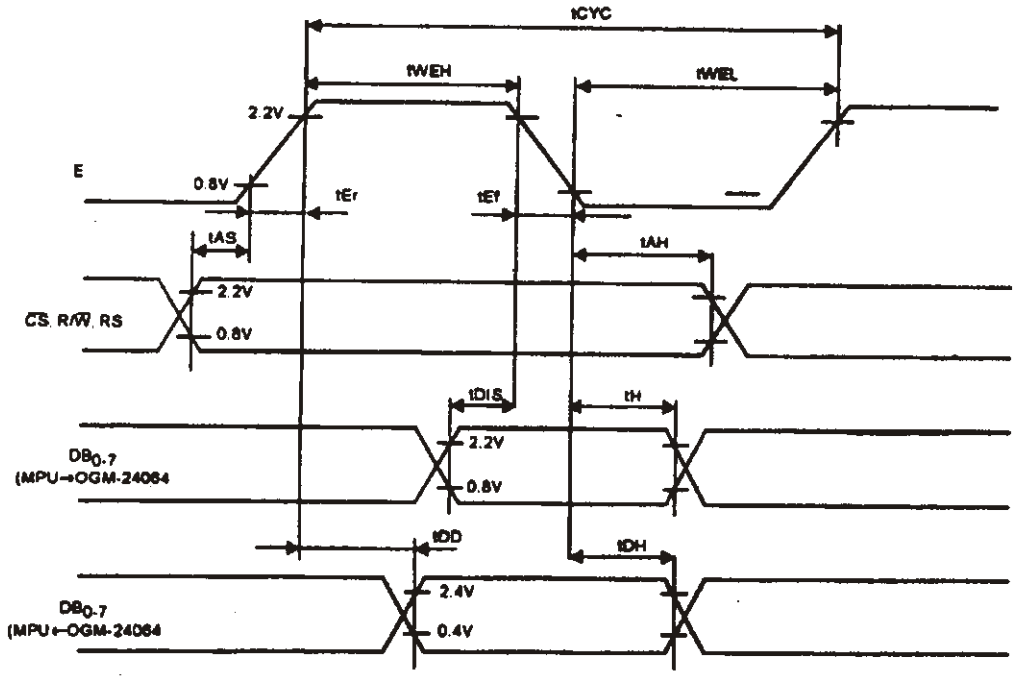
$$K = \frac{\text{Brightness of non-selected segment } (B_2)}{\text{Brightness of selected segment } (B_1)}$$



5. Timing Characteristics

5.1 MPU Interface

ITEM		SYMBOL	MIN	TYP	MAX	UNIT
Enable cycle time		T_{CYC}	1.0	-	-	µs
Enable pulse width	High level	T_{WEH}	0.45	-	-	µs
	Low level	T_{WEL}	0.45	-	-	µs
Enable rise time		T_{ER}	-	-	25	ns
Enable fall time		T_{ER}	-	-	25	ns
Setup time		T_{AS}	140	-	-	ns
Data set-up time		T_{ASW}	225	-	-	ns
Data delay time		T_{DDR}	-	-	225	ns
Data hold time		T_H	10	-	-	ns
Address hold time		T_{AH}	10	-	-	ns
Data hold time		T_{DH}	20	-	-	ns



6. Pin Connections

NO.	SYMBOL	FUNCTION
1	V_{SS}	GROUND
2	V_{DD}	POWER SUPPLY FOR LOGIC CIRCUIT
3	V_O	BRIGHTNESS CONTROL
4	RS	INSTRUCTION / DATA
5.	R / $\overline{W}$	READ / WRITE
6.	E	ENABLE
7-14	DB0-DB7	DATA BUS LINE
15	$\overline{CS}$	CHIP SELECT (ACTIVE LOW)
16	$\overline{RES}$	RESET (ACTIVE LOW)
17	V_{EE}	NEGATIVE VOLTAGE (-15V)
18-20	N.C.	NO CONNECTION

7. Communication between CPU and Module

7.1 Display Control Instructions

Display is controlled by writing data into the instruction register and 13 data registers. The RS signal distinguishes the instruction register from the data registers. Address of the data register is written into the instruction register with RS=1. After that, the 8-bit data is written in the data register and the specified instruction is executed with RS=0. During the execution of the instruction, no new instruction can be accepted. Since the busy flag is set during this, read the busy flag and make sure it is 0 before writing the next instruction.

7.1.1 Mode Control

Code $"00" (hexadecimal) written into the instruction register specifies the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	0
Mode control reg.	0	0	0	0	Mode Data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor / blink	CG	Graphic/character
1/0	1/0	0	0	0	0	Cursor OFF	Internal CG	Character mode
		0	1			Cursor ON		
		1	0			Cursor OFF character blink		
		1	1			Cursor blink		
		0	0		1	Cursor OFF	External CG	
		0	1			Cursor ON		
		1	0			Cursor OFF character blink		
		1	1			Cursor blink		
		0	0	1	0			Graphic mode

→ 1 : Master mode
2 : Slave mode

→ 1 : Display ON
2 : Display OFF

7.1.2 Set Character Pitch

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	1
Character pitch reg.	0	0	(Vp-1) binary				0	(Hp-1) binary		

Vp indicates the number of vertical dots per character. The space between the vertically displayed characters is considered for determination. This value is meaningful only during character display (in the character mode) and becomes invalid in the graphic mode.

The Hp indicates the number of horizontal dots per character in the display including the space between horizontally displayed characters. In the graphic mode, the Hp indicates the number of bits of 1-byte display data to be displayed.

There are three Hp values

Hp	DB2	DB1	DB0	
6	1	0	1	Horizontal character pitch 6
7	1	1	0	Horizontal character pitch 7
8	1	1	1	Horizontal character pitch 8

7.1.3 Set Number of Characters

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	0
Number of Character reg.	0	0	0	(Hn-1) binary						

Hn indicates the number of horizontal characters in the character mode or the number of horizontal bytes in the graphic mode. Since the total sum of horizontal dots on the screen is (240).

Hn should be set to a value $= \frac{240}{Hp}$

If Hp is set to 8 then Hn becomes 30 decimal i.e. 1E (hex).

7.1.4. Set Number of Time Divisions (Inverse of display duty ratio)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	1
Number of time share reg.	0	0	0	(Nx-1) binary						

Nx indicates the number of time division in multiplex display. 1/Nx is a display duty ratio.
For 24064S Nx = 64 (decimal).
For 24011S Nx = 128 (decimal).

7.1.5 Set Cursor position

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	1	0	0
Cursor position reg.	0	0	0	0	0	0	(Cp - 1) binary			

Cp indicates the position in a character where the cursor is displayed in the character mode. For example, in 5x7 dot font, the cursor is displayed under a character by specifying Cp=8. The cursor horizontal length is equal to the horizontal character Pitch Hp. A value of 1 to 16 (decimal) can be sent to Cp. If a smaller value than the number of vertical character pitches Vp is set (Cp <Vp), and a character is overlapped with the cursor, the cursor has higher priority of display (at cursor display ON). If Cp is greater than Vp, no cursor is displayed.

7.1.6 Set Display Start Low Order Address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	0
Display start address reg. (low order byte)	0	0	(Start low order address) binary							

7.1.7 Set Display Start High Order Address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	1
Display start address reg. (High order byte)	0	0	(Start high order address) binary							

These instructions cause display start address to be written in the display start address registers. The display start address indicates a RAM address at which the data displayed at the top left end on the screen is stored. In the graphic mode, the start address is composed of high/ low order 16 bits. In the character display, it is composed of the lower 4 bits of higher order address (DB3-DB0) and 8 bits of low order address. The upper 4 bits of high order address are ignored.

7.1.8 Set cursor Address (Low Order) (Ram write low order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	0
Cursor address Counter (low order byte)	0	0	(Cursor low order address) binary							

7.1.9. Set cursor Address (High Order) (Ram write high order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	1
Cursor address Counter (High order byte)	0	0	(Cursor high order address) binary							

These instructions cause cursor address to be written in the cursor address counters. The cursor address indicates an address for sending or receiving display data and character codes to or from the RAM. Namely, data at address specified by the cursor address are read/written. In the character mode, the cursor is displayed at the digit specified by the cursor address.

A cursor address consists of the low-order address (8 bits) and the high-order address (8 bits)

Satisfy the following requirements when setting the cursor address.

1.	When you want to rewrite (set) both the low order address and high order address	Set the low order address and then set the high order address
2.	When you want to rewrite only the low order address	Don't fail to set the high order address after setting the low order address
3.	When you want t rewrite only the high order address	Set the high order address. You don't have to set the low order address again.

The cursor address counter is a 16 bit up-counter with SET and RESET functions. When the bit N changes from 1 to 0, the bit N+1 is incremented. When setting the low order address, the LSB (bit 0) of the high order address is added by 1 if the MSB (bit 7) of the low order address changes from 1 to 0. Therefore, set both the low order address and the high order as shown in above table.

7.1.10 Write Display Data.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (Pattern data, character code) LBS							

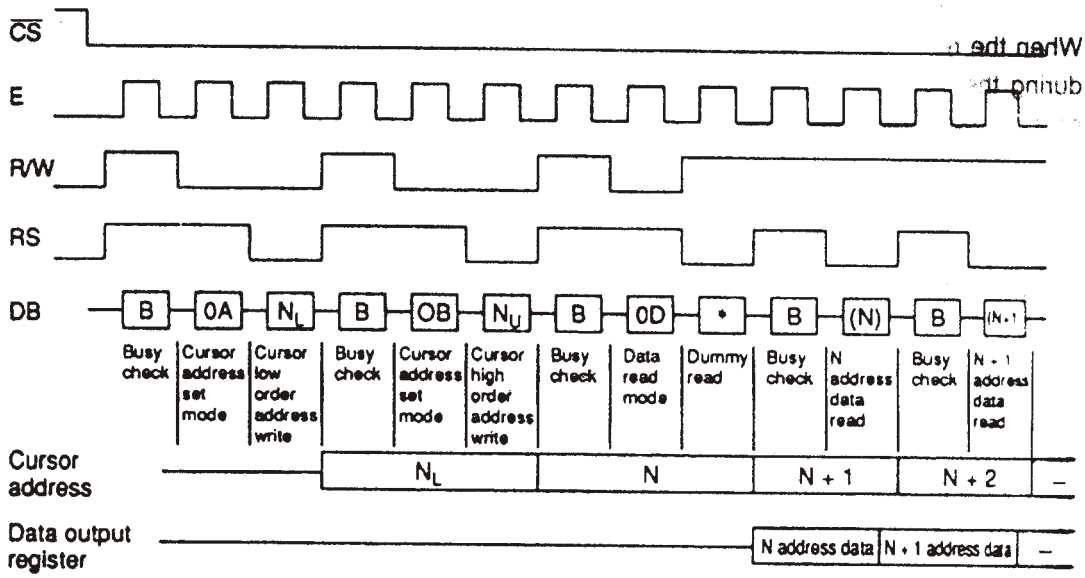
After the code $ `0C' is written into the instruction register with RS=1, 8 bit data with RS=0 should be written into the data register. This data is transferred to the RAM specified by the cursor address as display data or character code. The cursor address is increased by 1 after this operation.

7.1.11 Read Display Data

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	1
RAM	0	0	MSB (Pattern data, character code) LBS							

Data can be read from the RAM with RS=0 after writing code $ `0D' into the instruction register. The read procedure is as follows:

This instruction outputs the contents of data output register on Data Bus (DB0 to DB7) and then transfers RAM data specified by a cursor address to the data output register, also increasing the cursor address by 1. After setting the cursor address, correct data is not output at the first read but at the second time. Thus, make one dummy read when reading data after setting the cursor address.



7.1.12 Clear bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	0
Clear bit reg.	0	0	0	0	0	0	0	N_B		

7.1.13 Set Bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	1
Bit set reg.	0	0	0	0	0	0	0	N_B		

The clear/set bit instruction sets 1 bit in a byte of display data RAM 0 or 1 respectively. The position of the bit in a byte is specified by N_B and RAM address is specified by cursor address. After the execution of the instruction, the cursor address is automatically increased by 1. N_B is a value of 0 to 7. N_B = 0 and N_B = 7 indicates LSB and MSB, respectively.

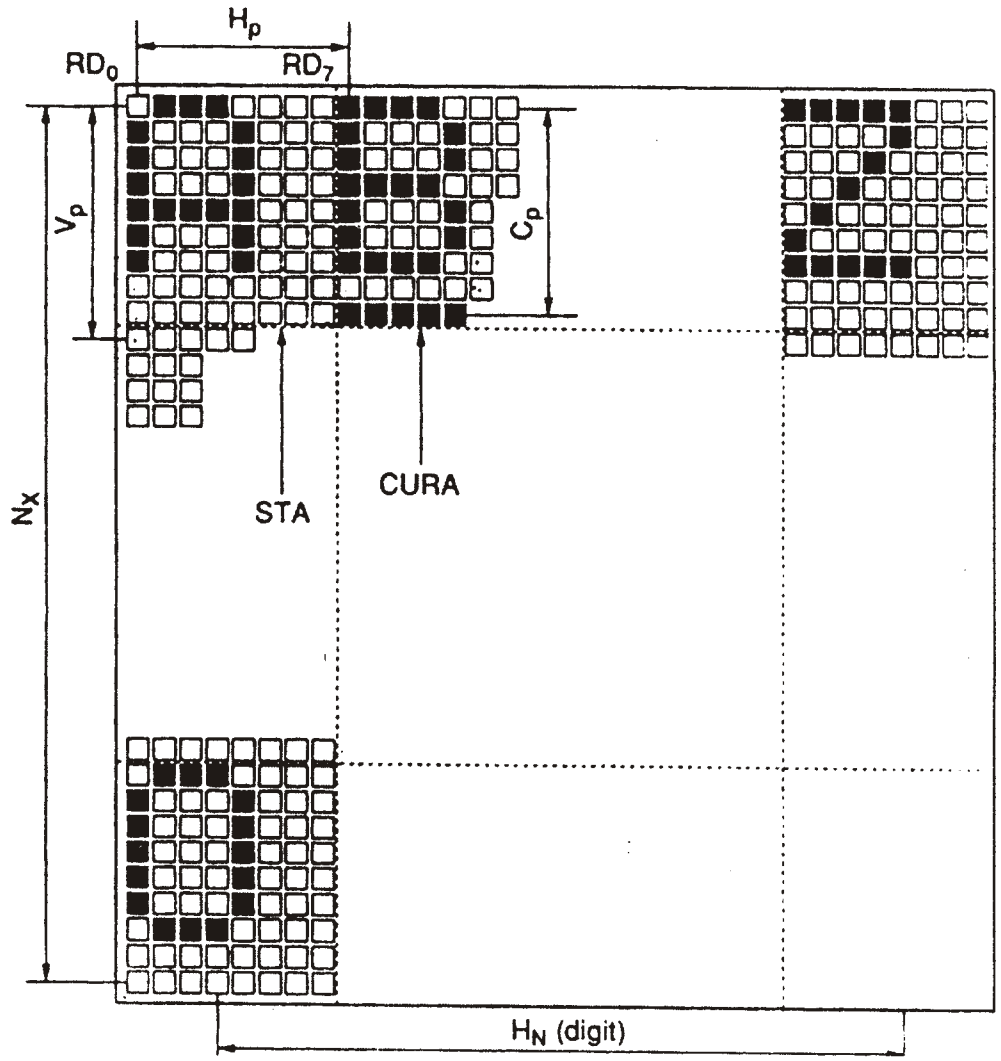
7.1.14. Read Busy Flag.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy flag	1	1	1/0	*						

When the read mode is set with RS=1, the busy flag is output to DB7. The busy flag is set to 1 during the execution of any of instructions (1) to (13). After the execution, it is set to 0. The next instruction can be accepted. No instruction can be accepted when busy flag = 1. Before execution an instruction or writing data, perform a busy flag check to make sure the busy flag is 0. When data is written in the register (RS=1), no busy flag changes. Thus, no busy flag check is required just after the write operation into the instruction register with RS=1.

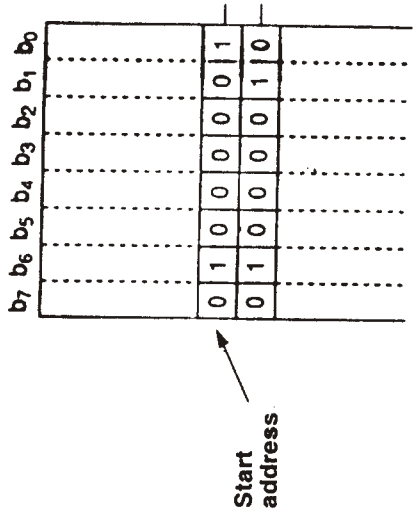
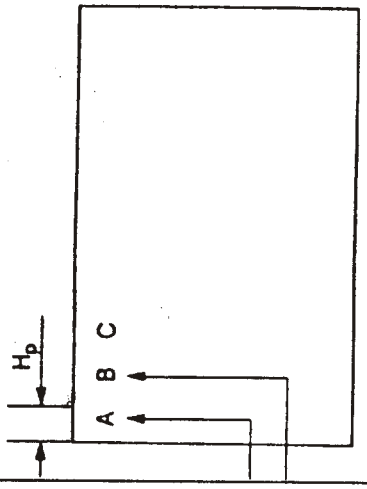
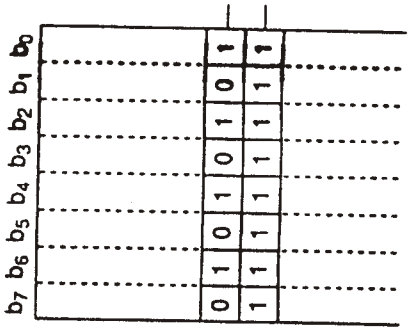
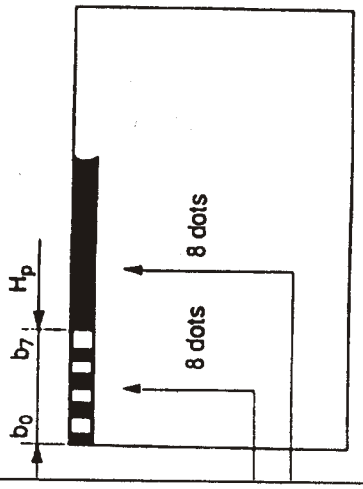
The busy flag can be read without specifying any instruction register.

7.2. LCD Panel Display



Symbol	Name	Meaning	Value
H_P	Horizontal character pitch	Lateral character pitch	6 to 8 dots
H_N	Number of horizontal characters	Number of lateral characters per line (number of digits) in the character mode or number of bytes per line in the graphic mode.	2 to 40 digits (an even number)
V_P	Vertical character pitch	Longitudinal character pitch	1 to 16 dots
C_P	Cursor position	Line number on which the cursor can be displayed	1 to 16 lines
N_X	Number of the time division	Inverse of display duty ratio	1 to 128 lines

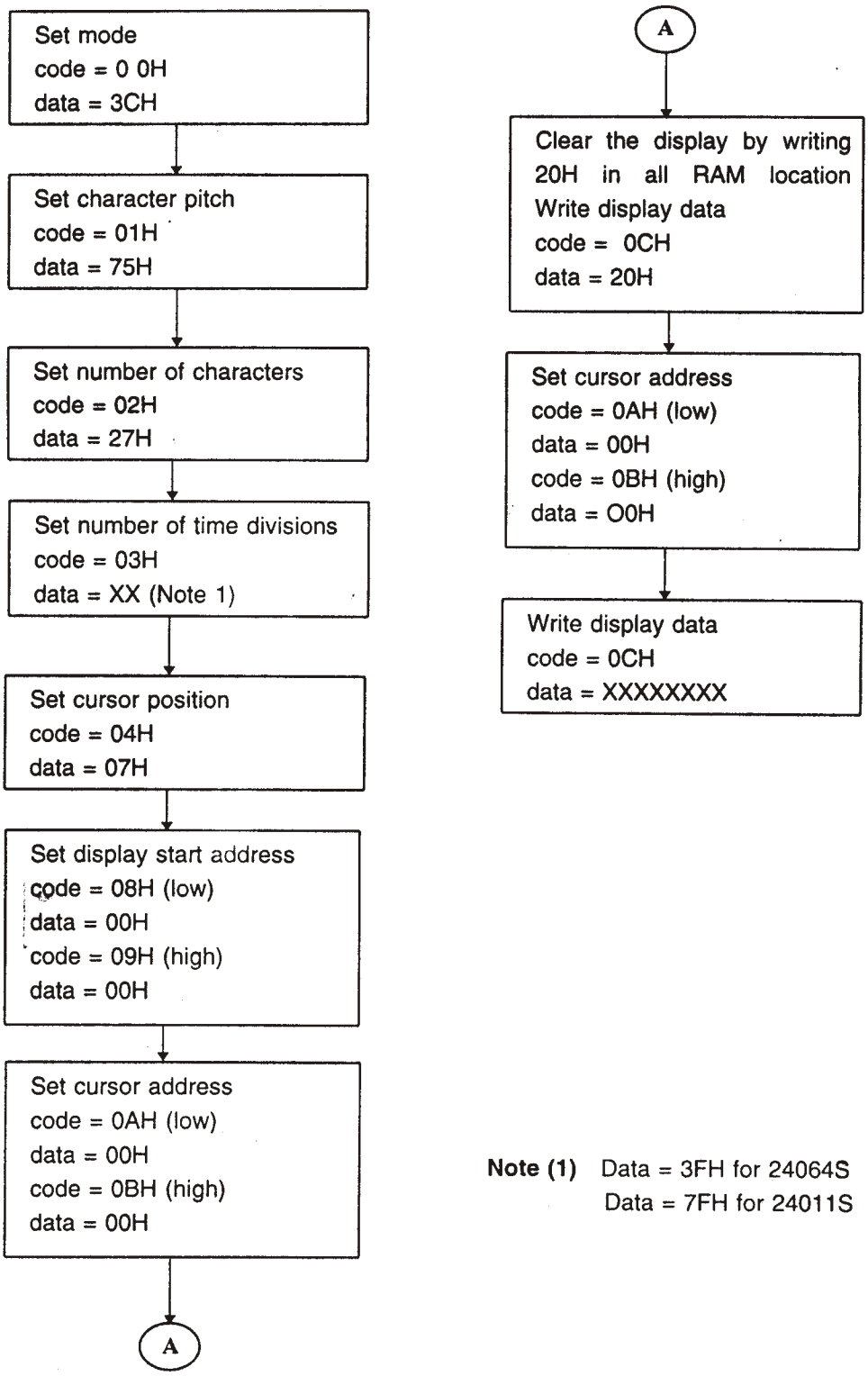
7.3. Display Mode

DISPLAY MODE	DISPLAY DATA FROM MPU	RAM	LIQUID CRYSTAL DISPLAY PANEL
Character Display	Character code (8 bits)		
Graphic	Display pattern (8 bits)		

7.4. Internal Character Generator Patterns and Character Codes

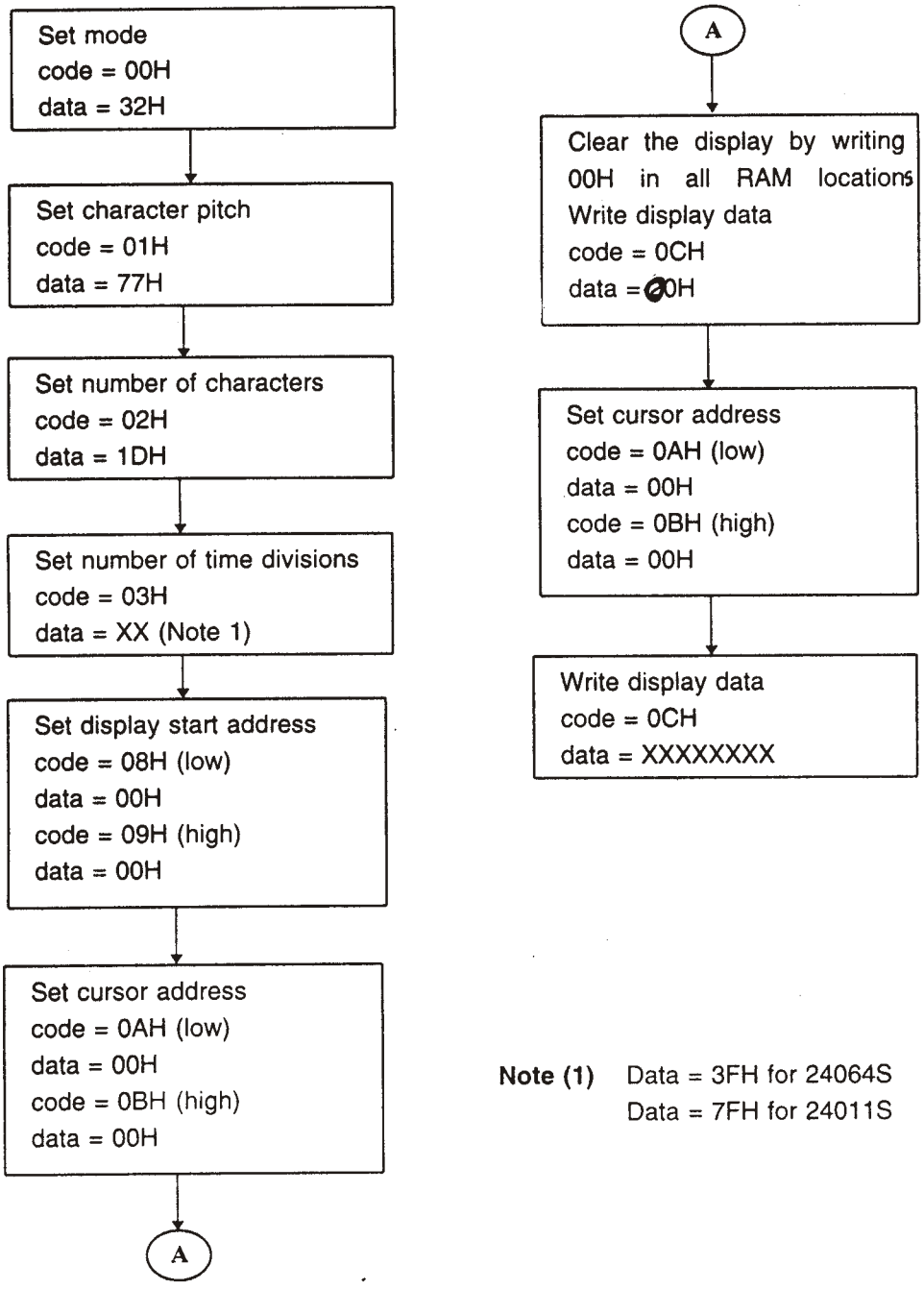
7.5 Control Sequence

7.5.1 Character mode



Note (1) Data = 3FH for 24064S
Data = 7FH for 24011S

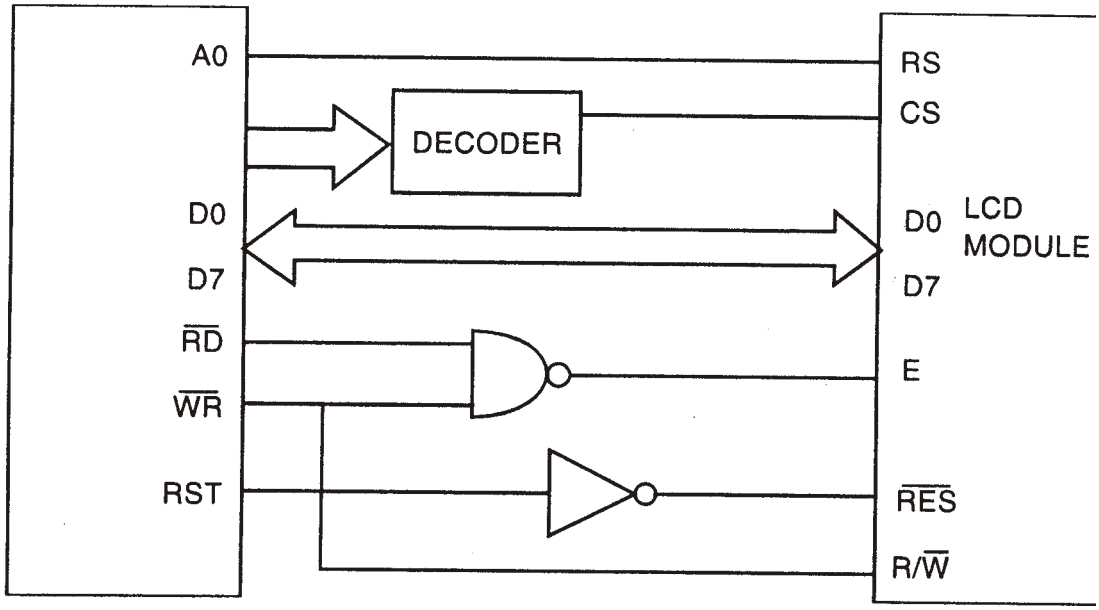
7.5.2 Graphic Mode



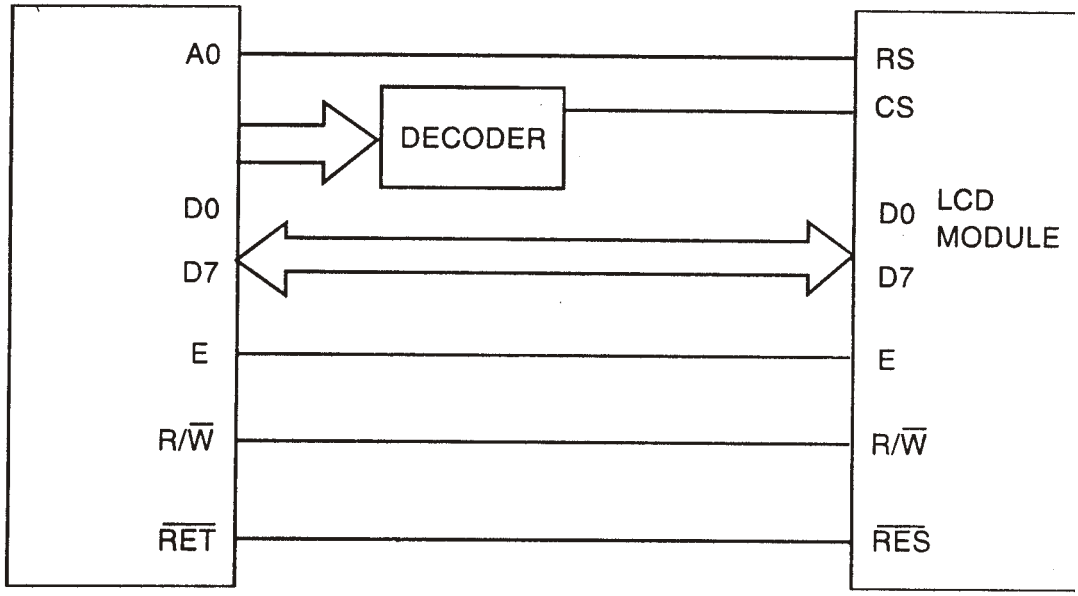
Note (1) Data = 3FH for 24064S
Data = 7FH for 24011S

8. Application Circuit

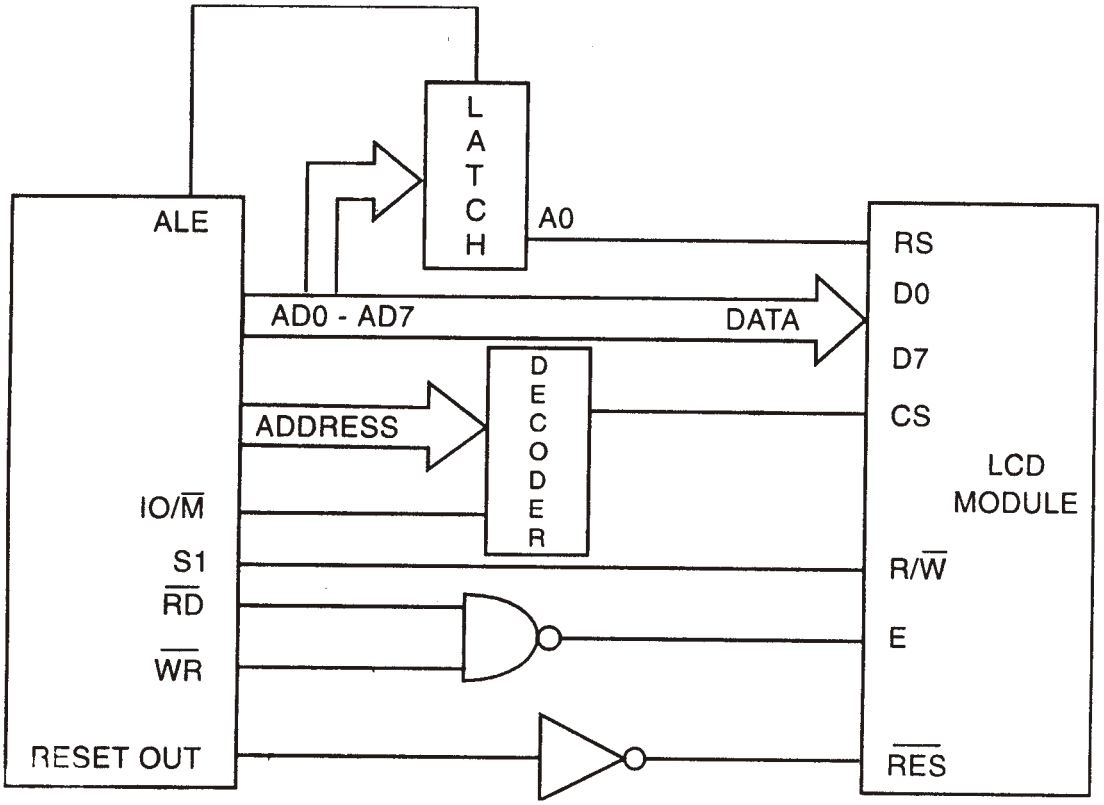
(A) 8051 Family



(B) 68 Family



(C) 8085


LATCH
ALE
A0
RS
AD0 - AD7
DATA
D0
D7
DECODER
ADDRESS
CS
LCD
MODULE
IO/M
S1
R/W
RD
E
WR
RESET OUT
RES

9. Handling Precautions

1. Do not take the LCD Module out of it's antistatic bag until just before assembly.

2. The LCD module is made of glass. Do not subject the LCD module to strong mechanical shocks or vibrations.

3. If LCD breaks and liquid crystal material leaks out, do not inhale, ingest or be in contact with it. If the LC gets on your hands, feet or clothes, wash it off immediately.

4. Applying pressure to the module surface will cause it to change its color tone. Avoid pressing on the surface of the LCD.

5. Do not work on the printed circuit board of the module except for soldering the connector.

6. Clean the flux between connector terminals with the recommended solvent after soldering. Ensure that the solution during cleaning flows towards and out of the PCB edge nearest to the connector.

7. Peel off the LCD protective film only just before the final fitment of the module in your system. Do not twist, bend or distort the LCD module during installation.

8. Do not input any signal before power is on.

9. To protect the module against static electricity ground the working area to discharge static electricity. Always use a no-leak earthed soldering iron for soldering the module connections. Ground the wrist strap when handling the module.