Simulate on Proteus:

1. (Make one schematic for the entire problem)
   a) Take a number from 0 to 255 (8 bit) using logic-states and count the number of 1 bits using a **counter**.

   b) Count the number of 1 bits at odd positions using a **counter.**(Indexing starts from 0 at LSB)

   Example- $(11111110)_2$ == $(254)_{10}$
   Number of 1 bits=7
   Number of 1 bits at odd position=4 (1,3,5,7)

2. Take a 7 bit number from 5-127 and add 5 to it in one clock cycle and divide by 2 in the next clock cycle alternately until it becomes 5.
   Count the number of clock cycles it took to become 5 using a counter and display the output as logic probes.

3. A 2732 ROM has an array of 5 numbers, 0 <= each number <= 15. Find the **sum** of all the numbers and display the output as logic probes.
   Run the python file to get the Ass_2.bin file or directly use the Ass_2.bin file given.
   Download Link
   Given array:- [10,2,9,3,15]

PCB Design Problem (ONLY FOR DIGISIM):

4. Implement the PCB design for a **full adder** (*1 bit for 1st yearites and 2 bit for 2nd yearites*)
   The PCB components selected should be of surface mount type.
   U are free to use any company or ic number of the components , however sparkfun is recommended
   PCB should have 2 layers top and bottom
   Using Autorouter is allowed
   U are also required to write ur name on the PCB

   Take the screenshots of the schematic , board and Gerber file and upload them as well as the files on a folder in your drive or github repo. Submit the drive link/github repo in the form with view access to everyone.