

FTDI_RX是FPGA下载器的UART发送端，连接FPGA的RX；
FTDI_TX是FPGA下载器的UART接收端，连接FPGA的TX
UART_RX是CMSIS-DAP的UART接收端，连接FPGA的TX；
UART_TX是CMSIS-DAP的UART发送端，连接FPGA的RX；

| Title | | |
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| Size | Number | Revision |
| A3 | | |
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| File: | D:\work\IPAGE03_ARTIX7 Bank14 & Bank15 | Doc |

UID

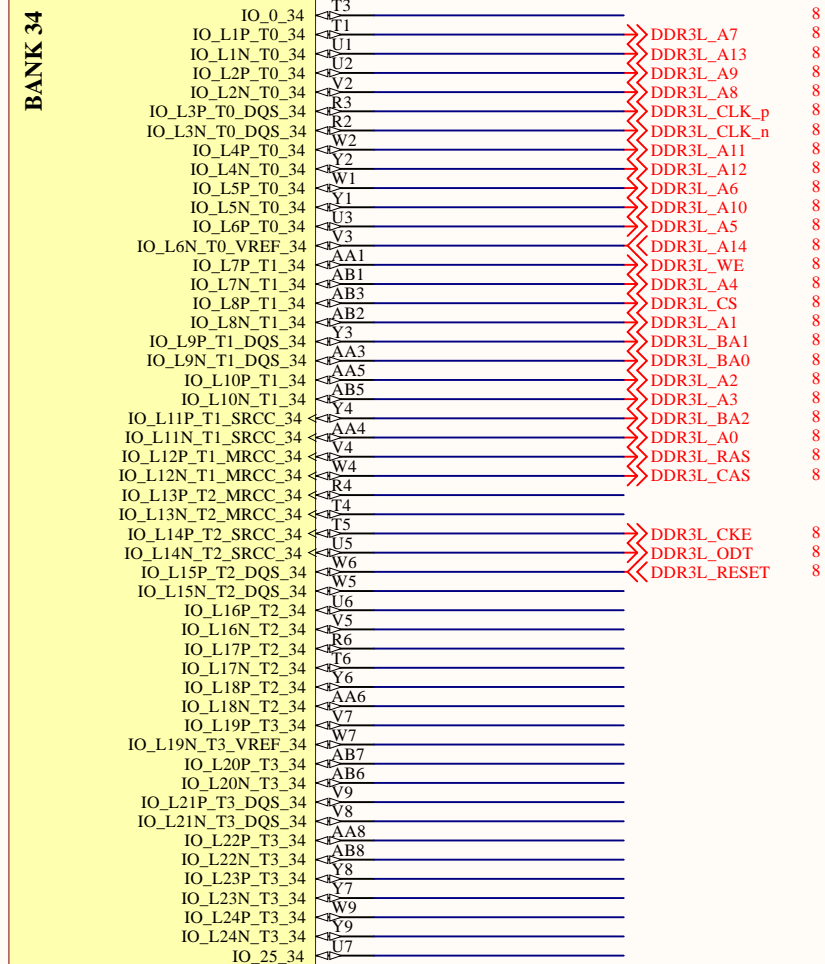
BANK 16

| | | | |
|--------------------|-----|---------------------|----|
| IO_0_16 | F15 | | |
| IO_L1P_T0_16 | F13 | | |
| IO_L1N_T0_16 | F14 | | |
| IO_L2P_T0_16 | F16 | >>> SDIO_CD | 15 |
| IO_L2N_T0_16 | E17 | >>> SDIO_D3 | 15 |
| IO_L3P_T0_DQS_16 | C14 | >>> SDIO_D2 | 15 |
| IO_L3N_T0_DQS_16 | C15 | >>> SDIO_D1 | 15 |
| IO_L10P_T1_16 | A13 | >>> SDIO_D0 | 15 |
| IO_L10N_T1_16 | A14 | >>> SW5 | 13 |
| IO_L5P_T0_16 | E16 | >>> SW7 | 13 |
| IO_L5N_T0_16 | D16 | >>> SW11 | 13 |
| IO_L6P_T0_16 | D14 | >>> Audio_I2S_SCLK | 20 |
| IO_L6N_T0_VREF_16 | D15 | >>> SW6 | 13 |
| IO_L7P_T1_16 | B15 | >>> SW8 | 13 |
| IO_L7N_T1_16 | B16 | >>> SW9 | 13 |
| IO_L8P_T1_16 | C13 | >>> SW0 | 13 |
| IO_L8N_T1_16 | B13 | >>> SW3 | 13 |
| IO_L9P_T1_DQS_16 | A15 | >>> SW4 | 13 |
| IO_L9N_T1_DQS_16 | A16 | >>> SW10 | 13 |
| IO_L4P_T0_16 | E13 | >>> Audio_I2S_LRCK | 20 |
| IO_L4N_T0_16 | E14 | >>> SW2 | 13 |
| IO_L11P_T1_SRCC_16 | B17 | >>> SW1 | 13 |
| IO_L11N_T1_SRCC_16 | B18 | >>> SDIO_CMD | 15 |
| IO_L12P_T1_MRCC_16 | D17 | >>> SDIO_CLK | 15 |
| IO_L12N_T1_MRCC_16 | C17 | >>> Audio_IIC_SDA | 20 |
| IO_L13P_T2_MRCC_16 | C18 | >>> Audio_I2S_SDIN | 20 |
| IO_L13N_T2_MRCC_16 | C19 | >>> Audio_I2S_MCLK | 20 |
| IO_L14P_T2_SRCC_16 | E19 | >>> Audio_IIC_SCL | 20 |
| IO_L14N_T2_SRCC_16 | D19 | >>> Audio_I2S_SDOUT | 20 |
| IO_L15P_T2_DQS_16 | F18 | >>> AD/DA_CLK | 9 |
| IO_L15N_T2_DQS_16 | E18 | >>> ADC_D1 | 9 |
| IO_L16P_T2_16 | B20 | >>> ADC_D0 | 9 |
| IO_L16N_T2_16 | A20 | >>> DAC_D1 | 9 |
| IO_L17P_T2_16 | A18 | >>> ADC_D7 | 9 |
| IO_L17N_T2_16 | A19 | >>> DAC_D0 | 9 |
| IO_L18P_T2_16 | F19 | >>> ADC_D6 | 9 |
| IO_L18N_T2_16 | F20 | >>> ADC_D2 | 9 |
| IO_L19P_T3_16 | D20 | >>> ADC_D3 | 9 |
| IO_L19N_T3_VREF_16 | C20 | >>> ADC_D5 | 9 |
| IO_L20P_T3_16 | C22 | >>> ADC_D4 | 9 |
| IO_L20N_T3_16 | B22 | >>> DAC_D8 | 9 |
| IO_L21P_T3_DQS_16 | B21 | >>> DAC_D9 | 9 |
| IO_L21N_T3_DQS_16 | A21 | >>> DAC_D7 | 9 |
| IO_L22P_T3_16 | E22 | >>> DAC_D6 | 9 |
| IO_L22N_T3_16 | D22 | >>> DAC_SCLK | 9 |
| IO_L23P_T3_16 | E21 | >>> DAC_DIN | 9 |
| IO_L23N_T3_16 | D21 | >>> DAC_D4 | 9 |
| IO_L24P_T3_16 | G21 | >>> DAC_D5 | 9 |
| IO_L24N_T3_16 | G22 | >>> DAC_D2 | 9 |
| IO_25_16 | F21 | >>> DAC_CS | 9 |
| | | >>> DAC_D3 | 9 |

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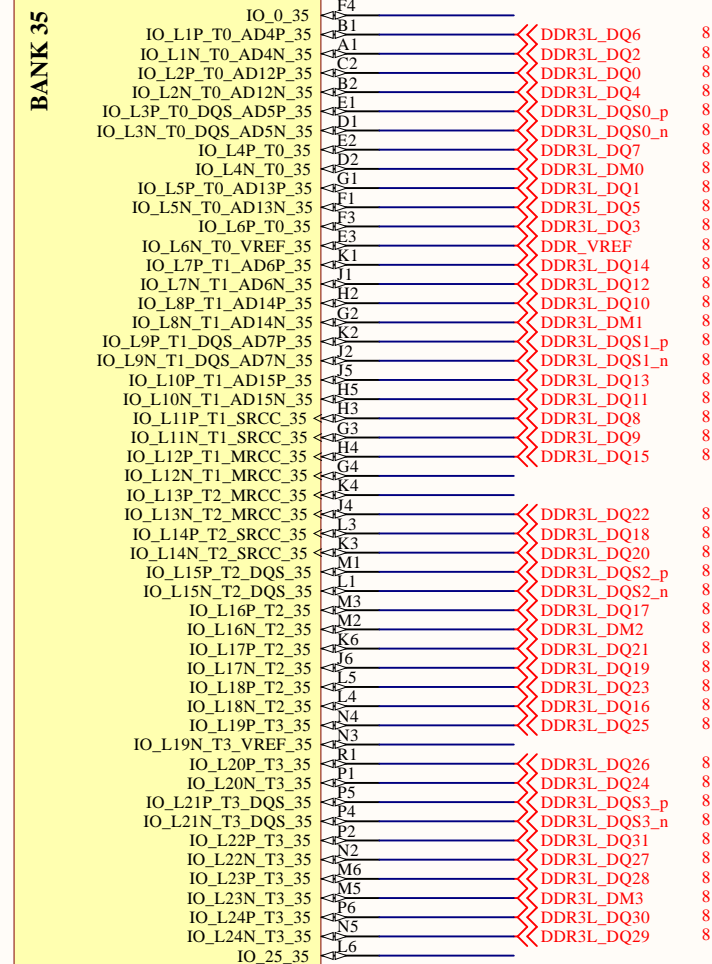
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| Size | Number | Revision |
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| Date: | 2020/4/28 | Sheet of |
| File: | D:\work\...\PAGE04 ARTIX7 Bank16 & Bank15 Bgm Doc | |

UIE



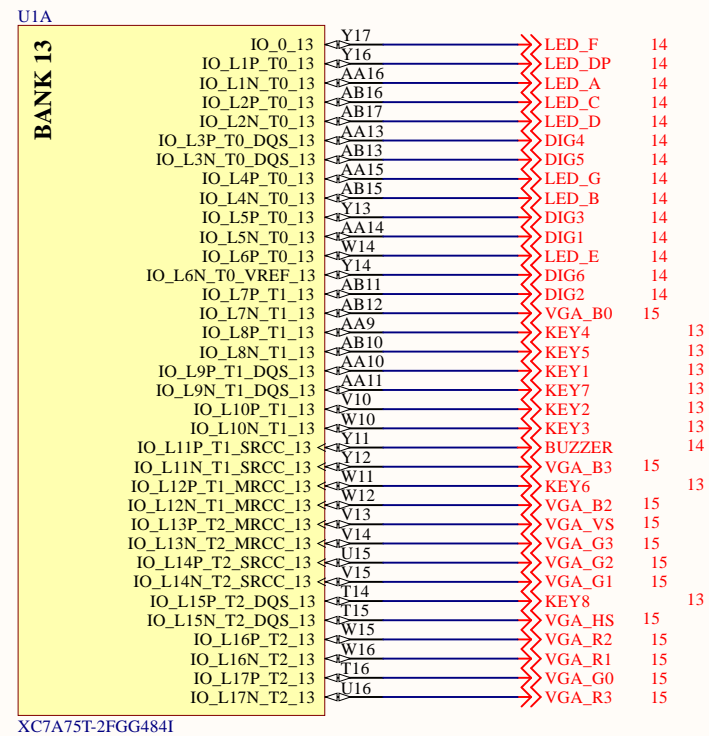
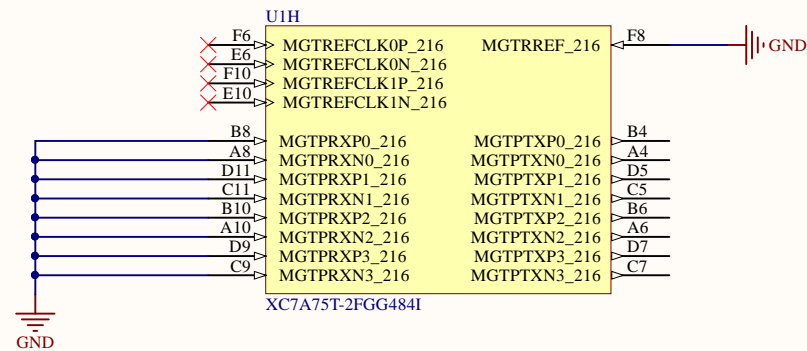
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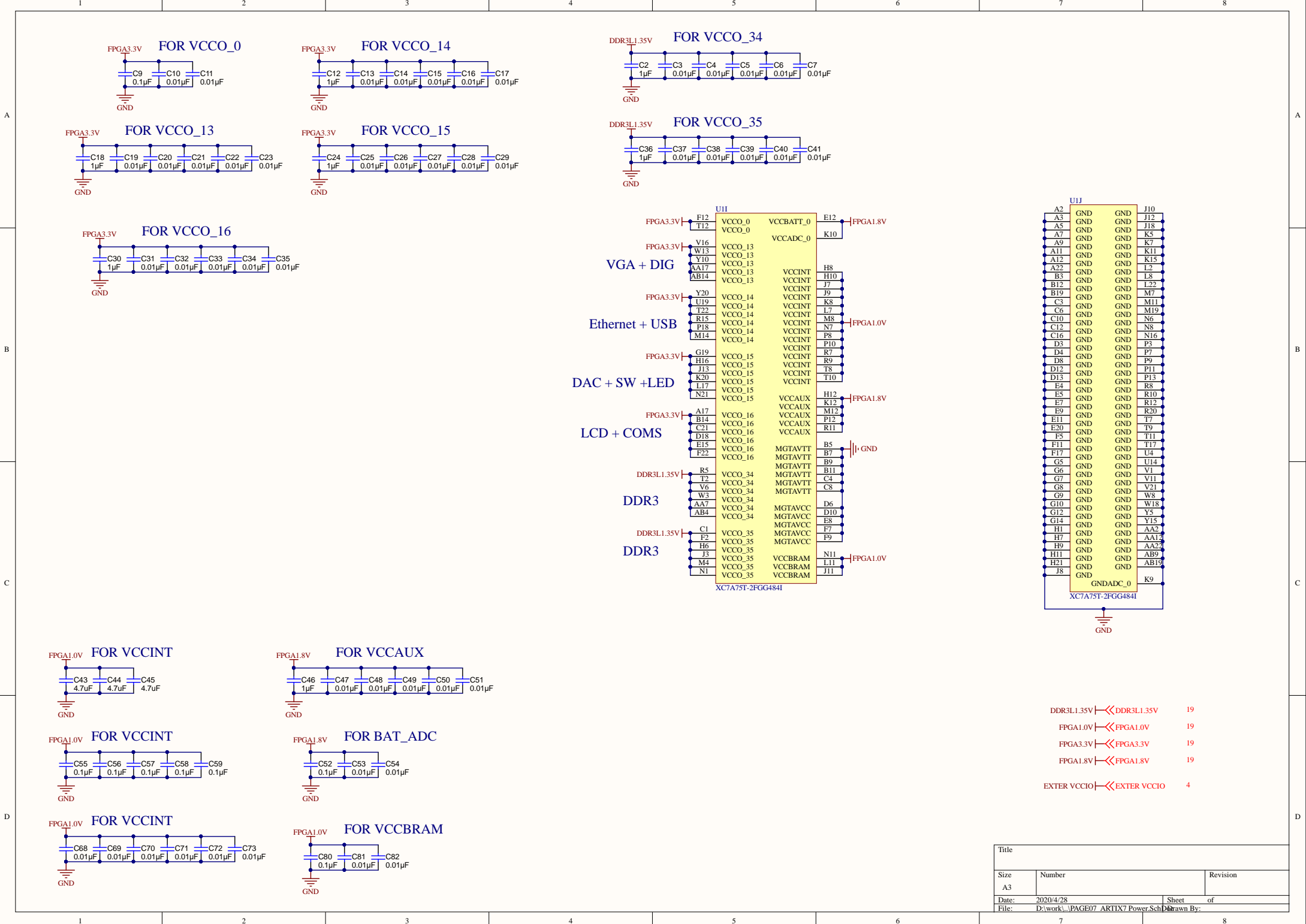


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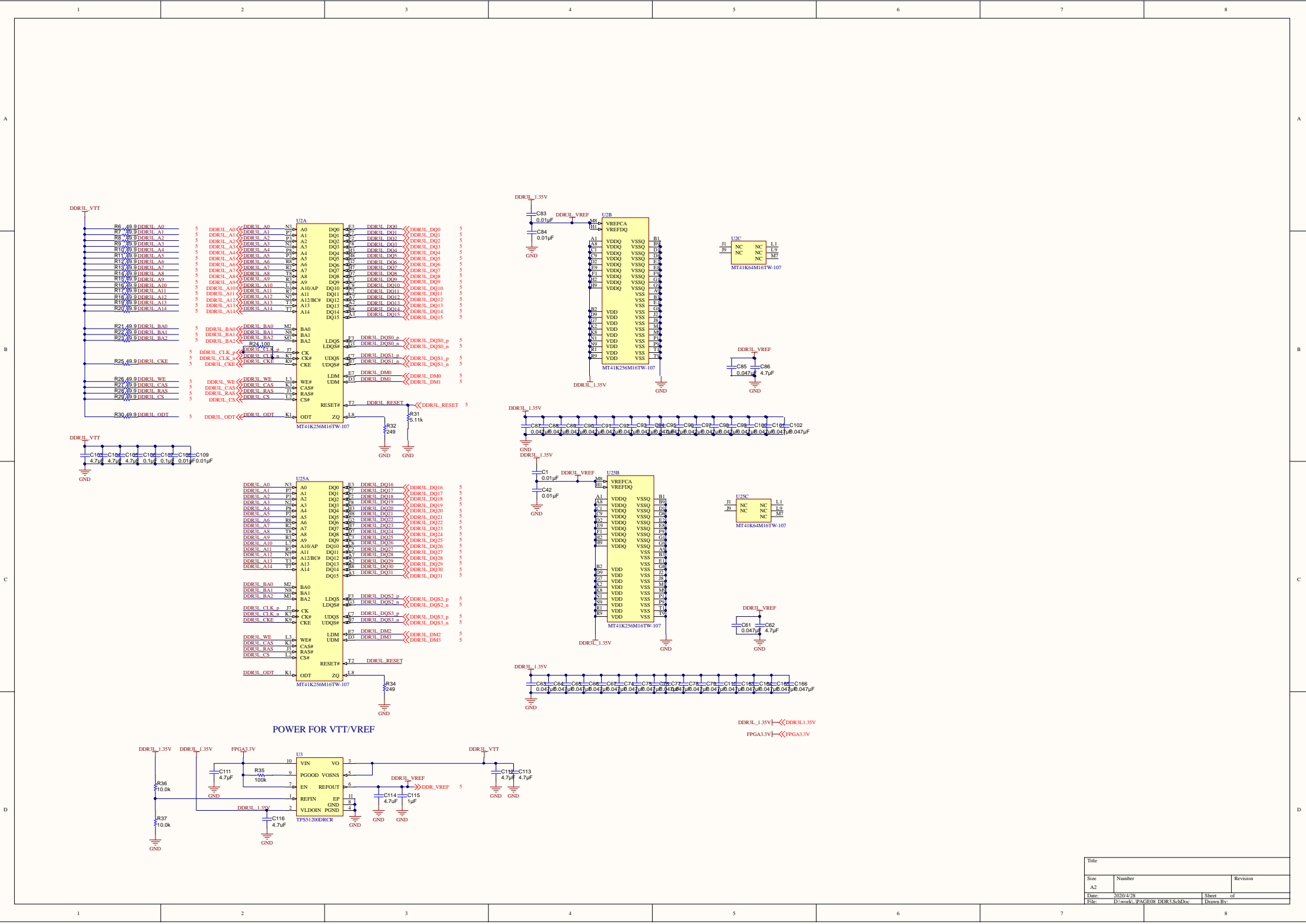
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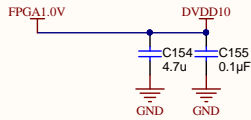


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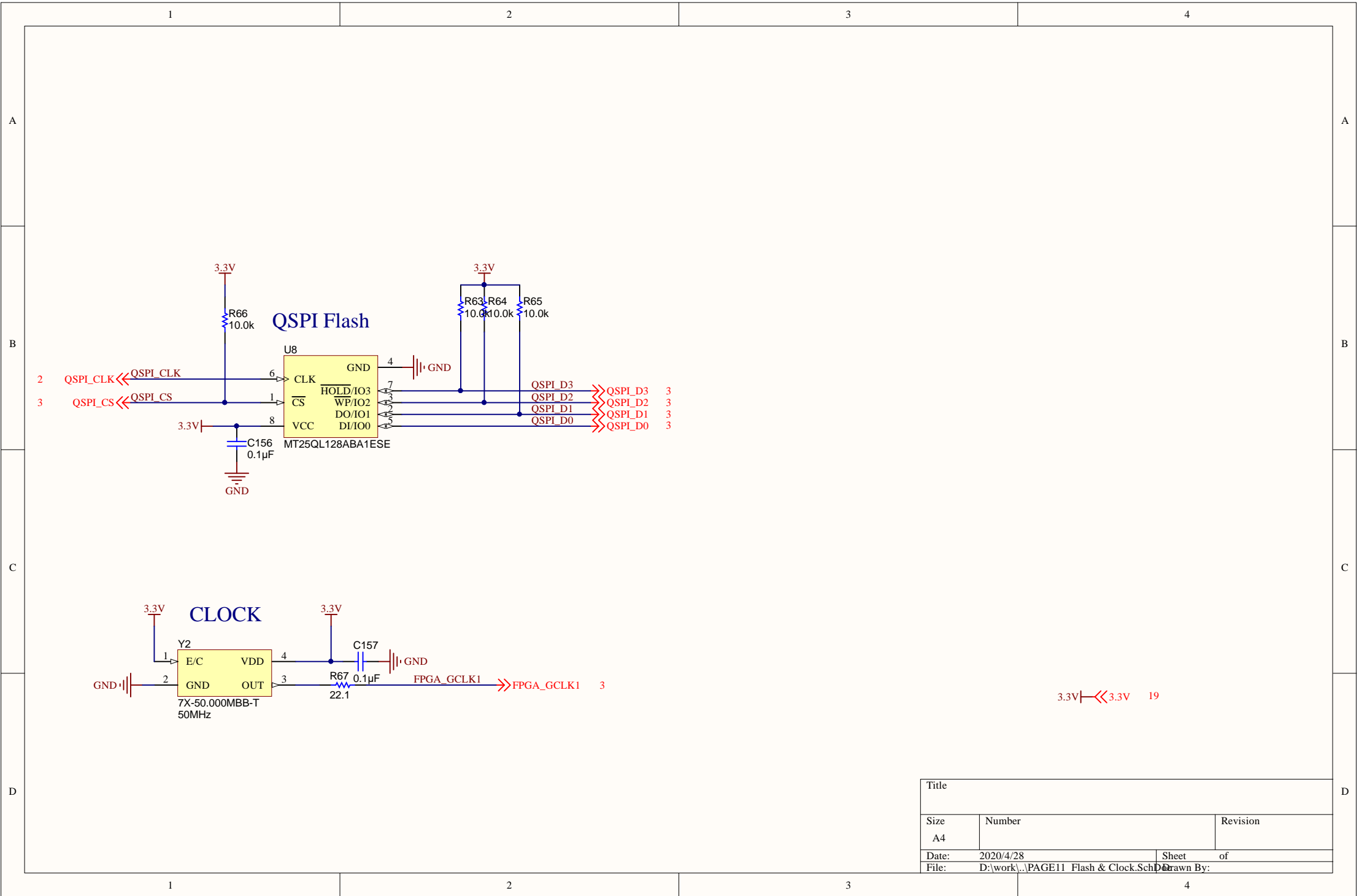


POWER FOR VTT/VREF

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| A2 | | |
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A

B

C

D

A

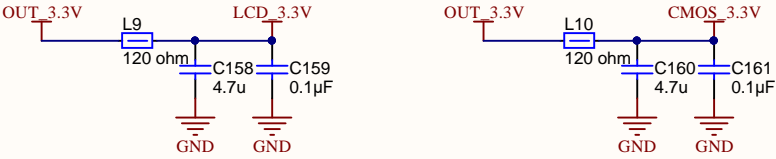
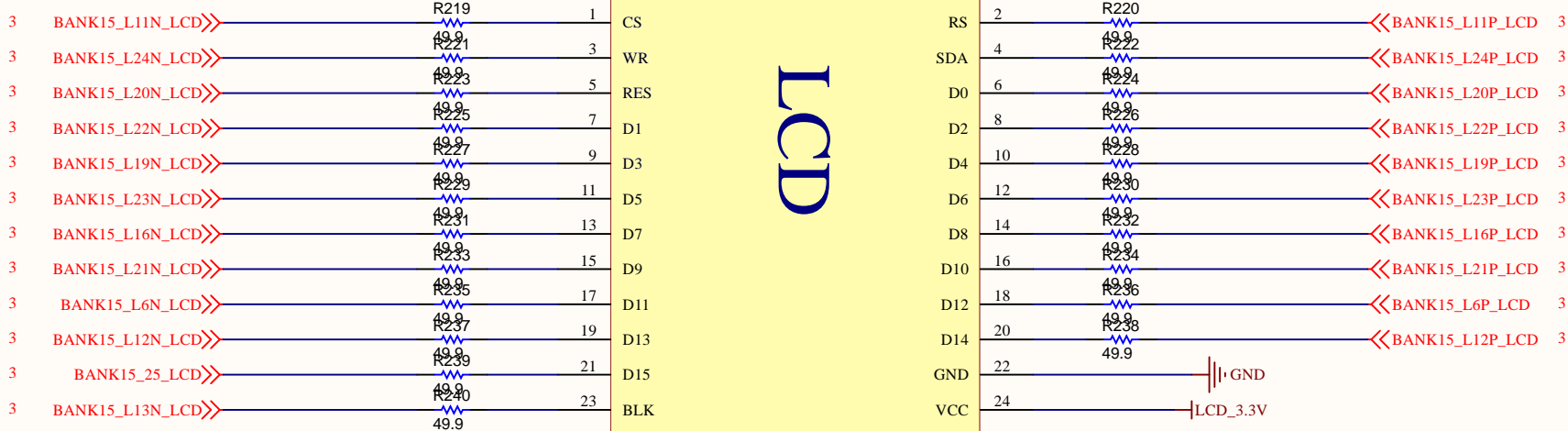
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C

D

修改

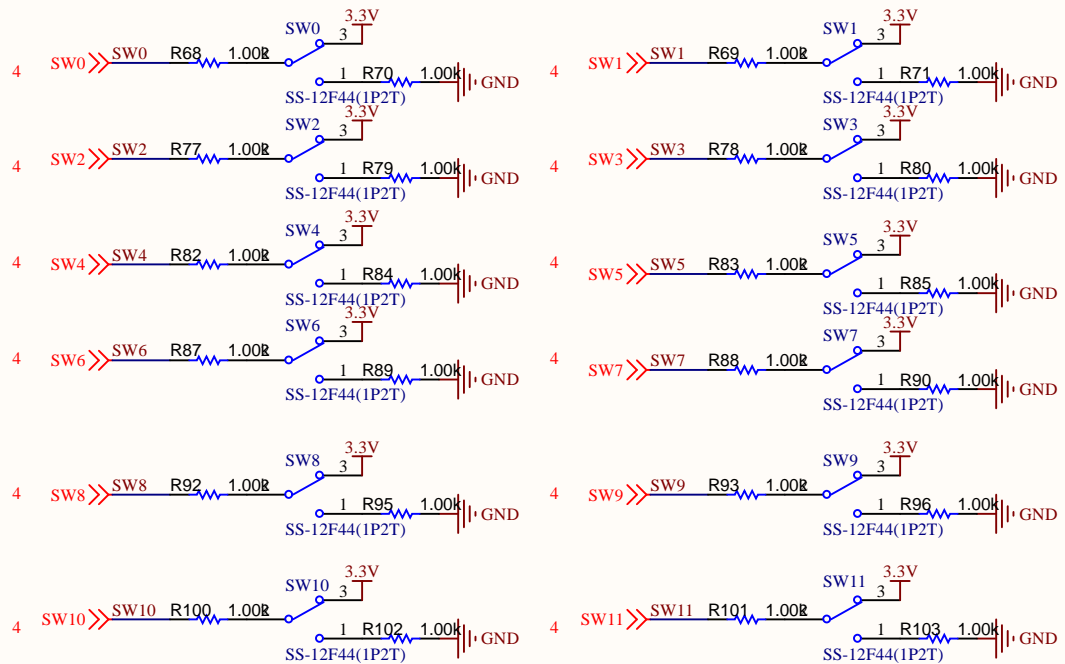
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修改



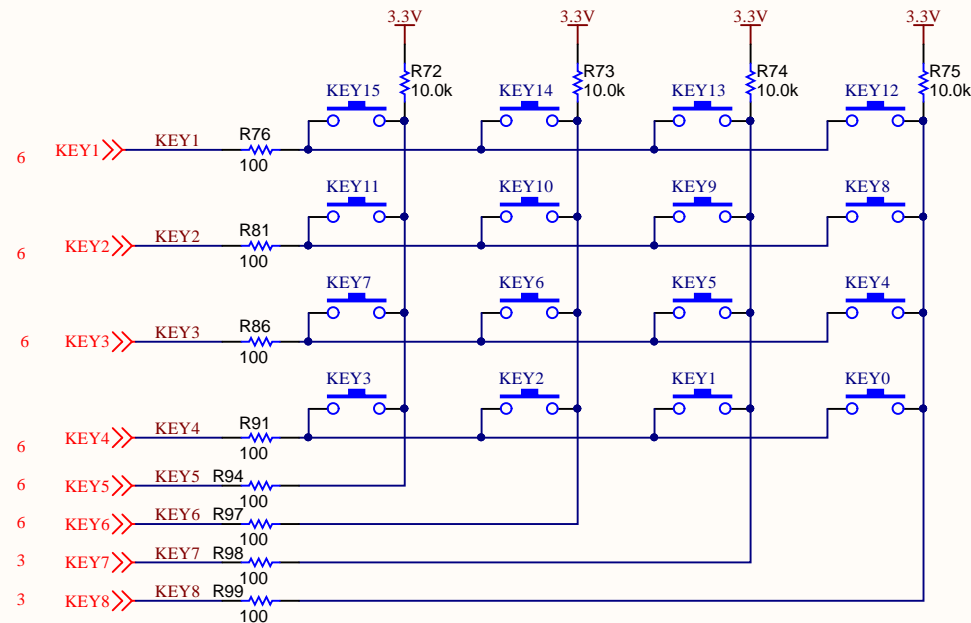
OUT_3.3V

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SWITCH



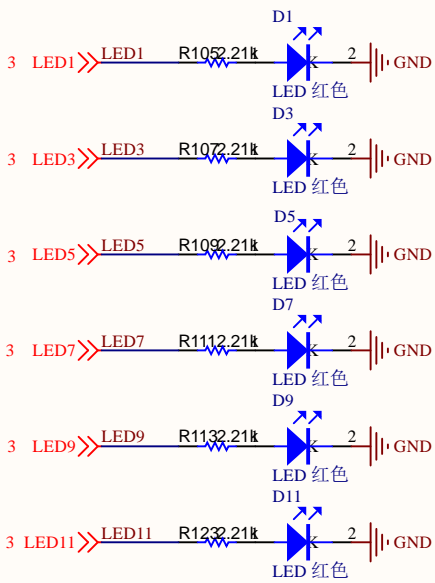
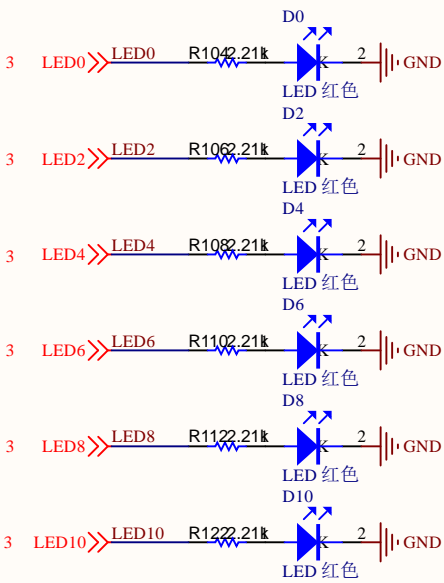
KEY



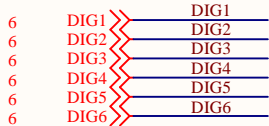
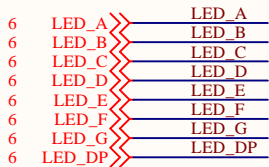
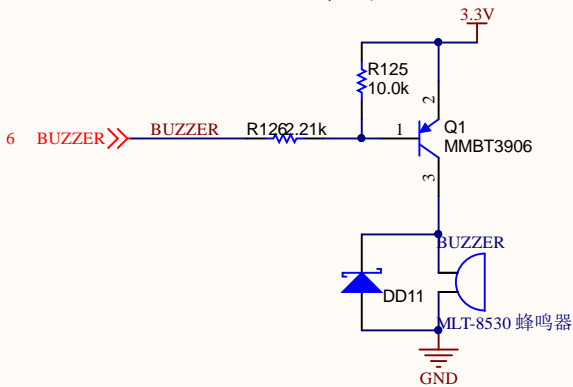
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LED



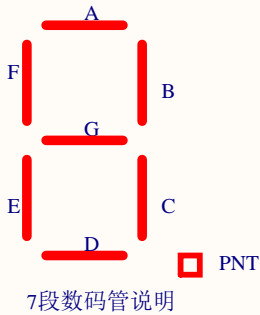
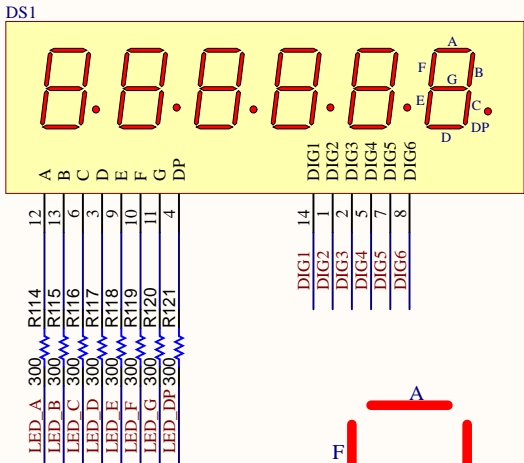
蜂鸣器



DIG

六位共阴数码管

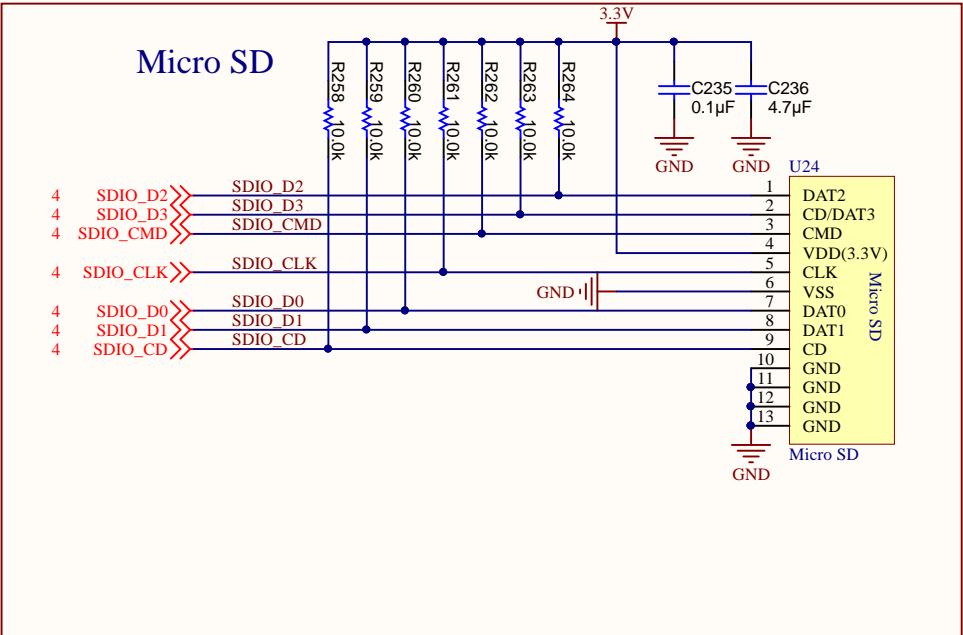
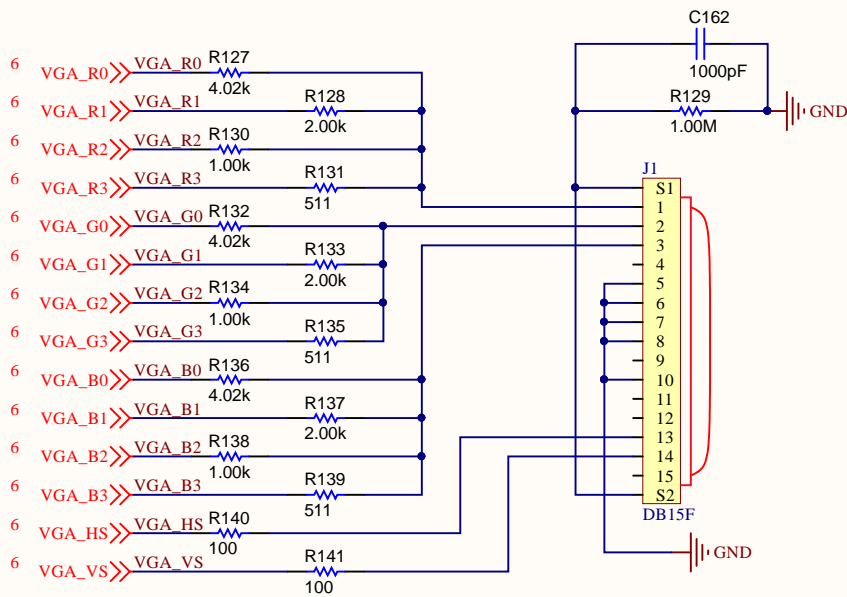
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3.3V 3.3V 19

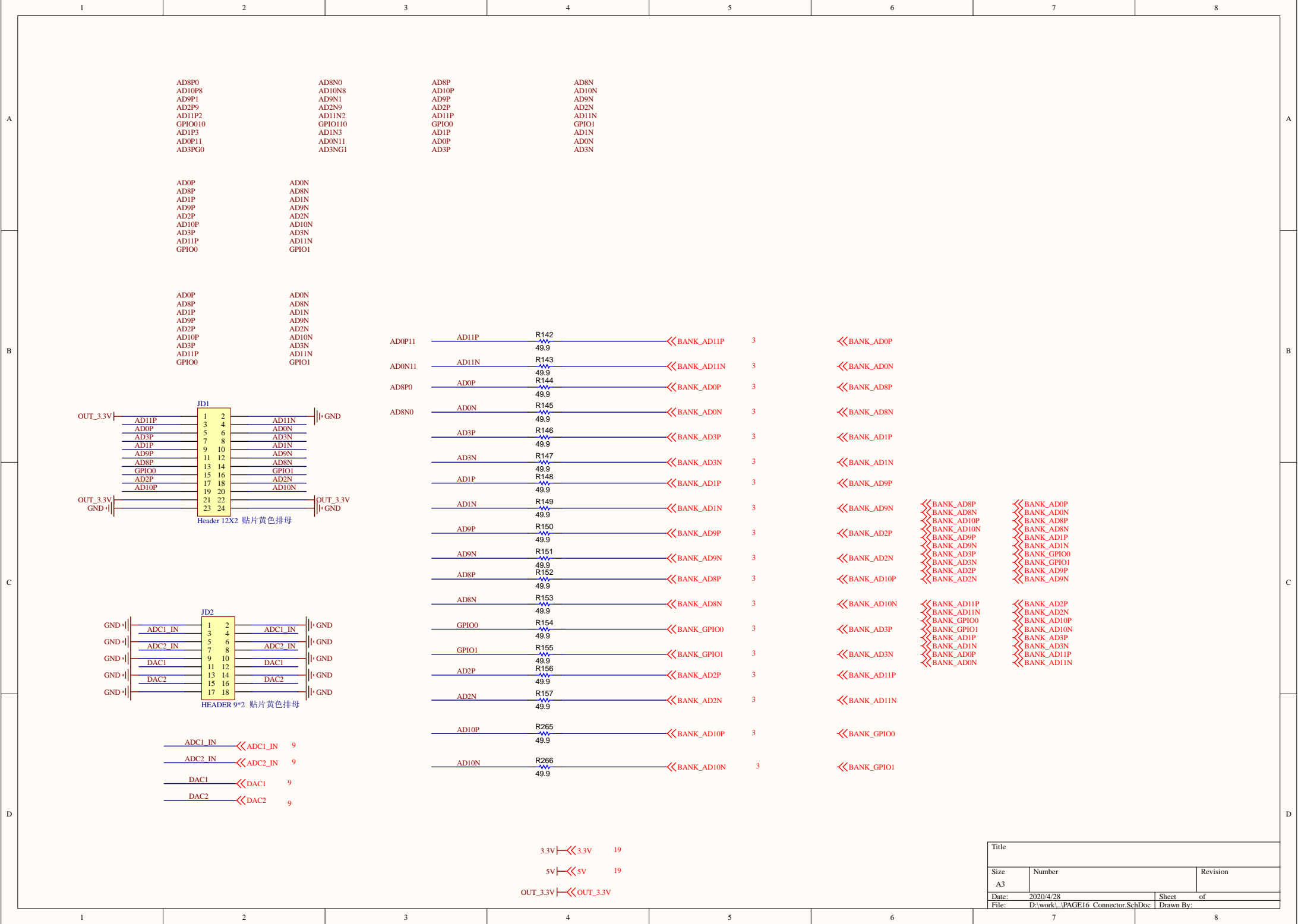
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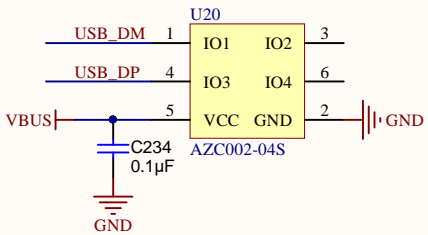
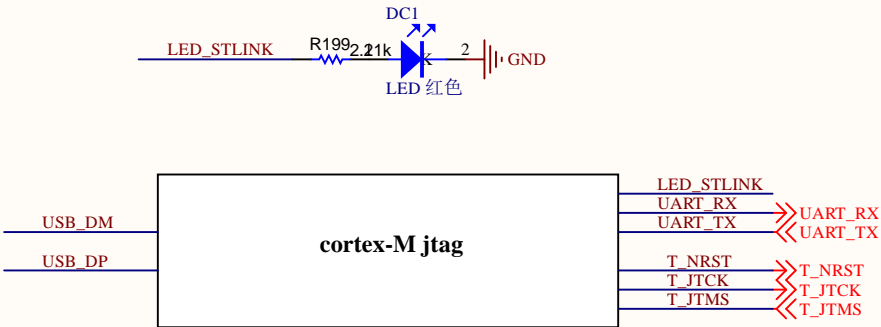
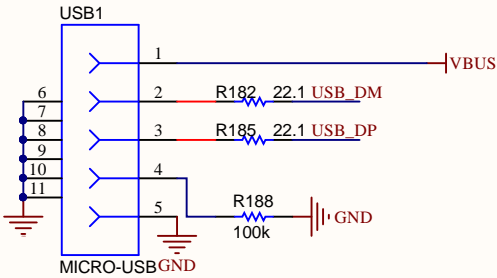
VGA



3.3V 19

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VBUS 19
3.3V 19

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