

# Sandeep

Kumar



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## Education

B.Tech Dual Degree  
Electrical Engineering |  
National Institute of Technology,  
Rourkela | 2017 | GPA:8.91/10

## Skills

**Languages:** System Verilog, C, C++,  
VHDL, Python, Matlab, SQL

**Design and Simulation Tool :**  
SpyGlass, DC compiler, Cadence CLP,  
UPF, CPF, Synplify Pro, Vivado, Verdi,  
VCS, QuestaSim, ModelSim, Vivado  
**Protocol:** PCIe, SoundWire, CXS,  
USB3/2, I3C/AVSBus/SPMI/SMBus,  
RFFE

**Other:** MS Office, JIRA, Git, ClearCase

## Thesis

**Hardware realization of Singular Value  
Decomposition Technique**

Matrix multiplication and PCA  
hardware engines for de-noising a  
corrupted 1-D signal on Altera  
Cyclone V FPGA (Low Rank  
Approximation).

-Proposed and implemented  
normalised Singular Value  
Decomposition. Uses a novel fixed  
point representation based on the  
Frobenius norm of the input matrix to  
guarantee convergence (no overflow)  
with low quantization error.

-Scalable architecture with  
parallel/iterative blocks based on  
FPGA size.

Jan'17-Jun'17

## Work Experience and Research Internships

Since Nov'21 **Lead Engineer, Senior**

Qualcomm, Bangalore

**ASIC Design:**

- Design and integration of USB3 Subsystem with USB Gen2 controller.
- Proposed and designed clock gating and memory sleep control (with/without retention) logic to put certain regions of SRAMs (supporting TX/RX buffers) of the USB controller in low power mode based on the activity on the USB link. Peak Power Reduction on Memory Rail by **20 percent** and overall power reduction by **7-10 percent (patent under process)**.
- Increased debug feasibility of USB controller's test buses by implementing logic employing Time Division Multiplexing and Trigger-Capture support.
- Experience in RTL to Netlist of ASIC design flow, MBIST Insertions, low power, multi-voltage designs, and resolving various timing constraint issues.

Jul'17-Oct'21 **Senior Engineer**

Qualcomm, Bangalore

**ASIC Design:**

- Design and Integration of USB4 Subsystem, blocks include CIO router, USB Gen2 controller, PCIe controller, debug interface.

**FPGA Prototyping:**

- Design, synthesize and simulate micro-architecture of functional RTL blocks with AHB/AXI interfaces to support subsystem level peripheral IPs emulation (CXS, PCIe, SoundWire, I3C, RFFE, AVSBus) for early software development/verification of the HW design on FPGA.

- Developed and adapted MAC-PCS layers for Xilinx GTH transceivers and PCIe Controller. Typical blocks include pipelines, reset blocks, serdes clock distributor, L1 sub state enabler and channel bonding between transceivers.

- Implemented ASIC RTL code on UltraScale series prototyping environment by using FPGA specific primitives (IDDR, GTH, BUFG, MMCM).

- Lab bringup/debug of various peripherals in Emulation with Analyzer, DSOs and Lauterbachs.

- Collaborate with PCB teams for schematic review and rework on daughter boards on FPGA platforms.

Aug-Oct'16

**Graduate Student Researcher**

Prof. Supratim Gupta, NIT Rourkela, India

- Designed hardware components for image pre-processing algorithms on Alters Cyclone V FPGA. Key Tasks completed:

- Filtering Operation: Max, Min, Median, Gaussian, Gradient, and Custom Filters. Implemented Canny Edge Detection.

- Transfer Image data to/from Matlab GUI from/to FPGA and compare precision/accuracy with time complexity.

Summer'16

**Summer Intern**

Late Prof. Alain Wegmann, LAMS, EPFL, Switzerland

- Designed capacitive and gas sensors for TailNode sensing using SX1272 on LoRaWAN and their interfacing with TI MSP430.

- Upgraded data logger board design and software to work on LoRaWAN. Collaborated with on-chip antenna vendors for matching networks.

Summer'15

**Summer Intern**

Late Prof. Alain Wegmann, LAMS, EPFL, Switzerland

- Designed a Data logger based on TI MSP430 for low-power field applications. Key tasks completed:

- Battery Charging circuit with under voltage protection and Buck-Boost design for powering diverse sets of environment sensors.

- Software Design for micro-controller targeting communication protocols-DDI serial, SDI-12, Digital, and Ublox Modem.

- Website (Backend and Frontend) for data logging with live data feeds and graphs.

Feb-Aug'14

**Research Intern**

Prof. Dayal Parhi, Robotics Lab, NIT Rourkela, India

- Testing and Designing Mobile Robot Navigation Techniques using Obstacle Avoiding Robot.

- Designed an autonomous robot similar to the Khepera robot by interfacing proximity sensors placed at different angles to test a route planning-based invasive weed optimization (IWO) algorithm.

# Extra-Curricular —

## Mountaineering Tasks Sept 2019

Expedition to Machadhar Peak  
(15000 ft)

Basic Mountaineering Course 259  
NIM (Grade Received: A)

## Robotics Team Member

- Won and Participated in numerous robotics competitions across major events in the country.
- Won **Kshitj 2014 | 20K INR** at Indian Institute of Technology, Kharagpur. (1/94 teams)
- Designed an autonomous robot that could find arena checkpoints (light sources) and avoid earthquake-affected vibration zones. Robots have photo-resistors and accelerometers to detect light sources and vibration zones.

## Technical Team Member at Monday Morning 2015

- Maintained the official E-Newsletter of NIT Rourkela, Monday Morning. Tasks included improving the website performance and publication of articles on the website.

## NIT Rourkela Electrical Engineering Merit Award 2013

Among Top 2 Students of the UnderGraduate Branch-Specialization.

## Software Designer for a Balloon Payload 2014

- Interfaced and Calibrated sensors for a balloon payload launched to an approximate altitude of 1 km above sea level .
- Project was funded by NIT Rourkela as part of an initiative to design student satellites to be launched in space.

## Patents, Posters and Other Presentations

2020	<b>US10528517B1</b> Systems and methods for power conservation in a SOUNDWIRE audio bus through pattern recognition <b>Granted</b> Overall power reduction of 100 uW with 70-80 percent reduction in GPIO toggling during PDM transmission.
2020	<b>US10359827B1</b> Systems and methods for power conservation in an audio bus <b>Granted</b> Overall power reduction of 100 uW with 60-70 percent reduction in GPIO toggling during PCM transmission.
2021	<b>US20210216490</b> Optimal I3C In-Band Interrupt Handling through Reduced Slave Arbitration Cycles <b>Granted</b>
2020	<b>US20200192455</b> Reducing power consumption of communication interfaces by clock frequency scaling and adaptive interleaving of polling <b>Granted</b>
2020	<b>QUALSTAR</b> Successful Implementation of Xilinx PCIe single slot x4 Lane-Bifurcation for Two PCIe Root Complexes (x2x2 or x4 mode) for a Compute SoC Emulation Model with L1ss Support.
2020	<b>QUALSTAR</b> AVSBus Slave synthesizable UVM VIP for DV and FPGA Emulation- <b>Presented a poster in Qualcomm Innovation Forum 2020</b> - Designed a PMBus Spec-compliant AVSBus (Adaptive Voltage Scaling Bus) slave to replace a third-party protocol-compliant IP that was purchased as a VIP or an ASIC slave with an analyzer in validation for Master verification. <b>(100k USD cost reduction)</b> - Implementation caters to specific features- In Band Reset, Interrupt, CRC check with corruption feasibility, Enumeration and Data Transport support. Added Basic Assertion for protocol violation checks.
2019	<b>QUALSTAR</b> Systems for power conservation in an audio bus and Demonstration of virtual sniffer on Audio Bus <b>Presented a poster in Qualcomm GSOC Summit-Cork Ireland 2019</b> - Proposed Architecture and Design implementation for Audio Packets (PCM/PDM) transmitted on SoundWire Link. - Designed Python GUI to parse protocol packets and eliminate the need for external logic analyzer and debug probes. This was critical for ASIC High Volume Testing and OEMs <b>(50k USD cost reduction)</b>
2021	<b>QUALSTAR</b> Successful bring-up of Chip to Chip CXS-PCIe Link Data Aggregation and Packet forwarding Designed CCIX data forwarder/aggregator which converts incoming/outgoing AHB data traffic to CXS compliant packets by handling credits and link ownership with CCIX PCIe controller VC1. (Outbound/Inbound Traffic)
2021	<b>QUALSTAR</b> RFFE DMAC implementation - Designed DMA Channels which performs data and command transfer on RIF interface for RFFE Master on current and pending queues. - Handles interface ownership based on priority, out of order transactions and read/write to memory.