Rice University | Statement of Purpose | Sandeep Kumar

As an ASIC/FPGA engineer at Qualcomm, my work has been centered around designing and improving Wired Peripherals Digital IPs. Major contributions range from developing new low-power cores, coming up with novel methods to improve their performance, and tackling software/customer (OEM) issues in pre and post-silicon. During this process, I have discovered a deep passion for research development with a constant thirst for collaboration, innovation, and execution. As an incoming Ph.D. student, I am driven to build on this approach and venture deep into the area of circuit design with a strong focus on Analog/RFIC design and hardware architecture. I think Rice offers an excellent atmosphere that will allow me to experiment, learn new skills, and become an expert in this area.

At Rice, I am particularly interested in the work of Prof. Taiyun Chi in the area of Millimeter-Wave and Terahertz Systems. Integrated high-power THz arrays with beam-steering, modulation, and higher radiated power can enable new applications in communication, sensing, imaging, and spectroscopy. Current implementations for THz wave generation in CMOS technology have been centered around harmonic oscillators and multipliers, followed by the rejection/suppression of unwanted harmonics. I hope to work with Professor Chi to advance this work and develop better harmonic boosting techniques which are critical in the design of a THz radiator. For example, I hope to advance this approach by designing novel harmonic injection mixers using Schottky diodes (similar to HRMs) whose each LO signal is phase shifted with the final output from each path being summed up.

I am also interested in Prof. Chi's work in sub-THz Radiation (60-140 GHz) Sources. This includes power amplifiers (PA), low noise amplifiers (LNA), wideband phased-array receivers and other front-end circuits. To overcome higher route loss and provide Gb/s data to many users with minimal latency, base stations and user equipment rely on directed communications. This means that these units are subject to nonlinear effects owing to variations in phased array scan angles. Because of beam steering, power amplifiers linked to an antenna array might suffer varying voltage levels. In this instance, consideration of PA outputs servicing distinct bands is also an important factor. At Rice, I look to investigate nonlinear effects (reflected input voltages) on power amplifiers that can arise due to variations in antenna impedance (VSWR) at different scan angles and develop a good mitigation circuit that can ensure enhanced power transmission and communication reliability.

Another reason why I want to pursue building new THz systems under Prof. Chi is because of their potential applications in machine learning and inference tasks. Modern DNNs consume significant power, which is primarily driven by data movements and high computational complexity. I think that the ability to add and multiply two vectors (MAC) can be achieved instantly on EM waves (through superposition and phase delay) with no energy cost. With receiver and transceiver units placed at relatively short distances (slightly above near field) in novel architectures, these results can be directed to the right location on the RX side thereby reducing data movements. Analog computation and inferences are already being done at optical frequencies, but consume high power and cost. I believe, because of the larger antenna sizes and associated transceiver complexity, no work has been done on this application in the RF to mm-wave range. However, with the recent realization of THz systems having desired antenna responses using multiple electronic feeds, I see that it can be investigated, and thus I am highly motivated to pursue this path during my time at Rice.

My experience has mostly been in digital design. Building ASIC digital IPs for Wired Protocols (particularly USB, CCIX, and Audio) and adapting them for actual software use cases, has implanted in me a design mindset for optimal hardware (while keeping the big picture intact). I am highly driven to put my skills to use in the field of RFIC and Hardware design.

At Qualcomm, I have had the opportunity to work on several state-of-the-art projects where I have constantly tried to approach them with a research mindset. During the early days, I was entrusted with creating an FPGA prototype for a newly built Audio core based on the SoundWire protocol that was soon to hit the market. During pre-silicon bring-up, I observed dense toggling of FPGA IOs on DSO for a 24 Mbps NRZI transmission, indicating considerable switching power. I knew that streams of raw 32/24-bit audio PCM samples, like images, are highly correlated. Could I create a method that uses this temporal correlation to decrease IO toggling? To evaluate the effectiveness of this strategy, I created Python models for sending NRZI packets and tested them with various audio patterns (a voice call, multimedia audio, etc.). It lowered the toggling power for PCM transmission, and the results were compelling. I extended this model to investigate PDM streams that included delta sigma up/down conversion and sampling. The model demonstrated that a configurable threshold for different tones might convey this density, thereby decreasing the logic 1s on the link. I approached the Architecture team in Haifa, Israel, and we worked together on hardware design. Later, we presented a poster on this approach at the Company-wide Global SoC Summit. This very activity of modeling, questioning, designing, and collaborating excites me to pursue research. I feel certain that I will be able to make meaningful contributions to the field of Analog/RFIC design by continuing with this approach.

Similarly, while working on I3C and RFFE IPs, I had to monitor their performance with tapped-out chips. I could see that with the sheer number of sensors/RFFE devices attached, it was difficult for a master to cater to diverse interrupts. The highest priority can always prevent lower priorities from being serviced. This leads to software never considering stalled slaves just because protocol mandates giving priority to saves. To improve interrupt service and optimize system decisions, I devised a one-of-a-kind addressing method that allows the master to view at least 5-6 slaves in a single interrupt. The same thirst for optimization and developing new frameworks also propelled me toward approaches that could reduce organizational costs. I intend to maintain this perspective throughout my chosen research.

As a current contributor to USB design, I proposed and implemented techniques to reduce power and improve performance in USB controllers when communicating with an external host/device. One such instance includes coming up with hardware architectures (and testing/simulating them) to keep unused regions of SRAMs used in large data buffers in sleep with/without retention based on their real-time software usage and USB protocol requirements. Now that I look back, the constant what/why/when questions that I dealt with these IPs propelled me to come up with these approaches, and the ability to deftly break down and prioritize tasks for strict deadlines allowed me to execute them. Ramping up and gaining expertise in new endeavors is not alien to me. I hope to do the same in RFIC and hardware design.

I now understand the joy and satisfaction that come from working on engineering tasks and delving deeply into the study of new methodologies, frameworks, and tools. It has also made me realize that a Ph.D. is the ideal setting for me to develop my research abilities and push sustainable technology to the forefront of the market. Obtaining a Ph.D. in Analog/RFIC design from Rice with a focus on energy-efficient hardware will be critical in achieving this goal.