Stanford EE | Statement of Purpose | Sandeep Kumar

As an ASIC/FPGA engineer at Qualcomm, my work has been centered around designing and improving Wired Peripherals Digital IPs. Major contributions range from developing new low-power cores, coming up with novel methods to improve their performance, and tackling software/customer (OEM) issues in pre and post-silicon. During this process, I have discovered a deep passion for research development with a constant thirst for collaboration, innovation, and execution. As an incoming Ph.D. student, I am driven to build on this approach and venture deep into the area of circuit design with a strong focus on Analog/RFIC design and hardware architecture. I feel Stanford offers an excellent atmosphere that will allow me to experiment, learn new skills, and become an expert in this area.

At Stanford, I am particularly interested in the work of Prof. Boris Murmann in the area of domain-specific mixed-signal design for energy-efficient hardware catering to machine learning and inference tasks. Modern DNNs consume significant power, which is primarily driven by data movements and high computational complexity. Professor Murmann's research has addressed this issue by bringing machine learning closer to the sensor and decreasing the bandwidth required to connect devices. As this technology is frequently used for applications like object identification that operate on streams of image (video) or audio, I believe there is a great opportunity to extend this method to create an input-aware network, avoiding some repetitive computations (convolutions) in the process. For example: given a video stream, it is expected that there is a lot of redundancy in the sequence of images. Thus, for a given filter/kernel size, one may hop/bypass certain convolution processes if the input image/feature map values in that region are the same as the previous input. This can significantly reduce computations for the initial FC layers, which are often denser and closer to the actual input layers than the layers below. I am eager to investigate and contribute to such efforts.

Prof. Murmann’s group has also developed novel ADC architectures targeting data compression in brain action potential's digitization or in-sensor machine learning. Removing redundancy from incoming data contributes to a significant reduction in ADC power consumption. I look to expand on this approach by leveraging the slow temporal change of physical signals (neural or images) in comparison to the ADC's sampling frequency and developing new ADC architectures based on the findings. For example, Current DACs employed in SAR ADC or RAMP ADCs are independent of temporal variation of input signals, resulting in convergence complexity of O(logN) (binary search) or O(n) (linear search) respectively. I intend to improve these search algorithms by employing unique DAC structures that take previously converged input samples into account, thereby offsetting the initial comparison, and bringing us closer to a hashmap complexity of order O(1). These application-specific architectures can lower the overall clock cycles required for convergence and hence, power consumption, with little area overhead.

I'm also highly interested in building on Prof. Amin Arbabian's work on Millimeter-Wave Imaging and Perception. To address image attenuation caused by phase imbalances and skews between each ADC/DAC unit, novel application-specific time-interleaved SAR ADCs and DACs for high-speed sensing are required. Along with the previously described ways, I am driven to create novel feedback control loop structures between each unit by sensing these mismatches, which will aid in calibrating and decreasing these imbalances. My recent experience has mostly been in digital design. Building ASIC digital IPs for Wired Protocols (particularly USB, CCIX, and Audio) and adapting them for actual software use cases, has implanted in me a design mindset for optimal hardware (while keeping the big picture intact). I am highly driven to put my skills to use in the field of Analog/RFIC design.

During my undergrad, I worked on academic projects and competed in robotics competitions, exposing me to a variety of technical disciplines. Interning in the Systemic Modeling Laboratory (LAMS) at the Swiss Federal University Lausanne (EPFL) during summers under the Late Prof. Alain Wegmann allowed

me to become a proficient system designer. Designing a real-time sensing and communication platform capable of communicating with multiple sensors while consuming only mW of power sharpened my investigative and debugging abilities. Conducting field research at EPFL and in India was a terrific learning experience. I'll never forget staying in these remote locations and building them to withstand severe dusty winds at 120 °F (50 ° C). Moreover, testing and strengthening the platform after analyzing its failures in extremely harsh environments aligned my thinking to cater to and differentiate the gaps between working in lab settings and fields.

During my time at Qualcomm, I have had the opportunity to work on several cutting-edge projects, approaching them with a research mindset. One project I was tasked with was creating an FPGA prototype for a new Audio core based on the SoundWire protocol. While working on this project, I noticed high levels of toggling in the FPGA IOs during transmission and realized that audio PCM samples, like images, have a strong temporal correlation. I then created a method that utilizes this correlation to decrease toggling power, testing it using various audio patterns. This strategy was successful and I then expanded it to investigate PDM streams. I presented this approach to the Architecture team in Haifa, Israel, and together we presented a poster on it at a company-wide summit. This very activity of modeling, questioning, designing, and collaborating excites me to pursue research. I feel certain that I will be able to make meaningful contributions to the field of RFIC and Energy-efficient Hardware design by continuing with this approach.

Similarly, while working on I3C and RFFE IPs, I had to monitor their performance with tapped-out chips. I could see that with the sheer number of sensors/RFFE devices attached, it was difficult for a master to cater to diverse interrupts. The highest priority can always prevent lower priorities from being serviced. This leads to software never considering stalled slaves just because protocol mandates giving priority to saves. To improve interrupt service and optimize system decisions, I devised a one-of-a-kind addressing method that allows the master to view at least 5-6 slaves in a single interrupt. The same thirst for optimization and developing new frameworks also propelled me toward approaches that could reduce costs for organizations. I intend to maintain this perspective throughout my chosen research.

As a current contributor to USB design, I proposed and implemented techniques to reduce power and improve performance in USB controllers when communicating with an external host/device. One such instance includes coming up with hardware architectures (and testing/simulating them) to keep unused regions of SRAMs used in large data buffers in sleep with/without retention based on their real-time software usage and USB protocol requirements. Now that I look back, the constant what/why/when questions that I dealt with these IPs propelled me to come up with these approaches, and the ability to deftly break down and prioritize tasks for strict deadlines allowed me to execute them.

I now understand the joy and satisfaction that come from working on engineering tasks and delving deeply into the study of new methodologies, frameworks, and tools. It has also made me realize that a Ph.D. is the ideal setting for me to develop my research abilities and push sustainable technology to the forefront of the market. Obtaining a Ph.D. in analog/RFIC design from Stanford, with a focus on energy-efficient hardware, will be critical in achieving this goal.