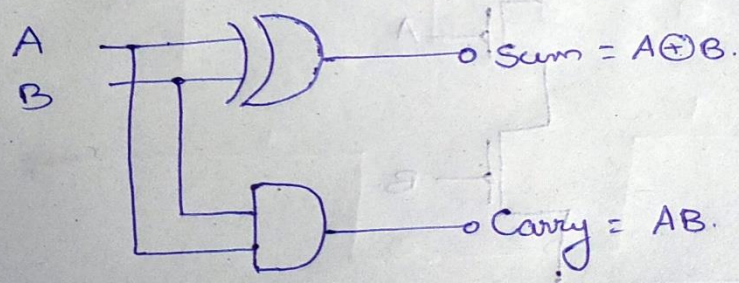
Aim:- Implementation of Halfadder using CMOS in Cadence Virtuoso.

Introduction:-

Half Adder is a combinational Arithmetic circuit that adds two numbers and produces a sum bit and a carry bit both as output. The addition of 2 bits is done using a combinational circuit called a Half adder. The input variables are augend and added bits and output variables are Sum & Carry bits.

Logic Diagram:-

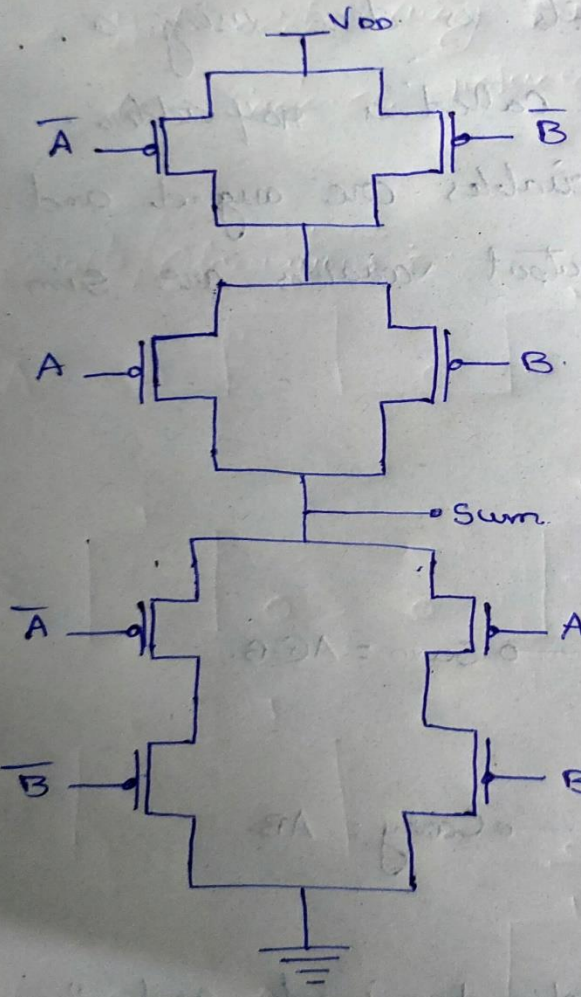


* Half adder has only two inputs and there is no provision to add a Carry coming from the lower order bits when multi addition done.

Truth Table :-

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half-adder using CMOS.



$Sum = A \oplus B$

$= \bar{A}B + B\bar{A}$

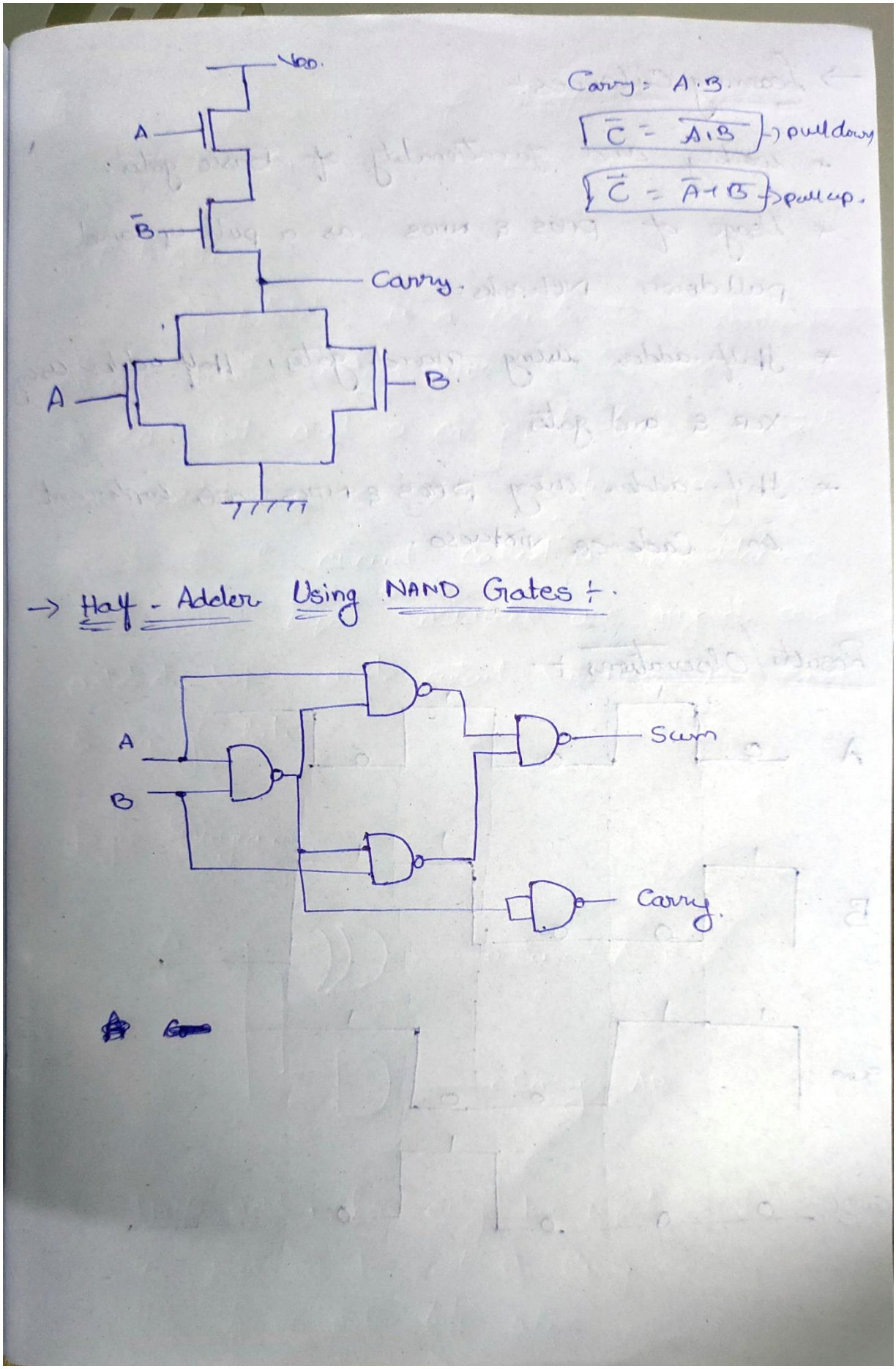
NMOS $\bar{S} = \bar{A}B + B\bar{A}$

$\bar{\bar{S}} = \bar{A}\bar{B} + AB$

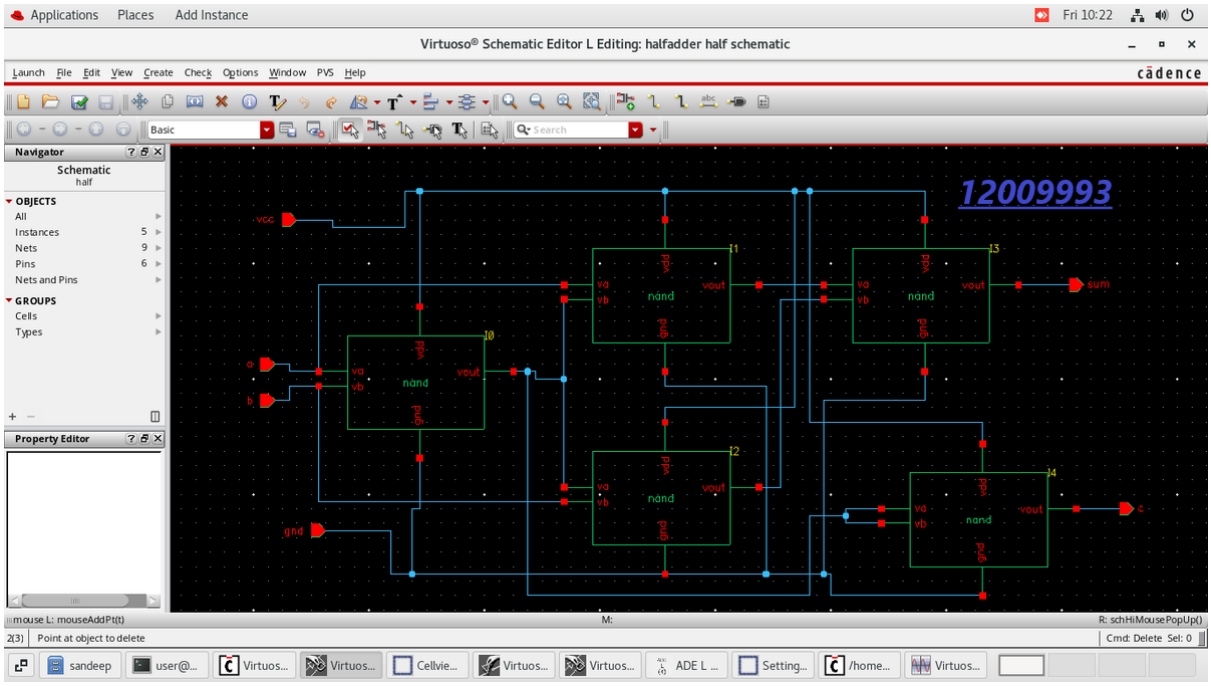
NMOS pull down network

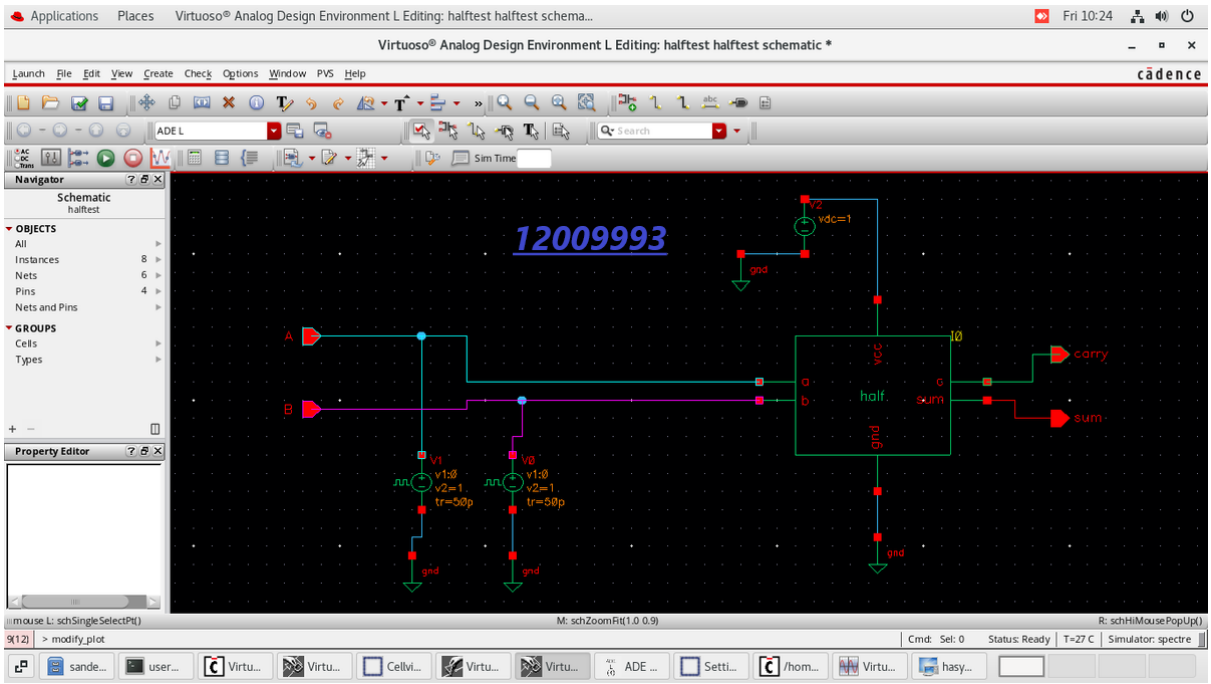
$\bar{S} = (\bar{A} + \bar{B}) \cdot (A + B)$

Pull-up (PMOS).


Vdd.
A
B
Carry.
A
B
Carry = A.B
$\bar{C} = \overline{A.B}$ → pull down
$\bar{C} = \bar{A} + \bar{B}$ → pull up.
→ Half - Adder Using NAND Gates :-
A
B
Sum
Carry.

Schematics from the cadence:-





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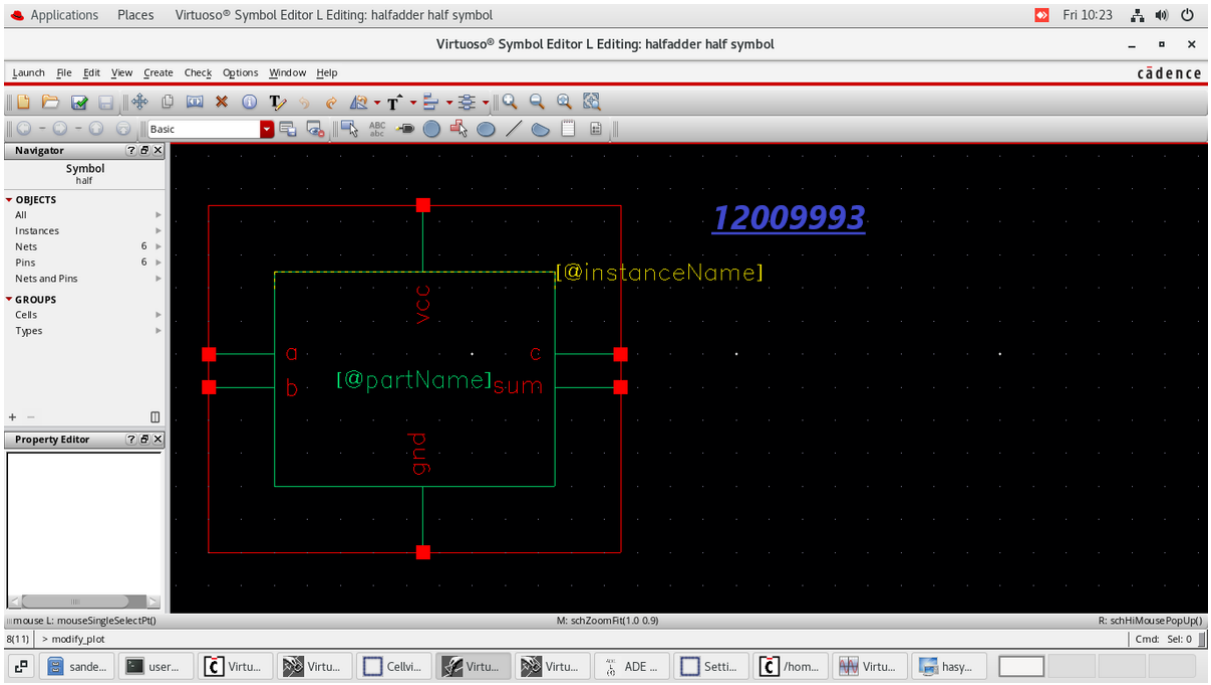

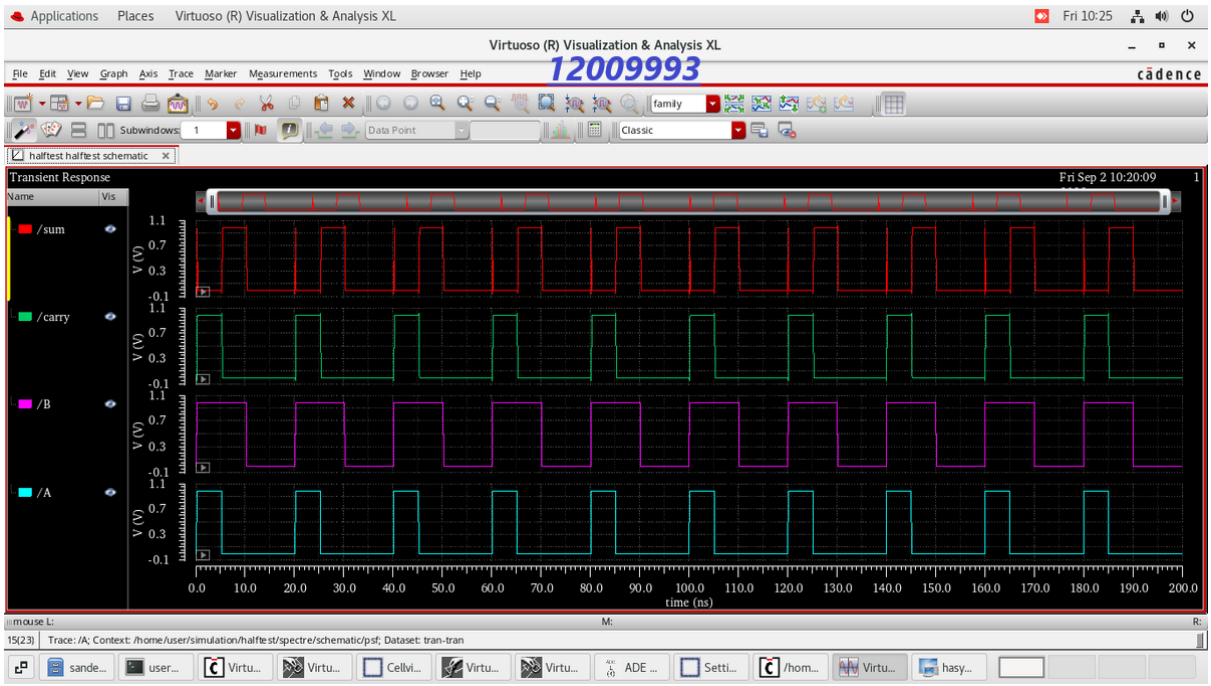

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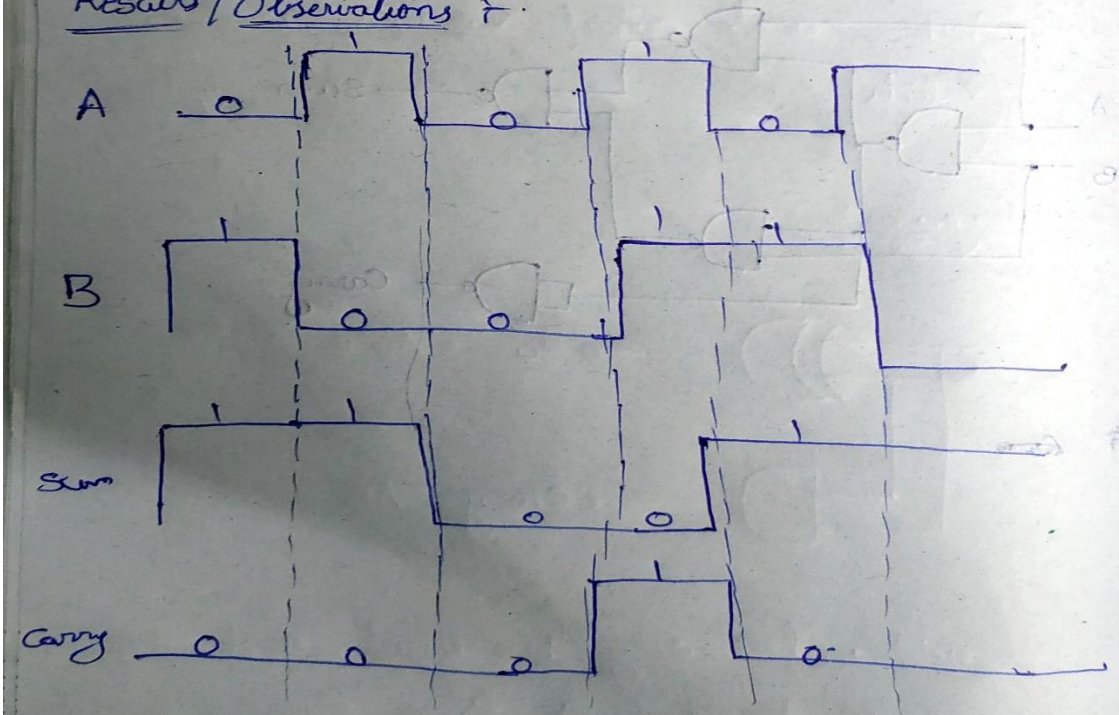
→ Learning Outcomes :-

* Working and functionality of Basic gates.
* Usage of PMOS & NMOS as a pull-up and pull down Networks.
* Half-adder using nand gates; Half adder using XOR & and gates.
* Half-adder using PMOS & NMOS are implemented in Cadence Virtuoso.

Results / Observations :-



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