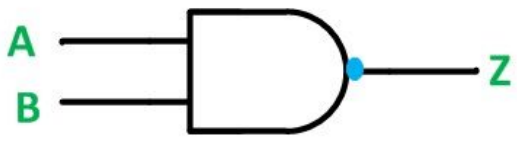
AIM:- *Nand gate using PMOS &NMOS Using Cadence Virtueso.*

INTRODUCTION:-

- *The NAND gate is a combination of an AND gate and NOT gate. They are connected in cascade form. It is also called* ***Negated And gate****. The NAND gate provides the false or low output only when their outputs is high or true. The NAND gate is essential because different types of a boolean function are implemented by using it.*
- *The NAND gate has the property of functional completeness. The function completeness means any types of gates can be implemented by using the NAND gate. It performs the function of OR, NOR and AND gate.*

- *The logic symbol for the gate is shown below:*



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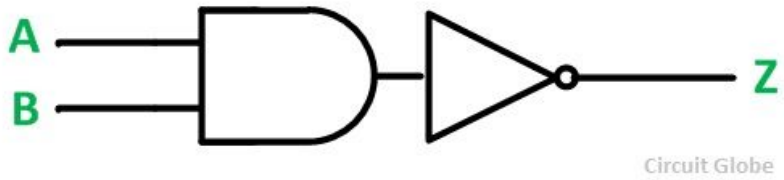
- *The logic circuit of the NAND gate is shown below:*



- *From the logic circuit, the output can be expressed as:*

$$Z = \overline{A \cdot B}$$

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

From the truth table of the gate, it is clear that all the inputs must be high to get a low output and if any of the input is low, the output obtained will be high. If any one of the input is also high the output will be high that is 1.

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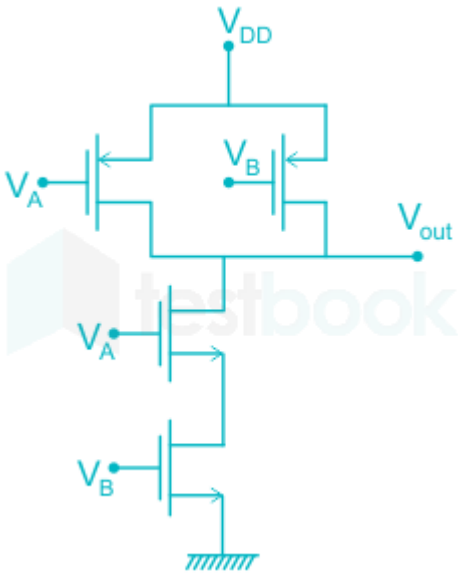
***CMOS NAND Gate*:-**

It consists of two series NMOS transistors between Y and Ground and two parallel PMOS transistors between Y and VDD.

If either input A or B is logic 0, at least one of the NMOS transistors will be OFF, breaking the path from Y to Ground. But at least one of the pMOS transistors will be ON, creating a path from Y to VDD.

Hence, the output Y will be high. If both inputs are high, both of the nMOS transistors will be ON and both of the pMOS transistors will be OFF. Hence, the output will be logic low.



NAND GATE USING CMOS AND NMOS

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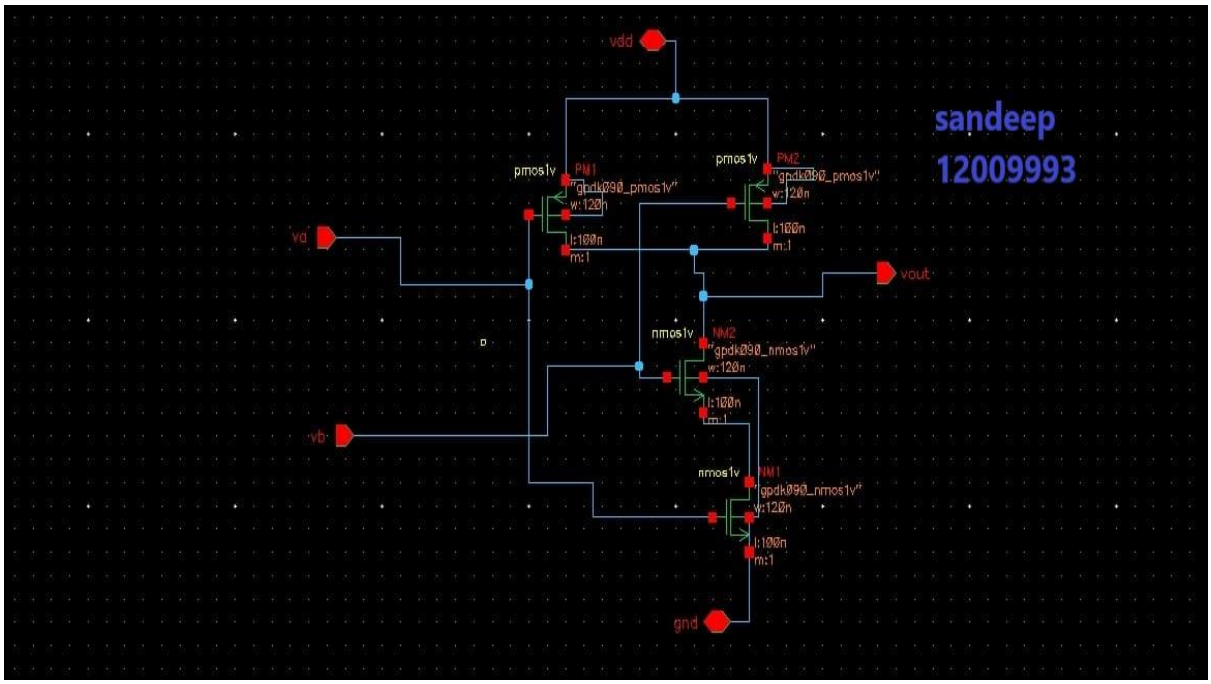
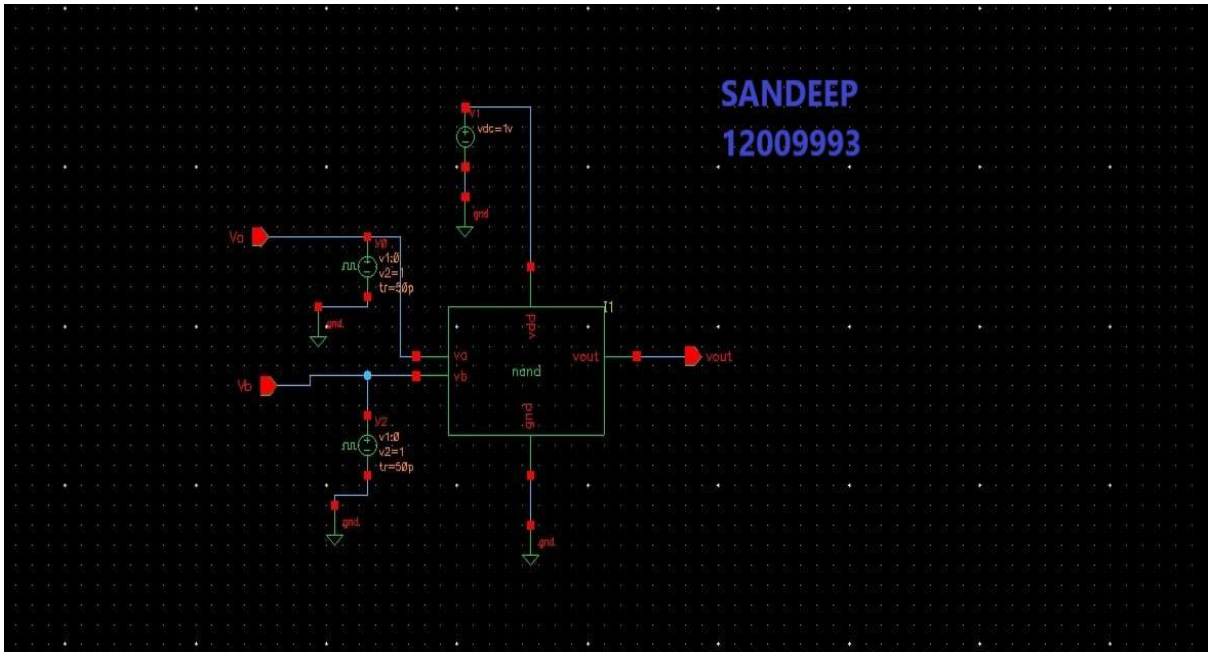
➢ ***SCHEMATICS SCREEN SHOTS FROM CADENCE***





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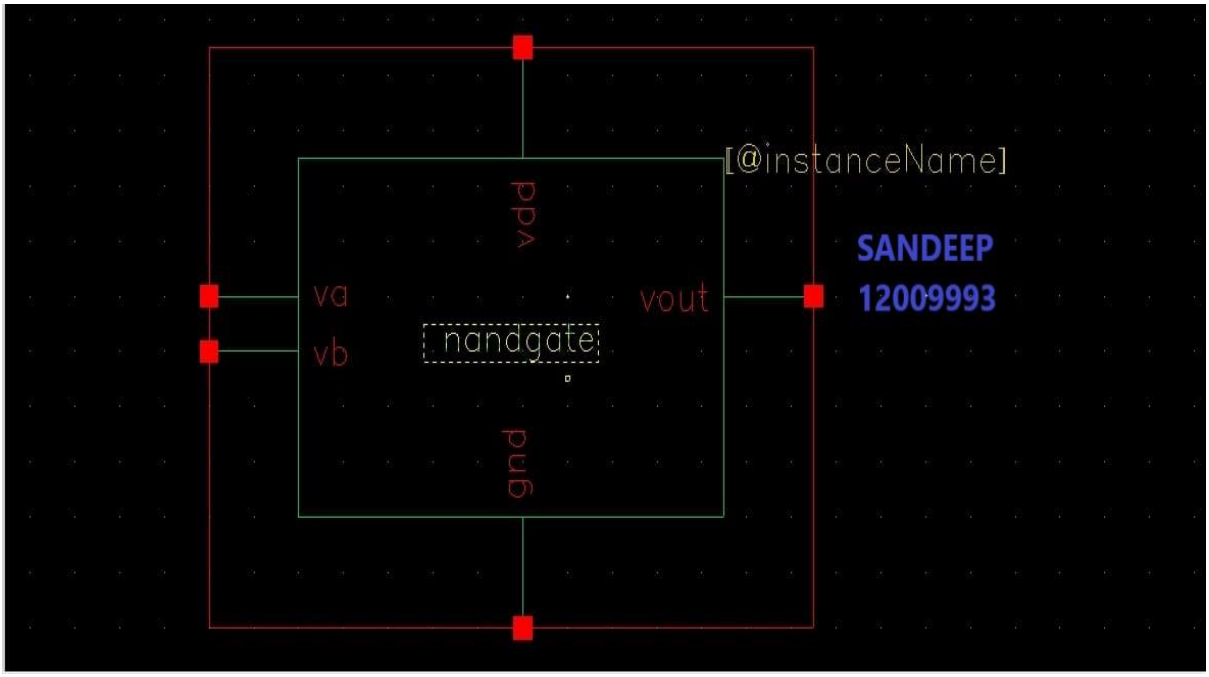

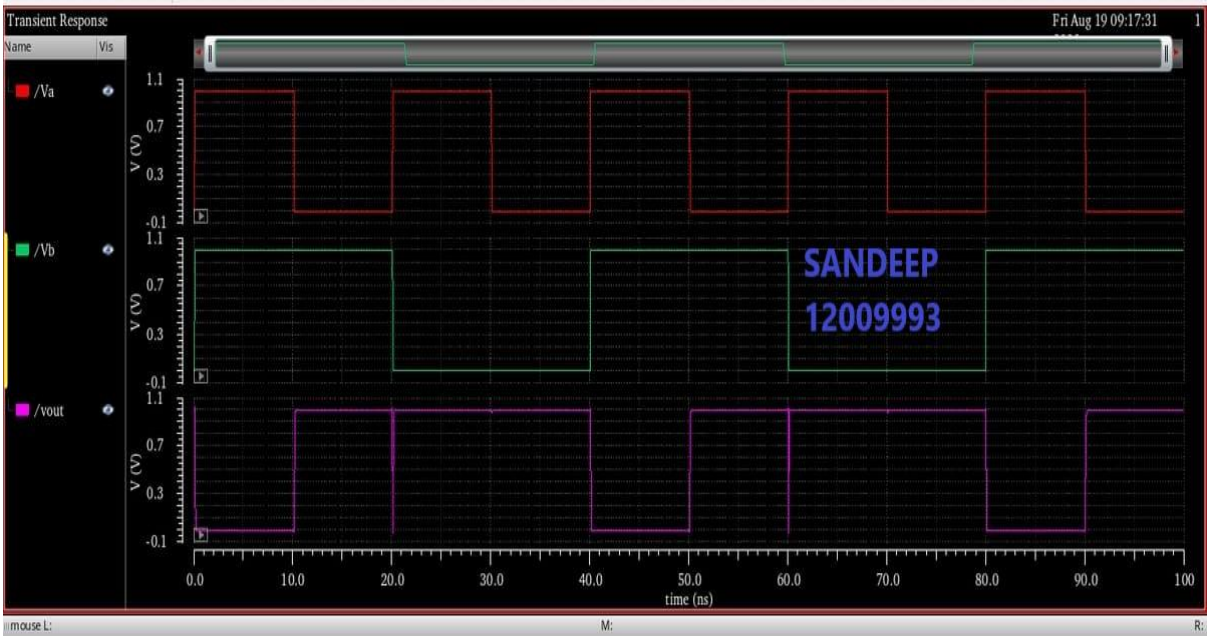

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THE-END