Aim :- Designing of D-flipflop using Cadence Virtuoso.

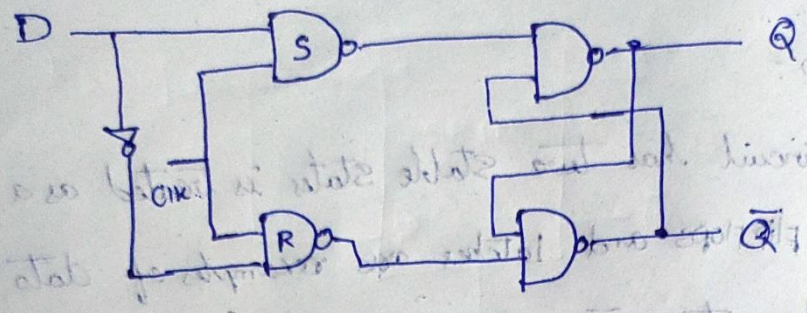
Introduction :-

A circuit has two stable states is treated as a flipflop. Flip Flops and latches are examples of data storage elements. In Sequential logical circuits, the flipflops is the basic storage elements. Flip Flops are of 4-Types ;- i) SR flipflops ii) J-K flipflops iii) D-flipflop iv) T-flipflops.

The D-flipflop is the most important flipflop from other clocked-types. It ensures that the same time, both the inputs, i.e S&R are not equal to 1. The Delay flip-flop is designed using a gated SR-flipflop with an inverter connected between the inputs allowing for a single Data input D.

The single Data input, which is labeled as "D" used in place of the "set" input and for the Complimentary "Reset" input that inverter is used.

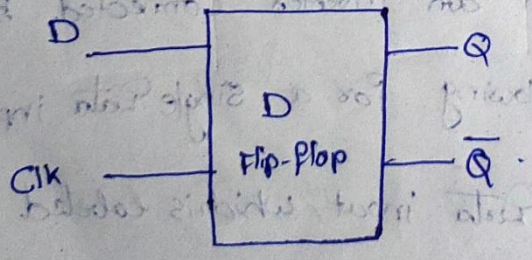
→ Circuit Diagram :-



→ Truth Table :-

Clk	D	Q	$\bar{Q}$	
↓	X	Q	$\bar{Q}$	Memory no change
↑	0	0	1	Reset
↑	1	1	0	Set

→ Block Diagram :-



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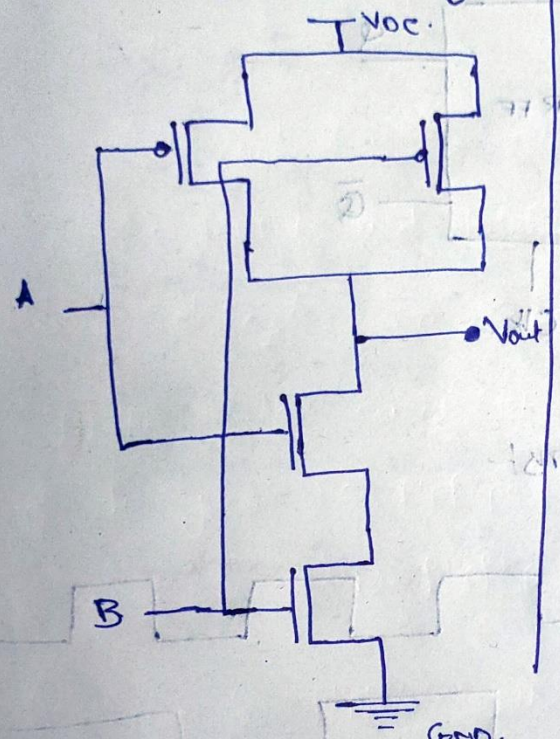
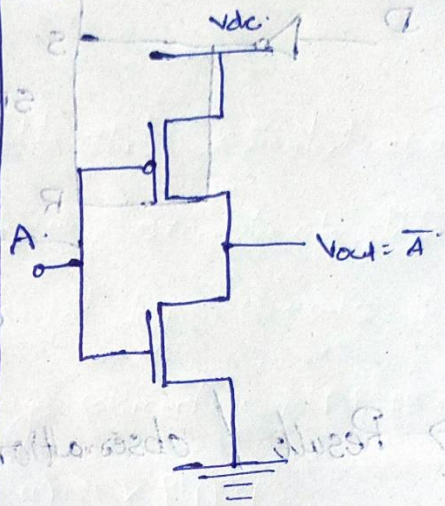
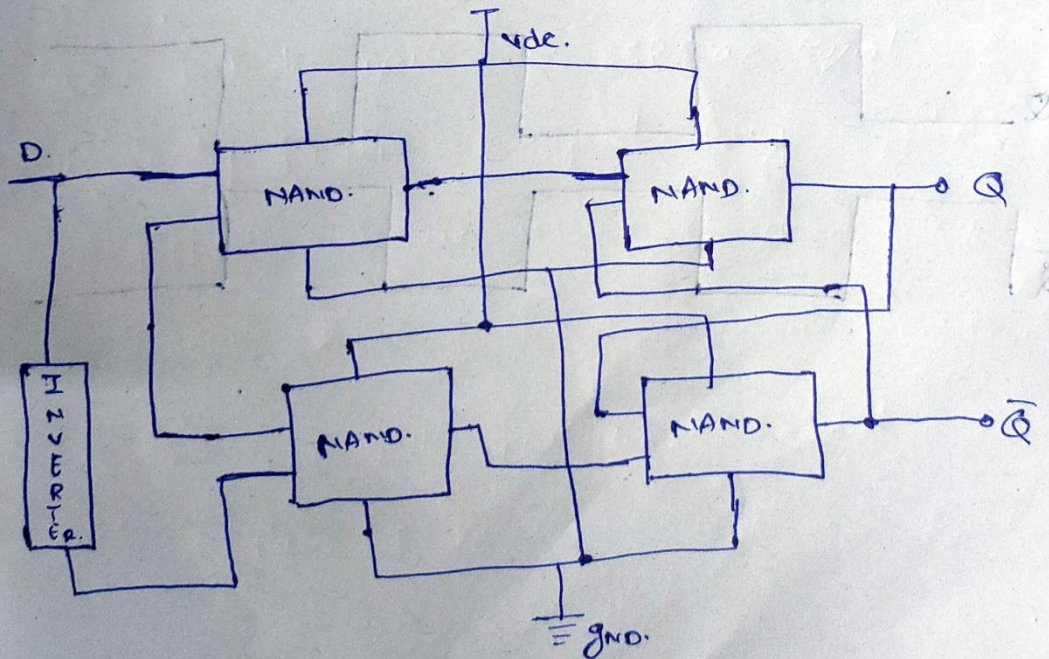
→ CMOS Designing :-

i) NAND gate designing.

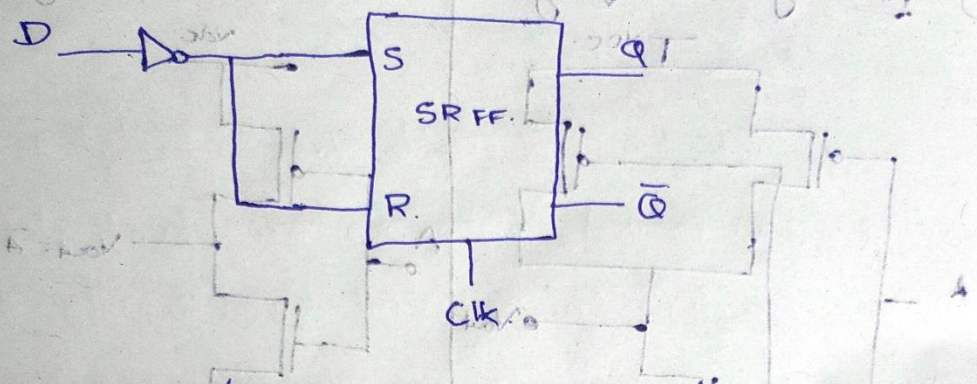


ii) Inverter Designing.

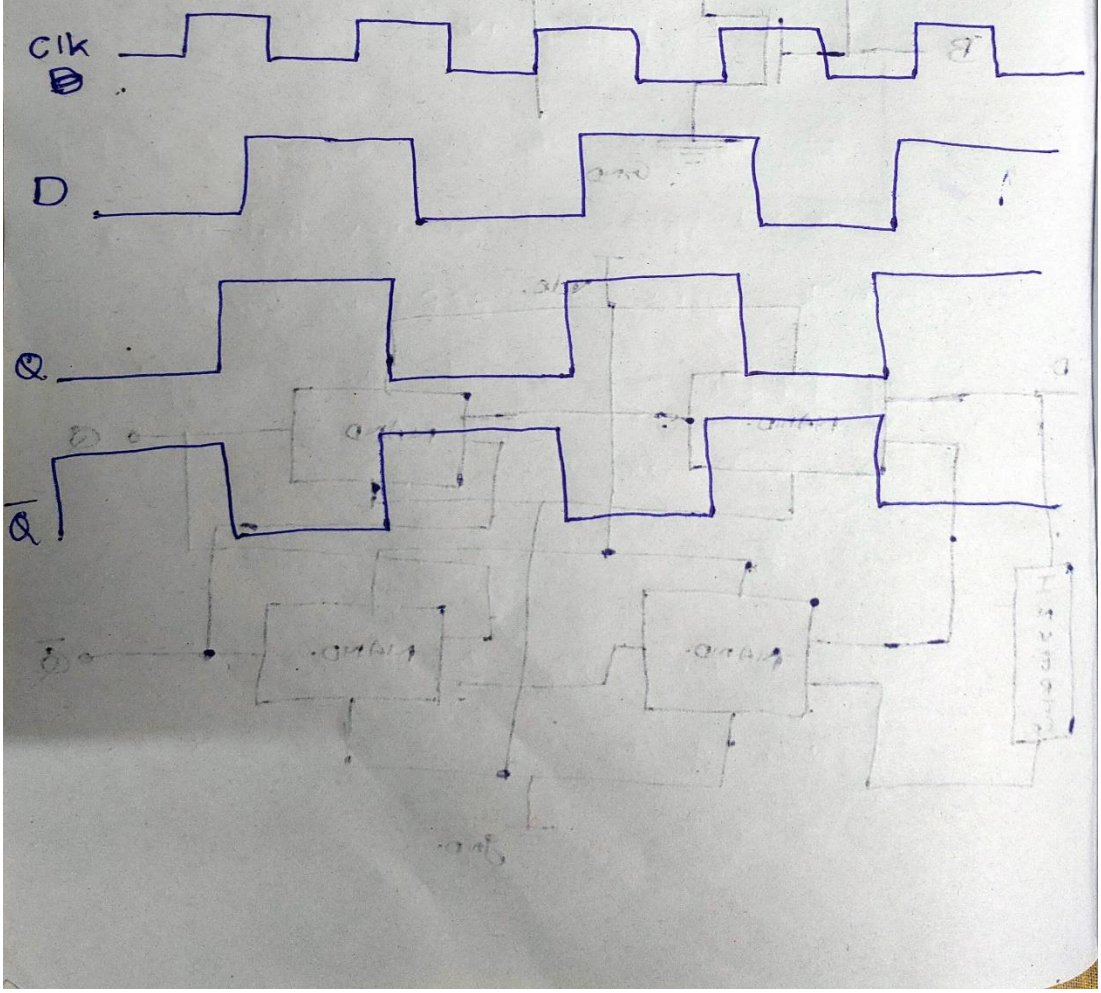




→ D-FlipFlop using SR FlipFlop Block Diagram



→ Result / observations:-



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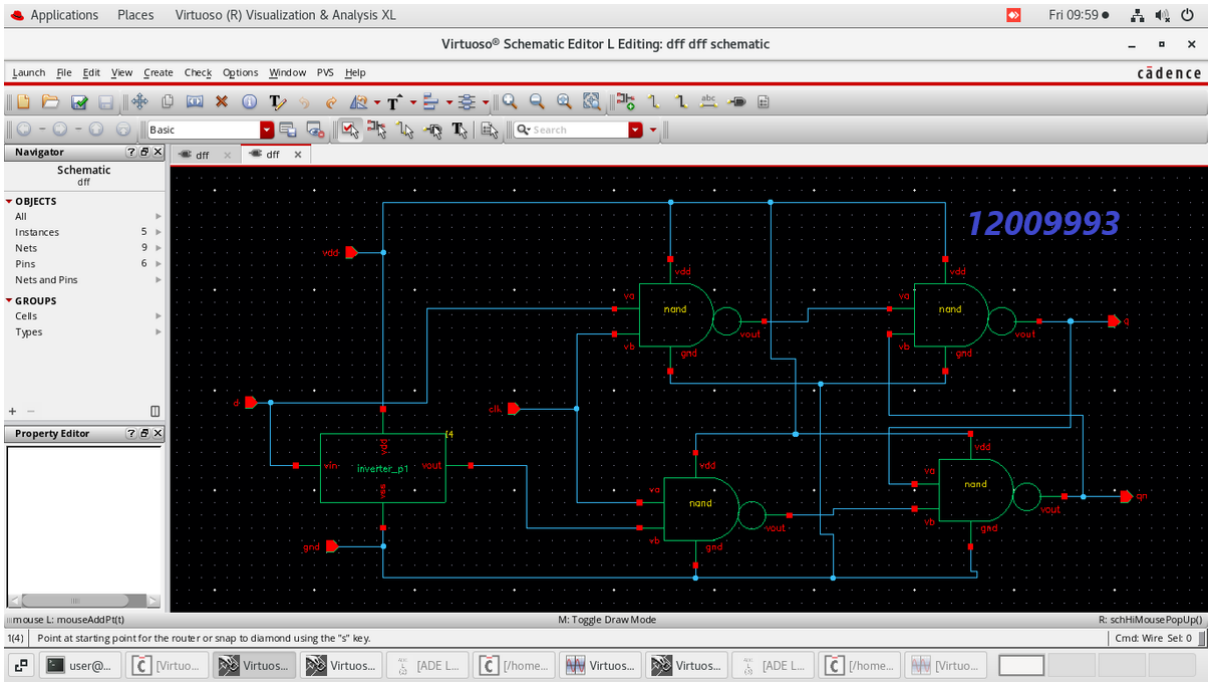
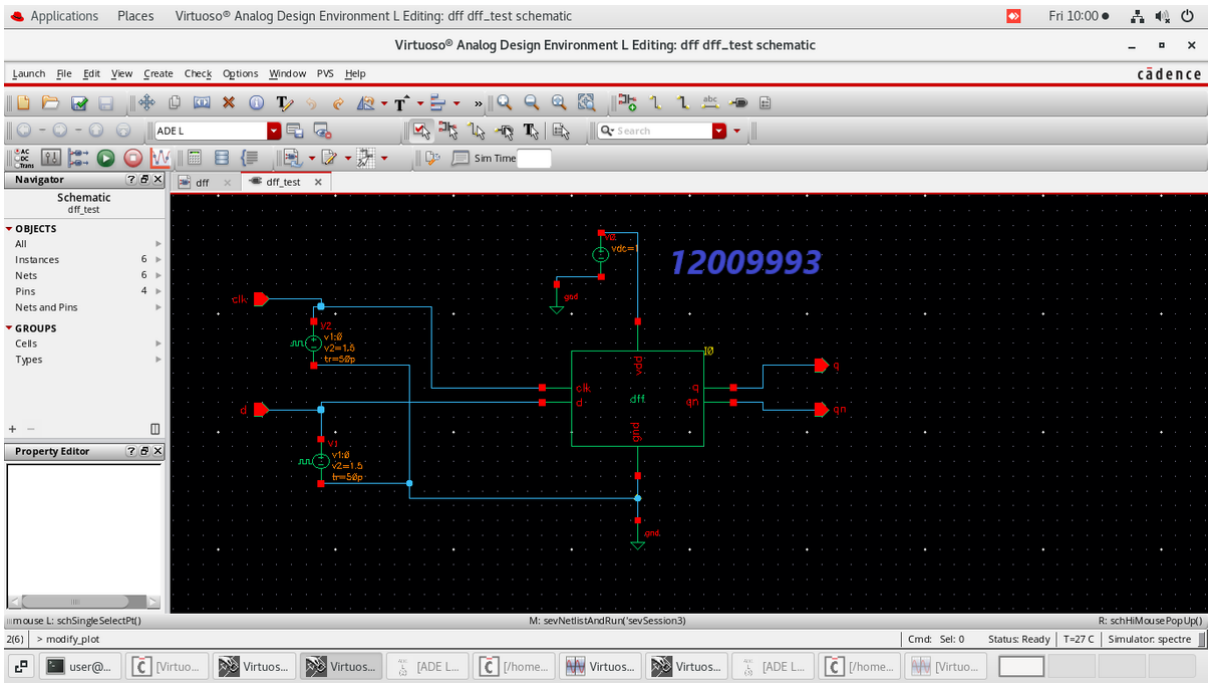
Schematics from cadence virtuoso





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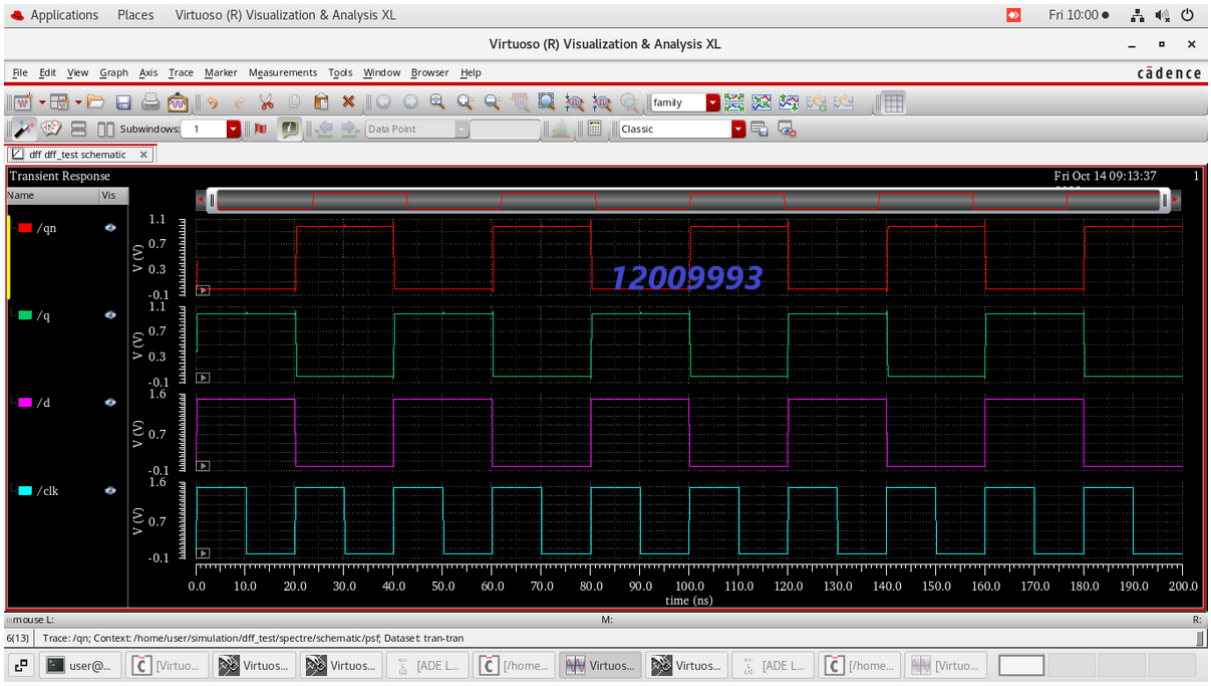

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→ Learning Outcomes :-

* we have learned about the implementation of logic gates in CMOS technology.
* working of D-flip flops and Actuall functionalities in flipflops.
* Usage of PMOS & NMOS as pull-up and pull-down networks in CMOS technology.
* Implementation of D-flipflop using SR flipflop.