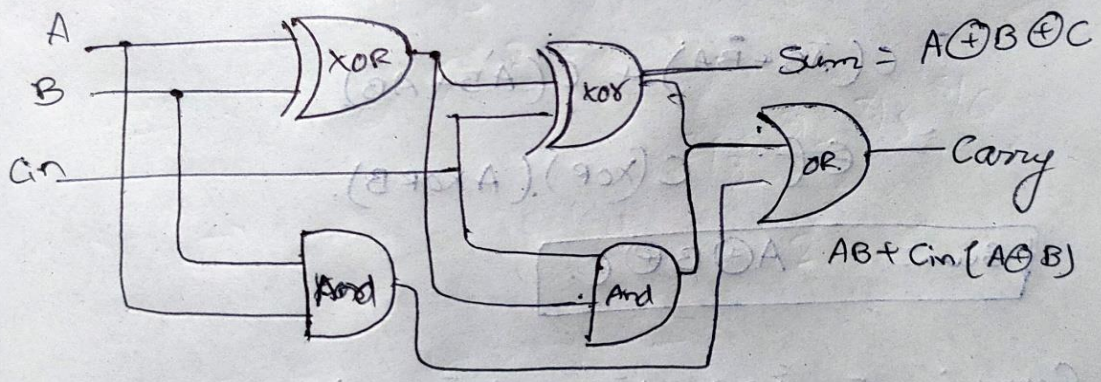
→ Aim :- Full adder using pmos & nmos using cadence virtuoso.

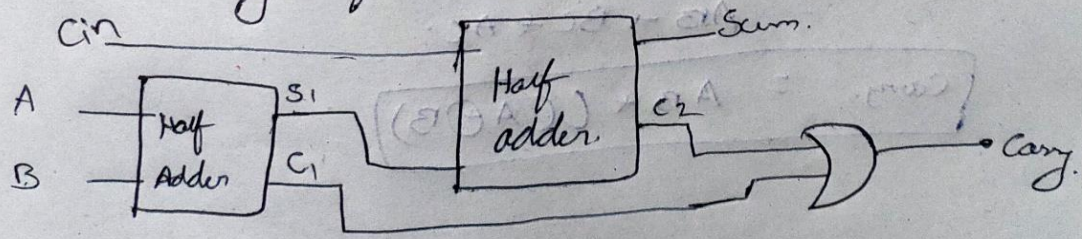
→ Introduction :-

Full adder is the adder that adds three inputs and produces two outputs. The first two inputs are A and B and the third input is C-in. The output Carry is designated as C-out and the normal o/p is designated as S which is Sum & Carry.

Logic Designs :-



Full adder using Half adder :-



Logic Table :-

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

Logical Expressions :-

$$Sum = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$= C(\bar{A}\bar{B} + \bar{B}A) + C(A\bar{B} + A\bar{B})$$

$$= C(XOR)(A XOR B).$$

$$\boxed{Sum = A \oplus B \oplus C.}$$

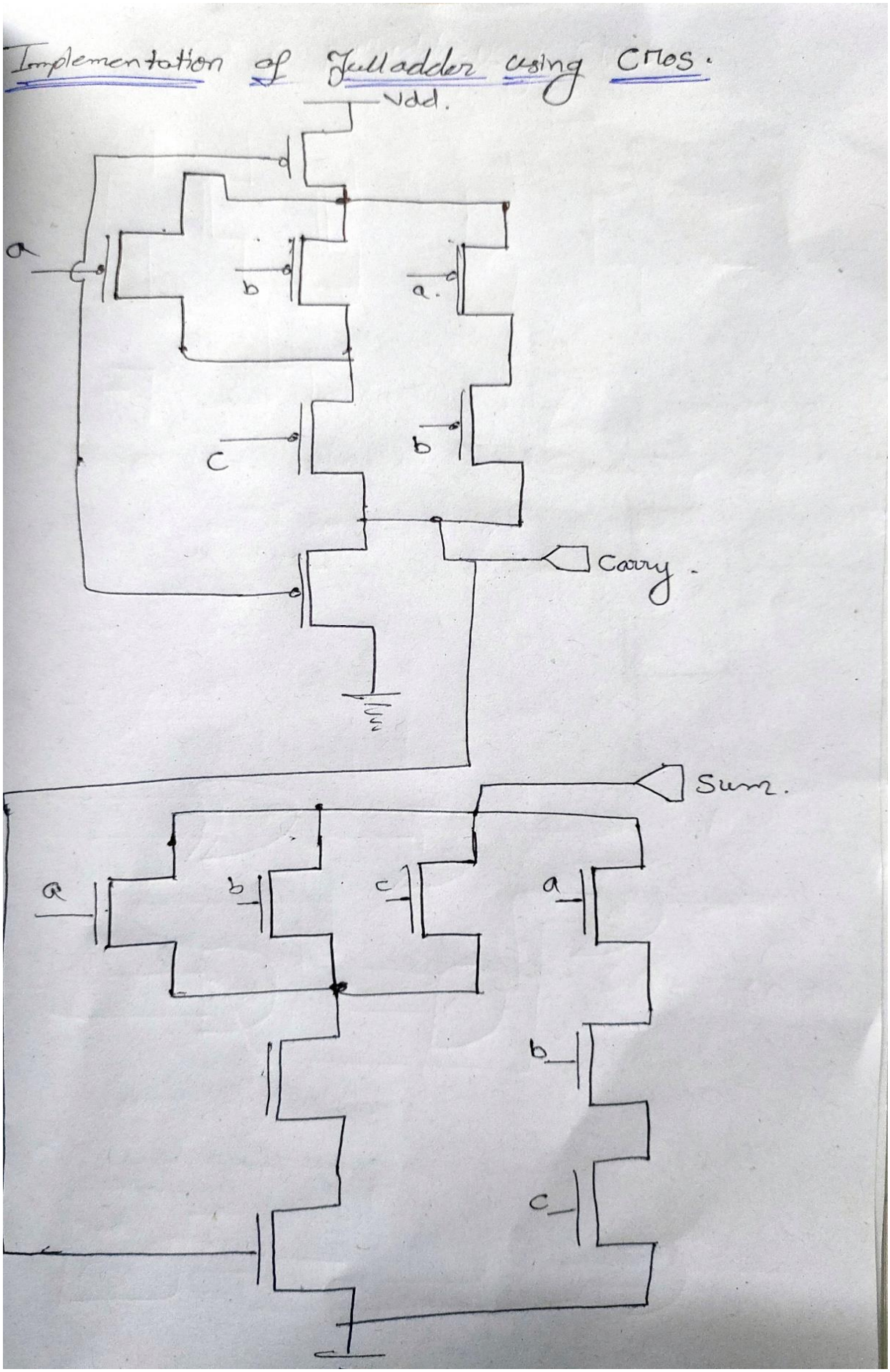
$$Carry : = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$= AB + BC + AC.$$

$$\boxed{Carry. = AB + (C(A \oplus B))}$$

12009993-sandeep

Implementation of Fulladder using CMOS.



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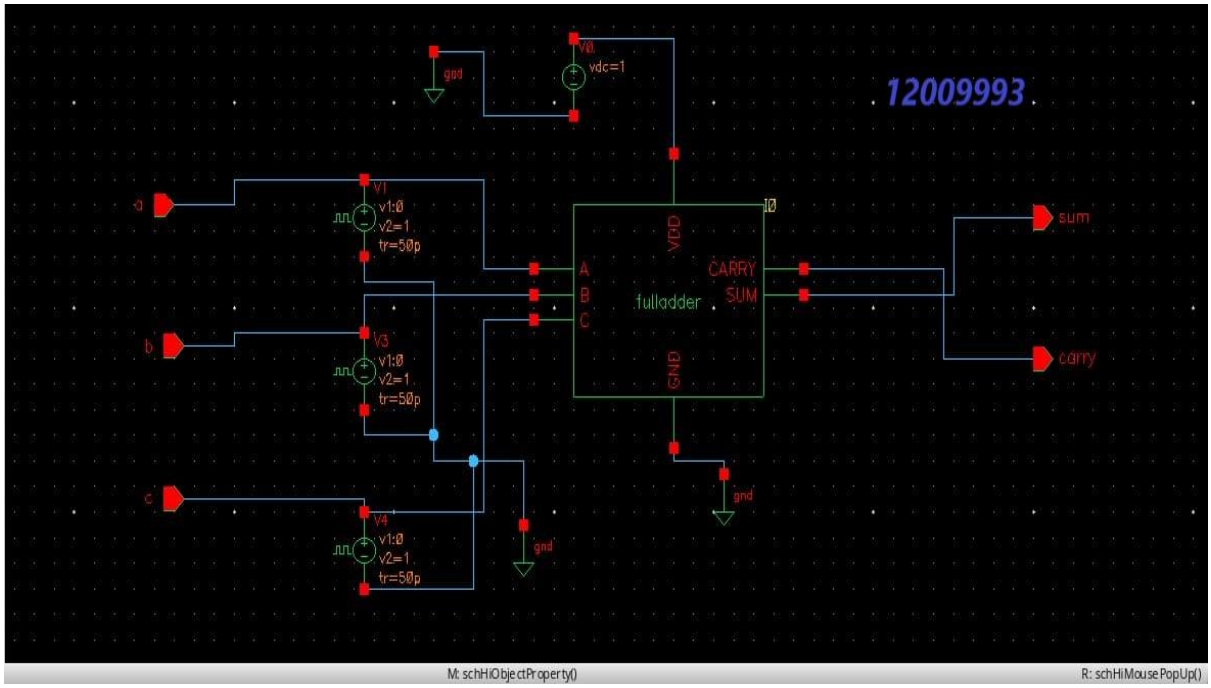
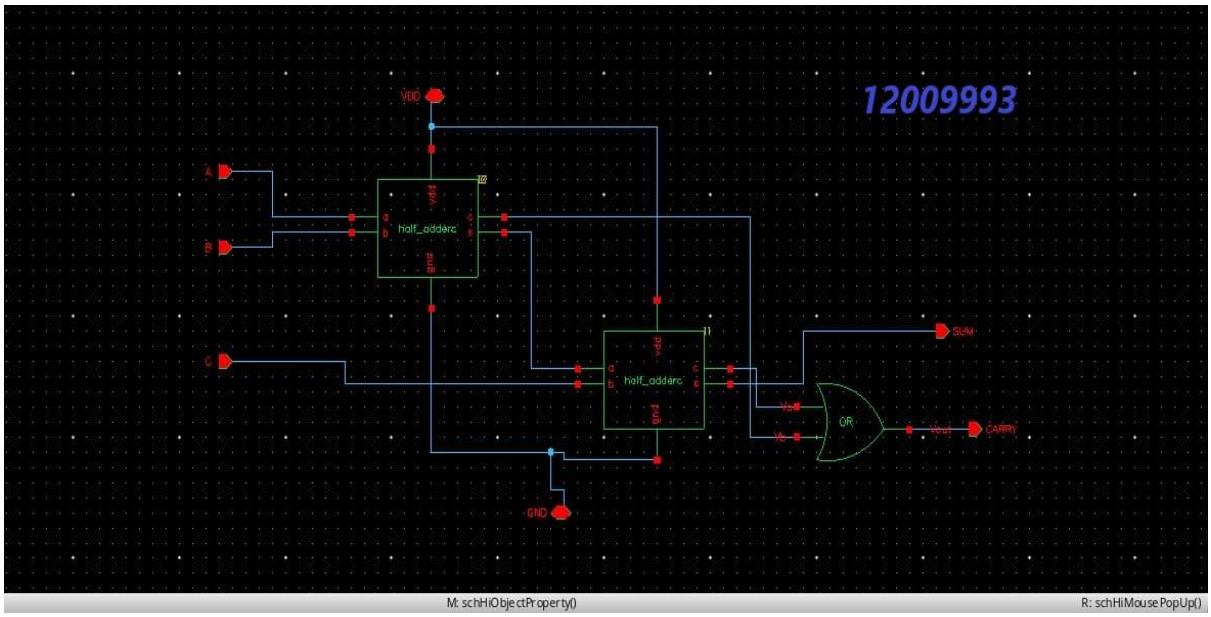
Schematics from the cadence:-





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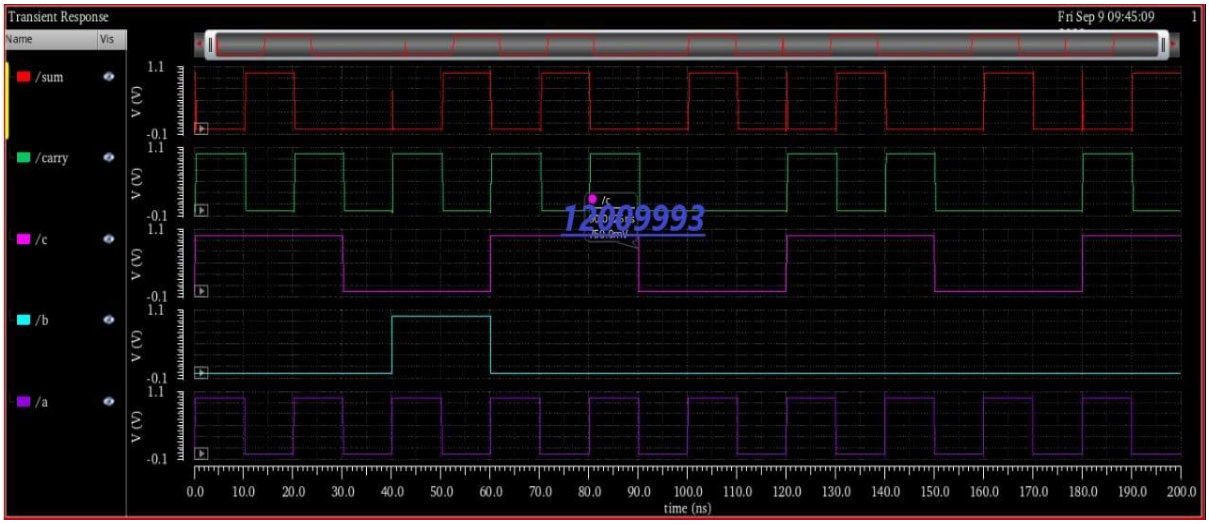
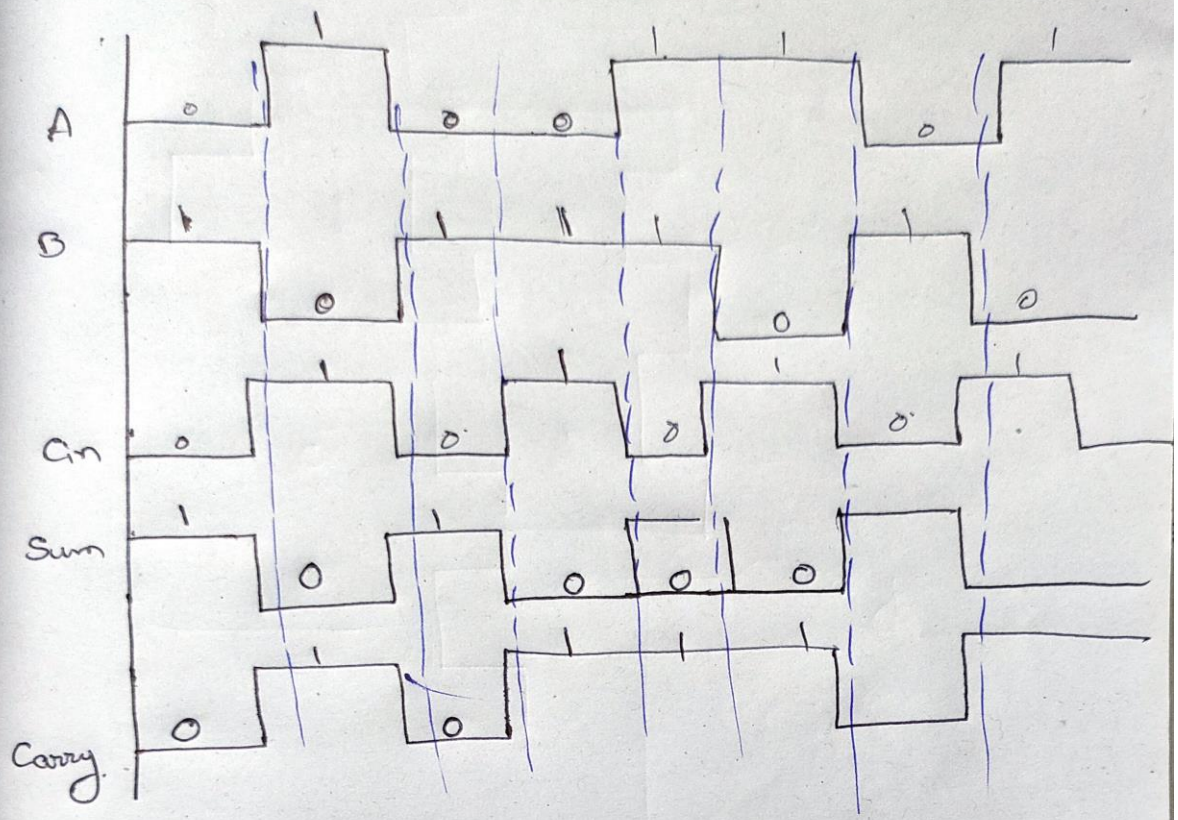

Transient Response
Fri Sep 9 09:45:09
1
Name
Vis
/sum
/carry
/c
/b
/a
1.1
-0.1
(V)
12009993
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0
160.0
170.0
180.0
190.0
200.0
time (ns)

→ Results / observations :-



→ Learning Outcomes :-

* we have understood that how to implement a logic with CMOS.
* Usage of PMOS & NMOS as a pull-up and pulldown network.
* Logical behaviour of Fulladder is known.
* Designing of Fulladder using Half adders.

Applications :-

* used in ALU operations.
* Used in Calculators.
* Used in various Digital Electronics circuits.

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