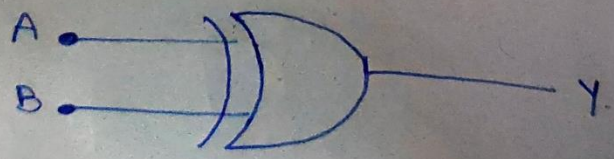
Aim:- Implementation of EX-OR and EX-NOR gates using CMOS in Cadence Virtuos

XOR- Gate:-

The Exclusive-OR gate is achelved by Combining standard logic gates togethex. XOR gate is used extensively in error detection circuits, Computational logic comparators and Arithmetic logic circuits. The Exclusive-OR gat gives an output only if two inputs are dissimilar, namely if one of them is high and the other is low (zero).



$Y = A \oplus B$

$Y = A\bar{B} + \bar{A}B$

12009993-sandeep

Truth Table :-

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

XOR gate using CMOS :-

$Y = \bar{A}B + A\bar{B}$

For (·) operation.

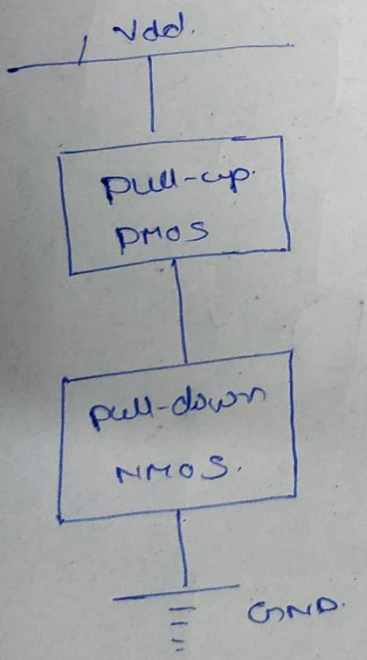
NMOS – series.

PMOS – parallel.

For (+) operation.

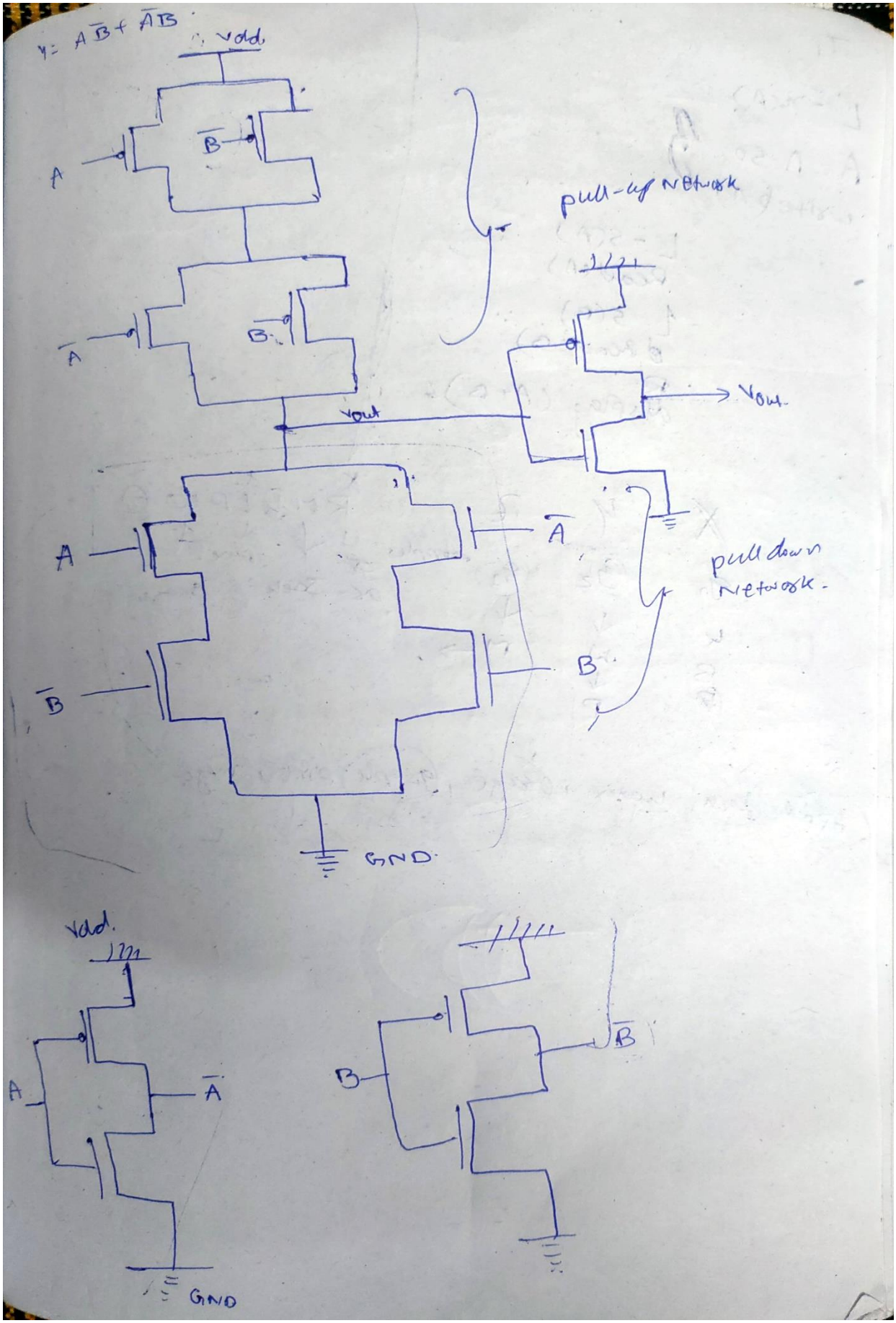
NMOS – parallel.

PMOS – series.

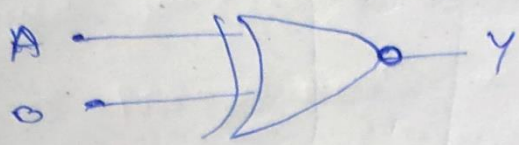


Total no of NMOS – 7.

Total no of PMOS – 7.


Y = AB̄ + ĀB
Vdd
A
B̄
Ā
B
pull-up Network
Vout
vout
A
B̄
Ā
B
pull down Network
GND
Vdd
A
Ā
B
B̄
GND

FOR XNOR gate using CMOS.



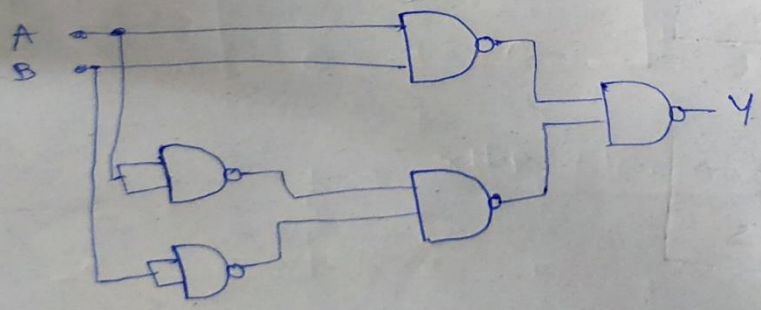
$Y = (\overline{A \oplus B})$

$Y = (\overline{A}B + A\overline{B})$.

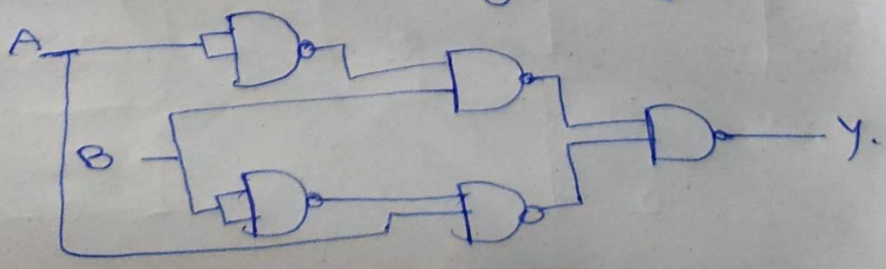
Truth Table:-

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

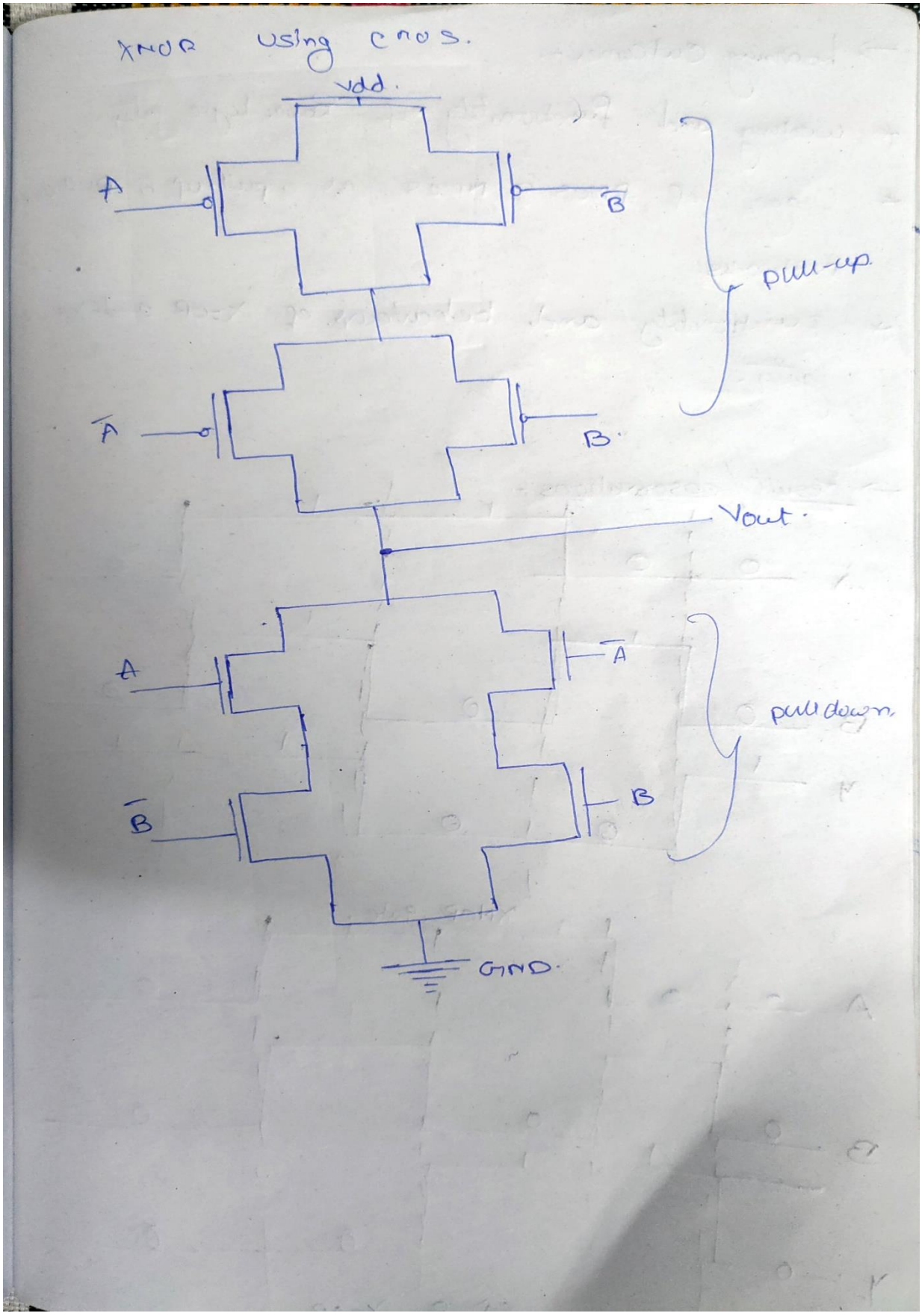
XNOR using NAND gates.



X-OR using NAND gate.



12009993-sandeep

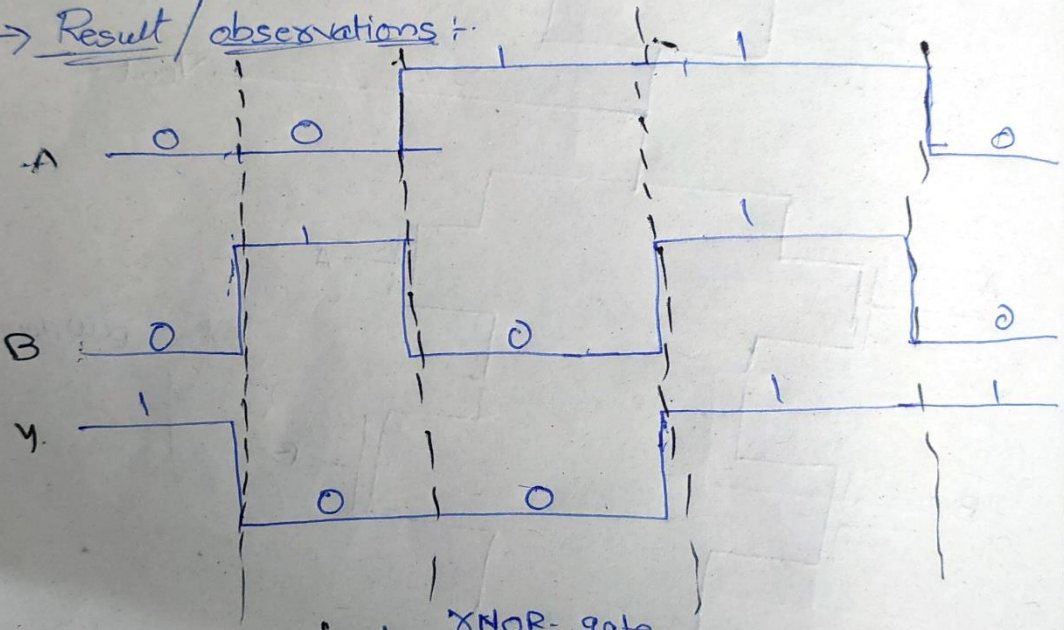


12009993-sandeep

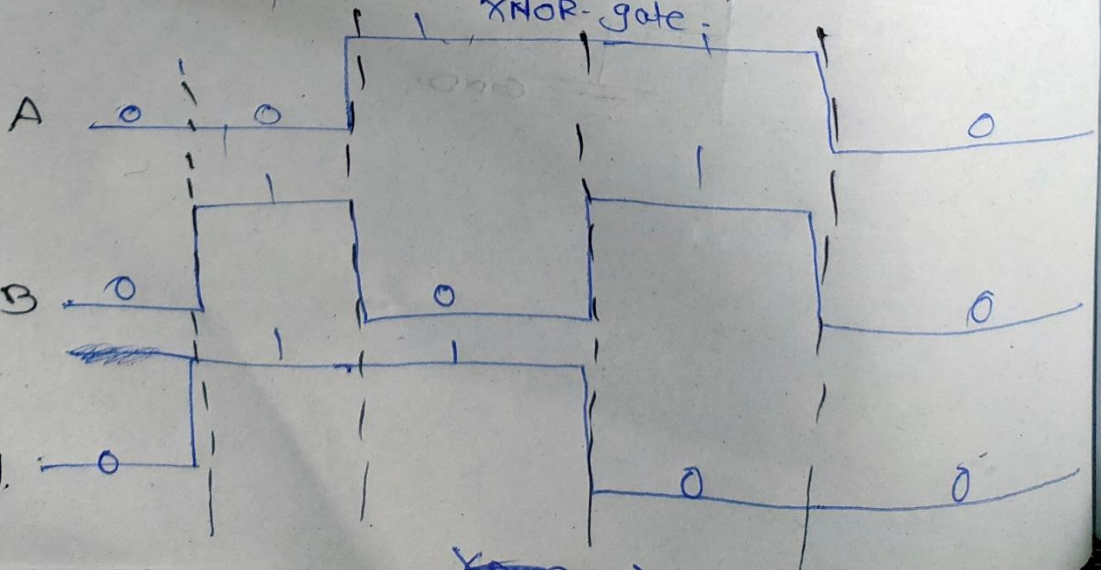
→ Learning Outcomes :-

* working and functionality of Basic Logic gates.
* Usage of PMOS & NMOS as a pull-up & pull-
  Networks.
* Functionality and behaviours of X-OR and X
  gates.

→ Result / observations :-



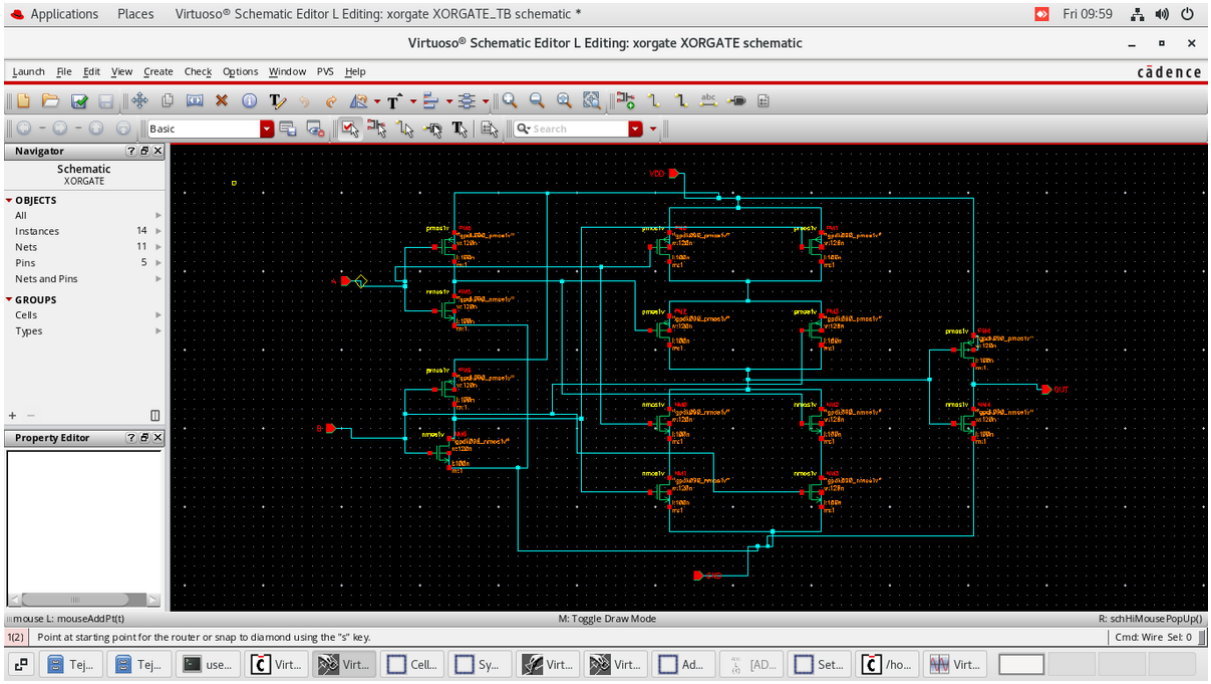
XNOR-gate :-

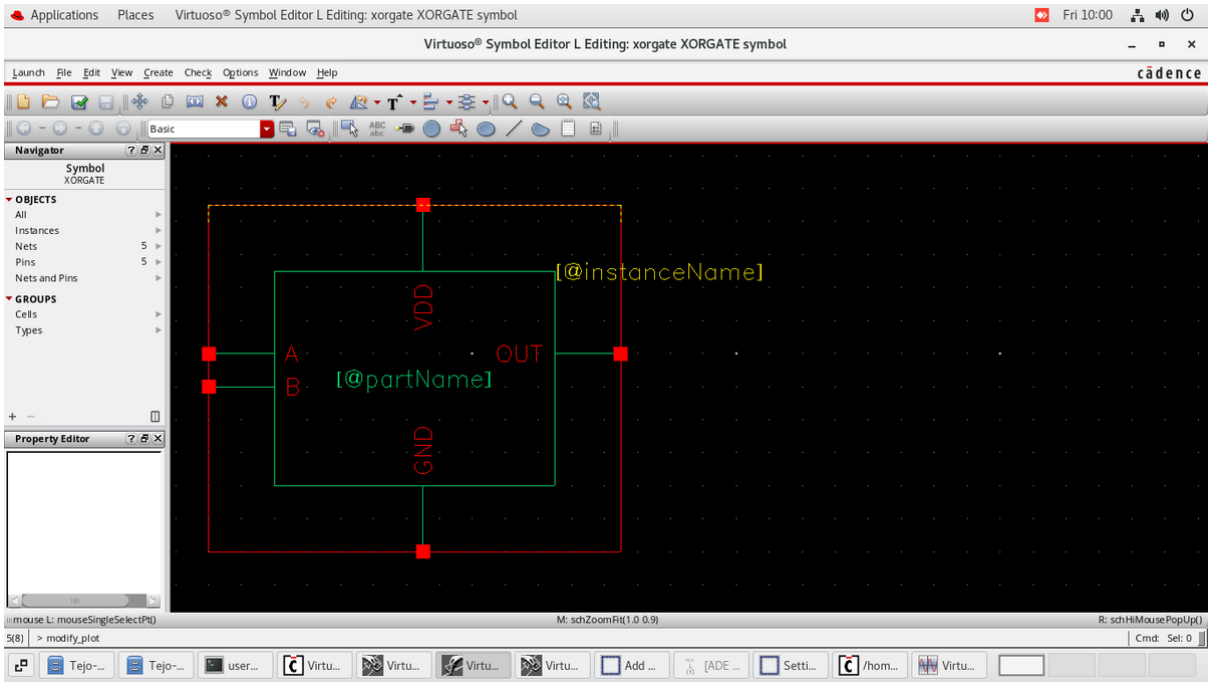


12009993-sandeep

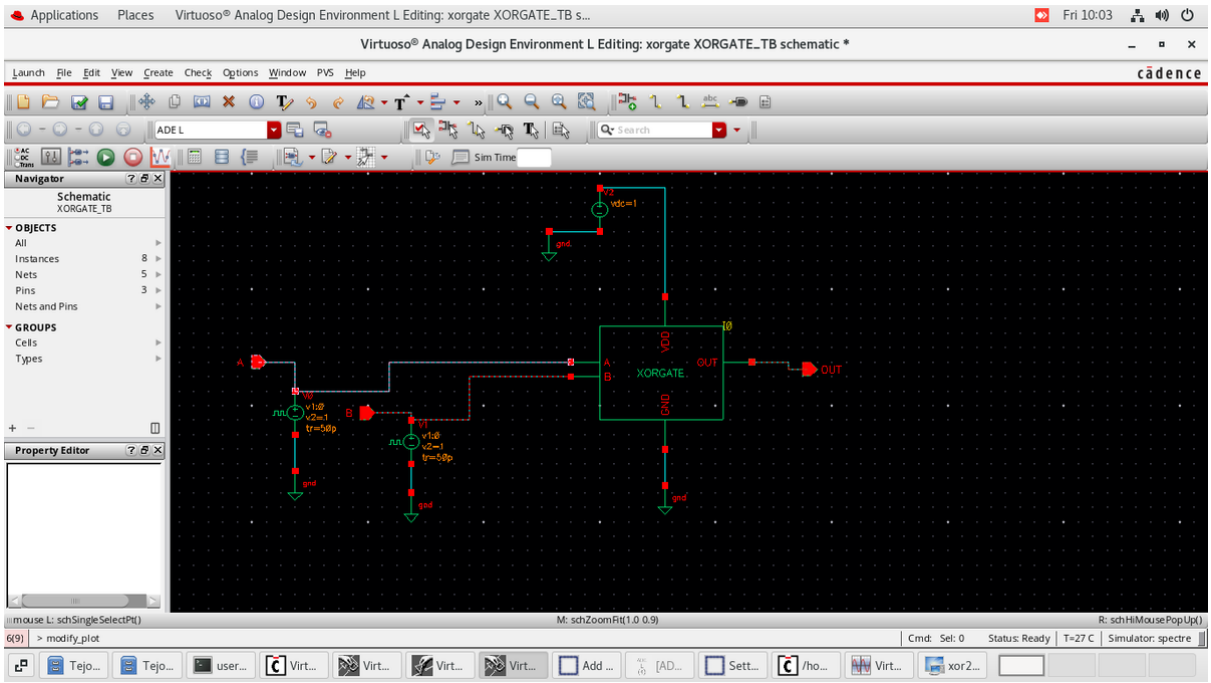
Schematics from cadence virtuoso

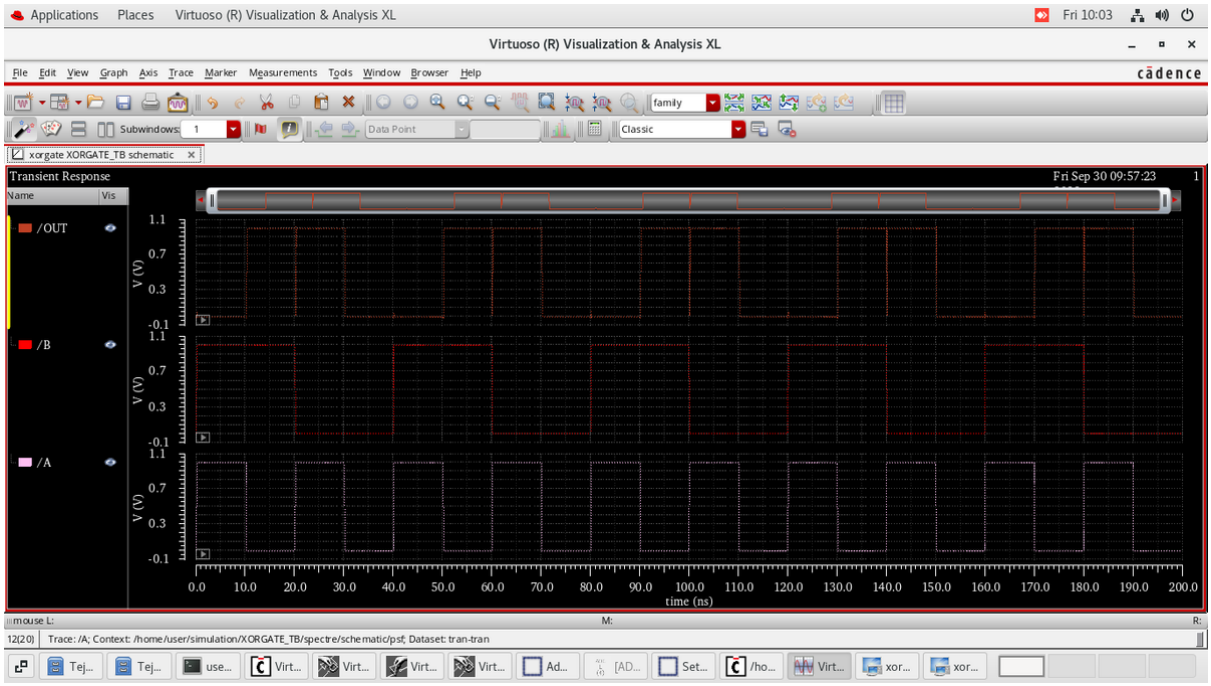
XOR Gate





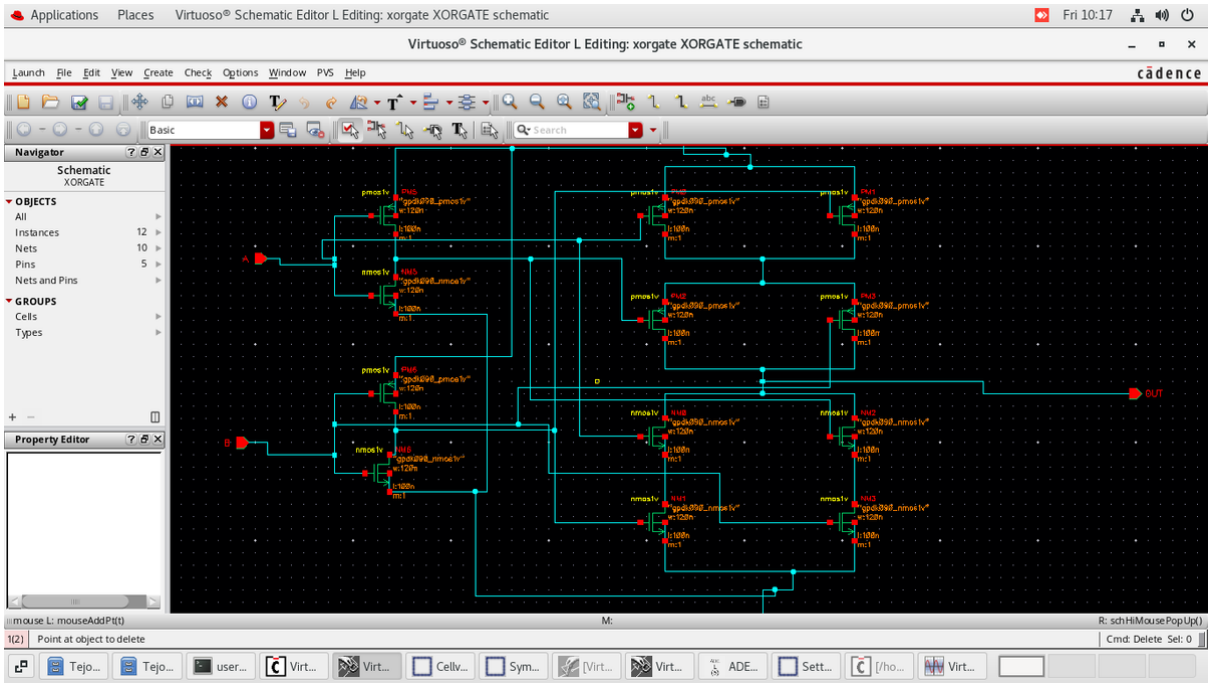
12009993-sandeep

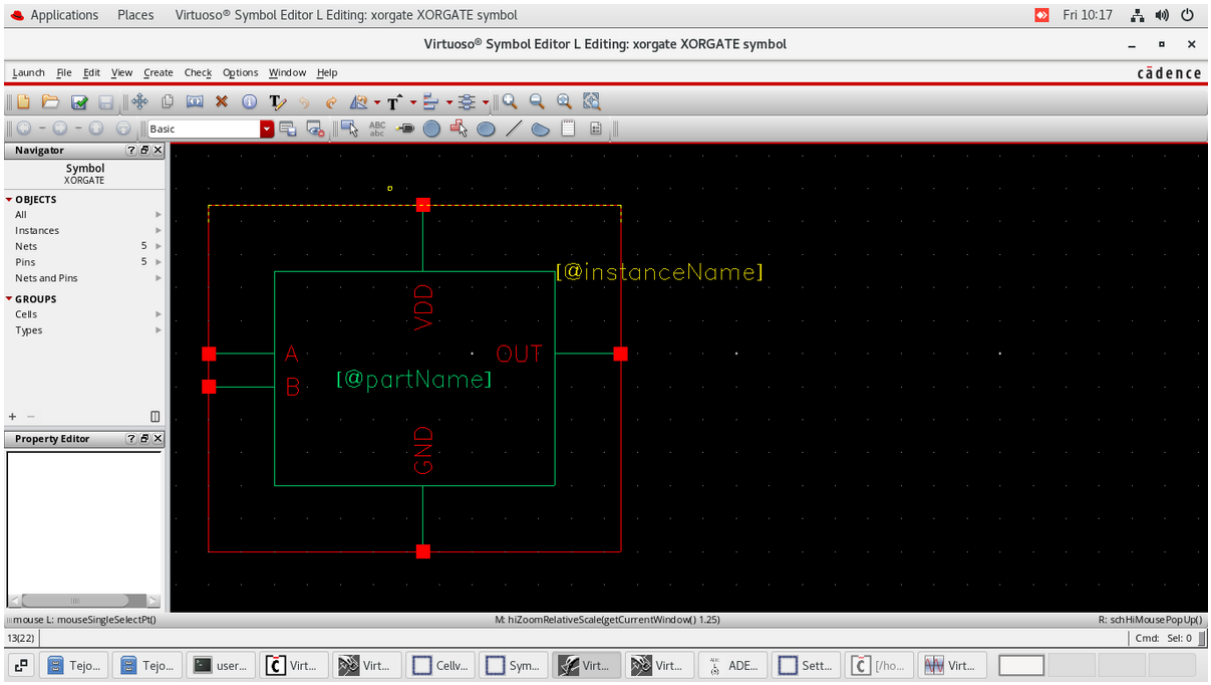




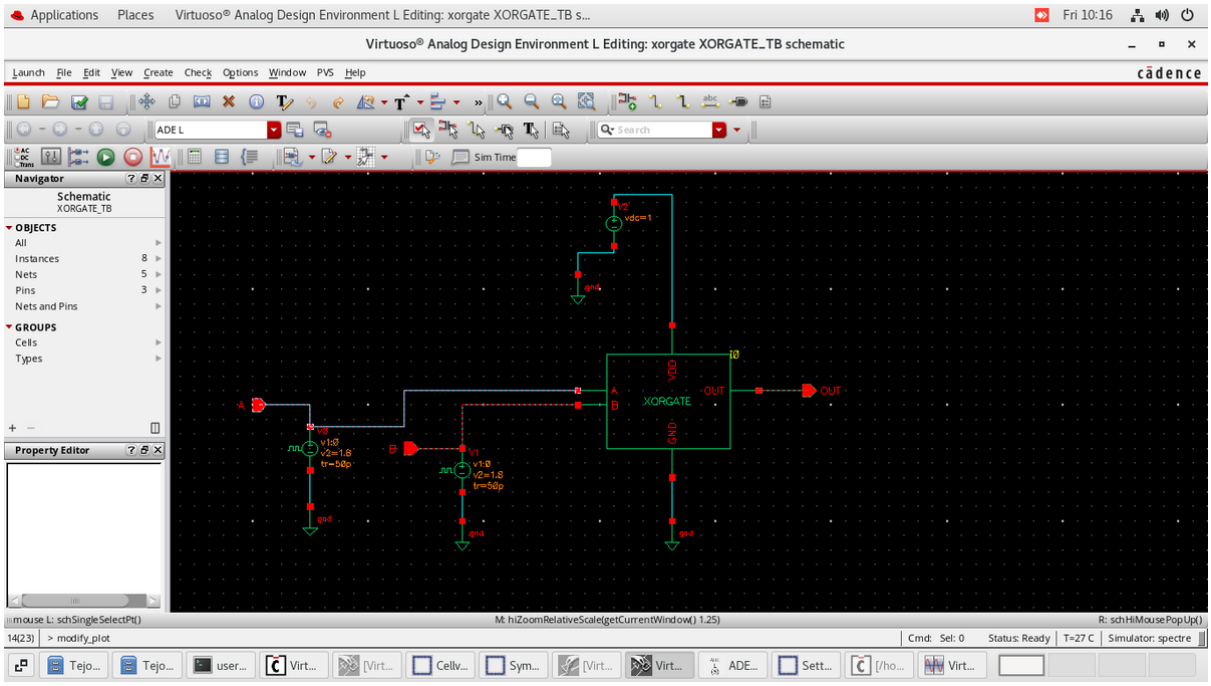
12009993-sandeep

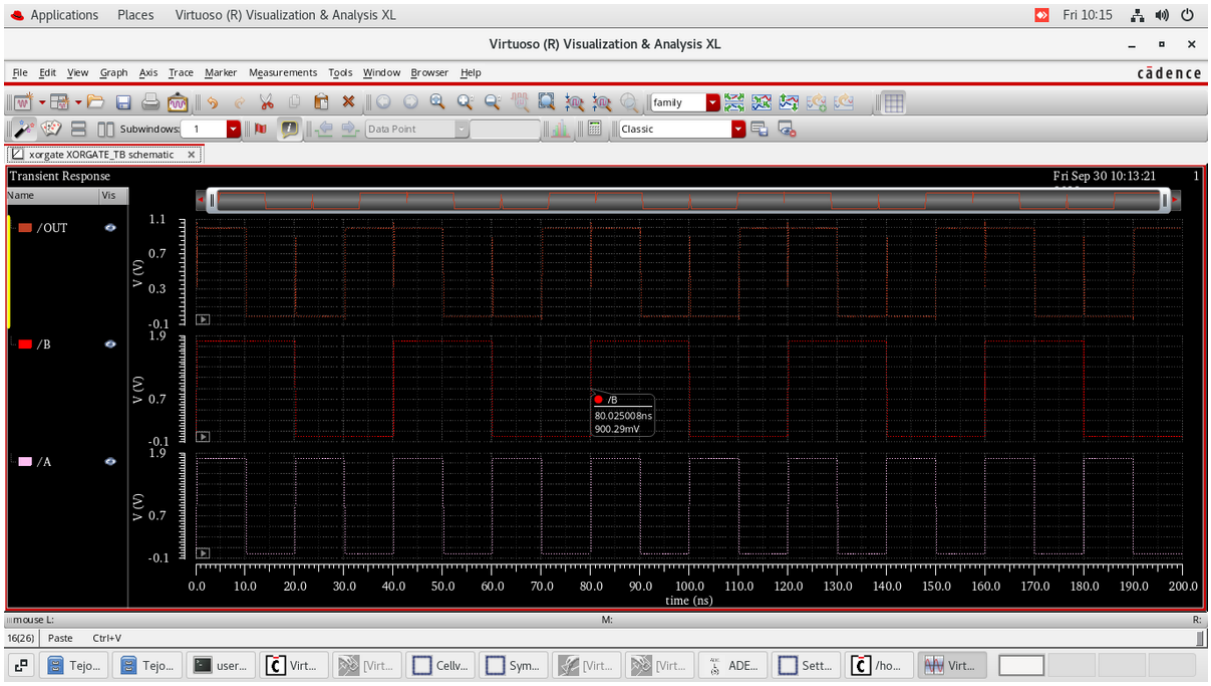
Xnor





12009993-sandeep





12009993-sandeep