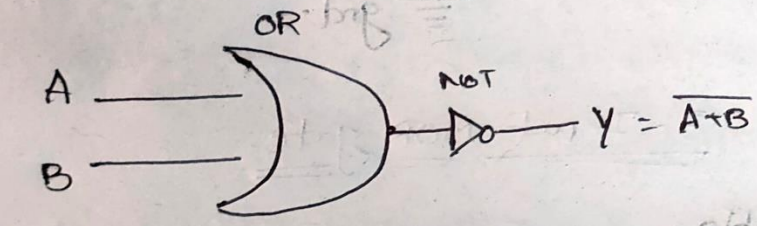
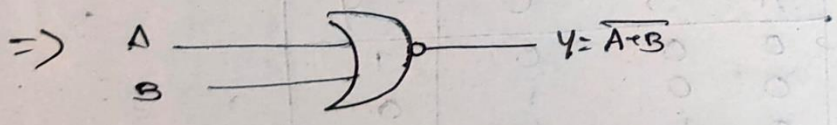
Aim :- NOR Gate using PMOS & NMOS using Cadence Virtuoso.

Introduction :-

A NOR gate is a logic gate that produces a high output (1) only if all its inputs are false, and low output. Hence the NOR gate is the inverse of an OR gate, and its circuit is provided by Connecting an OR gate to a NOT gate.

A NOT gate followed by an OR gate makes a NOR gate.



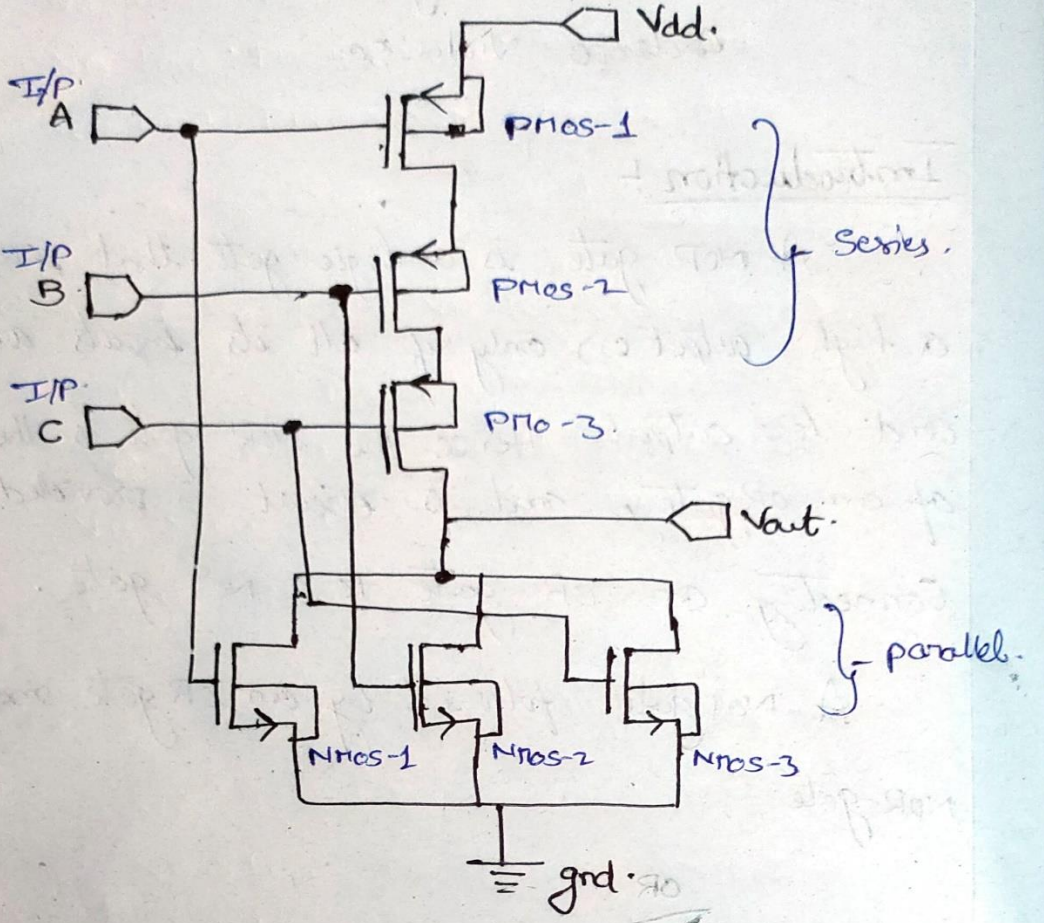


NOT gate.

Logic Table :-

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

NOR gate using CMOS



3-Input NOR gate.

Logic-Table.

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

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Case:1 (V_A = Low & V_B = Low & V_C = Low).

V_A - Low ; PMOS1 → ON ; nmos1 - OFF

V_B - Low ; PMOS2 → ON ; nMOS2 - OFF.

V_C - Low ; PMOS3 → ON ; nmos3 - OFF.

There is no Discharging so [Vout = High]

Case:2 (V_A = Low & V_B = Low & V_C = High);

V_A → Low ; PMOS1 - ON ; nMOS1 → OFF ;

V_B → High ; PMOS2 - OFF ; nMOS2 → ON ;

V_B → Low ; PMOS3 - ON ; nMOS3 → OFF ;

[Vout = Low].

Case:3 : (V_A = High & V_B - Low & V_C - Low);

V_A → High ; PMOS1 - OFF ; nmos1 → ON ;

V_B → Low ; PMOS2 - ON ; nmos2 → OFF ;

V_C → Low ; PMOS3 - ON ; nmos3 → OFF ;

[Vout = Low.]

Case:4 (V_A = Low & V_B = High & V_C = Low);

V_A → Low ; PMOS1 - ON ; NMOS1 - OFF

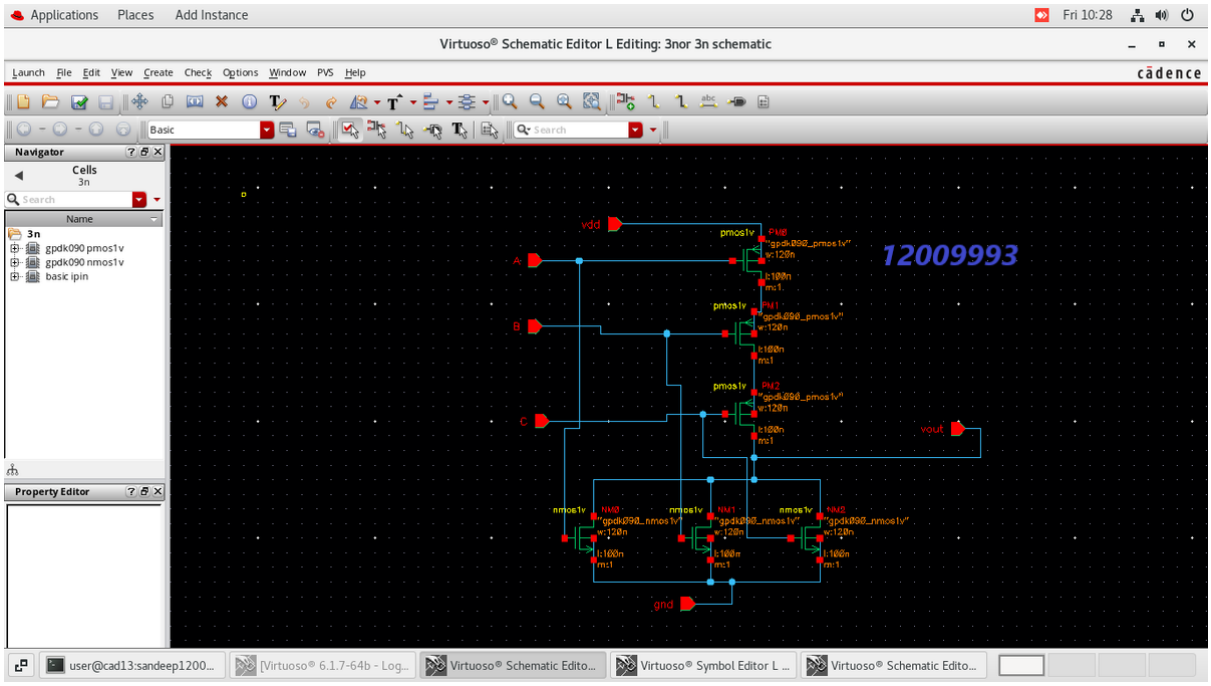
V_B → High ; PMOS2 - OFF ; NMOS2 - ON

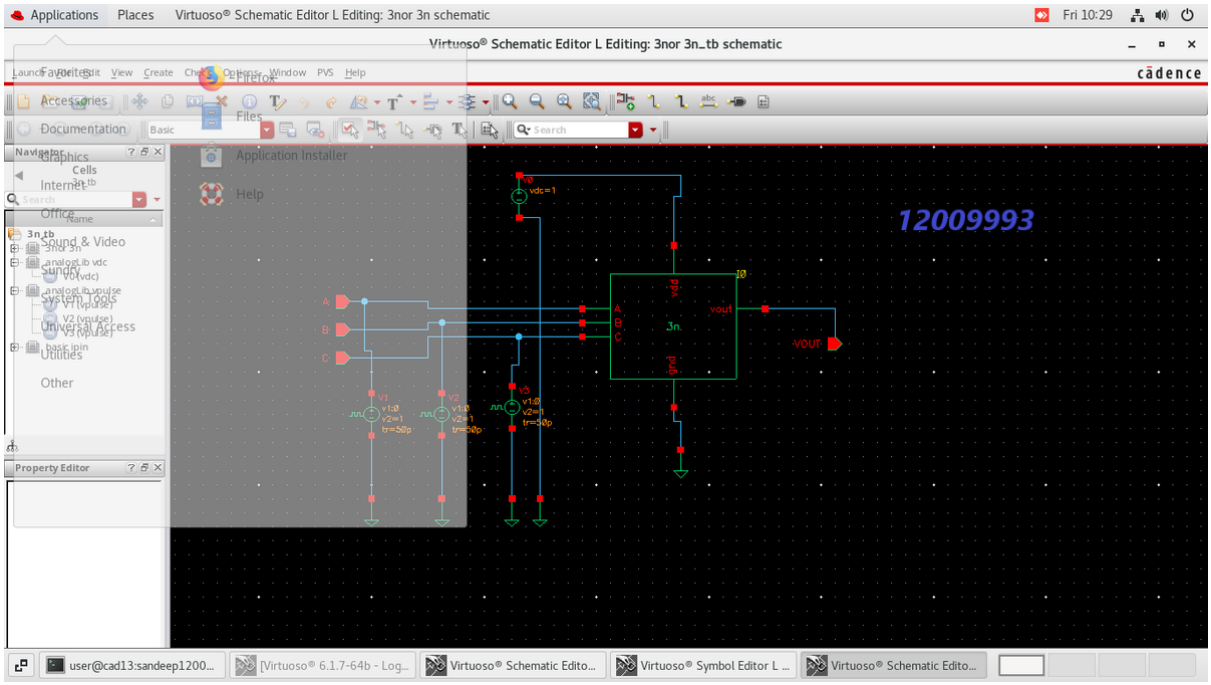
V_C → Low ; PMOS3 - ON ; NMOS3 - OFF.

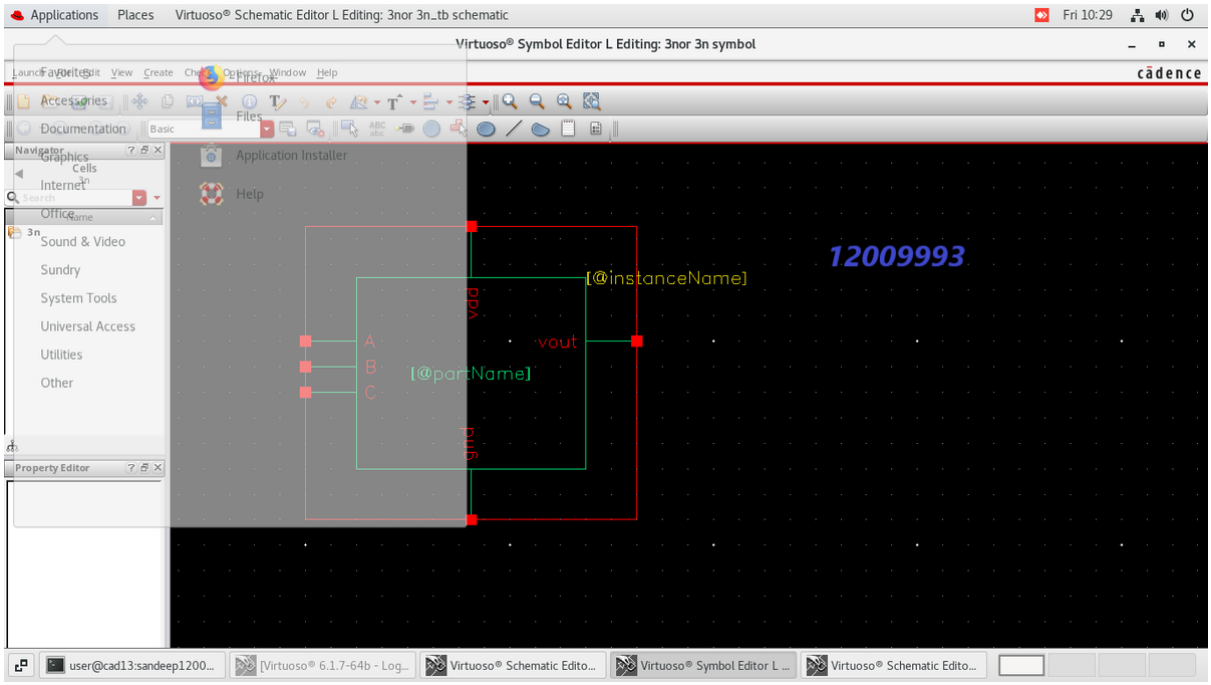
[Vout = Low.]

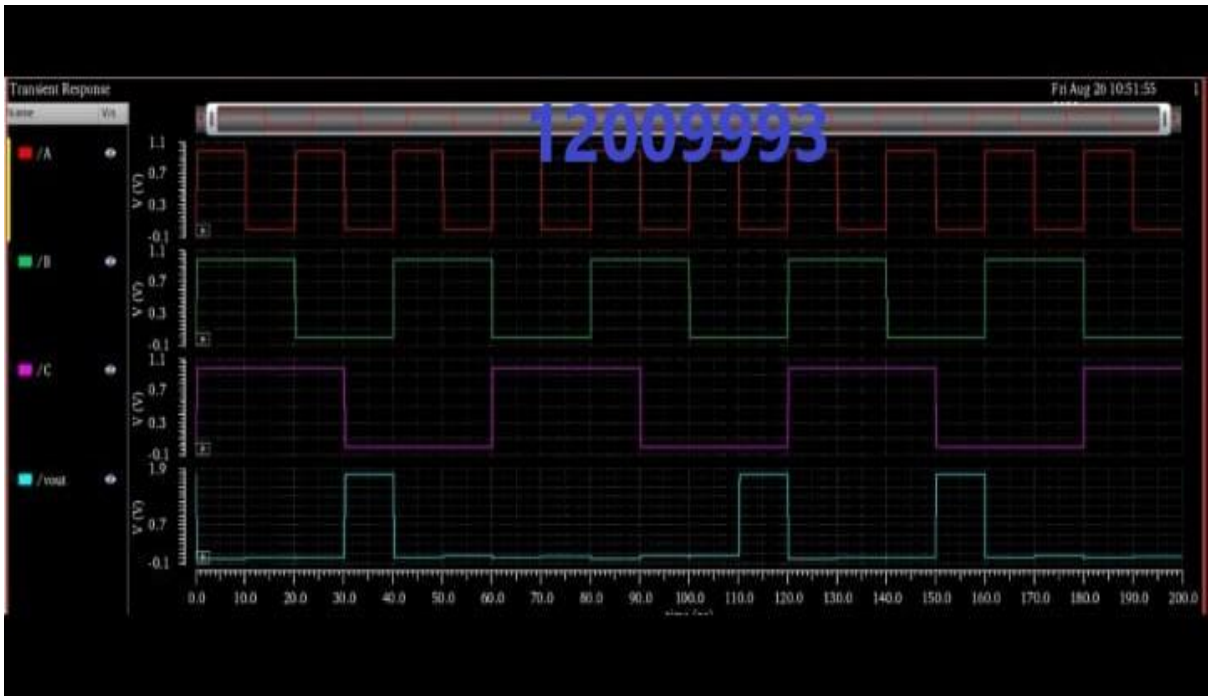
In the Similar way all the Combinations are satisfied. Vout = High only when All the inputs are Low (0); otherwise, it is Low.

Schematics from the cadence:-









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→ Learning outcomes :-

* working and functionality of OR Gate & NOR Gate.
* Usage of PMOS & NMOS and its workings.
* Functionality wave form of NOR Gate.
* Hands-on Experience with Cadence-Virtuoso Simulation Tool.

→ Results & observations :-