RTL CHALLENGE

DAY – 13 :- Today I Practiced Some problems based on Modules.

Website used:- HDL BITS

Problem Statement:-

This instantiates a module of type mod_a then Connects Module 3 pins (in1, in2, and out) to your top level module 3 ports (wire a, b, and out).

Write your solution here

[Load a previous submission] Load

```
1 module top_module ( input a, input b, output out );
2     mod_a (.in1(a),.in2(b),.out(out));
3 endmodule
4
```

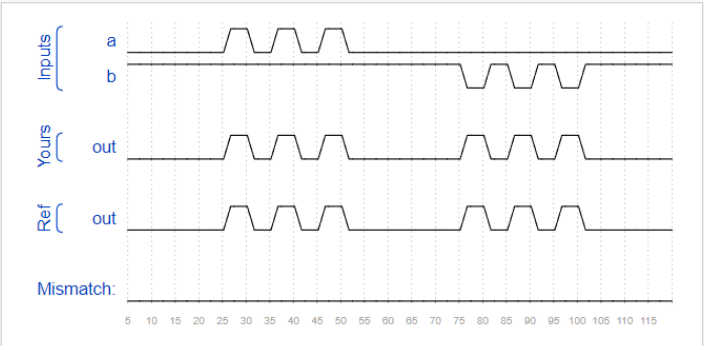
Submit | Submit (new window)

Status: Success!

You have solved 2 problems. See my progress...

Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).



RTL CHALLENGE

Problem Statement:-

This problem is similar to the previous one. You are given a module named mod_a that has 2 outputs and 4 inputs, in that order. You must connect the 6 ports *by position* to your top-level module's ports out1, out2, a, b, c, and d, in that order.

You are given the following module:

module mod_a (output, output, input, input, input, input);

Write your solution here

[Load a previous submission] Load

```
1  module top_module (
2      input a,
3      input b,
4      input c,
5      input d,
6      output out1,
7      output out2
8  );
9       mod_a (out1,out2,a,b,c,d);
10 endmodule
11
```

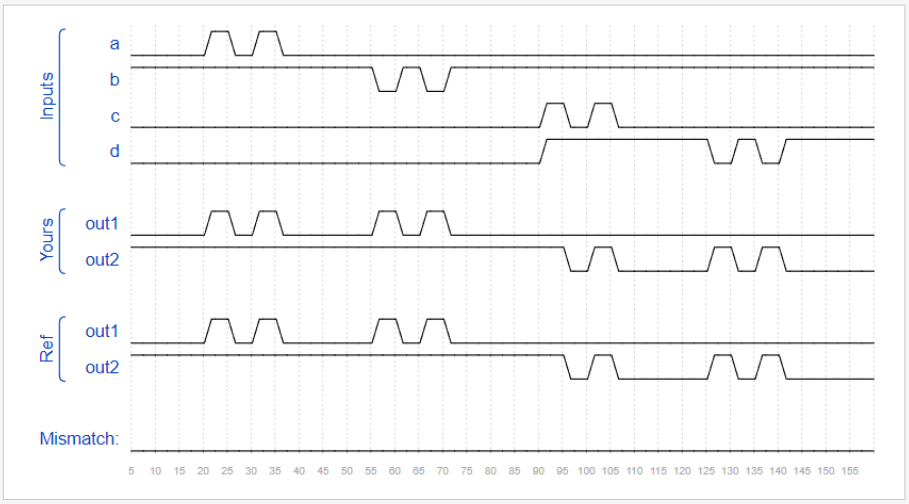
Submit | Submit (new window)

Status: Success!

You have solved 2 problems. See my progress...

Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).



RTL CHALLENGE

Problem Statement:-

This problem is similar to previous one . You are given a module named mod_a that has 2 outputs and 4 inputs, in some order. You must connect the 6 ports *by name* to your top-level module's ports:

module mod_a (output out1, output out2, input in1, input in2, input in3, input in4);

Write your solution here

[Load a previous submission] Load

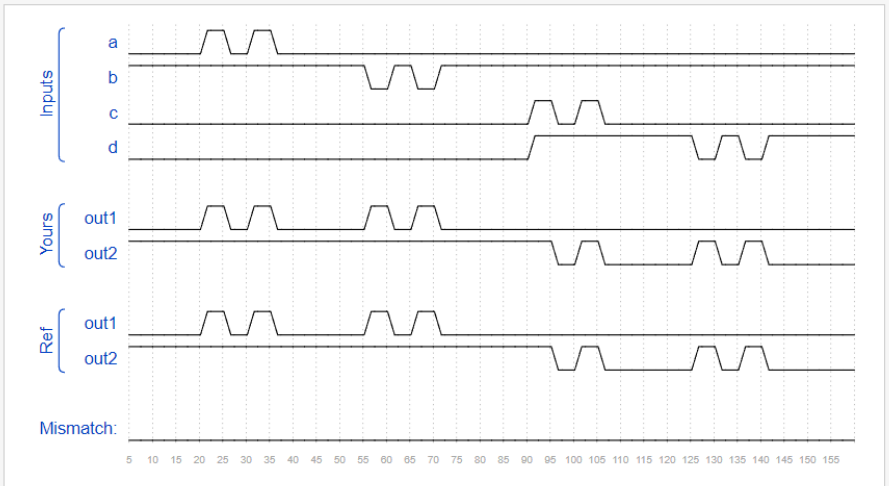
```
module top_module (
    input a,
    input b,
    input c,
    input d,
    output out1,
    output out2
);
    mod_a (.out1(out1),.out2(out2),.in1(a),.in2(b),.in3(c),.in4(d));
endmodule

```

Status: Success!

You have solved 3 problems. See my progress...

Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).

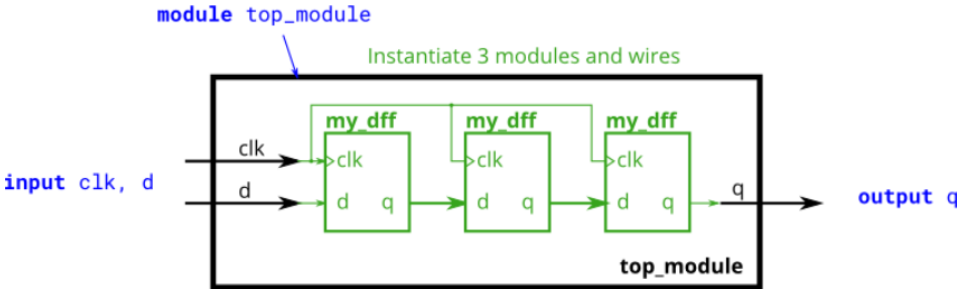


RTL CHALLENGE

Problem Statement:-

You are given a module my_dff with two inputs and one output (that implements a D flip-flop). Instantiate three of them, then chain them together to make a shift register of length 3. The clk port needs to be connected to all instances.

The module provided to you is: module my_dff (input clk, input d, output q);



Write your solution here

[Load a previous submission] Load

```
1 module top_module ( input clk, input d, output q );
2     wire w1,w2;
3     my_dff d1 (.clk(clk),.d(d),.q(w1));
4     my_dff d2 (.clk(clk),.d(w1),.q(w2));
5     my_dff d3 (.clk(clk),.d(w2),.q(q));
6 endmodule
7
```

Submit | Submit (new window)

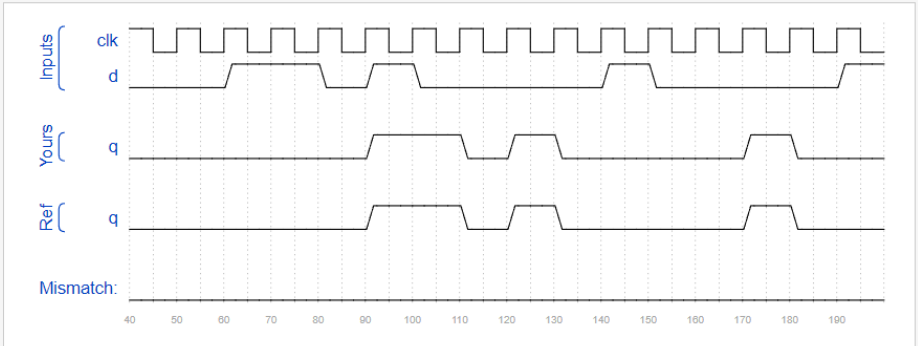
Status: Success!

You have solved 4 problems. See my progress...

Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).

Shift register



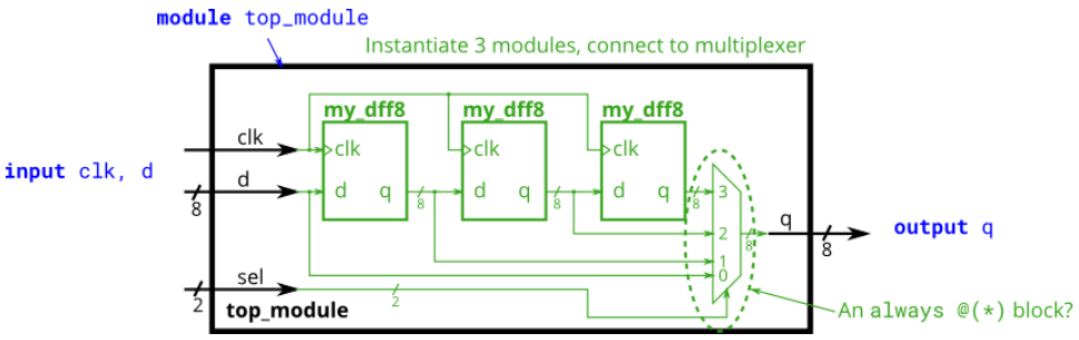
RTL CHALLENGE

Problem Statement:-

This exercise is an extension of module_shift. Instead of module ports being only single pins, we now have modules with vectors as ports, to which you will attach wire vectors instead of plain wires. Like everywhere else in Verilog, the vector length of the port does not have to match the wire connecting to it, but this will cause zero-padding or trucation of the vector. This exercise does not use connections with mismatched vector lengths.

You are given a module my_dff8 with two inputs and one output (that implements a set of 8 D flip-flops). Instantiate three of them, then chain them together to make a 8-bit wide shift register of length 3. In addition, create a 4-to-1 multiplexer (not provided) that chooses what to output depending on sel[1:0]: The value at the input d, after the first, after the second, or after the third D flip-flop.
(Essentially, sel selects how many cycles to delay the input, from zero to three clock cycles.)

The module provided to you is: module my_dff8 (input clk, input [7:0] d, output [7:0] q);



Write your solution here

[Load a previous submission] Load

```
module top_module (
    input clk,
    input [7:0] d,
    input [1:0] sel,
    output [7:0] q
);
    wire [7:0] w1,w2,w3;
    my_dff8 d1 (.clk(clk),.d(d),.q(w1));
    my_dff8 d2 (.clk(clk),.d(w1),.q(w2));
    my_dff8 d3 (.clk(clk),.d(w2),.q(w3));
    always@(*)
        begin
            case (sel)
                2'b00:q=d;
                2'b01:q=w1;
                2'b10:q=w2;
                2'b11:q=w3;
            endcase
        end
endmodule

```

Submit Submit (new window)

Status: Success!

You have solved 5 problems. See my progress...

Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).

Shift register