Department of Electronic and Telecommunication Engineering
Faculty of Engineering

University of Moratuwa

EN4021 - Advanced Digital Systems

SIMD Processor

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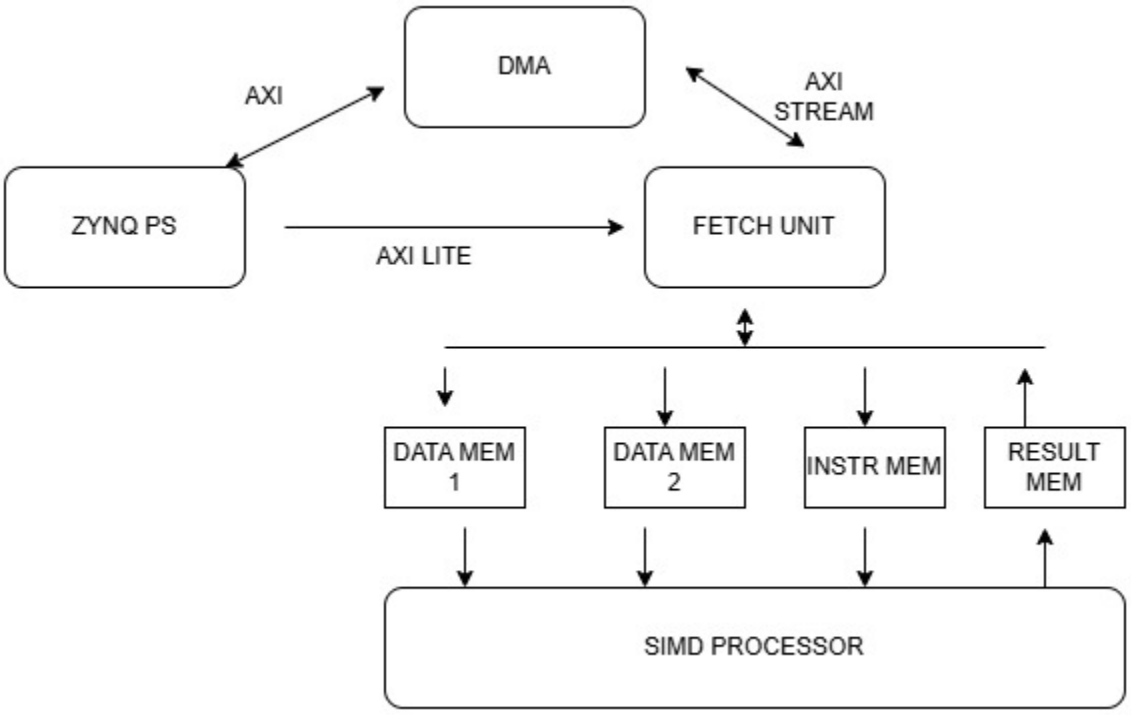
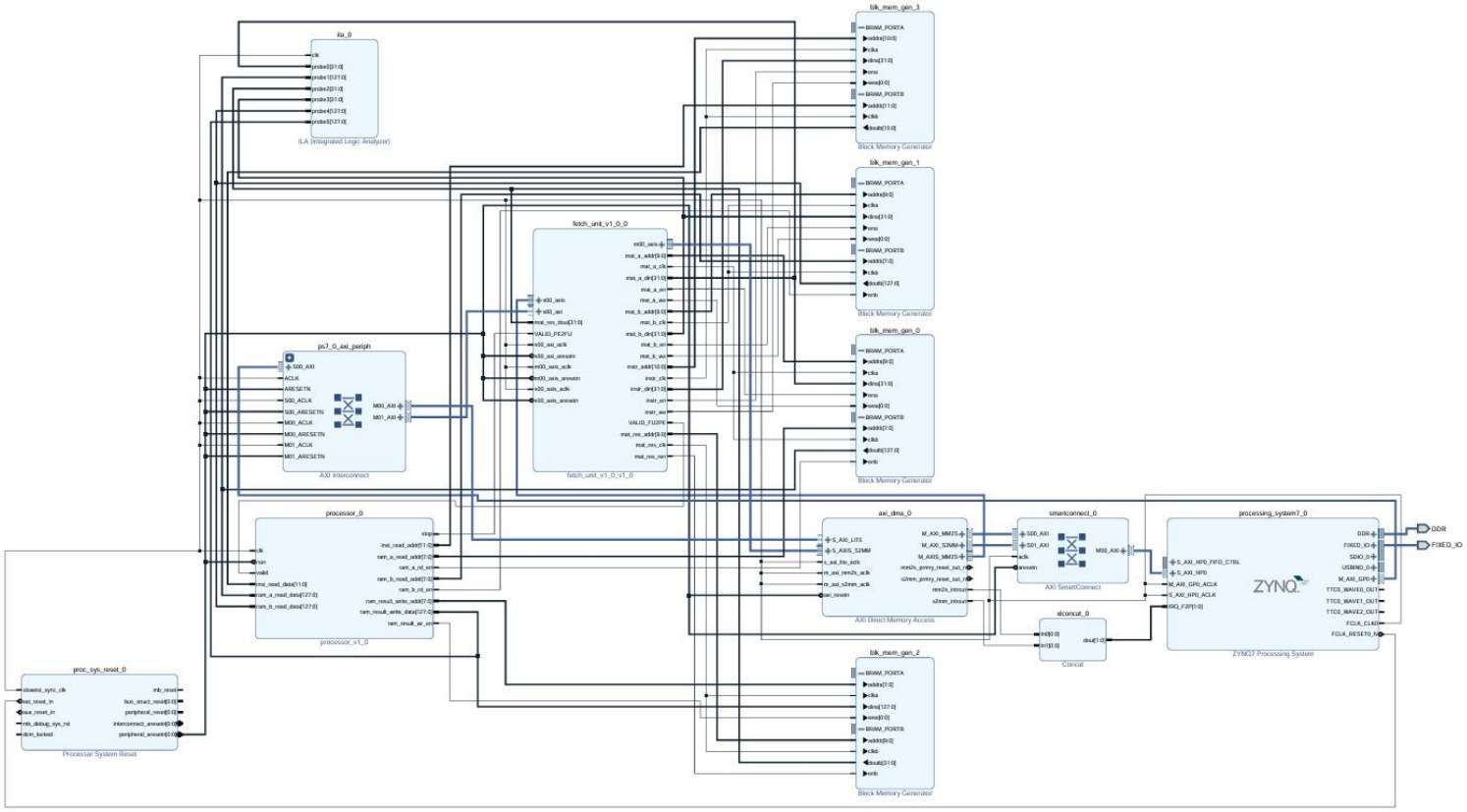
4th January 2025

Project Architecture

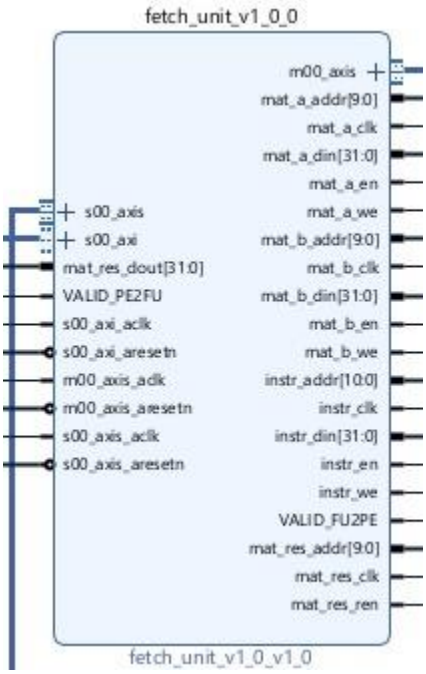


Block design



Fetch Unit

The fetch unit includes an AXI-LITE slave interface, an AXI-STREAM slave interface, and an AXI-STREAM master interface. The AXI-LITE slave interface connects directly to the master interface of the Zynq PS and is responsible for transferring control signals, such as the height and width of input matrices, to the PL side. Meanwhile, the two AXI-STREAM interfaces are linked to the DMA, facilitating data transfer from DDR to the PL side and vice versa.

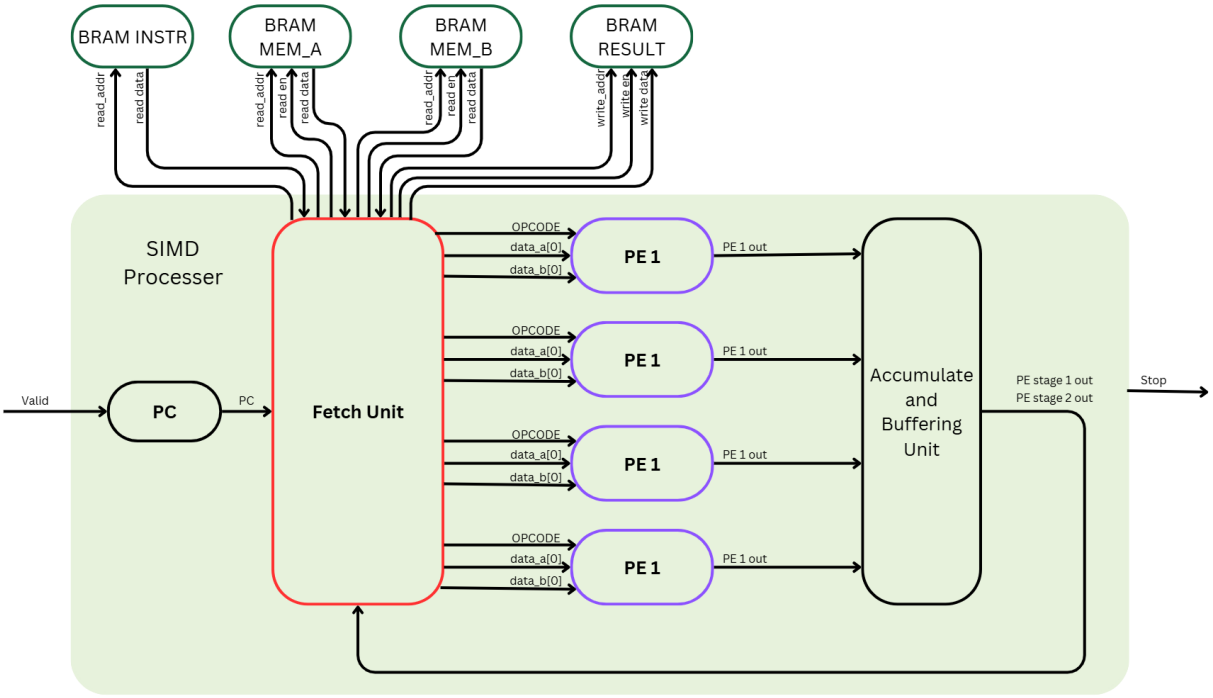


Instruction set Architecture

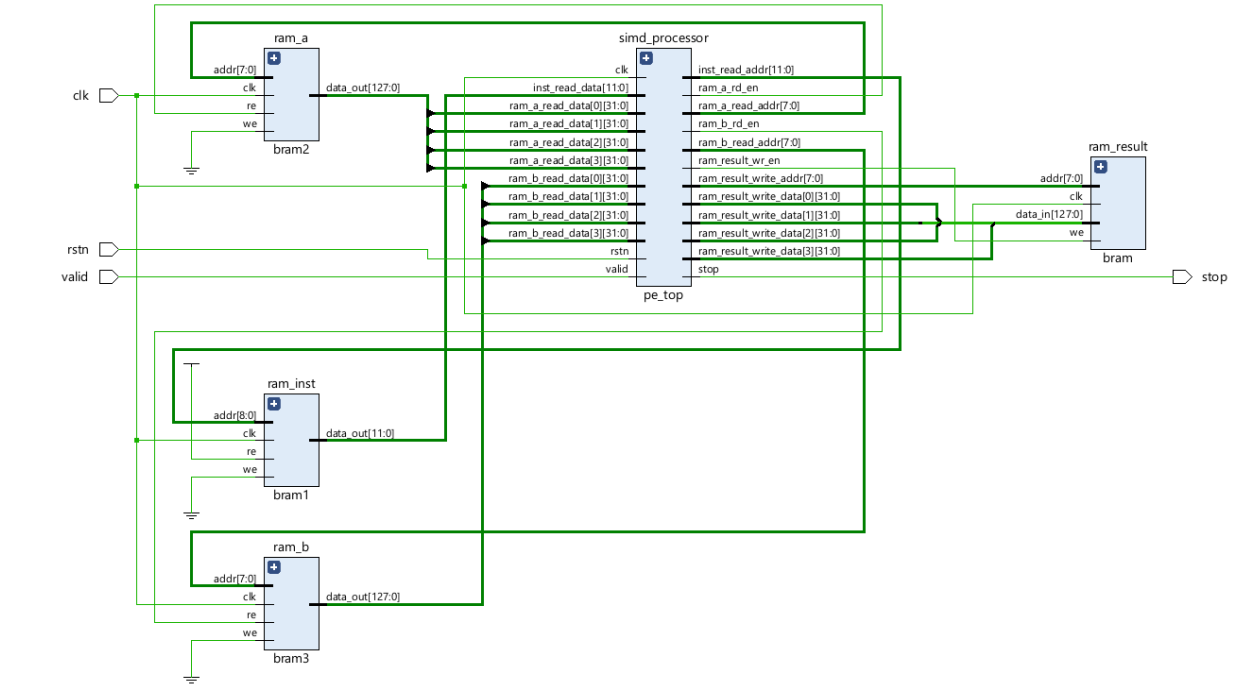
Instruction	Address (8-bit)								OPCODE (4-bit)			
NOOP									0	0	0	0
ADD									0	0	0	1
SUB									0	0	1	0
MUL									0	0	1	1
DOTP									0	1	0	0
STORE_TEMP_S1									0	1	0	1
STORE_TEMP_S2									0	1	1	0
STORE_RESULT									0	1	1	1
STOP									1	0	0	0
FETCH_A									1	0	0	1
FETCH_B									1	0	1	0

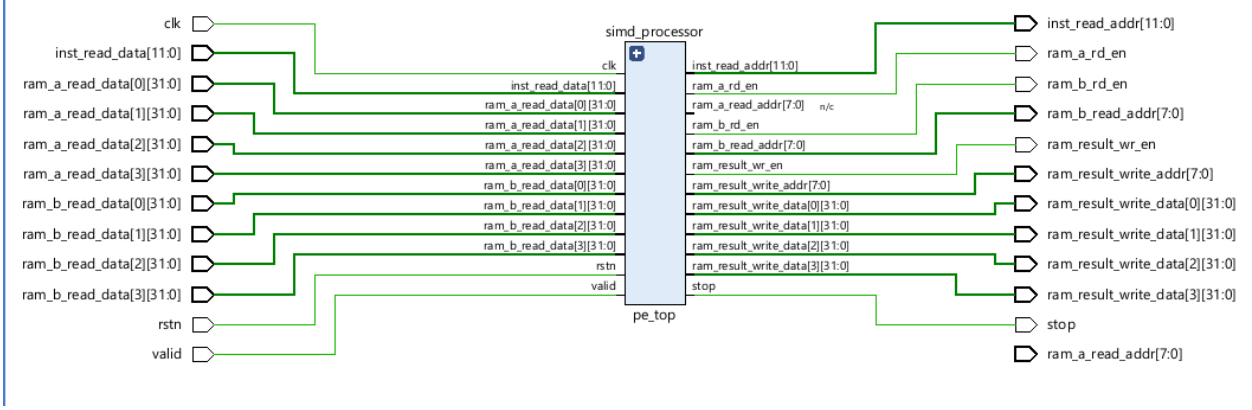
Instruction	Clock cycle
NOOP	1
ADD	3
SUB	3
MUL	4
DOTP	4
STORE_TEMP_S1	3
STORE_TEMP_S2	4
STORE_RESULT	4
STOP	2
FETCH_A	3
FETCH_B	3

SIMD Processor Architecture



Schematic



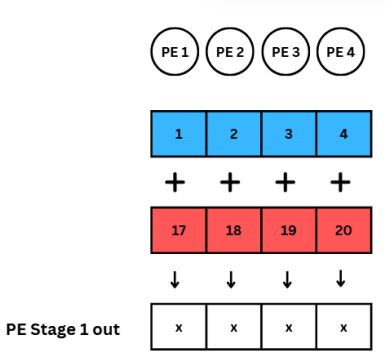


Algorithm

Addition

1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16

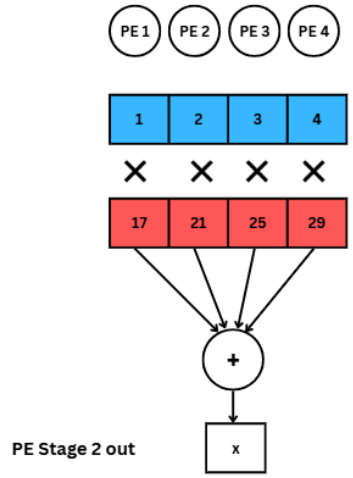
17	18	19	20
21	22	23	24
25	26	27	28
29	30	31	32



Multiplication

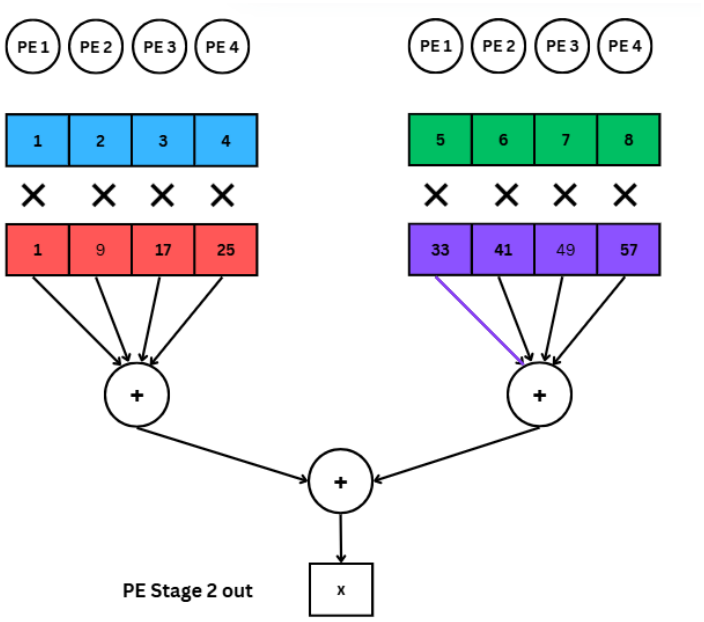
1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16

17	18	19	20
21	22	23	24
25	26	27	28
29	30	31	32



1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64



Compiler

compiler is implemented to generate the necessary instructions

```
NOP
FETCH_A 0
FETCH_B 0
DOT
FETCH_A 1
FETCH_B 1
DOT
STORE_TMP_F
FETCH_A 0
FETCH_B 2
DOT
FETCH_A 1
FETCH_B 3
DOT
STORE_TMP_F
FETCH_A 0
FETCH_B 4
DOT
FETCH_A 1
FETCH_B 5
DOT
STORE_TMP_F
FETCH_A 0
FETCH_B 6
```

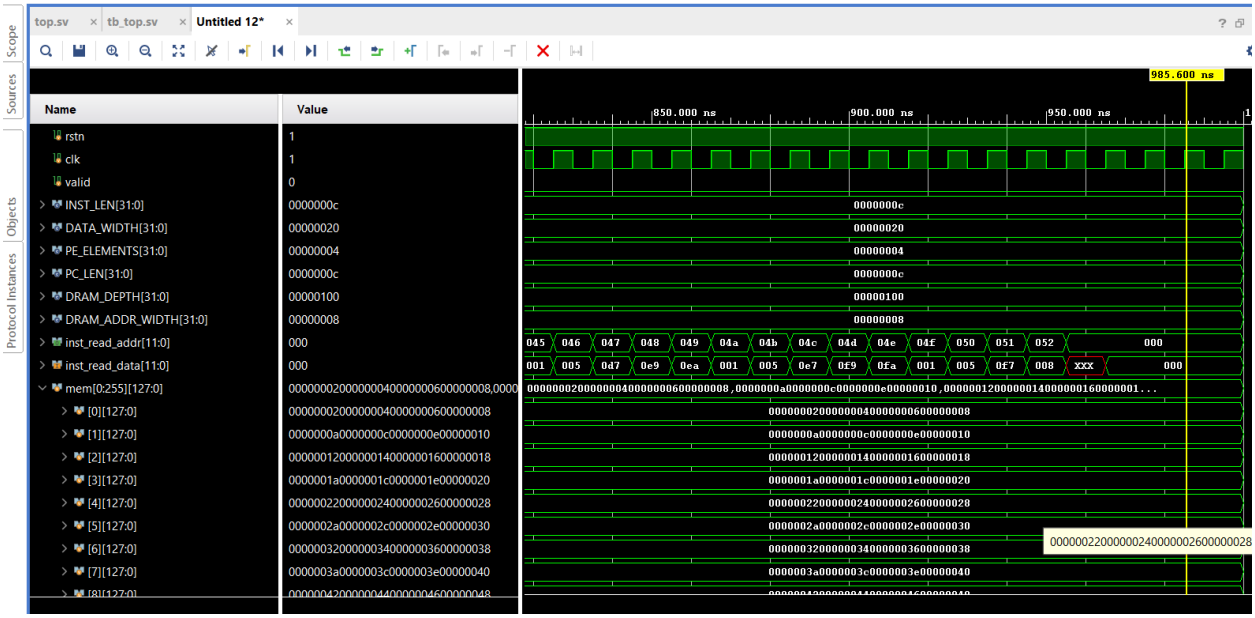
Assembly form

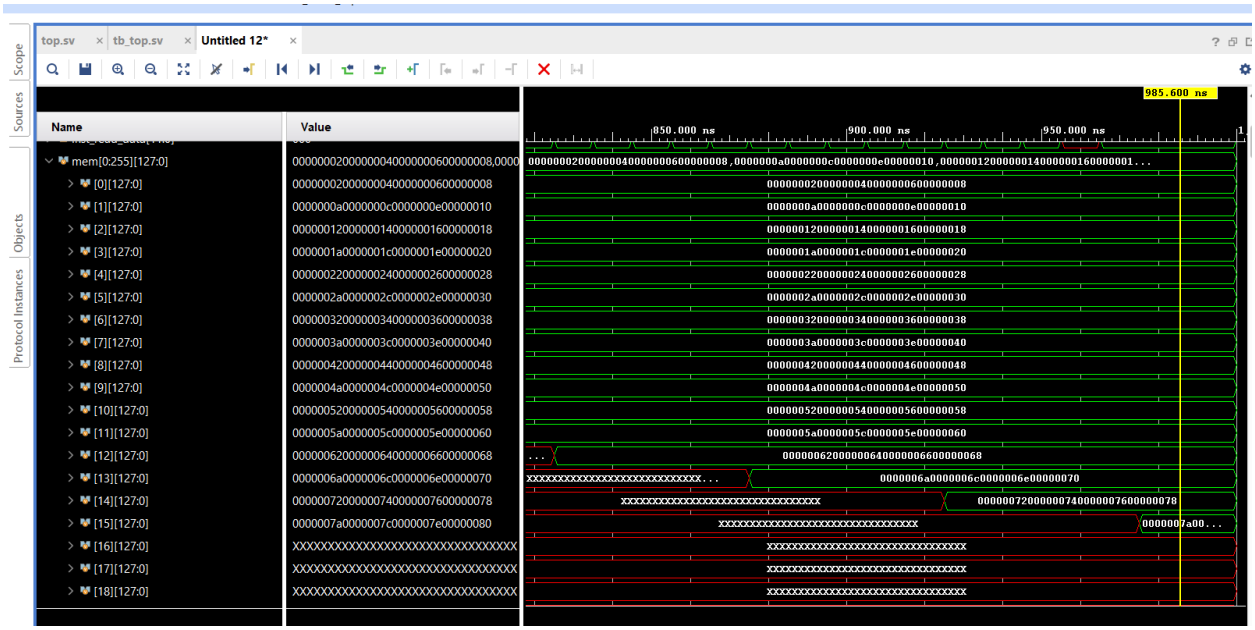
```
000000000000
000000000001
000000000010
000000000110
000000010001
000000010010
000000000110
000000001000
000000000001
000000100010
000000000110
000000010001
000000110010
000000000110
000000001000
000000000001
000001000010
000000000110
000000010001
000001010010
000000000110
000000001000
000000000001
000001100010
```

Binary Form

Simulation

Addition done



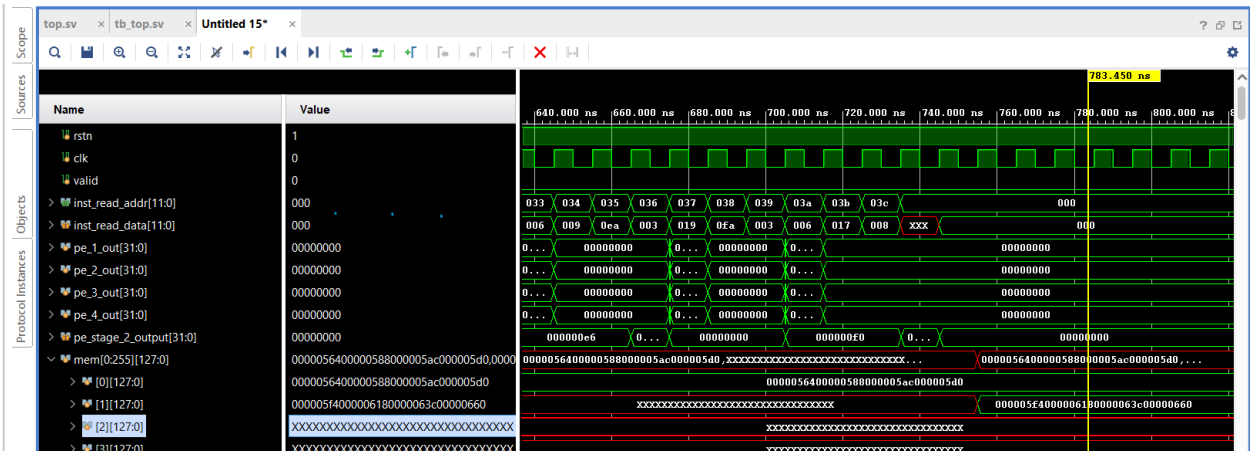


Matrix A			
1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16
17	18	19	20
21	22	23	24
25	26	27	28
29	30	31	32
33	34	35	36
37	38	39	40
41	42	43	44
45	46	47	48
49	50	51	52
53	54	55	56
57	58	59	60
61	62	63	64

Matrix B			
1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16
17	18	19	20
21	22	23	24
25	26	27	28
29	30	31	32
33	34	35	36
37	38	39	40
41	42	43	44
45	46	47	48
49	50	51	52
53	54	55	56
57	58	59	60
61	62	63	64

```
0000000200000004000000600000008
0000000a0000000c0000000e00000010
0000001200000014000000160000018
0000001a0000001c0000001e00000020
0000002200000024000000260000028
0000002a0000002c0000002e00000030
0000003200000034000000360000038
0000003a0000003c0000003e00000040
0000004200000044000000460000048
0000004a0000004c0000004e00000050
0000005200000054000000560000058
0000005a0000005c0000005e00000060
0000006200000064000000660000068
0000006a0000006c0000006e00000070
0000007200000074000000760000078
0000007a0000007c0000007e00000080
```

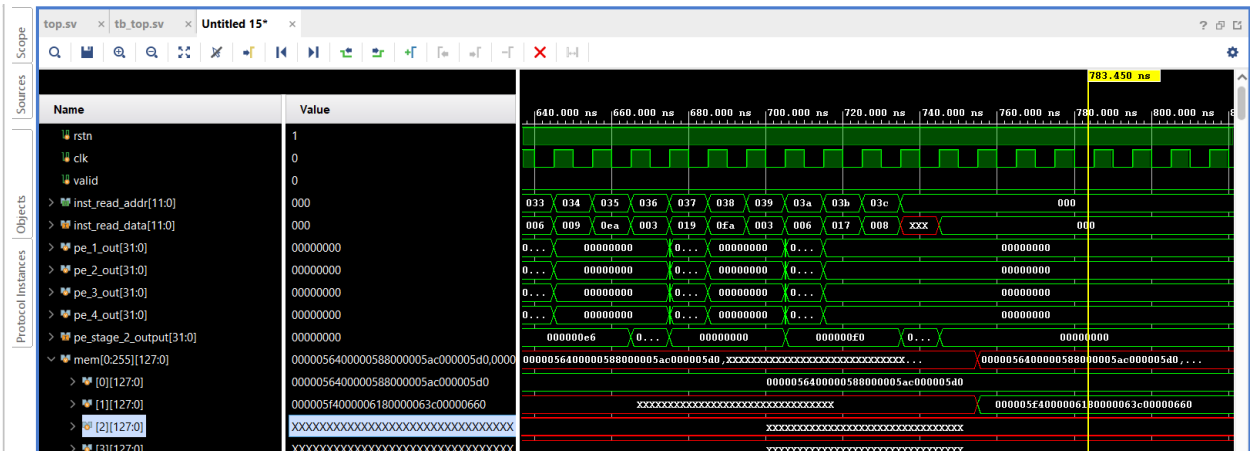
Multiplication



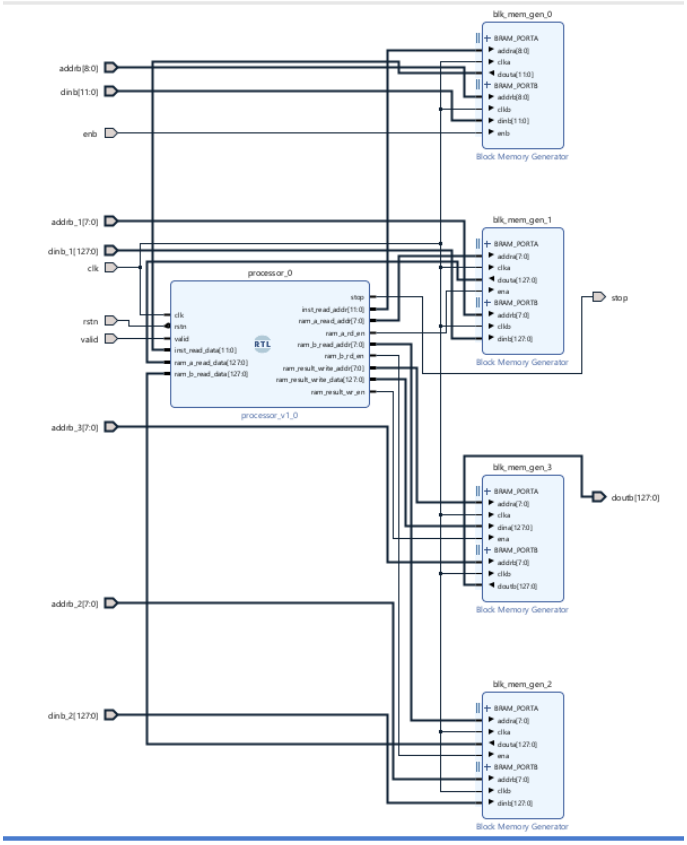
Matrix A										Matrix B							
1	2	3	4	5	6	7	8			1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16			9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24			17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32			25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40			33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48			41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56			49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64			57	58	59	60	61	62	63	64

Normal A								transpose B			
1	2	3	4					1	9	17	25
5	6	7	8					33	41	49	57
9	10	11	12					2	10	18	26
13	14	15	16					34	42	50	58
17	18	19	20					3	11	19	27
21	22	23	24					35	43	51	59
25	26	27	28					4	12	20	28
29	30	31	32					36	44	52	60
33	34	35	36					5	13	21	29
37	38	39	40					37	45	53	61
41	42	43	44					6	14	22	30
45	46	47	48					38	46	54	62
49	50	51	52					7	15	23	31
53	54	55	56					39	47	55	63
57	58	59	60					8	16	24	32
61	62	63	64					40	48	56	64

00000564 00000588 000005ac 000005d0 000005f4 00000618 0000063c 00000660



Processor with BRAM



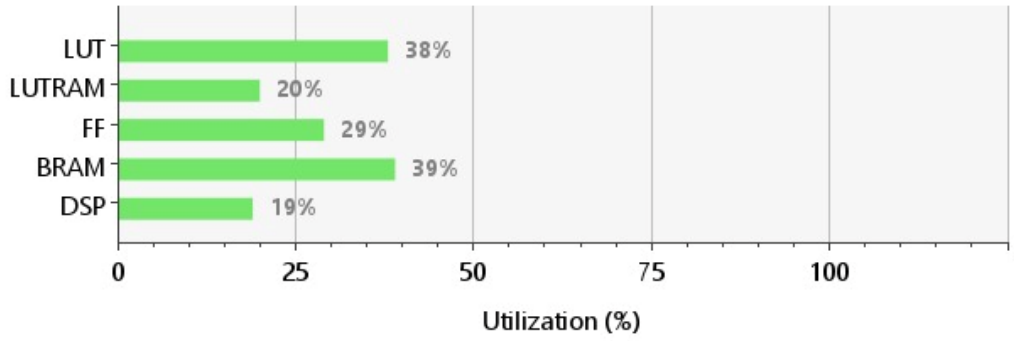
Implementation (Timing, Power and resource utilization)

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	1.109 ns	Worst Hold Slack (WHS):	0.011 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	30191	Total Number of Endpoints:	30175	Total Number of Endpoints:	12494

All user specified timing constraints are met.

Resource	Utilization	Available	Utilization %
LUT	6687	17600	37.99
LUTRAM	1191	6000	19.85
FF	10185	35200	28.93
BRAM	23.50	60	39.17
DSP	15	80	18.75



Clock frequency

Clock Summary

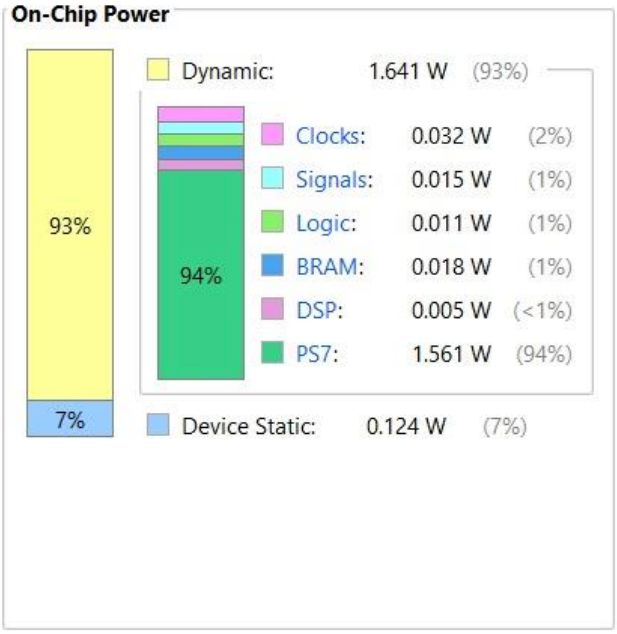
Name	Waveform	Period (ns)	Frequency (MHz)
clk_fpga_0	{0.000 5.000}	10.000	100.000

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.765 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**45.4°C**
Thermal Margin:	39.6°C (3.4 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium

Launch Power Constraint Advisor to find and fix invalid switching activity



Intra-Clock Paths

Clock	Edges (WNS)	WNS (ns)	TNS (ns)	Failing Endpoints (TNS)	Total Endpoints (TNS)	Edges (WHS)	WHS (ns)	THS (ns)	Failing Endpoints (THS)	Total Endpoints (THS)	WPWS (ns)
clk_fpga_0	rise - rise	1.109	0.000	0	29042	rise - rise	0.011	0.000	0	29042	3.750
dbg_hub/inst/BSCANID.u_xsdbm_id/	rise - rise	25.910	0.000	0	928	rise - rise	0.089	0.000	0	928	15.250

Inter-Clock Paths

From Clock	To Clock	Edges (WNS)	WNS (ns)	TNS (ns)	Failing Endpoints (TNS)	Total Endpoints (TNS)	Edges (WHS)	WHS (ns)	THS (ns)	Failing Endpoints (THS)
dbg_hub/inst/BSCANID.u_xsdbm_id/	clk_fpga_0	rise - rise	31.724	0.000	0	8				
clk_fpga_0	dbg_hub/inst/BSCANID.u_xsdbm_id/	rise - rise	8.621	0.000	0	8				