

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ, ಬೆಳಗಾವ
VISVESWARAIAH TECHNOLOGICAL UNIVERSITY, BELGAUM
KARNATAKA, INDIA



Certifies that

SANDEEP SINGH R

ಒಣ್ಣು ಡಿಲ್‌ ಅಷ್ಟು ಇಂಜಿನಿಯರಿಂಗ್
ಪದವಿಗೆ ಅಗತ್ಯವಾದ ಅರ್ಹತೆಗಳನ್ನು ಖಚಿತವಾಗಿ ಪರಿಗಣಿತವಾಗಿರುವ ಕಾರಣ
ಮೇಲೆ ಕಾಣುತ್ತಿರುವ ಪದವಿಗೆ ಅವರನ್ನು ಅಂಗೀಕರಿಸಲಾಗಿದೆ.

has been duly admitted to the Degree of

Bachelor of Engineering

in recognition of the fulfilment of requirements
for the said degree



ಉದ್ಯೋಗ ಸ್ಥಾನ

University Seat Number : 1SB03EC035

ವಿಷಯ

: Electronics & Communication Engineering

ಕ್ಲಾಸ್

: Second Class

D No 012126 ವಿಶ್ವವಿದ್ಯಾಲಯದ ಮುದ್ರಣಂದಿಗೆ ಕೊಡಲ್ಪಡಿದೆ
Given under the seal of the University

ಬೆಳಗಾವ
Belgaum

Date : APR 08, 2012

ಕುಲಚಂಡ

VICE CHANCELLOR



CONSOLIDATED ವಿಜ್ವೇಸ್ವರಾಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ, ಬೆಂಗಳೂರು
VISVESWARAIAH TECHNOLOGICAL UNIVERSITY, BELGAUM

KARNATAKA, INDIA

STATEMENT OF MARKS

First Semester B.E. D.U.M

Electronics & Communication Engineering

JUN 08
581914

Name of the Student

SANDEEP SINGH R

RAVINDRANATH C

Seal No.: 1STU03EC035

Name of the College

SHIRDI SAI ENGINEERING COLLEGE, BANGALORE

Sl. No.	Subject Code	Subject Title	Examination Marks			Internal Assessment Marks			Total Marks			Subject Result
			Max.	Min.	Obtained	Max.	Min.	Obtained	Max.	Min.	Obtained	
1	MAT11	Engineering Mathematics - I	100	35	46	25	-	21	125	50	67	JAN 2004
2	CHE12	Engineering Chemistry	100	35	35	25	-	18	125	50	63	JAN 2004
3	CCP13	Computer Concepts & 'C' Programming	100	35	35	25	-	15	125	50	60	JAN 2004
4	MES14	Elements of Mechanical Engineering	100	35	35	25	-	15	125	50	60	JUL 2004
5	ELN16	Basic Electronics	100	35	55	25	-	19	125	50	74	JAN 2004
6	CPL16	Computer Programming Lab	50	20	35	25	12	18	75	32	63	JAN 2004
7	CHE17	Engineering Chemistry Lab	50	20	21	25	12	20	75	32	41	JAN 2004
8	06CIP18	Constitution of India & Professional Ethics	50	18	20	25	-	20	75	30	40	JAN 2011
									GRAND TOTAL			775 314 375

Total Marks Obtained (in words) :

THREE HUNDRED AND SEVENTY FIVE ONLY
SECOND CLASS

Result of the Semester :

JUN 23, 2016

DATE :

06/10/14 CIP/PCM/18 is not considered for Grand Total and the Class Declaration

A - Absent NE - Not Eligible

Total Marks Obtained (in words) :

THREE HUNDRED AND SEVENTY FIVE ONLY

Result of the Semester :

JUN 23, 2016

Total Marks Obtained (in words) :

THREE HUNDRED AND SEVENTY FIVE ONLY

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JUN 23, 2016

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THREE HUNDRED AND SEVENTY FIVE ONLY

Result of the Semester :

JUN 23, 2016



CONSOLIDATED ವಿಷ್ವೇಶ್ವರಯ್ಯ ತಾಂಗೆ ವಿಶ್ವೇಶ್ವರಯ್ಯ, ಬೆಳಗಾಂ
VISVESVARAYAH TECHNOLOGICAL UNIVERSITY, BELGAUM
KARNATAKA, INDIA
581915

STATEMENT OF MARKS

SECOND SEMESTER BEDAM
Electronics & Communication Engineering

Name of the Student : SANODEEP SINGH R

Father's / Mother's Name : RAVINDRANATH C

Name of the College : SHIRDI SAI ENGINEERING COLLEGE, BANGALORE

Seal No. : 15B03EC035

Sl. No.	Code	Subject	Title	Examination Marks			Internal Assessment Marks			Total Marks			Subject Result
				Max.	Min.	Obtained	Max.	Min.	Obtained	Max.	Min.	Obtained	
1	MAT21	Engineering Mathematics - II		100	35	36	25	-	24	125	50	60	JUL 2006
2	PHY22	Engineering Physics		100	35	47	25	-	21	125	50	68	JUL 2004
3	CIV23	Elements of Civil Engineering		100	35	44	25	-	20	125	50	64	JUL 2004
4	GRA24	Engineering Graphics		100	35	42	25	-	22	125	50	64	JUL 2004
5	ELE25	Basic Electrical Engineering		100	35	35	25	-	16	125	50	51	JAN 2006
6	WSL26	Workshop Practice		60	20	28	25	25	12	75	32	53	JUL 2004
7	PHYL27	Engineering Physics Lab		50	20	37	25	25	12	75	32	60	JUL 2004
										GRAND TOTAL	775	314	303

Total Marks Obtained (in words) : THREE HUNDRED AND NINETY THREE ONLY
Result of the Semester : SECOND CLASS

DATE : JUN 23, 2016

A. Absent NE - Not Eligible

Three

Second Class

Registrar (Evaluation)





CONSOLIDATED

VISVESWARAJAH TECHNOLOGICAL UNIVERSITY, BELGAUM

JUN 08
581916

KARNATAKA, INDIA

STATEMENT OF MARKS

THIRD SEMESTER B.E.EXAM

Electronics & Communication Engineering

Name of the Student : SANDEEP SINGH R

Father's / Mother's Name : RAVINDRANATH C

Name of the College : SHIRDI SAI ENGINEERING COLLEGE, BANGALORE

Seat No. : 1SR03EC035

Sl. No.	Code	Subject	Title	Examination Marks		Internal Assessment Marks		Max.	Min.	Obtained	Max.	Min.	Obtained	Subject Result
				Max.	Min.	Max.	Min.							
1	MAT31	Engineering Mathematics - III		100	35	58	25	-	19	125	50	50	77	JAN 2005
2	EC32	Electronics Circuits		100	35	35	25	-	16	125	50	50	61	JAN 2007
3	CS33	Logic Design		100	35	35	25	-	19	125	50	50	64	JAN 2005
4	EE34	Network Analysis		100	35	44	25	-	15	125	50	50	69	JAN 2007
5	IT35	Electrical & Electronics Measurement		100	35	36	25	-	25	125	50	50	61	JAN 2005
6	EC38	Signals & Systems		100	35	35	25	-	19	125	50	50	64	JUL 2006
7	ECL37	Analog Electronics Lab		50	20	33	25	12	19	75	32	32	52	JUL 2005
8	ECL38	Digital Electronics Lab		50	20	33	25	12	22	75	32	32	55	JAN 2005
												GRAND TOTAL		900 364 377

Total Marks Obtained (In words) : THREE HUNDRED AND SEVENTY SEVEN ONLY

Result of the Semester : SECOND CLASS

DATE : JUN 23,2016

A - Absent NE - Not Eligible

Registrar (Evaluation)



CONSOLIDATED ವಿಷ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವೈಶ್ವಾಳಯ, ಬೆಳಗಾಂ
VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELGAUM

J 581876
08

KARNATAKA, INDIA

STATEMENT OF MARKS

FOURTH SEMESTER B.E EXAM

Electronics & Communication Engineering

SANDEEP SINGH R

RAVINDRANATH C

SHIRDI SAI ENGINEERING COLLEGE, BANGALORE

Name of the Student : SANDEEP SINGH R
Father's / Mother's Name : RAVINDRANATH C
Name of the College : SHIRDI SAI ENGINEERING COLLEGE, BANGALORE

Sl. No.	Subject Code	Title	Examination Marks			Internal Assessment Marks			Total Marks			Subject Result
			Max.	Min.	Obtained	Max.	Min.	Obtained	Max.	Min.	Obtained	
1	MAT41	Engineering Mathematics - IV	100	35	47	25	-	22	125	60	69	JUL 2005
2	EC42	Power Electronics	100	35	35	25	-	21	125	50	66	JUL 2005
3	EE43	Control Systems	100	35	38	25	-	16	125	50	64	JUL 2005
4	EC44	Field Theory	100	35	39	25	-	16	125	60	64	JAN 2010
5	EC45	Microprocessors	100	35	35	25	-	20	125	50	65	JUL 2005
6	CS46	Computer Organisation	100	35	35	25	-	17	125	50	62	JAN 2008
7	ECL47	Microprocessors Lab	50	20	24	25	12	23	75	32	47	JUL 2006
8	ECL48	Power Electronics Lab	50	20	41	25	12	22	75	32	63	JUL 2005
									GRAND TOTAL			
									900	364	404	

Total Marks Obtained (In words) : FOUR HUNDRED AND FOUR ONLY
Result of the Semester : SECOND CLASS

DATE : JUN 21,2016

Registrar (Engineering)

A - Absent NE - Not Eligible



CONSOLIDATED ವಿಸ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ, ಬೆಳಗಾಂ

VISVESVARAIAH TECHNOLOGICAL UNIVERSITY, BELGAUM

KARNATAKA, INDIA

STATEMENT OF MARKS

FIFTH SEMESTER B.E. EXAM

Electronics & Communication Engineering

Name of the Student : SANDEEP SINGH R

Father's / Mother's Name : RAVINDRANATH C

Name of the College : SHIRDI SAI ENGINEERING COLLEGE, BANGALORE

Seat No. : 1SB03EC035

Sl. No.	Subject Code	Title	Examination Marks			Internal Assessment Marks			Total Marks			Subject Result
			Max.	Min.	Obtained	Max.	Min.	Obtained	Max.	Min.	Obtained	
1	EC51	Analog Communication	100	35	35	25	-	21	125	50	66	JAN 2007
2	EC52	Digital Signal Processing	100	35	35	25	-	16	125	50	60	JUL 2009
3	EC53	Transmission Lines & Waveguides	100	35	35	25	-	15	125	50	50	JUL 2007
4	EC54	Advanced Microprocessor	100	35	39	25	-	17	125	50	56	JUL 2009
5	EC65	Telecom & Switching	100	35	47	25	-	15	125	50	62	JUL 2009
6	EC66	Solid State Devices & Technology	100	35	35	25	-	21	125	50	56	JUL 2010
7	ECL67	Advanced Microprocessor Lab	50	20	46	25	12	20	75	32	68	JAN 2007
8	ECL68	Communication Lab	50	20	42	25	12	24	75	32	68	JAN 2007
									GRAND TOTAL			900 304 352

Total Marks Obtained (in words) : THREE HUNDRED AND FIFTY TWO ONLY
 Result of the Semester : SECOND CLASS

DATE : JUN 27, 2016
 A - Absent NE - Not Eligible



H. M. Hosseini
 Registrar (Evaluation)

CONSOLIDATED ప్రతిభద్రులు, తాండ్రలు మరొక పత్రము
VISVESWARAIAH TECHNOLOGICAL UNIVERSITY, BELGAUM



KARNATAKA, INDIA

STATEMENT OF MARKS

SIXTH SEMESTER BE EXAM

Electronics & Communication Engineering

J 581977
08

Name of the Student

SANDEEP SINGH R

Father's / Mother's Name

RAVINDRANATH C

Name of the College

SHIRDI SAI ENGINEERING COLLEGE, BANGALORE

Sl. No.	Code	Subject	Title	Examination Marks			Internal Assessment Marks			Total Marks			Subject Result
				Max.	Min.	Obtained	Max.	Min.	Obtained	Max.	Min.	Obtained	
1	EC61	Digital Communication		100	35	38	25	25	-	16	125	50	54
2	EC62	Microwave Communication		100	35	35	25	25	-	18	125	50	53
3	EC63	Information Theory & Coding		100	35	36	25	25	-	19	125	50	55
4	EC64	Digital System Design using VHDL		100	35	35	25	25	-	15	125	50	50
5	EC65	Antenna & Propagation		100	35	35	25	25	-	15	125	50	50
6	EC662	DSP Architecture		100	35	43	25	25	-	16	125	50	53
7	ECL67	Advanced Communication Lab		60	20	32	25	25	12	24	75	32	32
8	ECL68	VHDL Lab		60	20	44	25	25	12	22	75	32	32
										GRAND TOTAL			900 304 301

Total Marks Obtained (In words) : THREE HUNDRED AND ONE ONLY
 Result of the Semester : SECOND CLASS

DATE : JUN 27,2016

A - Absent NE = Not Eligible

H. A. M. S. R.
Registrar (Evaluation)



CONSOLIDATED విశ్వేశవాయి తాంగె విశ్వవిద్యాలయ, బెంగళూరు

VISVESVARAIAH TECHNOLOGICAL UNIVERSITY, BELGAUM
KARNATAKA, INDIA

J 581978
08

STATEMENT OF MARKS
SEVENTH SEMESTER B.E. EXAM
Electronics & Communication Engineering

Name of the Student : SANDEEP SINGH R

Father's / Mother's Name : RAVINDRANATH C

Name of the College : SHIRDI SAI ENGINEERING COLLEGE, BANGALORE

Seal No. : 1SB03EC035

Sl. No.	Code	Subject	Title	Examination Marks			Internal Assessment Marks			Total Marks			Subject Result
				Max.	Min.	Obtained	Max.	Min.	Obtained	Max.	Min.	Obtained	
1	08EC71	Computer Communication Networks		100	35	35	25	-	15	125	50	60	JAN 2011
2	08ECT2	Optical Fiber Communication		100	35	39	25	-	16	125	50	55	JAN 2011
3	06EC756	Image Processing		100	35	44	25	-	18	125	50	62	JAN 2011
4	06EC767	H R Management		100	35	35	25	-	17	125	50	62	JAN 2011
5	06ECL77	VLSI Lab		50	20	20	25	12	15	75	32	35	JAN 2011
6	06ECL577	DSP Lab		50	20	30	25	12	16	75	32	46	JAN 2011
7	08AL617	Management & Entrepreneurship		100	35	38	25	-	17	125	50	55	JAN 2011
8	06EC567	Fundamentals of CMOS VLSI		100	35	35	25	-	15	125	50	50	JUL 2011
										GRAND TOTAL	800	364	360

Total Marks Obtained (In words) : THREE HUNDRED AND EIGHTY ONLY
Result of the Semester : SECOND CLASS

DATE : JUN 27, 2016

A - Absent NE - Not Eligible

Registrar (Evaluation)



ವಿಷ್ವೇಸ್ವರಾಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ, ಬೆಳಗಾಂ

VISVESVARAIAH TECHNOLOGICAL UNIVERSITY, BELGAUM

KARNATAKA, INDIA



F 07
099759

RE Eighth Semester (Electronics & Communication Engineering)

STATEMENT OF MARKS

Seat No. : 1SB03EC035

Name of the Student : SANDEEP SINGH R
 Father's / Mother's Name : RAVINDRANATH C
 Name of the College : SHIRDI SAI ENGINEERING COLLEGE, BANGALORE

Sl. No.	Subject	Code	Title	Examination Marks			Internal Assessment Marks			Total Marks			Month & Year of Passing
				Max	Min	Obtained	Max	Min	Obtained	Max	Min	Obtained	
1	06EC81	Wireless Communication		100	35	44	25	-	19	125	50	63	JUL 11
2	06EC82	Embedded System Design		100	35	38	25	-	17	125	50	55	JUL 11
3	06EC832	Network Security		100	35	57	25	-	19	125	50	76	JUL 11
4	06EC841	Multimedia Communication		100	35	48	25	-	18	125	50	68	JUL 11
5	06EC85	Project Work		100	40	85	100	50	68	200	90	173	JUL 11
6	06EC86	Seminar		-	-	-	50	20	45	50	20	45	JUL 11

*First Attempt Total (in words) : FOUR HUNDRED AND SEVENTY EIGHT ONLY

Result of the Semester : FIRST CLASS
 Results of V to VIII Semesters :

GRAND TOTAL 750 310 478

Semesters	V	VI**	VII**	VIII	V TO VIII
Marks at First Attempt	352	301	380	478	1511
Total Marks (Max)	800	900	900	750	3450
Result	SC	SC	SC	FC	SC

First Attempt Total (V to VIII Sem) In words : ONE THOUSAND FIVE HUNDRED AND ELEVEN ONLY
 Result of the Degree : SECOND CLASS

** Cleared during Jul 2011 exam
 Date : NOV 16, 2011

Prabhakar G.N.
 Registrar (Evaluation)