CPE301 – SPRING 2019

Design Assignment 2B

Student Name: Robert Sander

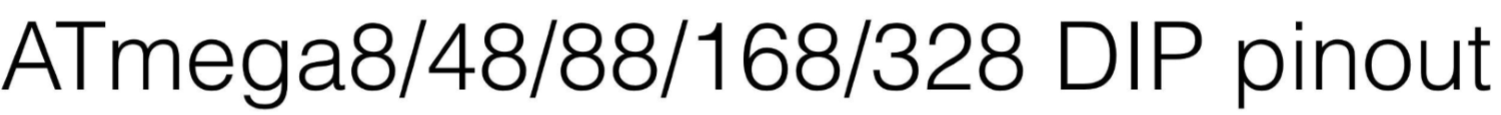
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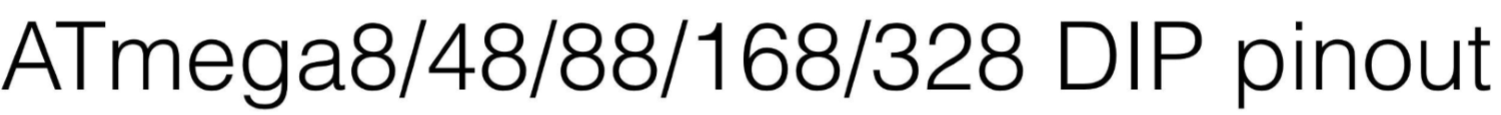
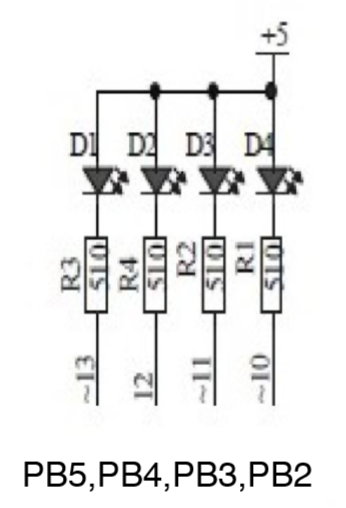
Student Email: sander1@unlv.nevada.edu

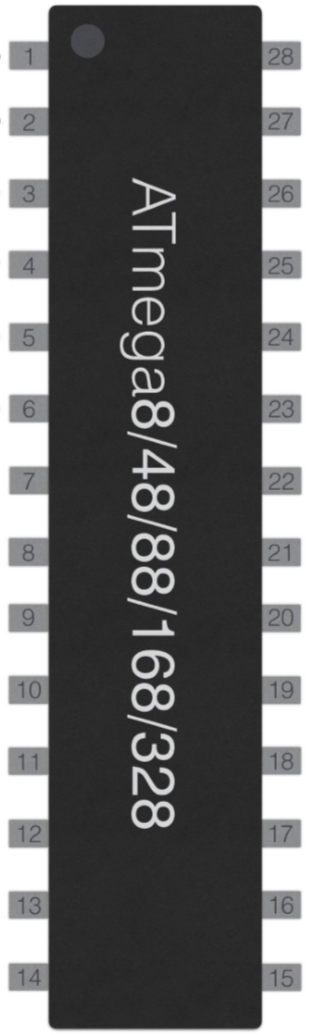
Primary Github address: <https://github.com/sanderUNLV/submission_DA.git>

Youtube link: <https://youtu.be/PSLQ-g448l0>

1. **COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS**









1. **INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1**

**Assembly:**

// DA2B\_T1\_A

// Author : Robert Sander

.include <m328pdef.inc>

.include "Delay1.asm"

.ORG 0 ;location for reset

JMP MAIN

.ORG 0x02 ;location for EXT\_INT0

JMP EX1\_ISR

MAIN:

LDI R20,HIGH(RAMEND);Initialize the stack

OUT SPH,R20 ;Initialize the stack

LDI R20,LOW(RAMEND) ;Initialize the stack

OUT SPL,R20 ;Initialize the stack

LDI R16, 0xFF ;load 0xFF into R16

OUT DDRB, R16 ;SET PORTB TO OUTPUT

LDI R16, 0x3C ;load 0x3C into R16

OUT PORTB, R16;'Turn off' by setting PB.2-5 high

SBI PORTD,2 ;pull-up activated, PD.2

LDI R20, (0<<ISC01)|(0<<ISC00) ;Low level interrupt

STS EICRA,R20 ;Low level interrupt

LDI R20,1<<INT0 ;Enable INT0

OUT EIMSK,R20 ;Enable INT0

SEI ;Set I (Enable Interrupts)

HERE:

JMP HERE ;Stay here indefinitely

EX1\_ISR:

LDI R20, 1<<INTF0

OUT EIFR, R20 ; clear flag, EXOR...LOADS 1, 1\*1=0

LDI R16, 0x38 ;LOAD THE VALUE 0x38 INTO R16

OUT PORTB, R16 ;'TURNS ON' PORTB...REVERSE LOGIC

RCALL Delay1

LDI R16, 0x3C ;LOAD THE VALUE 0x3C INTO R16

OUT PORTB, R16 ;'TURNS OFF' PORTB...REVERSE LOGIC

RETI

**C:**

// DA2B\_T1\_C

// Author : Robert Sander

#define *F\_CPU* 16000000UL

#include <avr/io.h>

#include <avr/interrupt.h>

#include <util/delay.h>

int main ()

{

DDRB |= 0xFF;// ENABLE PORTB AS OUTPUT

PORTB |= 0x3C;// TURN OFF PB.2-5

PORTD |= 1<<2;//pull-up activated FOR INT0

EICRA = 0x2;//make INT0 falling edge triggered

EIMSK = (1<<INT0);//enable external interrupt 0 PD.2

sei ();//enable interrupts, global

while (1)

{

// DO WHATEVER HERE, LOOPING INDEFINITELY

}

return 0;

}

ISR (INT0\_vect)//ISR for external interrupt 0

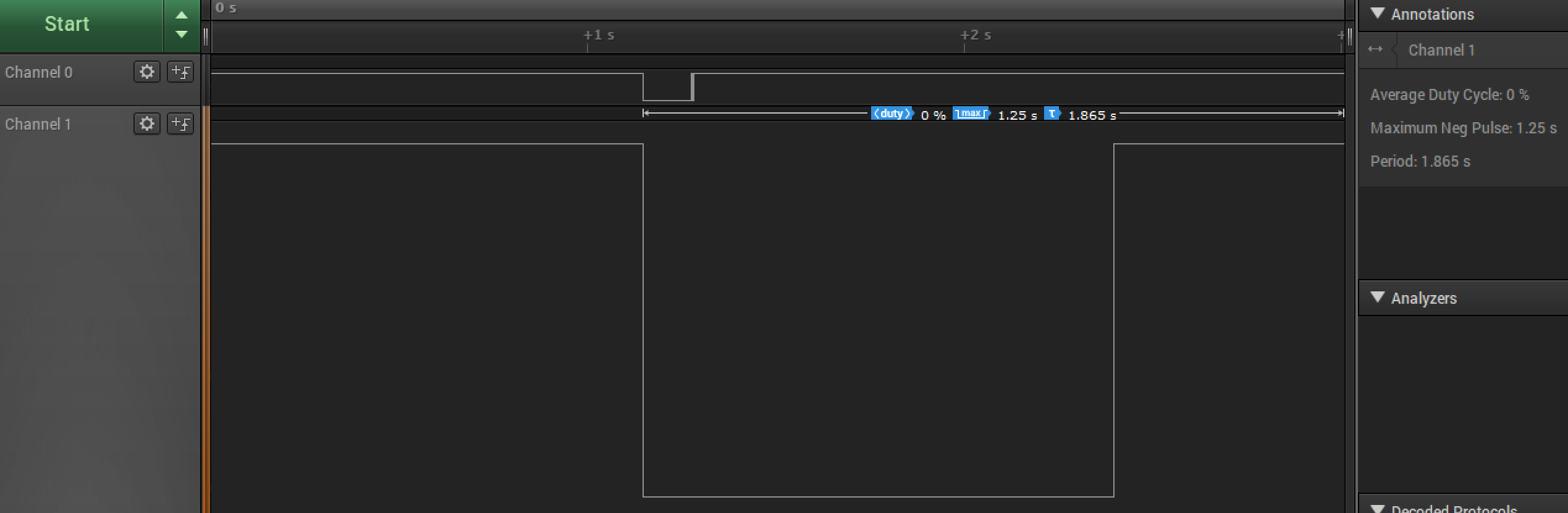
{

PORTB ^= (1<<2); // TURN ON PB.2

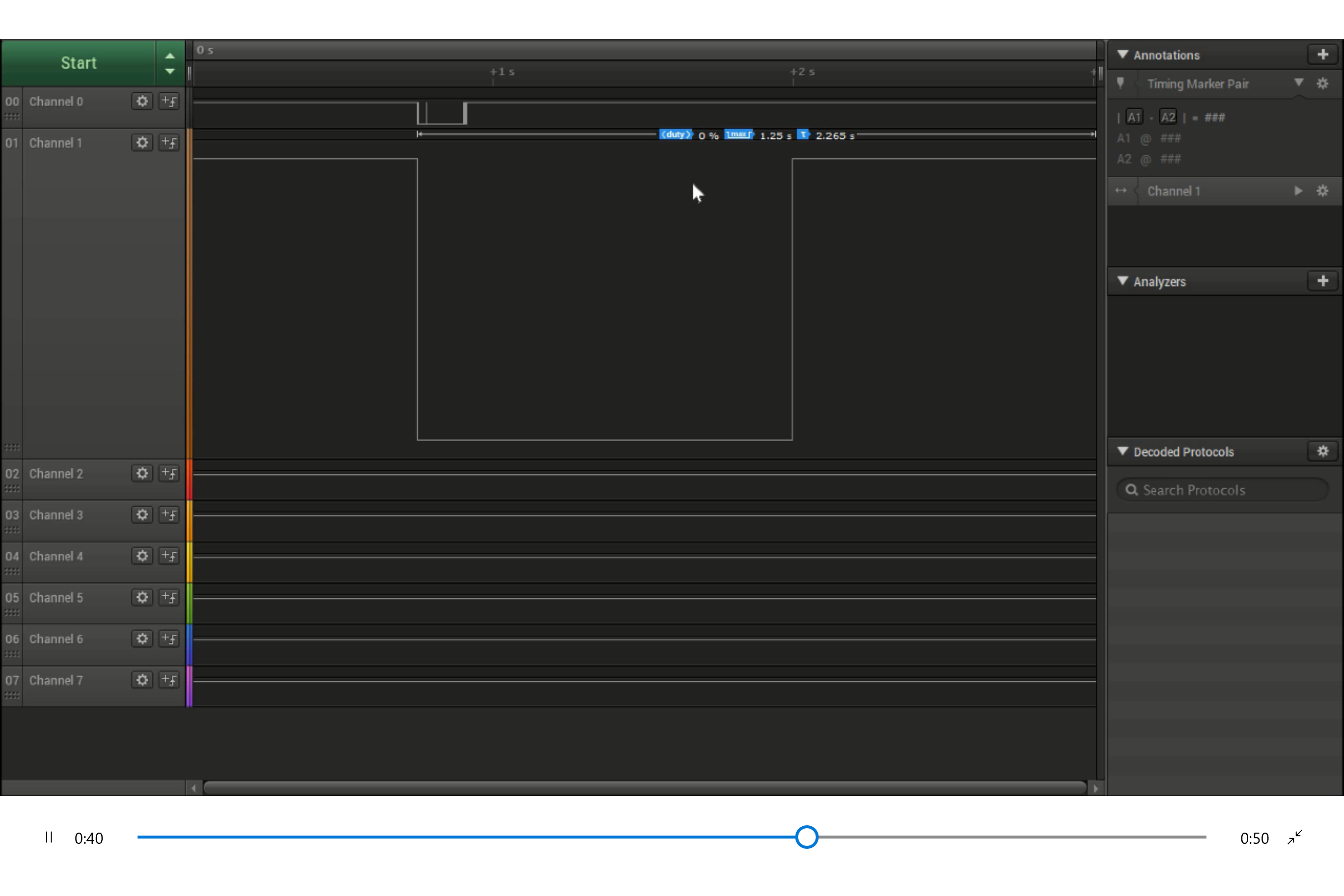
*\_delay\_ms*(1250); // DELAY 1.25s

}

1. **SCREENSHOTS OF EACH TASK OUTPUT**

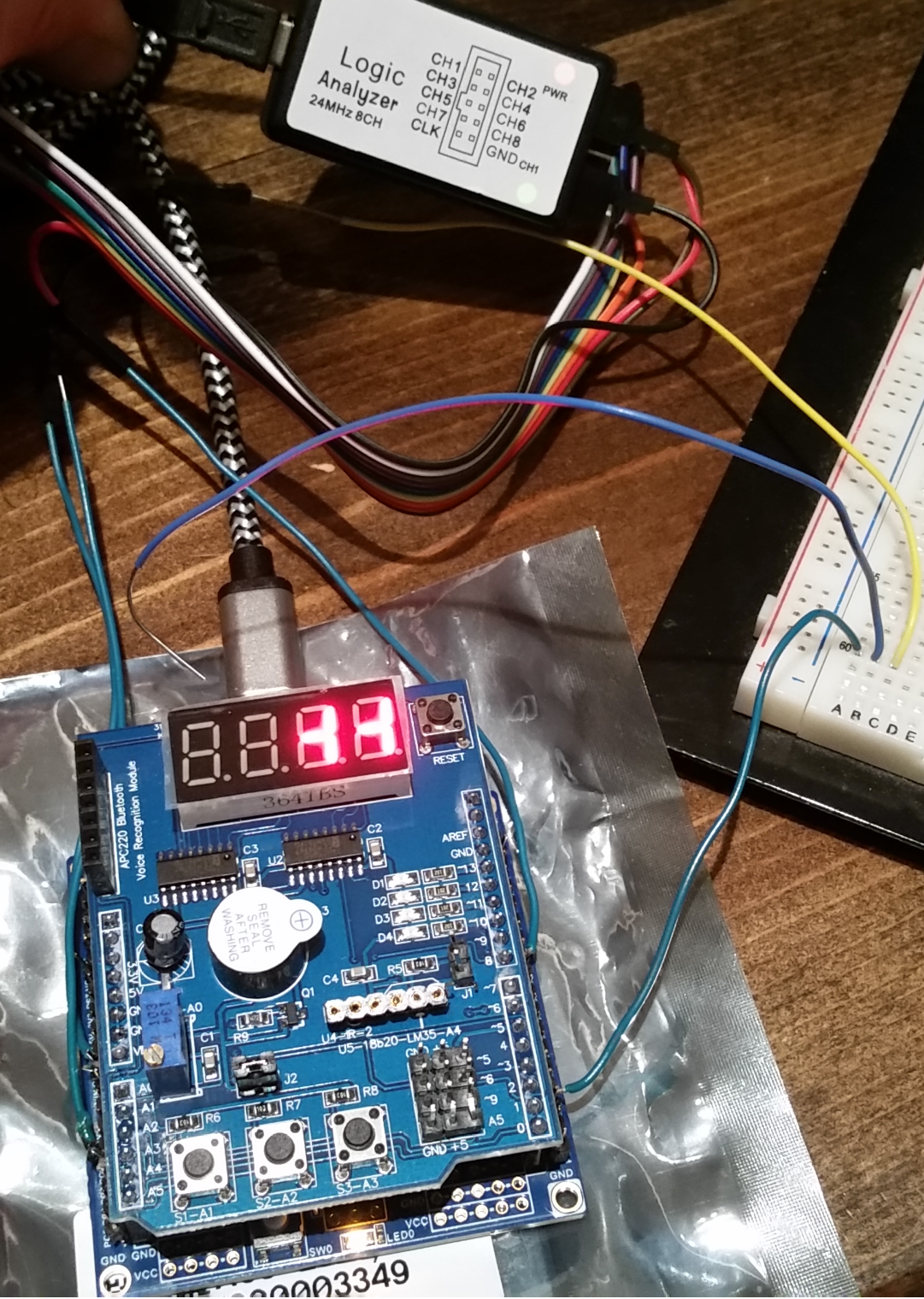


*Figure 1 – Logic Analyzer output (Assembly)*



*Figure 2 – Logic Analyzer output (C)*

1. **SCREENSHOT OF EACH DEMO (BOARD SETUP)**





*Figure 4 – Hardware Setup with Logic Analyzer*

*Figure 3 – Hardware Setup*

1. **VIDEO LINKS OF EACH DEMO**

<https://youtu.be/PSLQ-g448l0>

1. **GITHUB LINK OF THIS DA**

<https://github.com/sanderUNLV/submission_DA.git>

**Student Academic Misconduct Policy**

<http://studentconduct.unlv.edu/misconduct/policy.html>

“This assignment submission is my own, original work”.

-Robert Sander