CPE301 – SPRING 2019

Design Assignment 1

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Primary Github address: https://github.com/sanderUNLV/submission_DA.git
Youtube link: https://youtu.be/KoeopwFGWXE

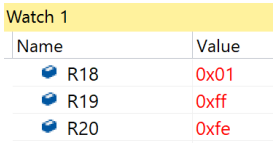
1. DEVELOPED CODE OF TASK 1/A

```
.include <m328pdef.inc>

.ORG 0              ;BEGIN AT THIS LOCATION

       LDI R22, 0xFF ;LOAD IN MULTIPLICAND_8 'BOTTOM NUMBER'
       LDI R24, 0xFF ;LOAD IN MULTIPLICAND_16_LOW 'TOP 'RIGHT PART' NUMBER'
       LDI R25, 0xFF ;LOAD IN MULTIPLICAND_16_HIGH 'TOP 'LEFT PART' NUMBER'
       LDI R26, 0    ;LOAD ZERO INTO REGISTER R26

       CPI R22, 0    ;IF MULTIPLIER EQUALS 0
       BREQ DONE     ;IF MULTIPLIER EQUALS 0 GO TO DONE:
L1:
       ADC R18, R24  ;ADD WITH CARRY THE VALUE OF R24 AND R18 AND STORE THE RESULT IN R18
       ADC R19, R25  ;ADD WITH CARRY THE VALUE OF R25 AND R19 AND STORE THE RESULT IN R19
       ADC R20, R26  ;ADD WITH CARRY THE VALUE OF R26 AND R20 AND STORE THE RESULT IN R20
       DEC R22       ;DECREMENT R22, ITERATIVE ADDITION FOR MULTIPLICATION
       CPI R22, 0    ;CHECK TO SEE IF REGISTER R22 IS ZERO
       BRNE L1       ;IF REGISTER R22 DOES NOT EQUAL ZERO GO TO L1: OTHERWISE CONTINUE
DONE:                ;GO HERE IF THE MULTIPLIER EQUALS ZERO
END: RJMP END        ;FINISHED AND THE DESIRED RESULT SHOULD BE IN R18
```

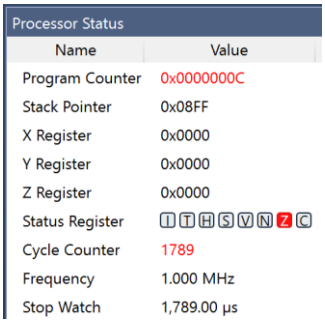
2. SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)

```
LDI R22, 0xFF   ;LOAD IN MULTIPLICAND_8 'BOTTOM NUMBER'
LDI R24, 0xFF   ;LOAD IN MULTIPLICAND_16_LOW 'TOP 'RIGHT PART' NUMBER'
LDI R25, 0xFF   ;LOAD IN MULTIPLICAND_16_HIGH 'TOP 'LEFT PART' NUMBER'
```

The test values are 255 in R22, 3840 in R24, and 61440 in R25.
Testing 255*65280.



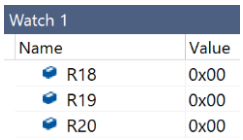
The result registers are R18, R19, and R20.



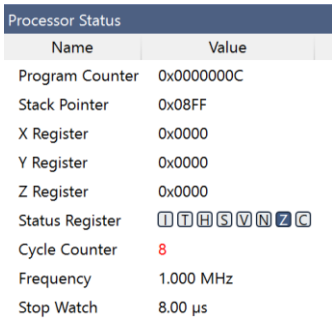
The maximum amount of clock cycles is 1789.

```
LDI R22, 0x00   ;LOAD IN MULTIPLICAND_8 'BOTTOM NUMBER'
LDI R24, 0xFF   ;LOAD IN MULTIPLICAND_16_LOW 'TOP 'RIGHT PART' NUMBER'
LDI R25, 0xFF   ;LOAD IN MULTIPLICAND_16_HIGH 'TOP 'LEFT PART' NUMBER'
```

The test values are 0 in R22, 3840 in R24, and 61440 in R25.
Testing 0*65280.



The result registers are R18, R19, and R20.



The minimum amount of clock cycles is 8.

This code has a maximum of 1789 cycles with 255*65535 and a minimum of 8 cycles with 0*anything.

3. VIDEO LINKS OF EACH DEMO

Youtube link: https://youtu.be/KoeopwFGWXE

4. GITHUB LINK OF THIS DA

Primary Github address: https://github.com/sanderUNLV/submission_DA.git

Student Academic Misconduct Policy
http://studentconduct.unlv.edu/misconduct/policy.html

"This assignment submission is my own, original work".
-Robert Sander