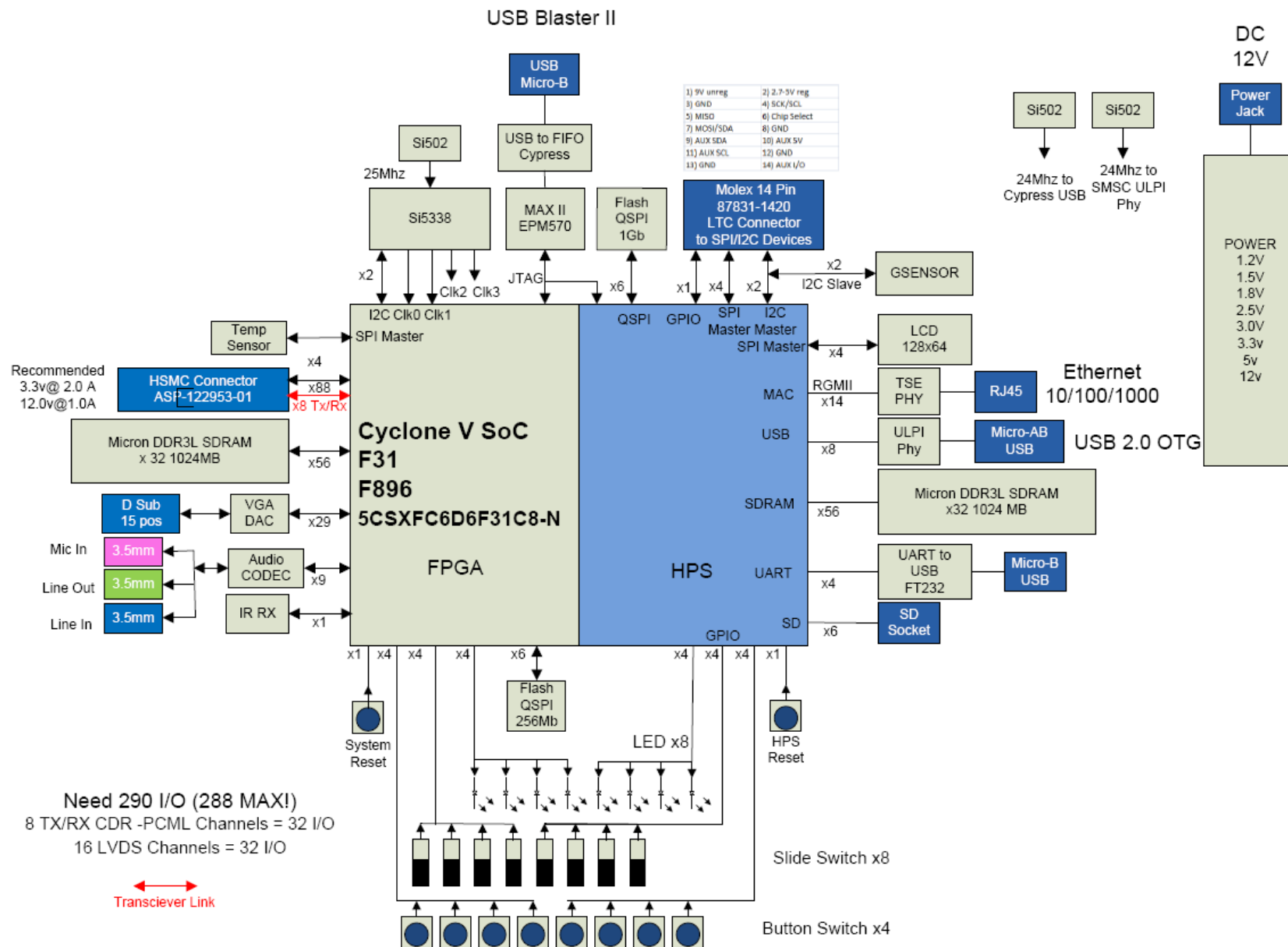


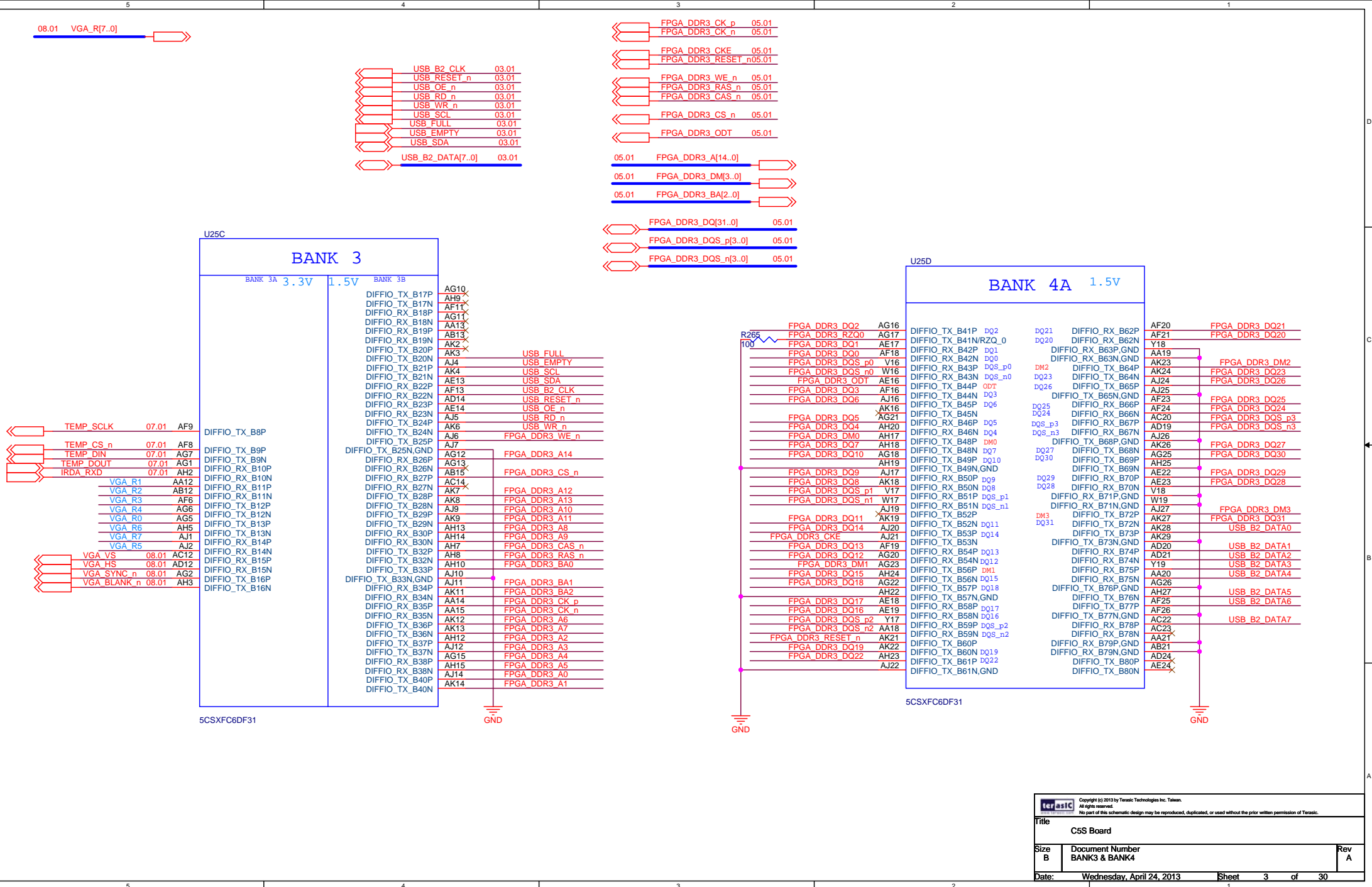
C5S

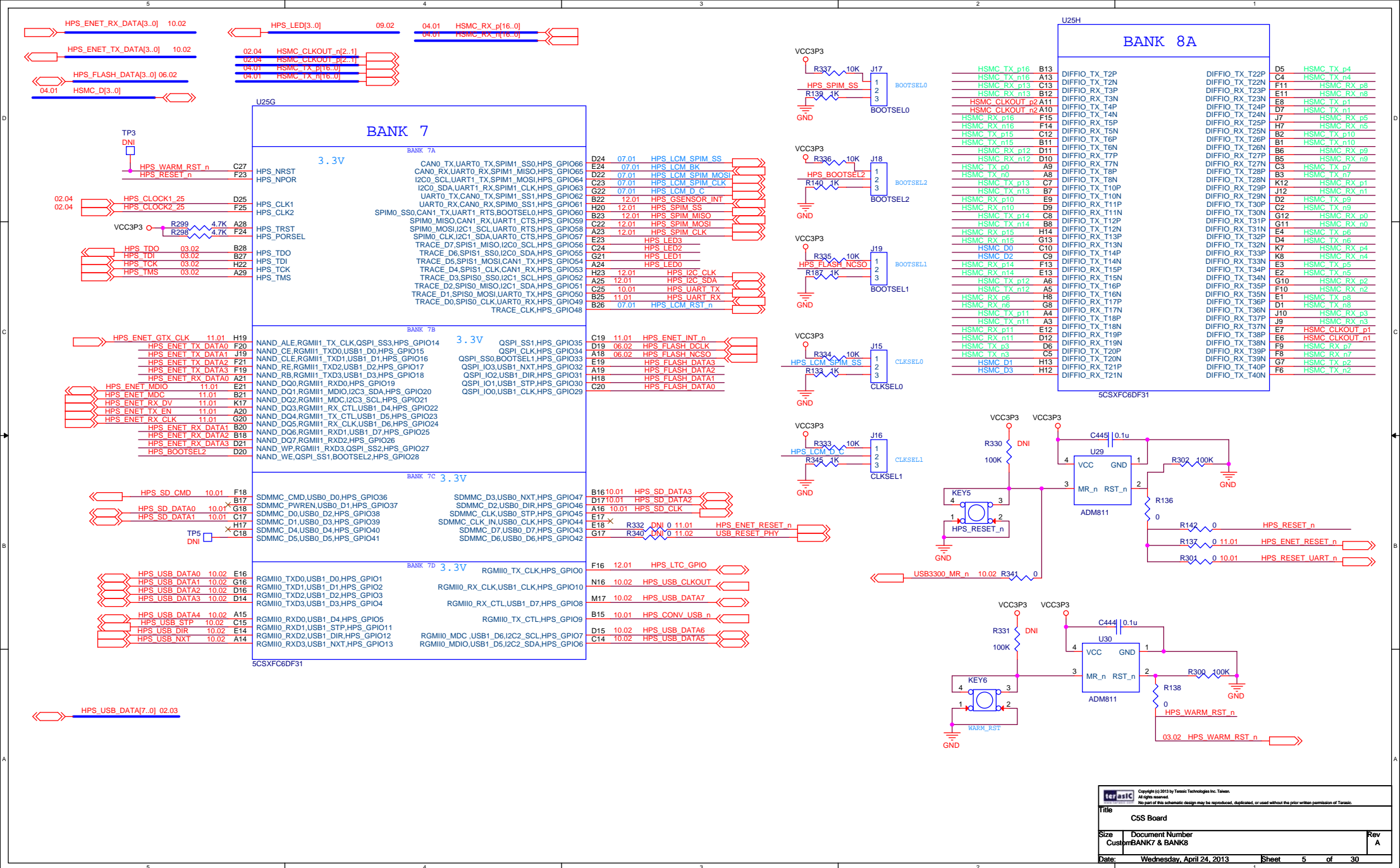
Section	Title	Page
01.0	Design Introduction	
1.01	Cover Page	1
1.02	Block Diagram	2
02.0	Cyclone V EP5CSXFC6DF31	
02.01	BANK3 & BANK4	3
02.02	BANK5 & BANK6	4
02.03	BANK7 & BANK8	5
02.04	Clock & GND	6
02.05	Transceiver	7
02.06	Power & Config	8
03.0	JTAG	
03.01	USB Blaster II	9
03.02	JTAG Chain	10
04.0	Expansion Port	
04.01	HSMC	11
05.0	Memory	
05.01	DDR3L SDRAM For FPGA	13
05.02	DDR3L SDRAM For HPS	14

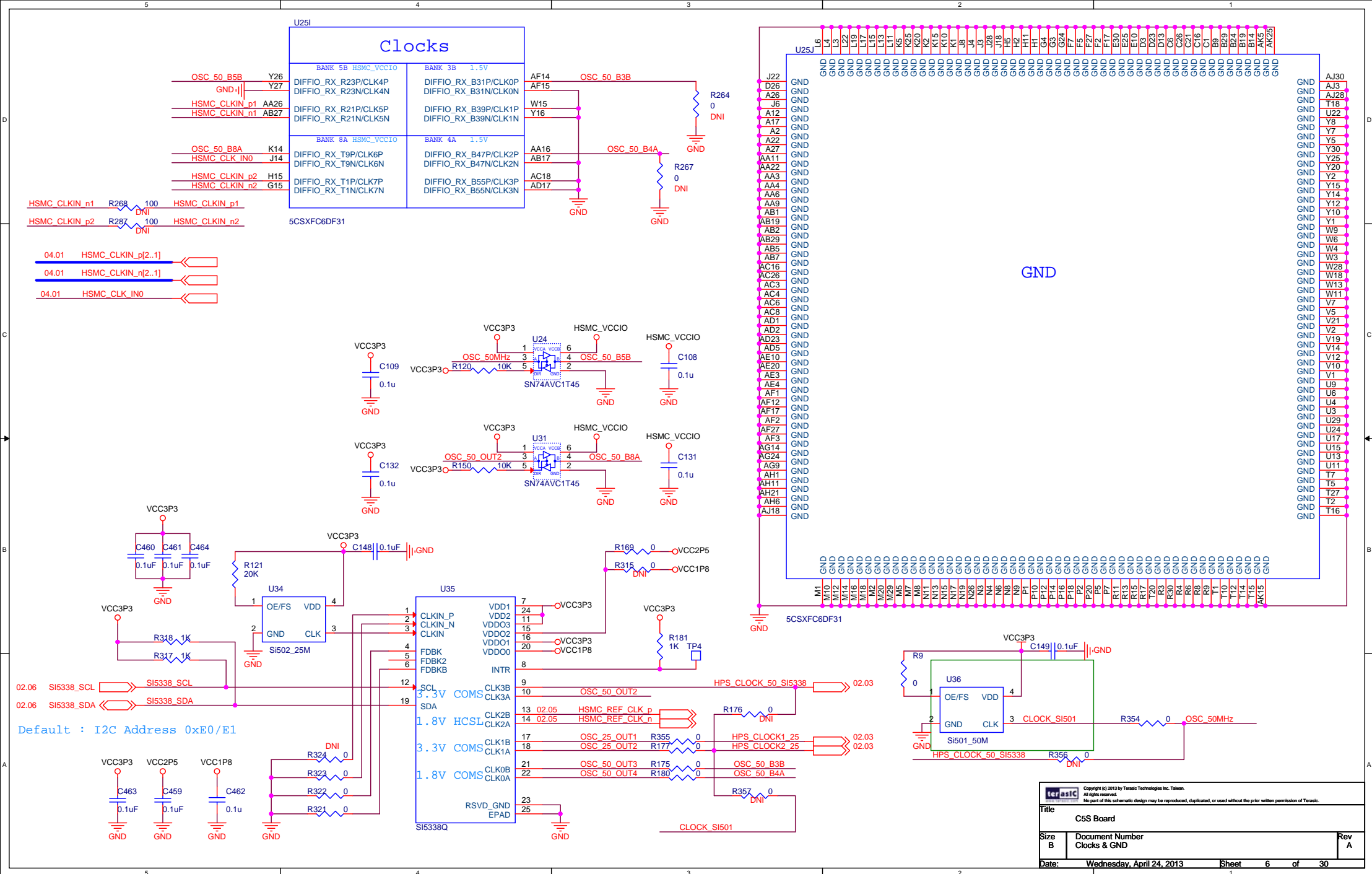
Section	Title	Page
06.0	Memory 2	
06.01	QSPI FLASH For FPGA	15
06.02	QSPI FLASH For HPS	16
07.0	LCD & Temp sensor & IRM	
07.01	LCD & Temp sensor & IRM	17
08.0	VGA & Audio	
08.01	VGA ADV7123	18
08.02	Audio SSM2603	19
09.0	FPGA & HPS IO	
09.01	LED & BUTTON & SWITCH For FPGA	20
09.02	LED & BUTTON & SWITCH For HPS	21
10.0	USB & SD CARD & UART	
10.01	UART TO USB & SD CARD	22
10.02	ULPI PHY USB3300	23
11.0	TSE PHY	
11.01	TSE PHY KSZ9021RN	24
12.0	LTC Connector & Gensor	
12.01	LTC Connector & Gensor	25

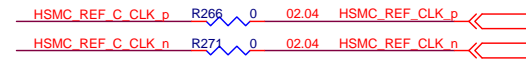
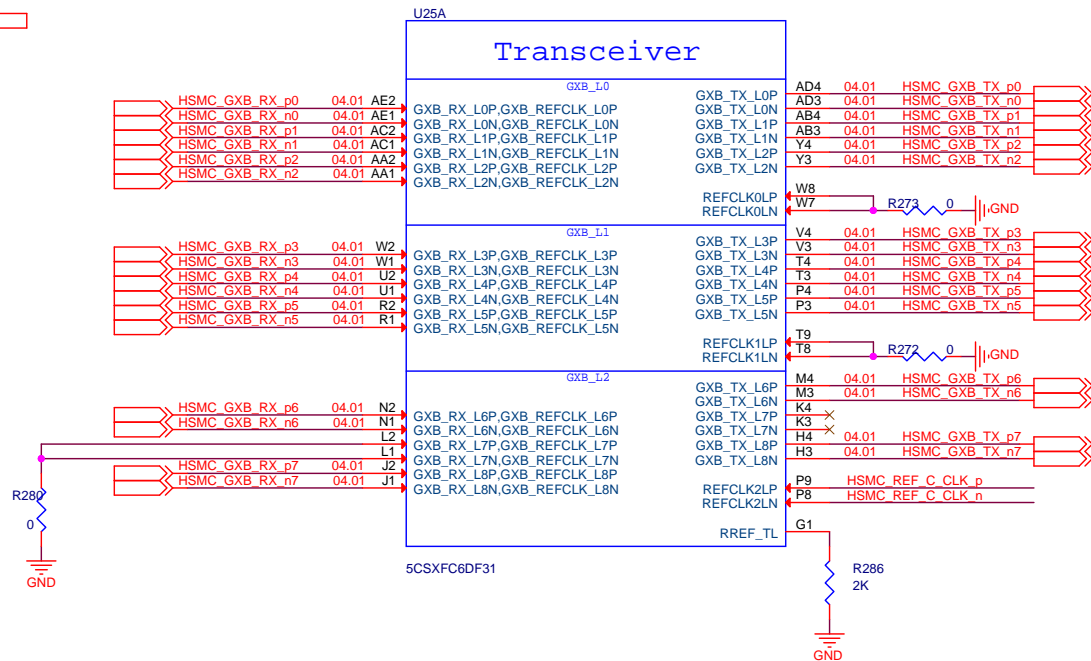
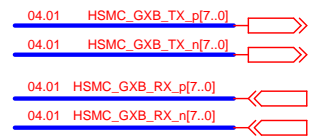
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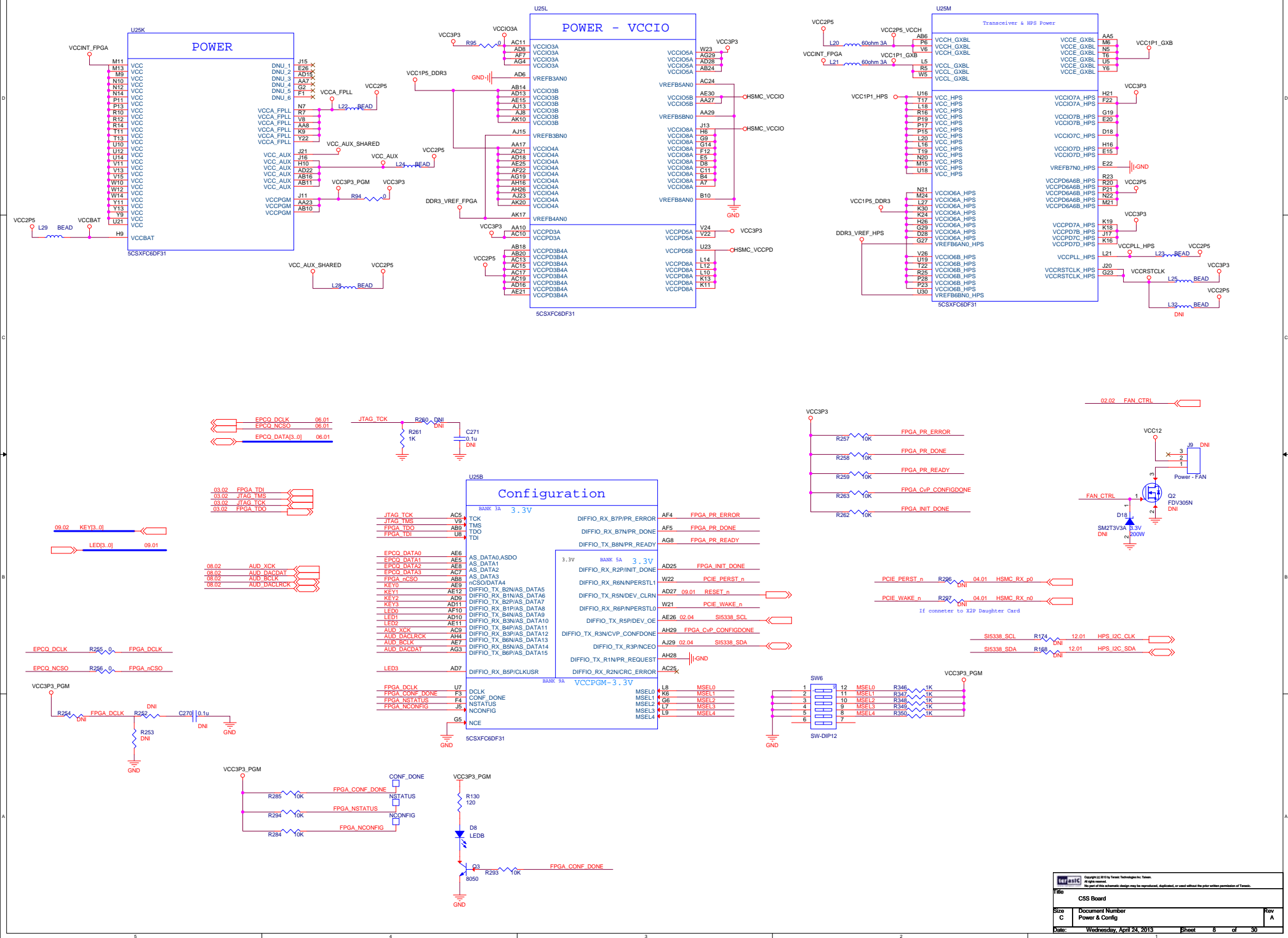


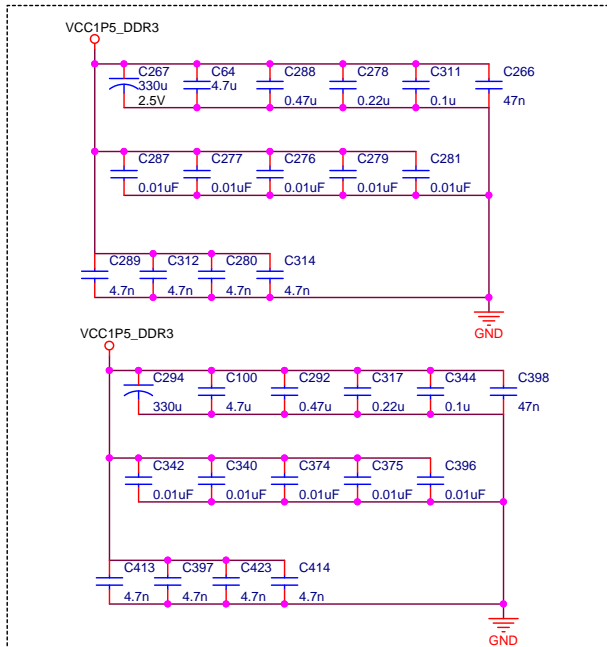
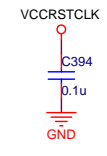
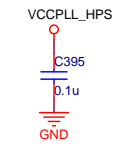
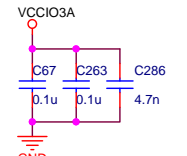
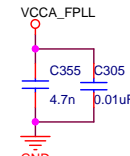
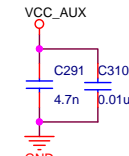
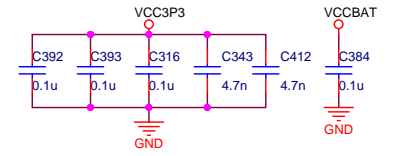
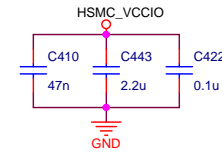
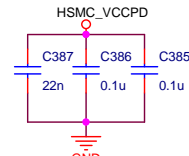
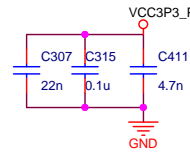
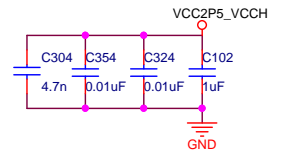
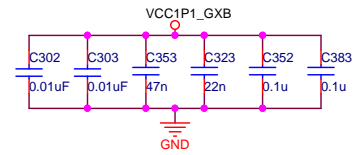
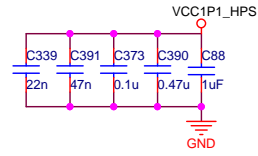
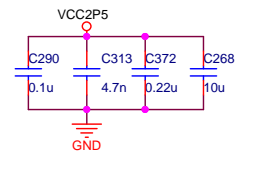
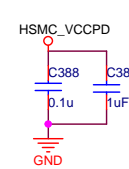
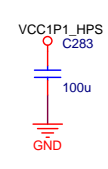
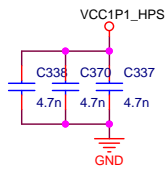
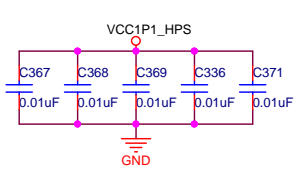
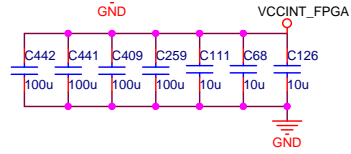
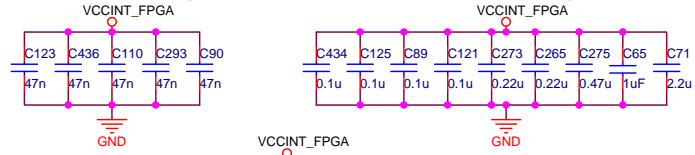
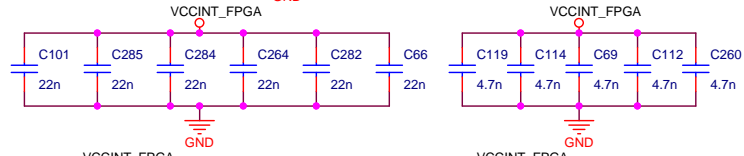
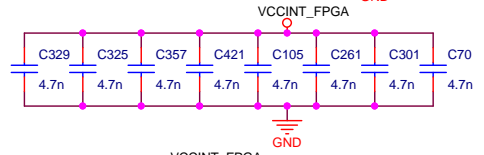
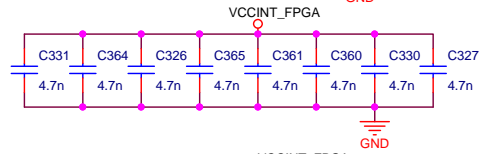
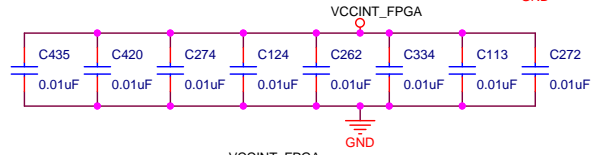
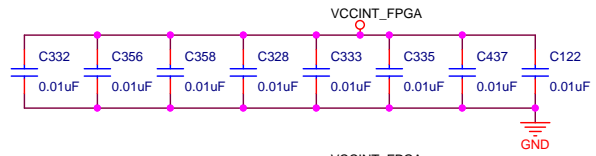
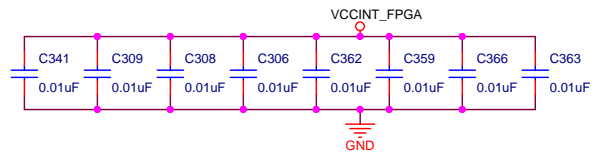





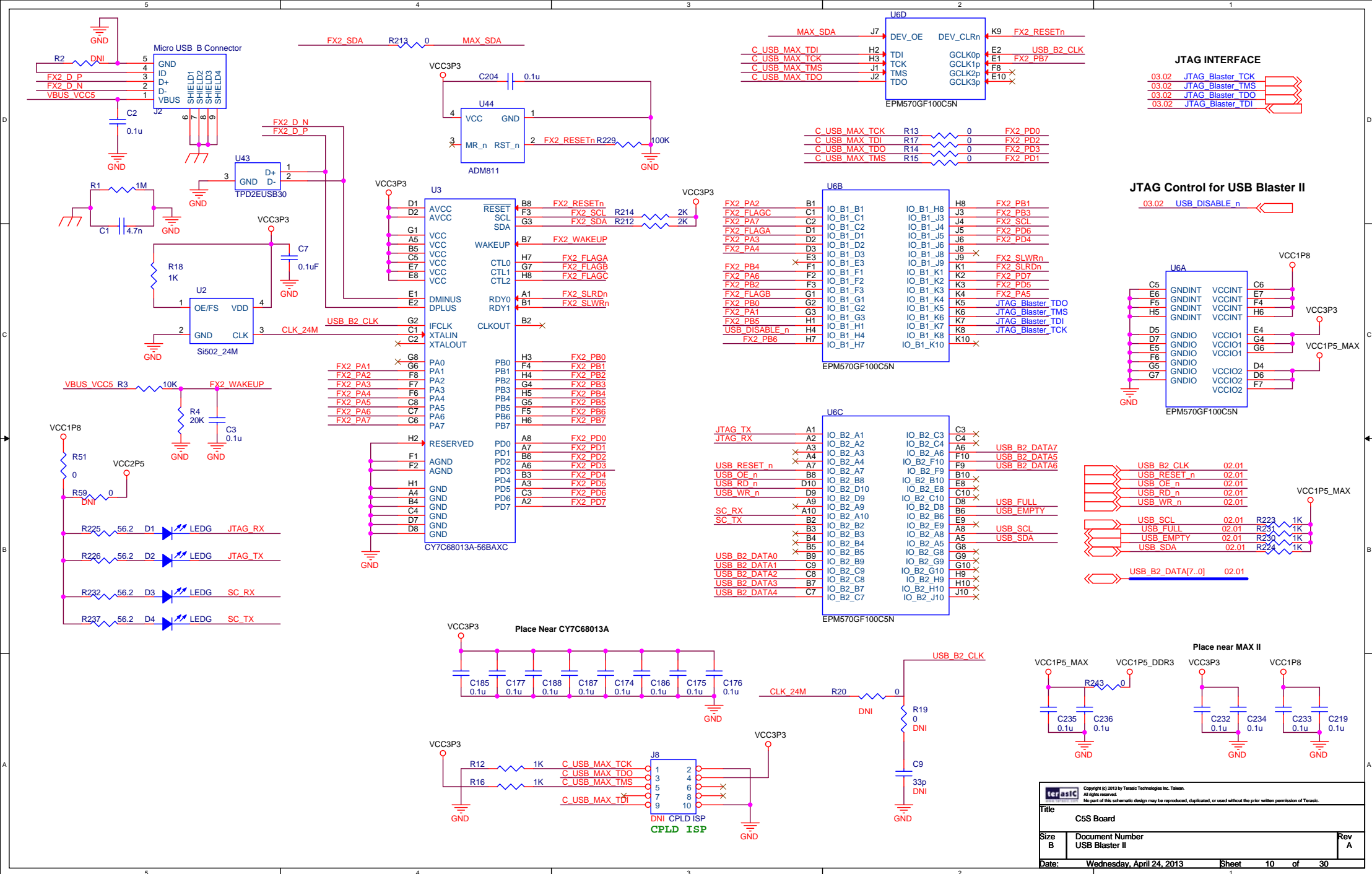








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Title C5S Board		
Size B	Document Number Decoupling	Rev A
Date:	Wednesday, April 24, 2013	Sheet 9 of 30



USB Blaster

03.01	JTAG Blaster TCK	
03.01	JTAG Blaster TMS	
03.01	JTAG Blaster TDO	
03.01	JTAG Blaster TDI	

FPGA JTAG INTERFACE

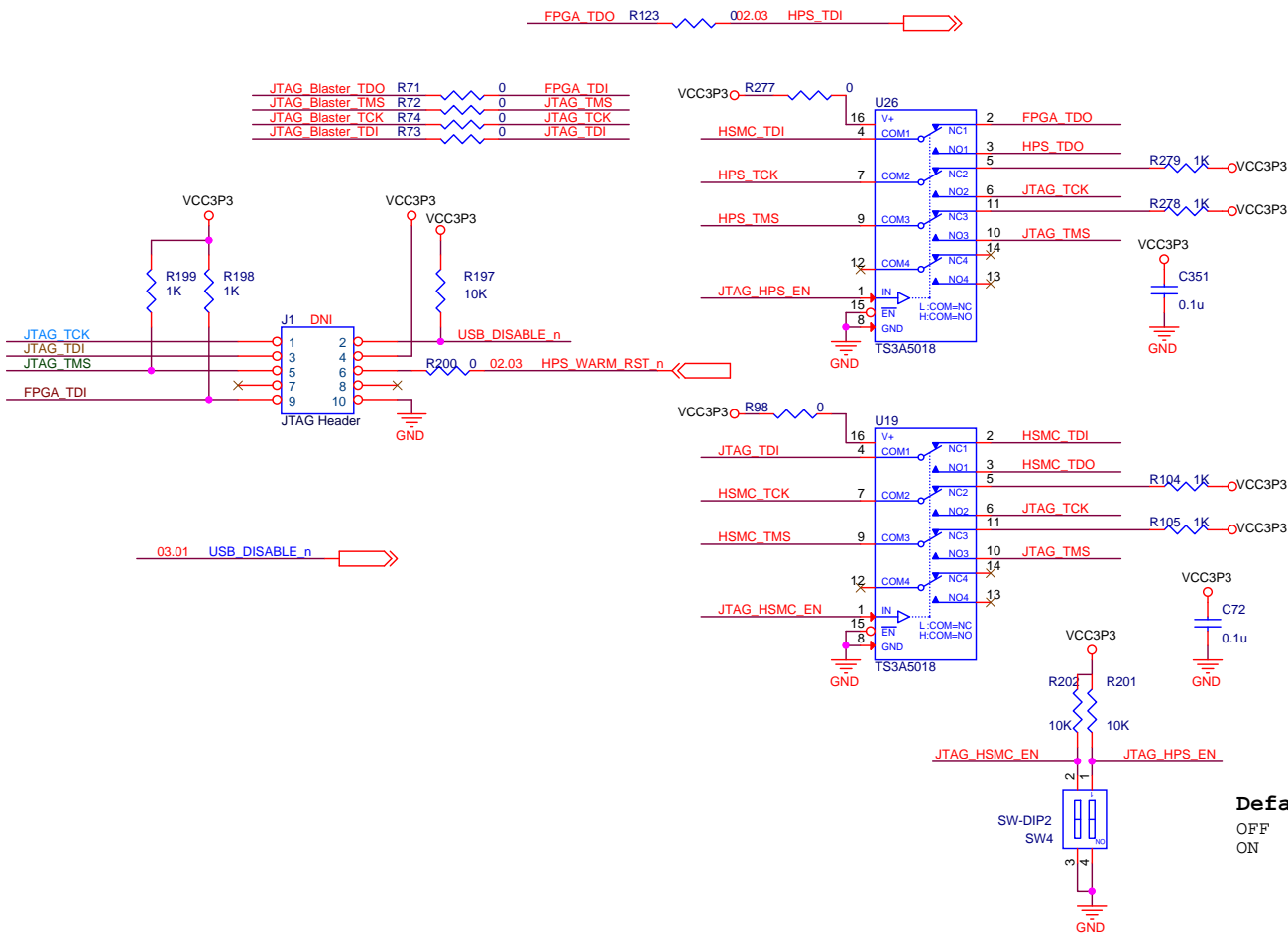
02.06	FPGA TDI	
02.06	JTAG TMS	
02.06	JTAG TCK	
02.06	FPGA TDO	

HSMC JTAG INTERFACE

04.01	HSMC TCK	
04.01	HSMC TMS	
04.01	HSMC TDI	
04.01	HSMC TDO	


HPS JTAG INTERFACE

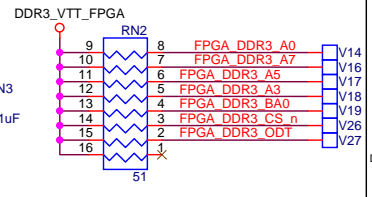
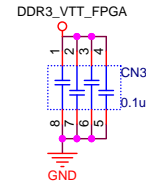
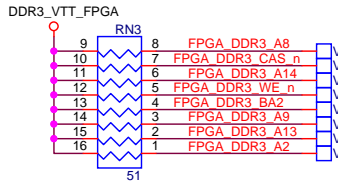
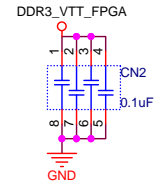
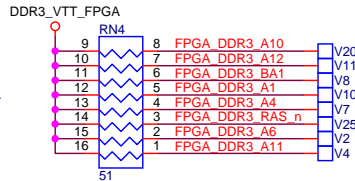
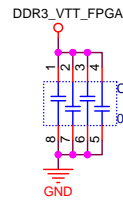
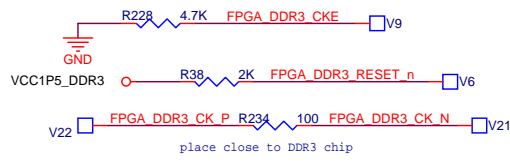
02.03	HPS TCK	
02.03	HPS TMS	
02.03	HPS TDI	
02.03	HPS TDO	



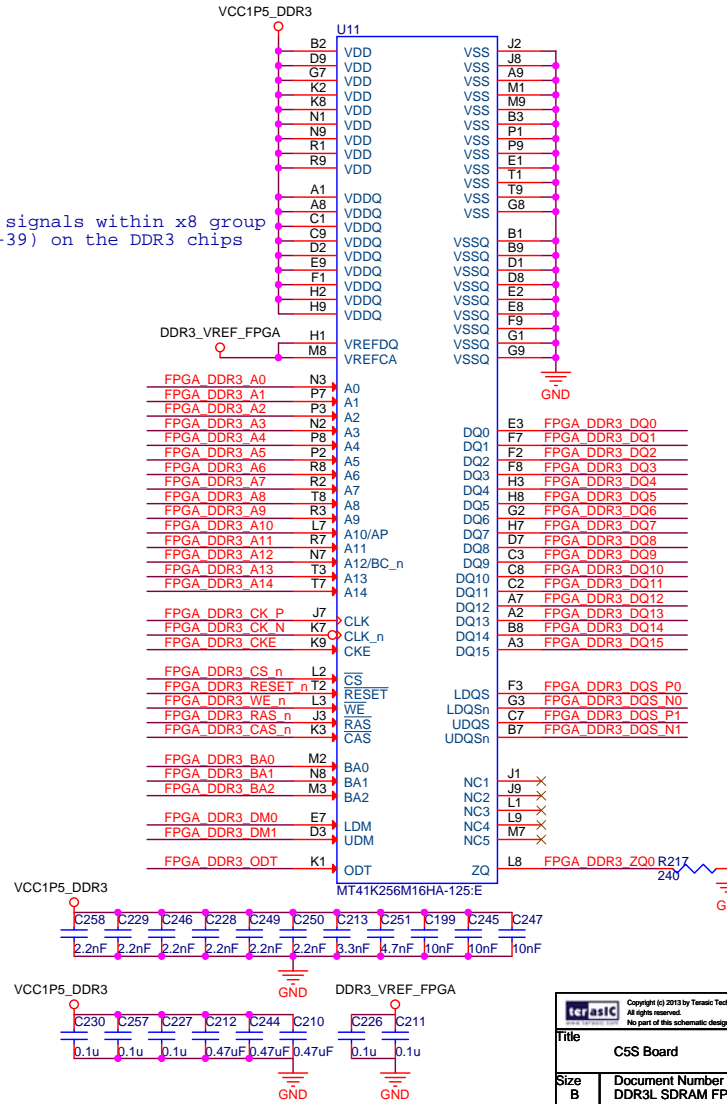
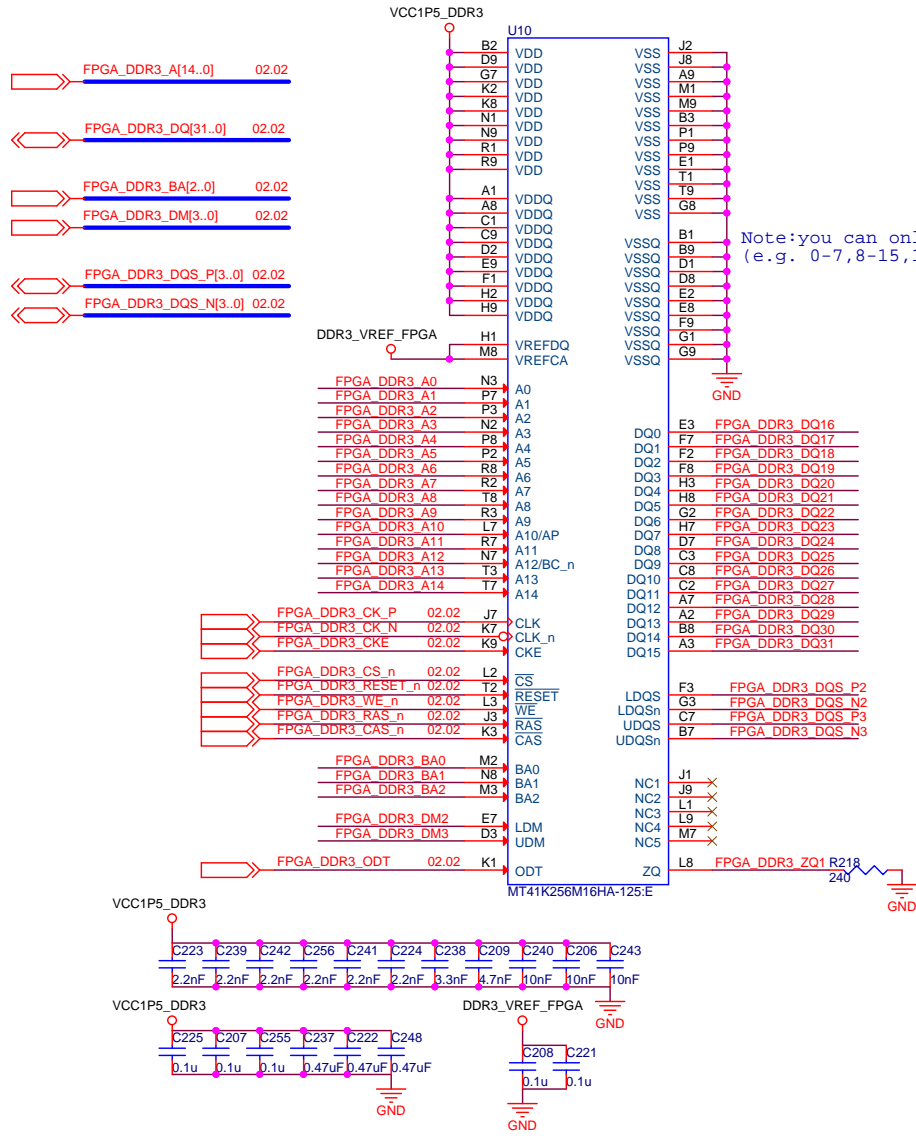
Default Disable (switch OFF)

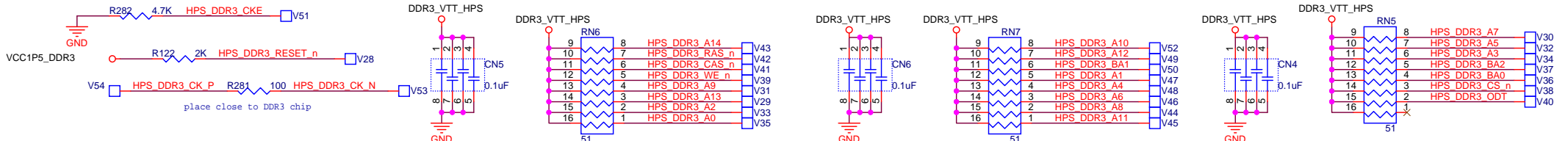
OFF = not-in-chain
ON = in-chain

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Title		
C5S Board		
Size	Document Number	Rev
B	JTAG Chain	A
Date:	Wednesday, April 24, 2013	Sheet 11 of 30



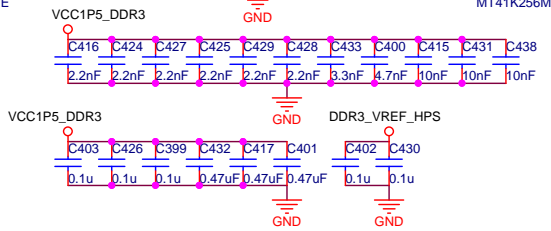
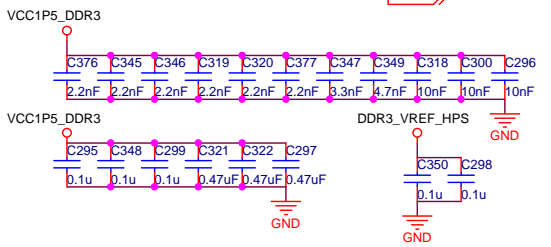
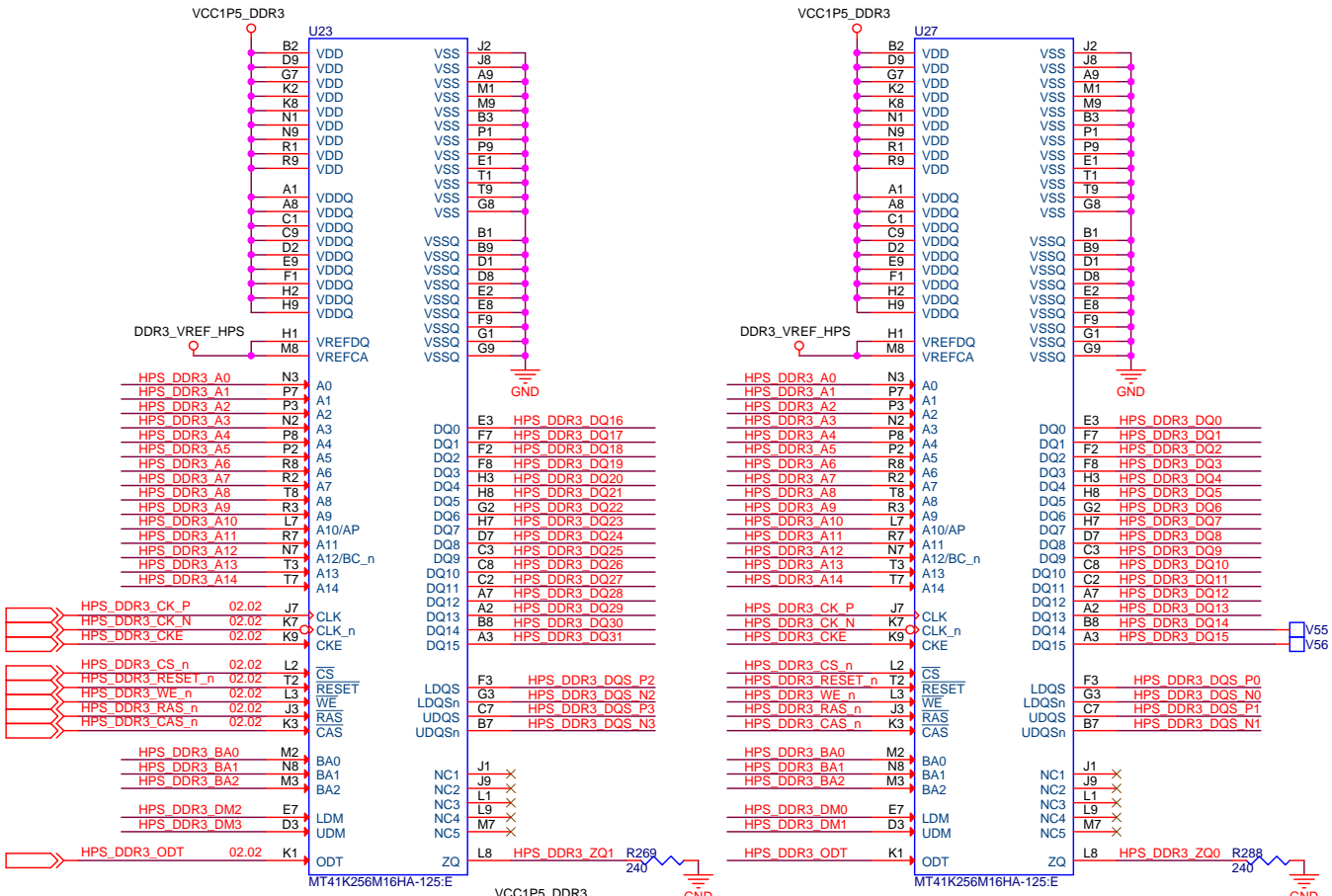
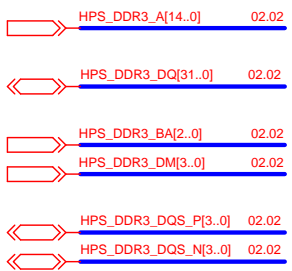
Note:you can swap the signals on the OCT resistor array(include NC pin)

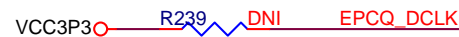
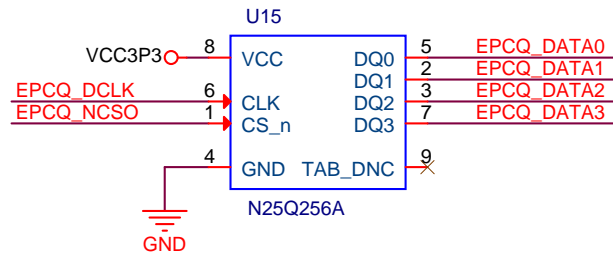
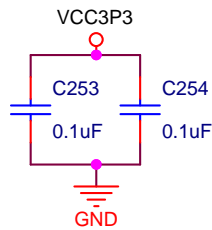
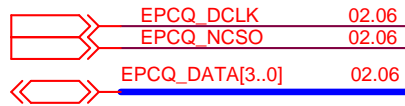




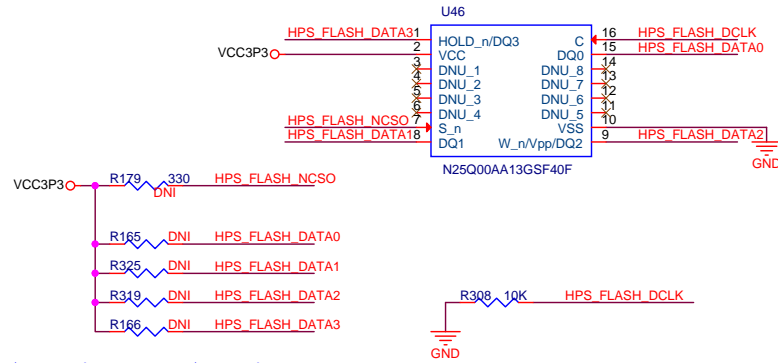
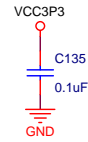
Note: you can only swap the DQ signals within x8 group (e.g. 0-7,8-15,16-23,24-31) on the DDR3 chips

Note: you can swap the signals on the OCT resistor array (include NC pin)




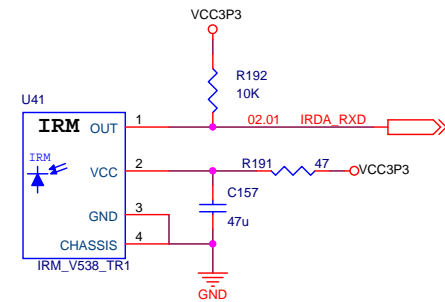
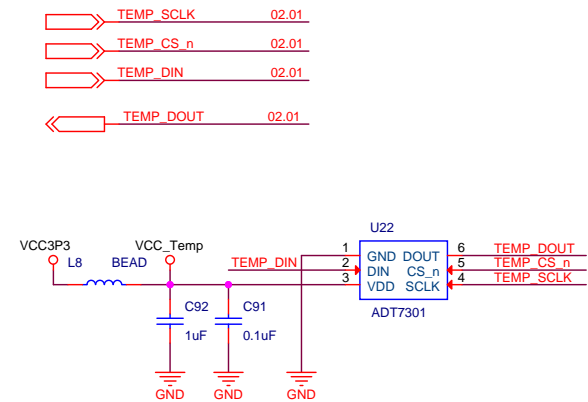
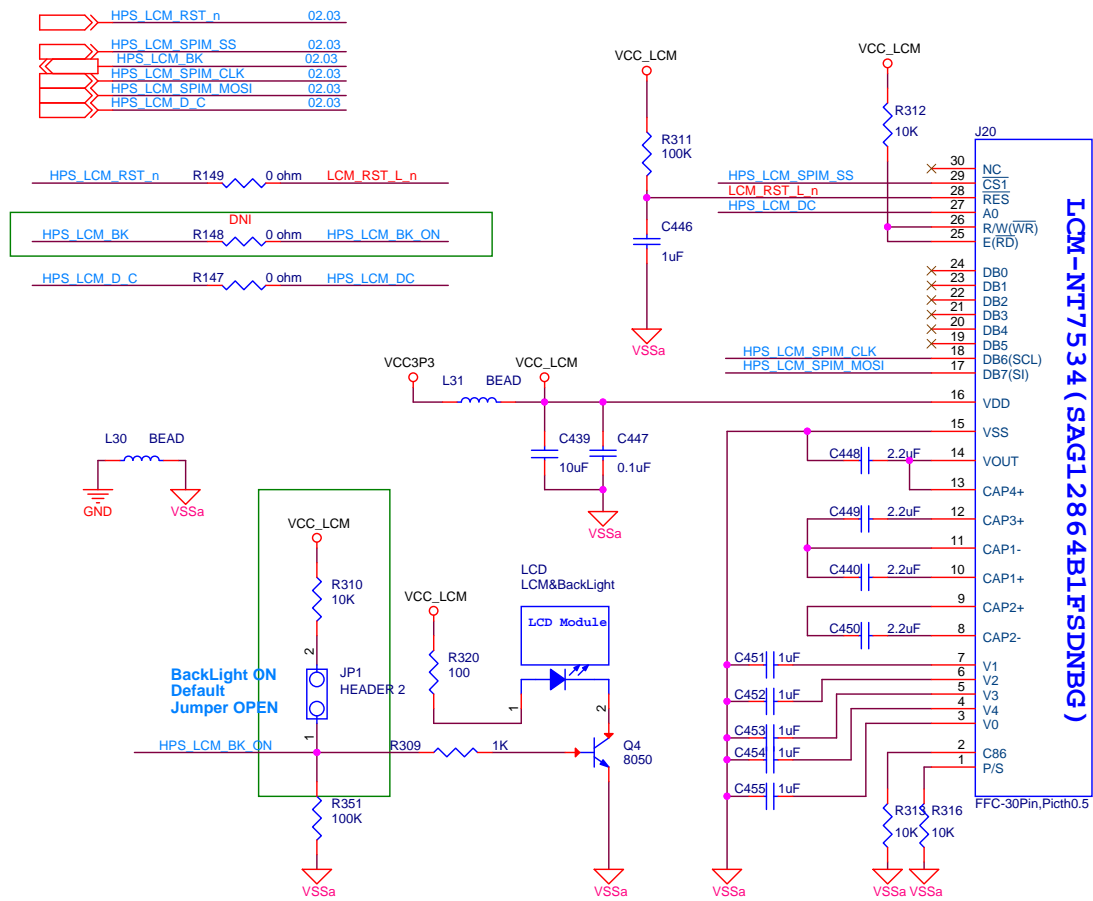


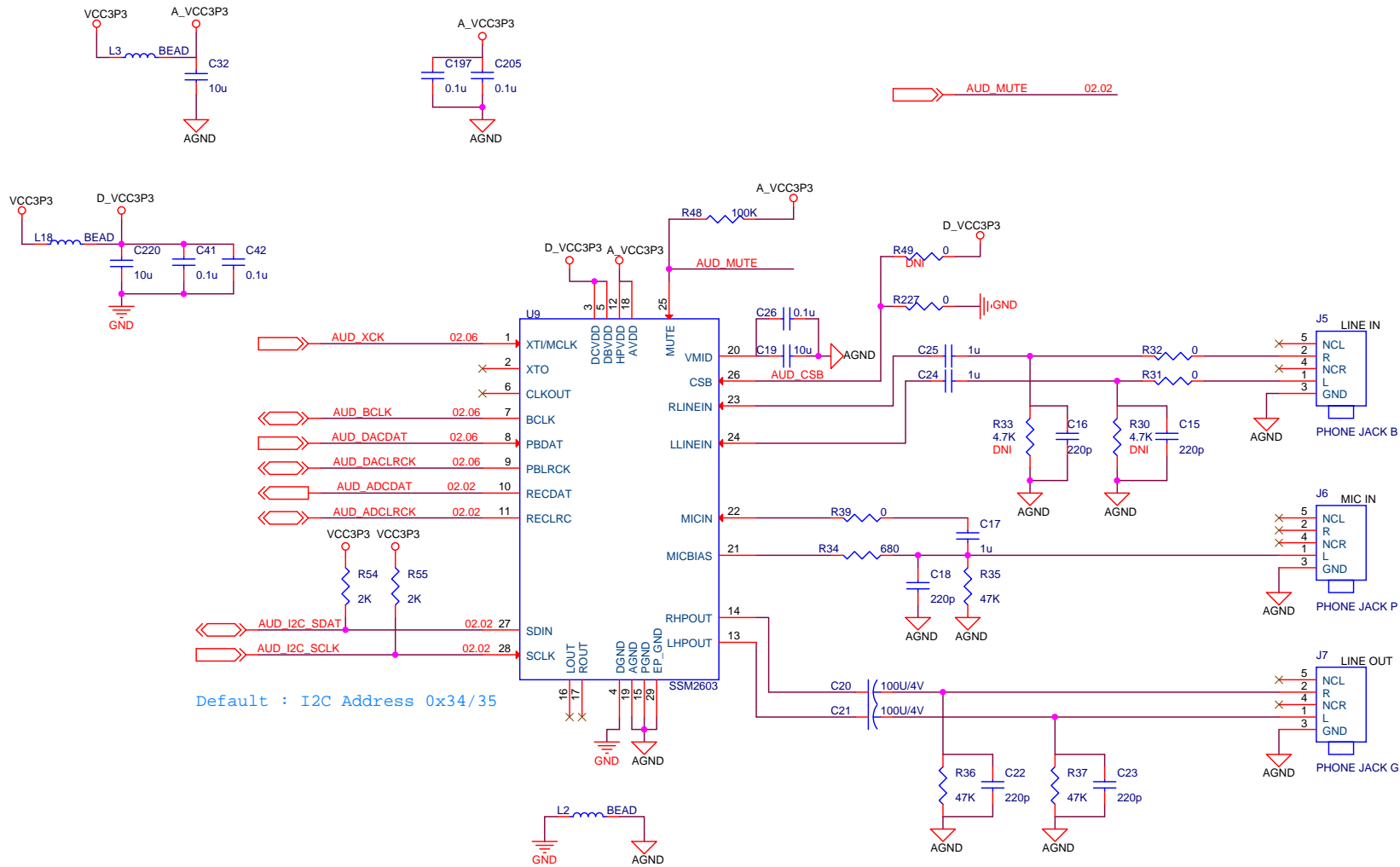
HPS_FLASH_DCLK 02.03
HPS_FLASH_NCSO 02.03
HPS_FLASH_DATA[3..0] 02.03

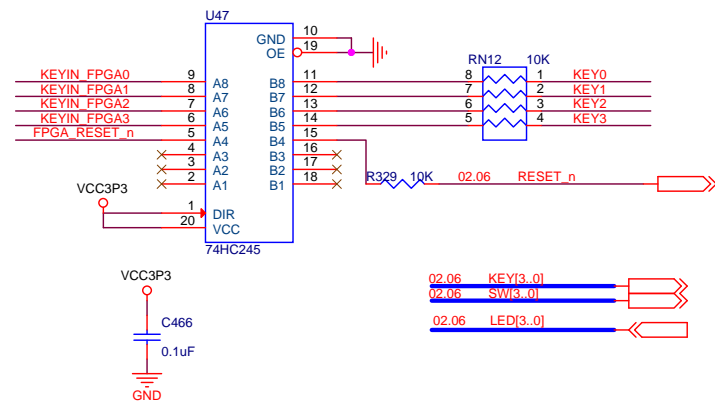
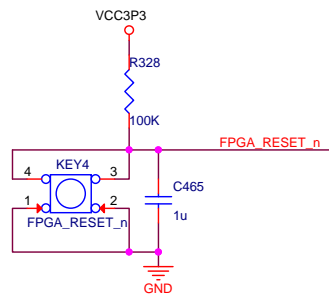
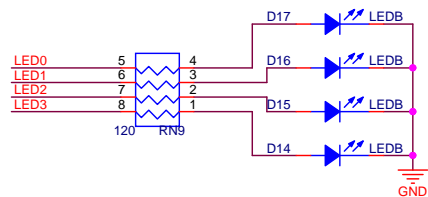
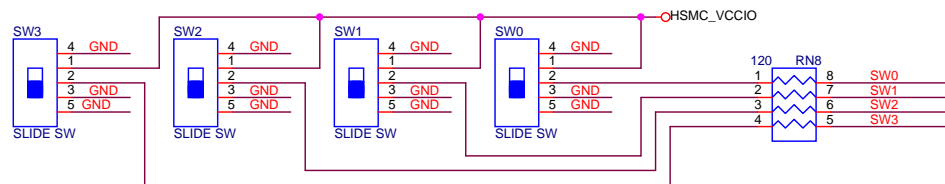
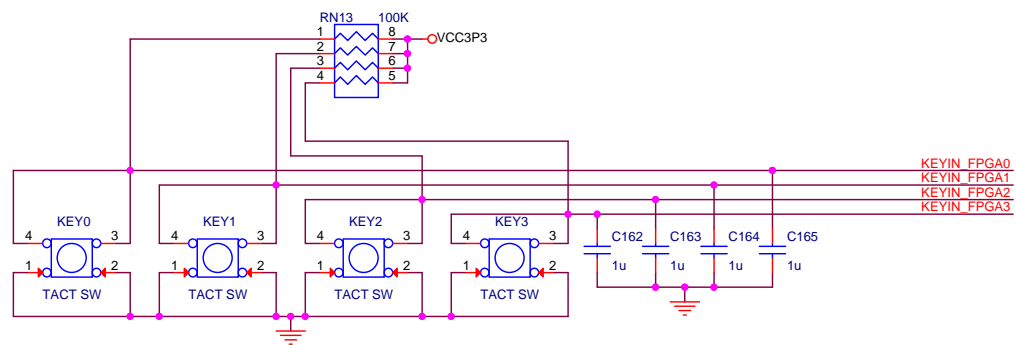


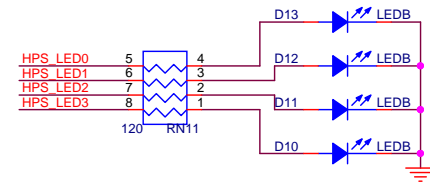
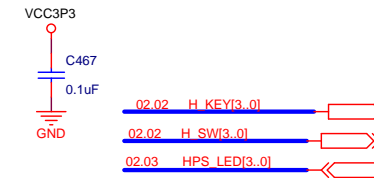
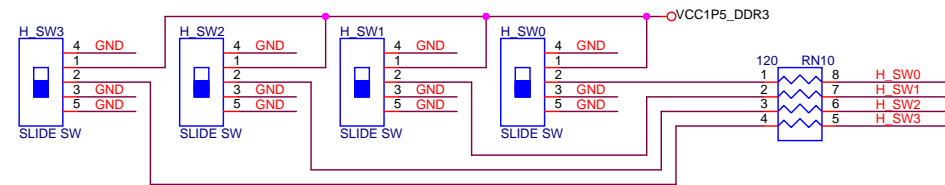
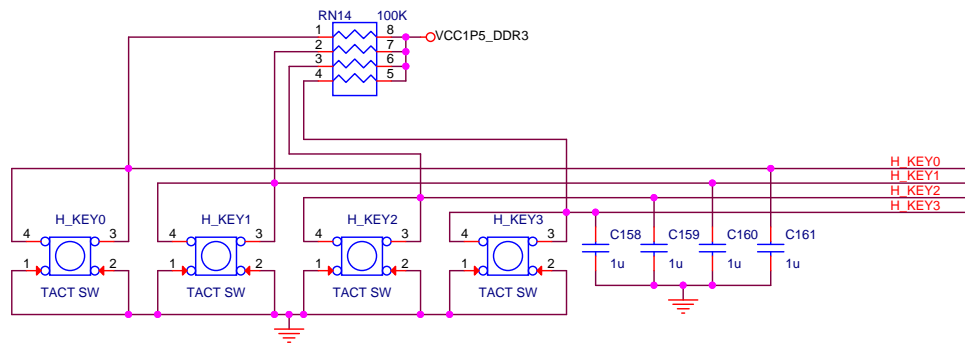
Note: place a pull down resistor on the FLASH_DCLK wire at the Master

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Title C5S Board		
Size B	Document Number QSPI FLASH HPS	Rev A
Date:	Wednesday, April 24, 2013	Sheet 16 of 30

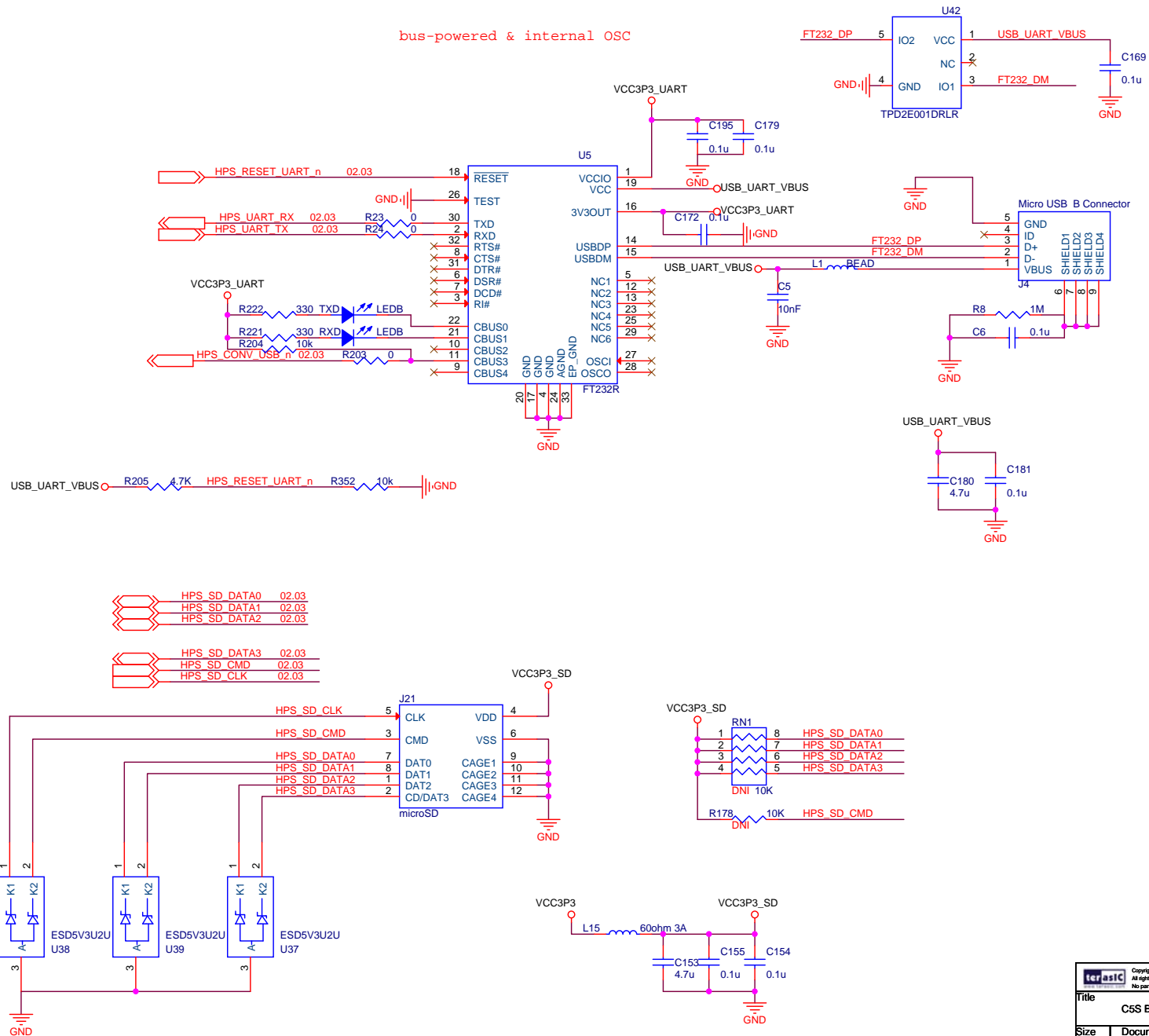


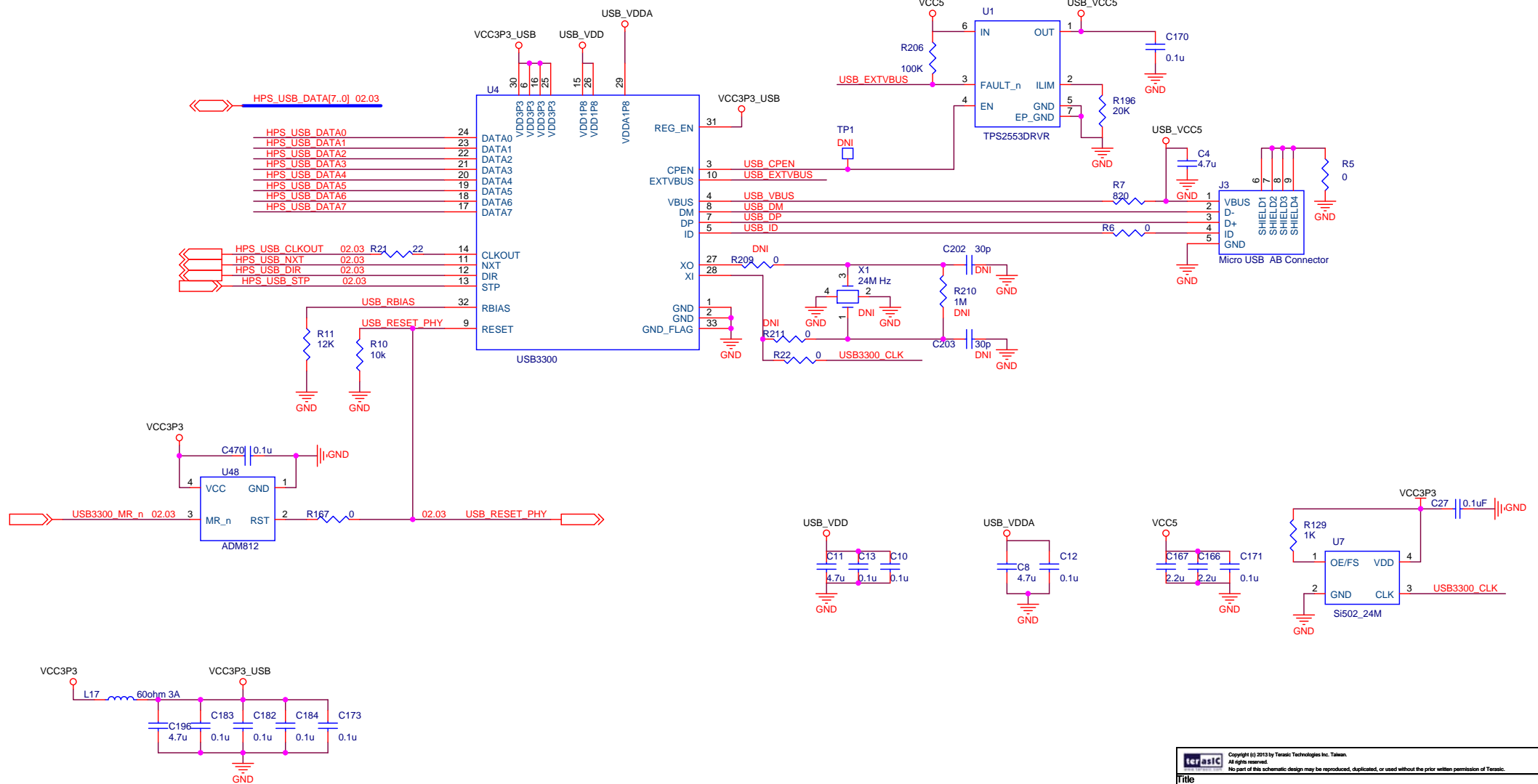






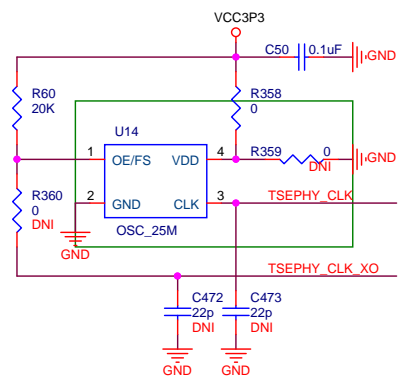
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C5S Board		Rev	
Size	Document Number	Rev	
B	HPS BUTTON & SW	A	
Date:	Wednesday, April 24, 2013	Sheet	21 of 30



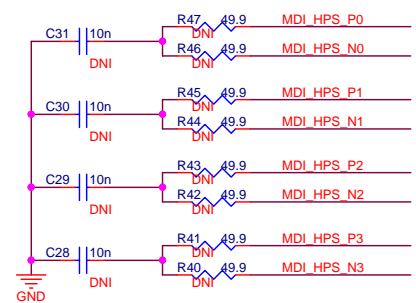
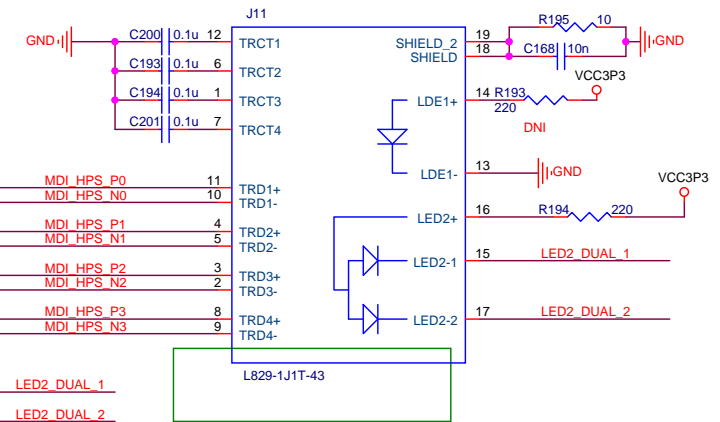
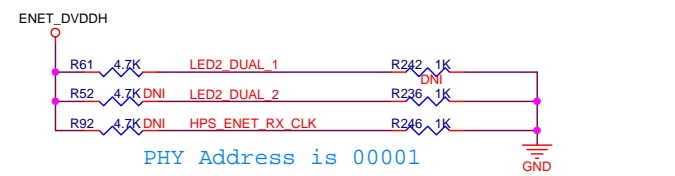
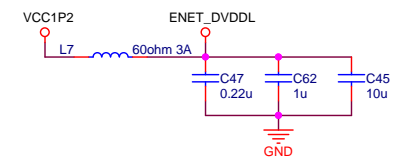
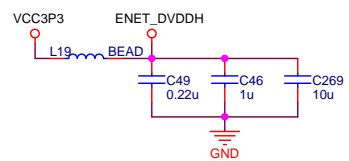
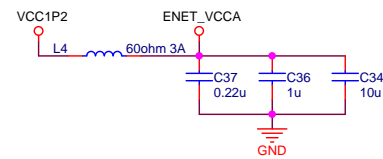
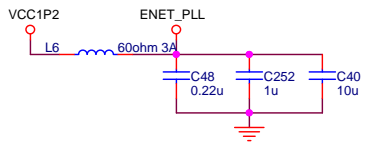
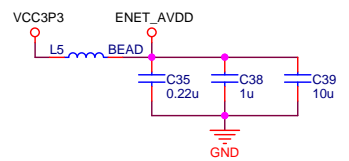
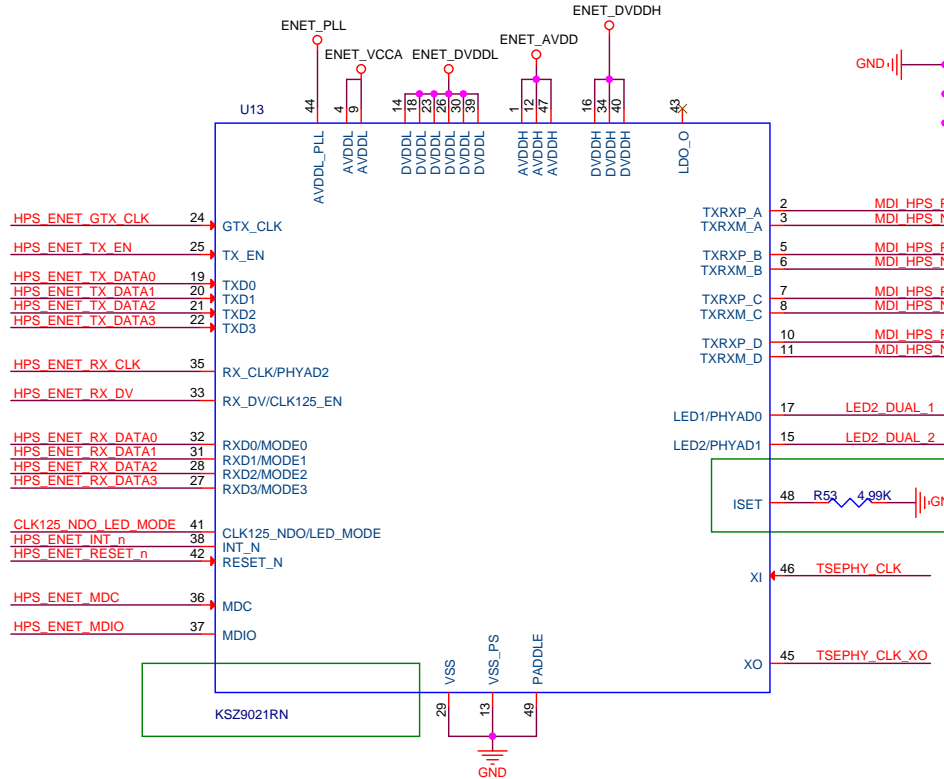
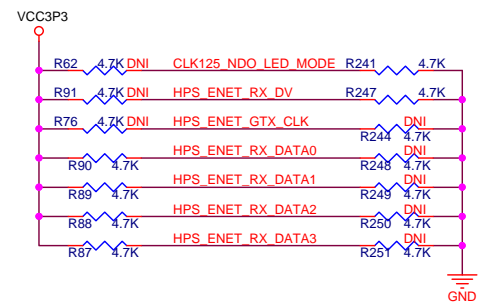


HPS_ENET_TX_DATA[3..0] 02.03
HPS_ENET_GTX_CLK 02.03
HPS_ENET_TX_EN 02.03
HPS_ENET_MDC 02.03
HPS_ENET_RESET_n 02.03

HPS_ENET_RX_DATA[3..0] 02.03
HPS_ENET_RX_CLK 02.03
HPS_ENET_RX_DV 02.03
HPS_ENET_INT_n 02.03
HPS_ENET_MDIO 02.03



VCC3P3
R77 4.7K HPS_ENET_INT_n
R93 4.7K HPS_ENET_MDC
R78 4.7K HPS_ENET_MDIO
R240 4.7K HPS_ENET_RESET_n



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Title			
C5S Board			
Size	Document Number	Rev	
B	TSE PHY	A	
Date:	Wednesday, April 24, 2013	Sheet	24 of 30



HPS_SPIM_CLK 02.03
HPS_SPIM_SS 02.03
HPS_SPIM_MOSI 02.03
HPS_SPIM_MISO 02.03

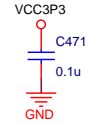
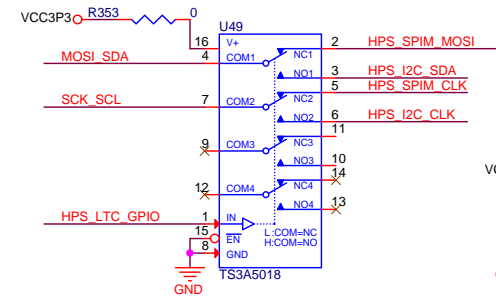
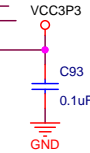
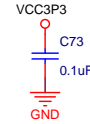
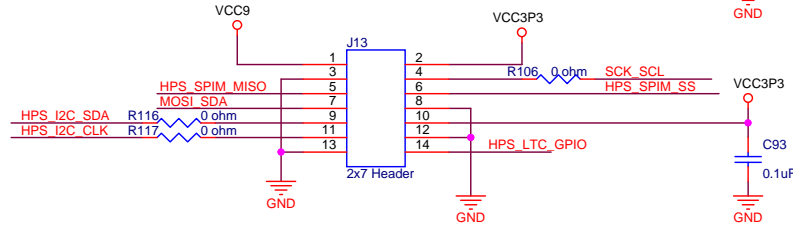
HPS_LTC_GPIO 02.03

HPS_I2C_SDA 02.03,02.06

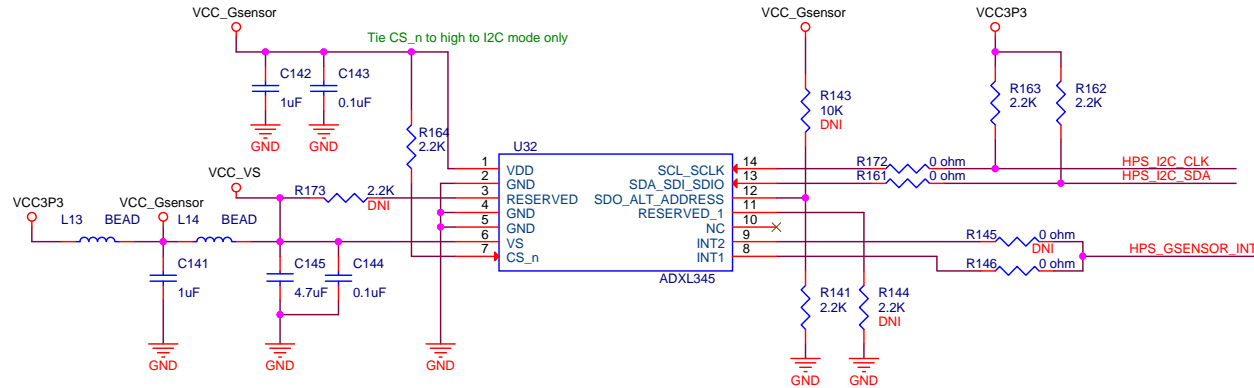
HPS_I2C_CLK 02.03,02.06

HPS_GSENSOR_INT 02.03


LTC 2x7 Connector

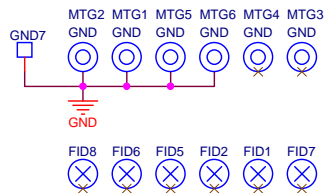


Digital Accelerometer

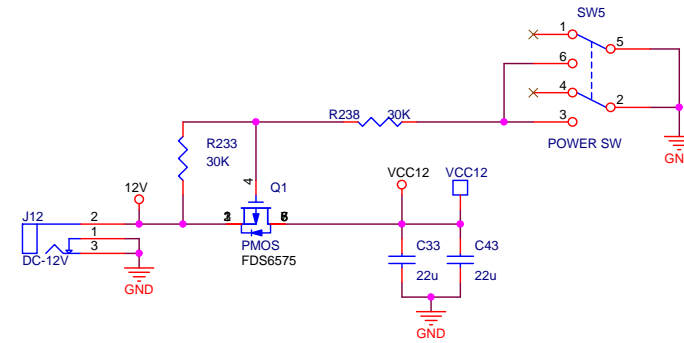
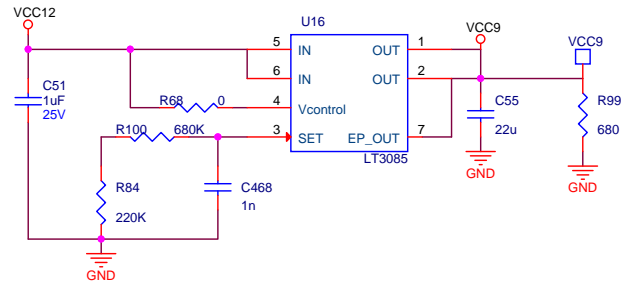


Default : I2C Address 0xA6/0xA7

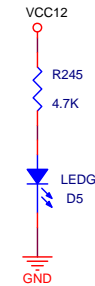
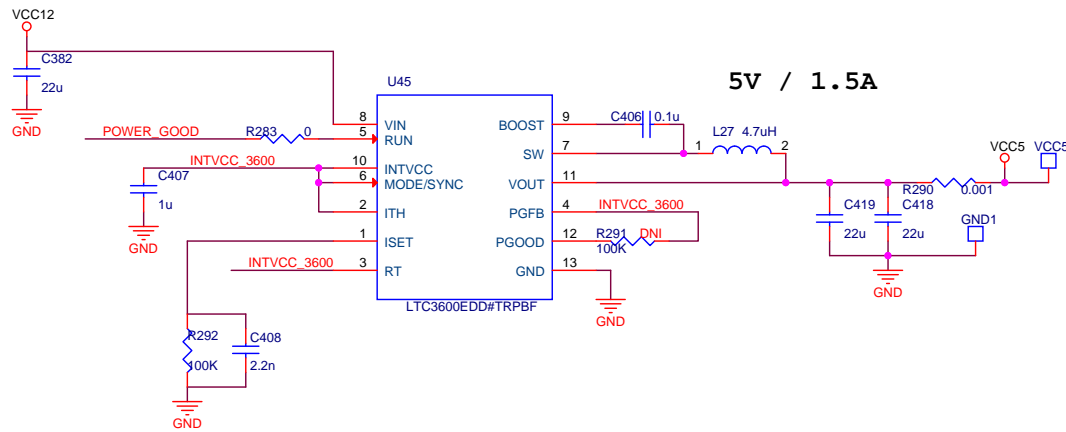
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Title C5S Board		
Size B	Document Number LTC Connector & G sensor	Rev A
Date:	Wednesday, April 24, 2013	Sheet 25 of 30



9V / 50mA

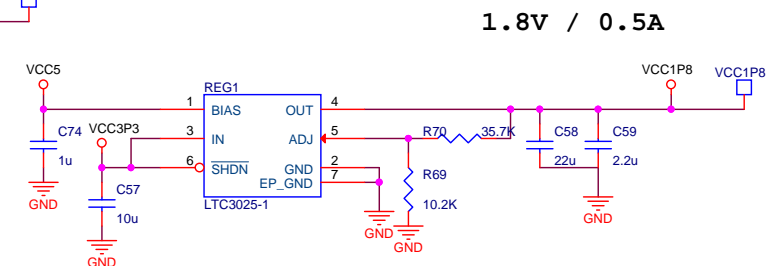
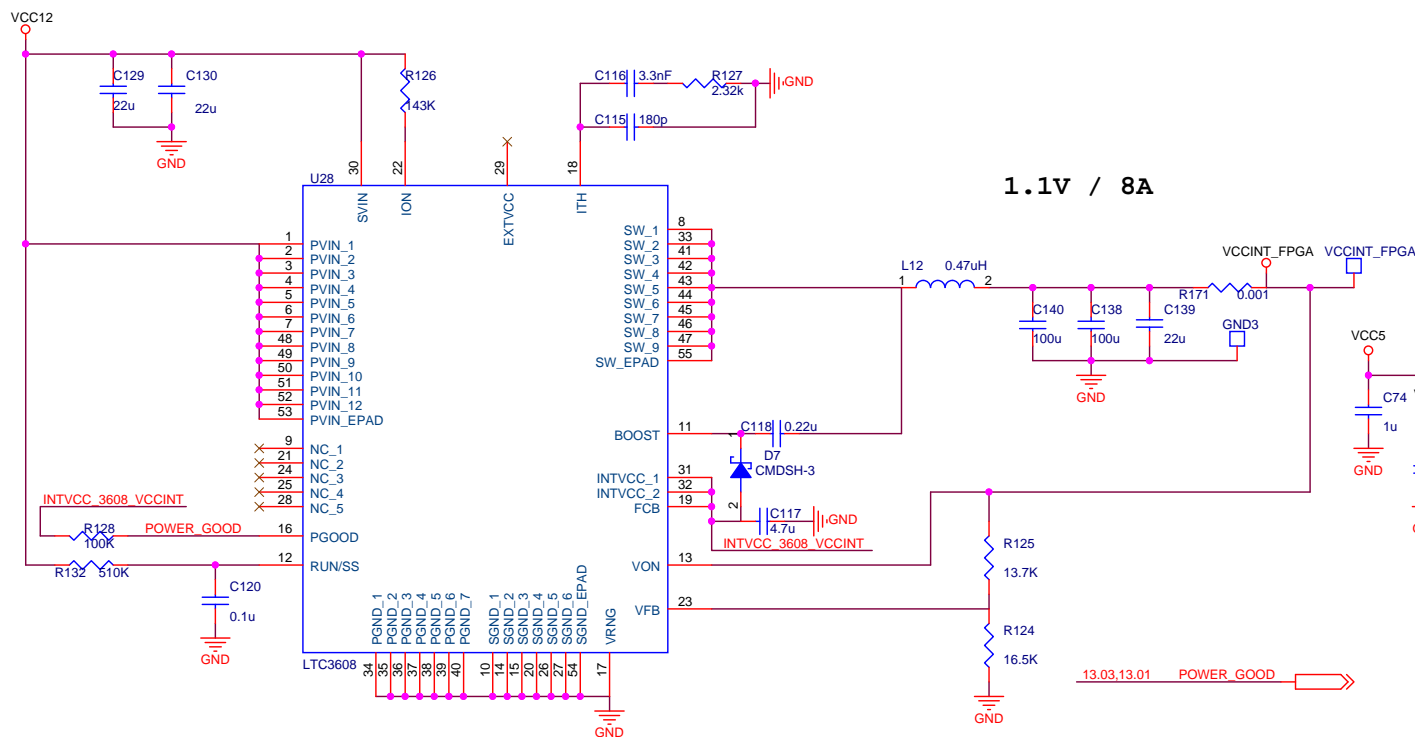
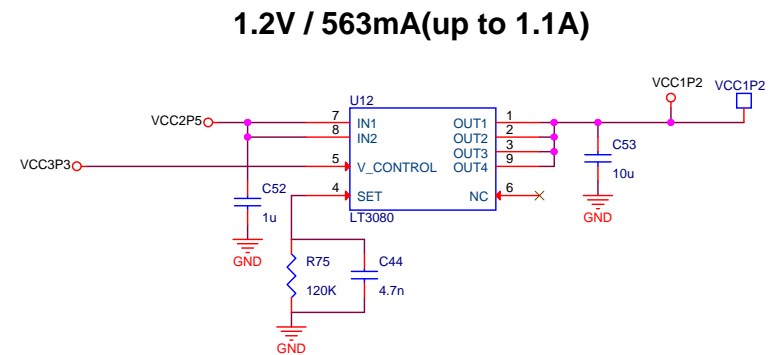
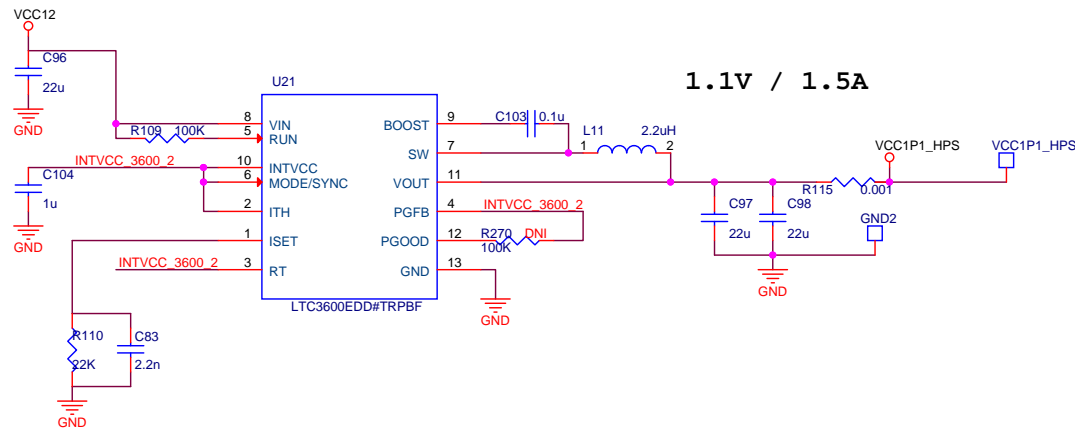


5V / 1.5A



POWER_GOOD 13.02

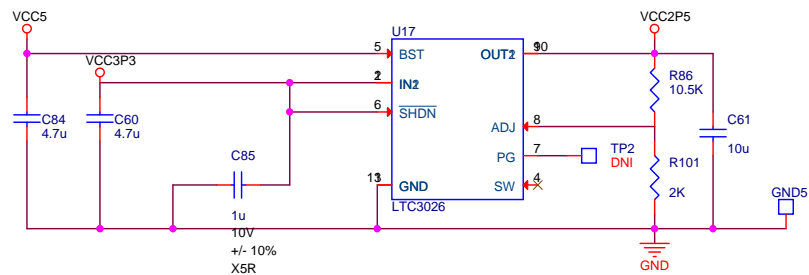
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Title C5S Board			
Size B	Document Number Power - 9V & 5V		Rev A
Date:	Wednesday, April 24, 2013	Sheet 26	of 30



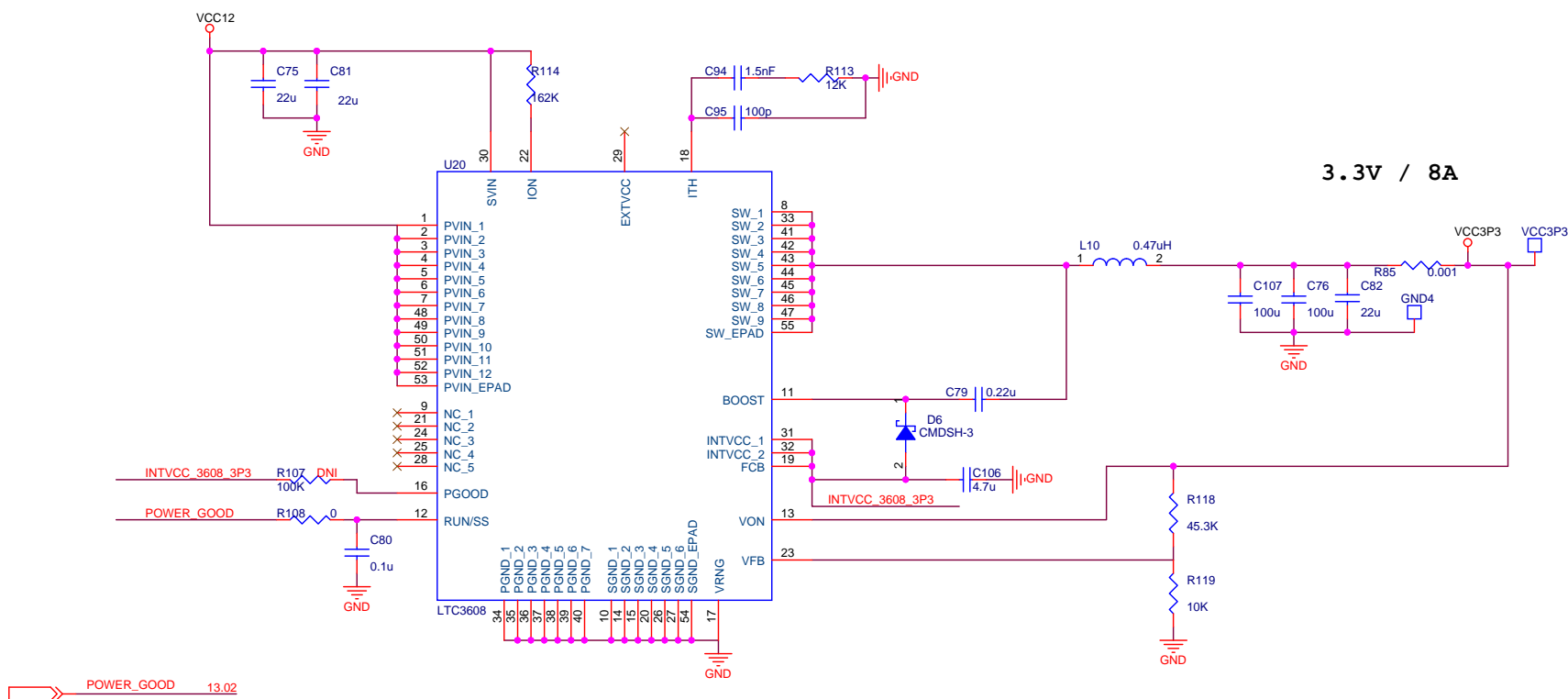
13.03.13.01 POWER GOOD


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Title C5S Board		
Size B	Document Number Power - 1.1V & 1.2V	Rev A
Date: Wednesday, April 24, 2013	Sheet 27	of 30

2.5V / 1.5A

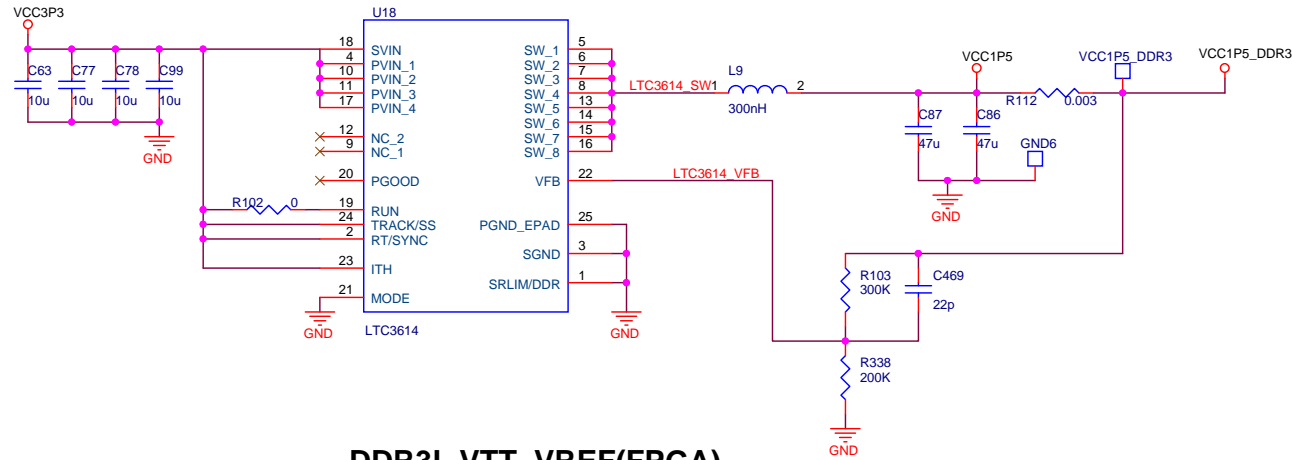


3.3V / 8A

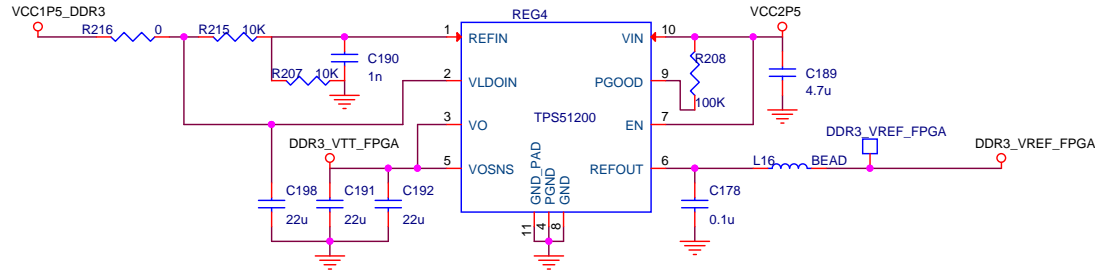


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Title C5S Board		
Size B	Document Number Power - 3.3V & 2.5V	Rev A
Date:	Wednesday, April 24, 2013	Sheet 28 of 30

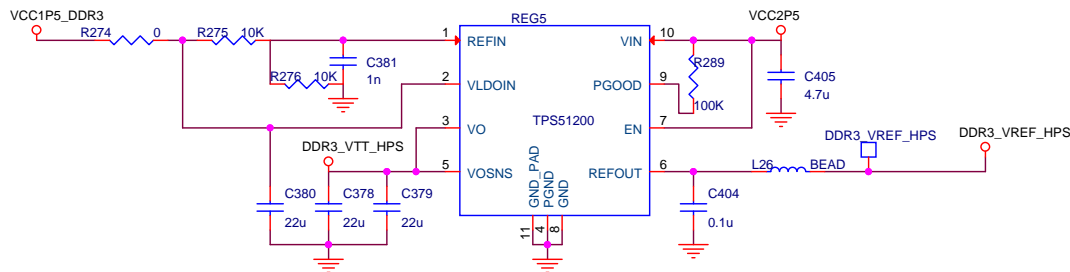
DDR3L VDD,VDDQ




DDR3L VTT, VREF(FPGA)



DDR3L VTT, VREF(HPS)



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Title C5S Board		
Size B	Document Number Power - 1.5V	Rev A
Date:	Wednesday, April 24, 2013	Sheet 29 of 30

