Exercise 3

|  |  |
| --- | --- |
|  | **Compilation Report** |
| **Device Name** | **EP4CE6F17C6** |
| **Total Design** | |
| **Total Logic Elements** | **0** |
| **Total Memory Bits** | **512** |
| **Total Embedded Multiplier 9-Bit Elements** | **1** |
| **Total Pins** | **44** |
| **mult subdesign** | |
| **Logic Cells (mult)** | **0** |
| **Dedicated Logic Registers (mult)** | **0** |
| **Memory Bits (mult)** | **0** |
| **M9Ks (mult)** | **0** |
| **DSP Elements (mult)** | **1** |
| **ram subdesign** | |
| **Logic Cells (ram)** | **0** |
| **Dedicated Logic Registers (ram)** | **0** |
| **Memory Bits (ram)** | **512** |
| **M9Ks (ram)** | **1** |
| **DSP Elements (ram)** | **0** |
| **Control signals & fan-out** | **clk1 / 3** |
| **wren / 1** |

Exercise 4

**Table 2**

|  |  |
| --- | --- |
|  | **Compilation Report** |
| **Device Name** | **EP4CE6F17C6** |
| **Total Design** | |
| **Total Logic Elements** | **107 (104 – Schematic)** |
| **Total Memory Bits** | **512** |
| **Total Embedded Multiplier 9-Bit Elements** | **0** |
| **Total Pins** | **44** |
| **mult subdesign** | |
| **Logic Cells (mult)** | **107 (104 – Schematic)** |
| **Dedicated Logic Registers (mult)** | **64** |
| **Memory Bits (mult)** | **0** |
| **M9Ks (mult)** | **0** |
| **DSP Elements (mult)** | **0** |
| **ram subdesign** | |
| **Logic Cells (ram)** | **0** |
| **Dedicated Logic Registers (mult)** | **0** |
| **Memory Bits (ram)** | **512** |
| **M9Ks (ram)** | **1** |
| **DSP Elements (ram)** | **0** |
| **Control signals & fan-out** | **clk1 / 65** |
| **wren / 1** |