**Synplify Log**

~~@N: CD720 :"C:\Synopsys\fpga\_D201003SP1\lib\vhd\std.vhd":123:18:123:21|Setting time resolution to ns~~

~~@N:"H:\Project\SG\_synthesis\_proj\VHDL\top\_synthesis.vhd":23:7:23:19|Top entity is set to top\_synthesis.~~

~~VHDL syntax check successful!~~

~~File H:\Project\SG\_synthesis\_proj\VHDL\top\_synthesis.vhd changed - recompiling~~

~~@N: CD231 :"C:\Synopsys\fpga\_D201003SP1\lib\vhd\std\_logic\_textio.vhd":79:15:79:16|Using onehot encoding for type mvl9plus ('U'="1000000000")~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\top\_synthesis.vhd":23:7:23:19|Synthesizing work.top\_synthesis.top\_synthesis\_rtl~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\mds\_top.vhd":31:7:31:13|Synthesizing work.mds\_top.rtl\_mds\_top~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\led.vhd":26:7:26:9|Synthesizing work.led.led\_rtl~~

~~Post processing for work.led.led\_rtl~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path.vhd":25:7:25:13|Synthesizing work.tx\_path.arc\_tx\_path~~

~~@W: CD326 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path.vhd":624:1:624:10|Port used of entity work.general\_fifo is unconnected~~

~~@W: CD326 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path.vhd":624:1:624:10|Port aempty of entity work.general\_fifo is unconnected~~

~~@W: CD326 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path.vhd":624:1:624:10|Port afull of entity work.general\_fifo is unconnected~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":25:7:25:17|Synthesizing work.tx\_path\_wbm.rtl\_tx\_path\_wbm~~

~~@N: CD233 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":69:17:69:18|Using sequential encoding for type wbm\_states~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":170:6:170:16|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":181:6:181:16|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":182:6:182:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":194:7:194:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":195:7:195:19|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":196:7:196:20|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":202:5:202:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":203:5:203:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":204:5:204:18|Removed redundant assignment~~

~~@W: CD604 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":221:4:221:17|OTHERS clause is not synthesized~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":249:4:249:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":251:4:251:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":263:4:263:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":265:4:265:17|Removed redundant assignment~~

~~Post processing for work.tx\_path\_wbm.rtl\_tx\_path\_wbm~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\wbs\_reg.vhd":26:7:26:13|Synthesizing work.wbs\_reg.rtl\_wbs\_reg~~

~~Post processing for work.wbs\_reg.rtl\_wbs\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment~~

~~Post processing for work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment~~

~~Post processing for work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment~~

~~Post processing for work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment~~

~~Post processing for work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment~~

~~Post processing for work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":61:7:61:18|Synthesizing work.general\_fifo.arc\_general\_fifo~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":245:6:245:10|Removed redundant assignment~~

~~Post processing for work.general\_fifo.arc\_general\_fifo~~

~~@N: CL134 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":96:7:96:9|Found RAM mem, depth=9, width=8~~

~~@N: CL177 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":136:2:136:3|Sharing sequential element read\_addr\_dup.~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\ram\_simple.vhd":45:7:45:16|Synthesizing work.ram\_simple.arc\_ram\_simple~~

~~Post processing for work.ram\_simple.arc\_ram\_simple~~

~~@N: CL134 :"H:\Project\SG\_synthesis\_proj\VHDL\ram\_simple.vhd":69:7:69:14|Found RAM ram\_data, depth=1024, width=8~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\checksum\_calc.vhd":62:7:62:19|Synthesizing work.checksum\_calc.arc\_checksum\_calc~~

@W: CG296 :"H:\Project\SG\_synthesis\_proj\VHDL\checksum\_calc.vhd":120:24:120:30|Incomplete sensitivity list - assuming completeness

@W: CG290 :"H:\Project\SG\_synthesis\_proj\VHDL\checksum\_calc.vhd":123:15:123:31|Referenced variable checksum\_init\_val is not in sensitivity list

~~Post processing for work.checksum\_calc.arc\_checksum\_calc~~

~~@W: CL170 :"H:\Project\SG\_synthesis\_proj\VHDL\checksum\_calc.vhd":122:1:122:2|Pruning bit <8> of checksum\_i(8 downto 0) - not in use ...~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":44:7:44:12|Synthesizing work.mp\_enc.rtl\_mp\_enc~~

~~@N: CD231 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":101:23:101:24|Using onehot encoding for type mp\_encoder\_states (idle\_st="100000000")~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":327:7:327:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":329:7:329:16|Removed redundant assignment~~

~~@W: CD604 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":377:5:377:18|OTHERS clause is not synthesized~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":384:4:384:9|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":386:4:386:13|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":387:4:387:10|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":450:5:450:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":451:5:451:13|Removed redundant assignment~~

~~Post processing for work.mp\_enc.rtl\_mp\_enc~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit eof\_blk(0) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit eof\_blk(1) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit eof\_blk(2) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit eof\_blk(4) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit eof\_blk(5) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit sof\_blk(0) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit sof\_blk(1) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit sof\_blk(3) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit sof\_blk(4) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit sof\_blk(7) to a constant 0~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 5 of eof\_blk(7 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 4 of eof\_blk(7 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 2 of eof\_blk(7 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 1 of eof\_blk(7 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 0 of eof\_blk(7 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 7 of sof\_blk(7 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 4 of sof\_blk(7 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 3 of sof\_blk(7 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 1 of sof\_blk(7 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 0 of sof\_blk(7 downto 0)~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_tx.vhd":39:7:39:13|Synthesizing work.uart\_tx.arc\_uart\_tx~~

~~@N: CD233 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_tx.vhd":70:24:70:25|Using sequential encoding for type uart\_tx\_fsm\_states~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_tx.vhd":157:7:157:13|Removed redundant assignment~~

~~@W: CD604 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_tx.vhd":162:5:162:18|OTHERS clause is not synthesized~~

~~Post processing for work.uart\_tx.arc\_uart\_tx~~

~~Post processing for work.tx\_path.arc\_tx\_path~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":26:7:26:13|Synthesizing work.rx\_path.rtl\_rx\_path~~

~~@N: CD231 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":82:16:82:17|Using onehot encoding for type wbm\_states (wbm\_idle\_st="100000")~~

~~@W: CD326 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":270:1:270:9|Port parity\_err of entity work.uart\_rx is unconnected~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":457:5:457:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":466:6:466:21|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":472:7:472:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":473:7:473:22|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":474:7:474:20|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":481:7:481:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":487:6:487:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":488:6:488:21|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":490:6:490:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":494:5:494:20|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":495:5:495:16|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":496:5:496:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":500:6:500:21|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":519:5:519:20|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":526:6:526:20|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":527:6:527:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":535:6:535:21|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":548:6:548:21|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":549:6:549:15|Removed redundant assignment~~

~~@W: CD604 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":552:4:552:17|OTHERS clause is not synthesized~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":578:4:578:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":582:5:582:16|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":586:4:586:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":587:4:587:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":617:4:617:12|Removed redundant assignment~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":52:7:52:12|Synthesizing work.mp\_dec.rtl\_mp\_dec~~

~~@N: CD231 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":108:19:108:20|Using onehot encoding for type mp\_dec\_states (sof\_st="1000000")~~

~~@W: CD604 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":310:5:310:18|OTHERS clause is not synthesized~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":337:5:337:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":340:4:340:10|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":445:4:445:12|Removed redundant assignment~~

~~@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":152:7:152:12|Signal sof\_sr is undriven~~

~~@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":153:7:153:16|Signal sof\_sr\_cnt is undriven~~

~~Post processing for work.mp\_dec.rtl\_mp\_dec~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":328:2:328:3|Optimizing register bit eof\_blk(0) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":328:2:328:3|Optimizing register bit eof\_blk(1) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":328:2:328:3|Optimizing register bit eof\_blk(2) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":328:2:328:3|Optimizing register bit eof\_blk(4) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":328:2:328:3|Optimizing register bit eof\_blk(5) to a constant 0~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":328:2:328:3|Pruning Register bit 5 of eof\_blk(7 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":328:2:328:3|Pruning Register bit 4 of eof\_blk(7 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":328:2:328:3|Pruning Register bit 2 of eof\_blk(7 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":328:2:328:3|Pruning Register bit 1 of eof\_blk(7 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":328:2:328:3|Pruning Register bit 0 of eof\_blk(7 downto 0)~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_rx.vhd":46:7:46:13|Synthesizing work.uart\_rx.arc\_uart\_rx~~

~~@N: CD231 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_rx.vhd":74:24:74:25|Using onehot encoding for type uart\_rx\_fsm\_states (idle\_st="10000")~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_rx.vhd":162:8:162:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_rx.vhd":231:7:231:16|Removed redundant assignment~~

~~@W: CD604 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_rx.vhd":302:4:302:17|OTHERS clause is not synthesized~~

~~Post processing for work.uart\_rx.arc\_uart\_rx~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_rx.vhd":119:2:119:3|Optimizing register bit parity\_bit to a constant 0~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_rx.vhd":119:2:119:3|Pruning Register parity\_bit~~

~~Post processing for work.rx\_path.rtl\_rx\_path~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\sdram\_controller.vhd":42:7:42:22|Synthesizing work.sdram\_controller.rtl\_sdram\_controller~~

~~@N: CD231 :"H:\Project\SG\_synthesis\_proj\VHDL\sdram\_controller.vhd":127:18:127:19|Using onehot encoding for type main\_states (idle\_st="1000000000000000")~~

~~@N: CD231 :"H:\Project\SG\_synthesis\_proj\VHDL\sdram\_controller.vhd":116:18:116:19|Using onehot encoding for type init\_states (init\_idle\_st="10000000")~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\sdram\_controller.vhd":456:4:456:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\sdram\_controller.vhd":559:3:559:16|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\sdram\_controller.vhd":592:4:592:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\sdram\_controller.vhd":597:4:597:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\sdram\_controller.vhd":603:4:603:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\sdram\_controller.vhd":633:4:633:14|Removed redundant assignment~~

~~Post processing for work.sdram\_controller.rtl\_sdram\_controller~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":35:7:35:19|Synthesizing work.disp\_ctrl\_top.rtl\_disp\_ctrl\_top~~

~~@W: CD326 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":972:0:972:11|Port wrfull of entity work.dc\_fifo is unconnected~~

~~@W: CD326 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":994:0:994:11|Port used of entity work.general\_fifo is unconnected~~

~~@W: CD326 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":994:0:994:11|Port aempty of entity work.general\_fifo is unconnected~~

~~@W: CD326 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":994:0:994:11|Port afull of entity work.general\_fifo is unconnected~~

@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":156:7:156:23|Signal dc\_fifo\_wr\_en\_log is undriven

@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":177:7:177:19|Signal sc\_fifo\_rd\_en is undriven

@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":179:7:179:17|Signal dc\_fifo\_din is undriven

@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":180:7:180:19|Signal dc\_fifo\_wr\_en is undriven

@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":220:7:220:28|Signal left\_frame\_reg\_din\_ack is undriven

@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":222:7:222:31|Signal left\_frame\_reg\_dout\_valid is undriven

@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":223:7:223:29|Signal right\_frame\_reg\_din\_ack is undriven

@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":225:7:225:32|Signal right\_frame\_reg\_dout\_valid is undriven

@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":255:7:255:17|Signal opu\_data\_in is undriven

@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":256:7:256:23|Signal opu\_data\_in\_valid is undriven

@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":271:7:271:12|Signal zero\_s is undriven

@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":272:7:272:13|Signal zeros\_s is undriven

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\Symbol\_Generator\_Top.vhd":23:7:23:26|Synthesizing work.symbol\_generator\_top.rtl\_symbol\_generator\_top~~

@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\Symbol\_Generator\_Top.vhd":208:8:208:22|Signal opu\_data\_in\_cnt is undriven

@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\Symbol\_Generator\_Top.vhd":239:8:239:19|Signal fifo\_a\_flush is undriven

@W: CD638 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\Symbol\_Generator\_Top.vhd":240:8:240:19|Signal fifo\_b\_flush is undriven

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\mux2.vhd":30:7:30:10|Synthesizing work.mux2.mux2\_rtl~~

~~Post processing for work.mux2.mux2\_rtl~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":61:7:61:18|Synthesizing work.general\_fifo.arc\_general\_fifo~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":245:6:245:10|Removed redundant assignment~~

~~Post processing for work.general\_fifo.arc\_general\_fifo~~

~~@N: CL134 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":96:7:96:9|Found RAM mem, depth=640, width=8~~

~~@N: CL177 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":136:2:136:3|Sharing sequential element read\_addr\_dup.~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\manager.vhd":45:7:45:13|Synthesizing work.manager.manager\_rtl~~

~~@N: CD231 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\manager.vhd":108:14:108:15|Using onehot encoding for type state\_t (idle\_st="10000")~~

~~@W: CD604 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\manager.vhd":331:4:331:17|OTHERS clause is not synthesized~~

~~Post processing for work.manager.manager\_rtl~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\manager.vhd":164:2:164:3|Pruning Register req\_in\_trg\_dev\_active~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\manager.vhd":164:2:164:3|Pruning Register req\_in\_trg\_counter(31 downto 0)~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\manager.vhd":447:2:447:3|Optimizing register bit sdram\_addr\_rd(22) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\manager.vhd":447:2:447:3|Optimizing register bit sdram\_addr\_rd(23) to a constant 0~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\manager.vhd":447:2:447:3|Pruning Register bit 23 of sdram\_addr\_rd(23 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\manager.vhd":447:2:447:3|Pruning Register bit 22 of sdram\_addr\_rd(23 downto 0)~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\RAM\_300.vhd":40:7:40:13|Synthesizing work.ram\_300.ram\_300\_rtl~~

~~Post processing for work.ram\_300.ram\_300\_rtl~~

~~@N: CL134 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\RAM\_300.vhd":56:9:56:11|Found RAM mem, depth=300, width=13~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\opcode\_store.vhd":33:7:33:18|Synthesizing work.opcode\_store.opcode\_store\_rtl~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":61:7:61:18|Synthesizing work.general\_fifo.arc\_general\_fifo~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":245:6:245:10|Removed redundant assignment~~

~~Post processing for work.general\_fifo.arc\_general\_fifo~~

~~@N: CL134 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":96:7:96:9|Found RAM mem, depth=400, width=24~~

~~@N: CL177 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":136:2:136:3|Sharing sequential element read\_addr\_dup.~~

~~Post processing for work.opcode\_store.opcode\_store\_rtl~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\opcode\_store.vhd":183:2:183:3|Pruning Register op\_cnt\_i(9 downto 0)~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\opcode\_unite.vhd":37:7:37:18|Synthesizing work.opcode\_unite.opcode\_unite\_rtl~~

~~@N: CD233 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\opcode\_unite.vhd":64:14:64:15|Using sequential encoding for type state\_t~~

~~@W: CD604 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\opcode\_unite.vhd":151:6:151:19|OTHERS clause is not synthesized~~

~~Post processing for work.opcode\_unite.opcode\_unite\_rtl~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\opcode\_unite.vhd":96:2:96:3|Pruning Register counter\_i(9 downto 0)~~

~~Post processing for work.symbol\_generator\_top.rtl\_symbol\_generator\_top~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\wbs\_reg.vhd":26:7:26:13|Synthesizing work.wbs\_reg.rtl\_wbs\_reg~~

~~Post processing for work.wbs\_reg.rtl\_wbs\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment~~

~~Post processing for work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment~~

~~Post processing for work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment~~

~~Post processing for work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment~~

~~Post processing for work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment~~

~~Post processing for work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":25:7:25:31|Synthesizing work.synthetic\_frame\_generator.rtl\_synthetic\_frame\_generator~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":154:4:154:14|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":184:6:184:9|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":185:6:185:9|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":192:5:192:8|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":193:5:193:8|Removed redundant assignment~~

~~Post processing for work.synthetic\_frame\_generator.rtl\_synthetic\_frame\_generator~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit lower\_frame(0) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit lower\_frame(1) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit lower\_frame(7) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit lower\_frame(8) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit lower\_frame(9) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit right\_frame(0) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit right\_frame(1) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit right\_frame(2) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit right\_frame(3) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit right\_frame(8) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit right\_frame(9) to a constant 0~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 9 of lower\_frame(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 8 of lower\_frame(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 7 of lower\_frame(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 1 of lower\_frame(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 0 of lower\_frame(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 9 of right\_frame(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 8 of right\_frame(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 3 of right\_frame(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 2 of right\_frame(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 1 of right\_frame(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 0 of right\_frame(9 downto 0)~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\vesa\_gen\_ctrl.vhd":75:7:75:19|Synthesizing work.vesa\_gen\_ctrl.rtl\_vesa\_gen\_ctrl~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\vesa\_gen\_ctrl.vhd":279:5:279:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\vesa\_gen\_ctrl.vhd":280:5:280:13|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\vesa\_gen\_ctrl.vhd":281:5:281:16|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\vesa\_gen\_ctrl.vhd":282:5:282:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\vesa\_gen\_ctrl.vhd":283:5:283:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\vesa\_gen\_ctrl.vhd":284:5:284:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\vesa\_gen\_ctrl.vhd":325:5:325:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\vesa\_gen\_ctrl.vhd":329:4:329:16|Removed redundant assignment~~

~~Post processing for work.vesa\_gen\_ctrl.rtl\_vesa\_gen\_ctrl~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":61:7:61:18|Synthesizing work.general\_fifo.arc\_general\_fifo~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":245:6:245:10|Removed redundant assignment~~

~~Post processing for work.general\_fifo.arc\_general\_fifo~~

~~@N: CL134 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":96:7:96:9|Found RAM mem, depth=4864, width=8~~

~~@N: CL177 :"H:\Project\SG\_synthesis\_proj\VHDL\general\_fifo.vhd":136:2:136:3|Sharing sequential element read\_addr\_dup.~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\dc\_fifo.vhd":42:7:42:13|Synthesizing work.dc\_fifo.syn~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\dc\_fifo.vhd":68:11:68:16|Synthesizing altera\_mf.dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1.syn\_black\_box~~

~~Post processing for altera\_mf.dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1.syn\_black\_box~~

~~Post processing for work.dc\_fifo.syn~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":30:7:30:15|Synthesizing work.sg\_wbm\_if.rtl\_sg\_wbm\_if~~

~~@N: CD231 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":74:17:74:18|Using onehot encoding for type wbm\_states (wbm\_idle\_st="10000000000")~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":115:4:115:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":236:6:236:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":277:6:277:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":356:6:356:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":397:5:397:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":400:4:400:10|Removed redundant assignment~~

~~Post processing for work.sg\_wbm\_if.rtl\_sg\_wbm\_if~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Pruning Register dbg\_cnt(30 downto 0)~~

~~@A:"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Feedback mux created for signal cnt[31:0]. Did you forget the set/reset assignment for this signal? Specifying a reset value will improve timing and area~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Optimizing register bit wbm\_tga\_o(0) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Optimizing register bit wbm\_tga\_o(2) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Optimizing register bit wbm\_tga\_o(3) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Optimizing register bit wbm\_tga\_o(4) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Optimizing register bit wbm\_tga\_o(6) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Optimizing register bit wbm\_tga\_o(7) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Optimizing register bit wbm\_tga\_o(8) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Optimizing register bit wbm\_tga\_o(9) to a constant 0~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Pruning Register bit 9 of wbm\_tga\_o(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Pruning Register bit 8 of wbm\_tga\_o(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Pruning Register bit 7 of wbm\_tga\_o(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Pruning Register bit 6 of wbm\_tga\_o(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Pruning Register bit 4 of wbm\_tga\_o(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Pruning Register bit 3 of wbm\_tga\_o(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Pruning Register bit 2 of wbm\_tga\_o(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Pruning Register bit 0 of wbm\_tga\_o(9 downto 0)~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":30:7:30:15|Synthesizing work.pixel\_mng.rtl\_pixel\_mng~~

~~@N: CD231 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":77:17:77:18|Using onehot encoding for type wbm\_states (wbm\_idle\_st="100000")~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":237:6:237:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":264:7:264:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":280:6:280:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":298:6:298:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":318:6:318:11|Removed redundant assignment~~

~~@W: CD604 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":321:4:321:17|OTHERS clause is not synthesized~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":345:5:345:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":349:4:349:14|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":370:4:370:10|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":375:5:375:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":380:4:380:14|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":385:5:385:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":390:4:390:14|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":395:5:395:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":399:4:399:10|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":400:4:400:14|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":421:5:421:10|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":427:4:427:9|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":473:4:473:14|Removed redundant assignment~~

~~Post processing for work.pixel\_mng.rtl\_pixel\_mng~~

~~Post processing for work.disp\_ctrl\_top.rtl\_disp\_ctrl\_top~~

@W: CL240 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":225:7:225:32|right\_frame\_reg\_dout\_valid is not assigned a value (floating) - a simulation mismatch is possible

@W: CL240 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":223:7:223:29|right\_frame\_reg\_din\_ack is not assigned a value (floating) - a simulation mismatch is possible

@W: CL240 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":222:7:222:31|left\_frame\_reg\_dout\_valid is not assigned a value (floating) - a simulation mismatch is possible

@W: CL240 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":220:7:220:28|left\_frame\_reg\_din\_ack is not assigned a value (floating) - a simulation mismatch is possible

~~@W: CL168 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":994:0:994:11|Pruning instance sc\_fifo\_inst - not in use ...~~

~~@A:"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Feedback mux created for signal vesa\_mux\_d2. Did you forget the set/reset assignment for this signal? Specifying a reset value will improve timing and area~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to upper\_frame\_rg\_d1(8) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to upper\_frame\_rg\_d1(9) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to right\_frame\_rg\_d1(0) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to right\_frame\_rg\_d1(1) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to right\_frame\_rg\_d1(2) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to right\_frame\_rg\_d1(3) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to right\_frame\_rg\_d1(5) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to right\_frame\_rg\_d1(7) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to right\_frame\_rg\_d1(8) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to right\_frame\_rg\_d1(9) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to lower\_frame\_rg\_d1(8) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to lower\_frame\_rg\_d1(9) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to left\_frame\_rg\_d1(0) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to left\_frame\_rg\_d1(1) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to left\_frame\_rg\_d1(2) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to left\_frame\_rg\_d1(3) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to left\_frame\_rg\_d1(5) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to left\_frame\_rg\_d1(7) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to left\_frame\_rg\_d1(8) assign '0', register removed by optimization~~

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|All reachable assignments to left\_frame\_rg\_d1(9) assign '0', register removed by optimization~~

~~@N: CL177 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Sharing sequential element left\_frame\_rg\_d1.~~

~~@N: CL177 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Sharing sequential element left\_frame\_rg\_d1.~~

~~@A:"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":857:2:857:3|Feedback mux created for signal blank\_d. Did you forget the set/reset assignment for this signal? Specifying a reset value will improve timing and area~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit left\_frame\_rg\_d2(0) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit left\_frame\_rg\_d2(1) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit left\_frame\_rg\_d2(2) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit left\_frame\_rg\_d2(3) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit left\_frame\_rg\_d2(5) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit left\_frame\_rg\_d2(7) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit left\_frame\_rg\_d2(8) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit left\_frame\_rg\_d2(9) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit lower\_frame\_rg\_d2(8) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit lower\_frame\_rg\_d2(9) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit right\_frame\_rg\_d2(0) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit right\_frame\_rg\_d2(1) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit right\_frame\_rg\_d2(2) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit right\_frame\_rg\_d2(3) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit right\_frame\_rg\_d2(5) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit right\_frame\_rg\_d2(7) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit right\_frame\_rg\_d2(8) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit right\_frame\_rg\_d2(9) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit upper\_frame\_rg\_d2(8) to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Optimizing register bit upper\_frame\_rg\_d2(9) to a constant 0~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 9 of left\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 8 of left\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 7 of left\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 5 of left\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 3 of left\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 2 of left\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 1 of left\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 0 of left\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 9 of lower\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 8 of lower\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 9 of right\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 8 of right\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 7 of right\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 5 of right\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 3 of right\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 2 of right\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 1 of right\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 0 of right\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 9 of upper\_frame\_rg\_d2(9 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 8 of upper\_frame\_rg\_d2(9 downto 0)~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_mng\_top.vhd":29:7:29:17|Synthesizing work.mem\_mng\_top.rtl\_mem\_mng\_top~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_mng\_top.vhd":505:4:505:14|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_mng\_top.vhd":506:4:506:14|Removed redundant assignment~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment~~

~~Post processing for work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment~~

~~Post processing for work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment~~

~~Post processing for work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment~~

~~Post processing for work.gen\_reg.rtl\_gen\_reg~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd.vhd":36:7:36:17|Synthesizing work.mem\_ctrl\_rd.rtl\_mem\_ctrl\_rd~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":35:7:35:21|Synthesizing work.mem\_ctrl\_rd\_wbm.rtl\_mem\_ctrl\_rd\_wbm~~

~~@N: CD231 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":97:17:97:18|Using onehot encoding for type wbm\_states (wbm\_idle\_st="10000")~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":219:7:219:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":226:6:226:16|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":231:5:231:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":232:5:232:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":233:5:233:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":266:6:266:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":267:6:267:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":268:6:268:16|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":279:6:279:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":284:7:284:20|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":298:8:298:20|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":308:7:308:19|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":309:7:309:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":310:7:310:20|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":311:7:311:19|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":317:5:317:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":318:5:318:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":323:6:323:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":347:6:347:21|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":386:5:386:18|Removed redundant assignment~~

~~@W: CD604 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":394:4:394:17|OTHERS clause is not synthesized~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":419:4:419:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":473:4:473:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":492:4:492:9|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":530:5:530:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":594:4:594:16|Removed redundant assignment~~

~~Post processing for work.mem\_ctrl\_rd\_wbm.rtl\_mem\_ctrl\_rd\_wbm~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbs.vhd":37:7:37:21|Synthesizing work.mem\_ctrl\_rd\_wbs.rtl\_mem\_ctrl\_rd\_wbs~~

~~@N: CD231 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbs.vhd":83:17:83:18|Using onehot encoding for type wbs\_states (wbs\_idle\_st="1000000")~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbs.vhd":149:7:149:16|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbs.vhd":152:6:152:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbs.vhd":171:6:171:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbs.vhd":188:7:188:16|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbs.vhd":196:6:196:15|Removed redundant assignment~~

~~@W: CD604 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbs.vhd":204:4:204:17|OTHERS clause is not synthesized~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbs.vhd":309:5:309:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbs.vhd":314:4:314:17|Removed redundant assignment~~

~~Post processing for work.mem\_ctrl\_rd\_wbs.rtl\_mem\_ctrl\_rd\_wbs~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\altera\_16to8\_dc\_ram.vhd":42:7:42:25|Synthesizing work.altera\_16to8\_dc\_ram.syn~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\altera\_16to8\_dc\_ram.vhd":62:11:62:20|Synthesizing altera\_mf.altsyncram\_work\_top\_synthesis\_top\_synthesis\_rtl\_1.syn\_black\_box~~

~~Post processing for altera\_mf.altsyncram\_work\_top\_synthesis\_top\_synthesis\_rtl\_1.syn\_black\_box~~

~~Post processing for work.altera\_16to8\_dc\_ram.syn~~

~~Post processing for work.mem\_ctrl\_rd.rtl\_mem\_ctrl\_rd~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd.vhd":382:2:382:3|Pruning Register rd\_addr\_reg\_d2(21 downto 0)~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd.vhd":382:2:382:3|Pruning Register type\_reg\_d2(7 downto 0)~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd.vhd":382:2:382:3|Pruning Register rd\_addr\_reg\_d1(21 downto 0)~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd.vhd":382:2:382:3|Pruning Register type\_reg\_d1(7 downto 0)~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_mng\_arbiter.vhd":30:7:30:21|Synthesizing work.mem\_mng\_arbiter.rtl\_mem\_mng\_arbiter~~

~~Post processing for work.mem\_mng\_arbiter.rtl\_mem\_mng\_arbiter~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr.vhd":41:7:41:17|Synthesizing work.mem\_ctrl\_wr.rtl\_mem\_ctrl\_wr~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":34:7:34:21|Synthesizing work.mem\_ctrl\_wr\_wbm.rtl\_mem\_ctrl\_wr\_wbm~~

~~@N: CD231 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":93:17:93:18|Using onehot encoding for type wbm\_states (wbm\_idle\_st="1000000000")~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":217:8:217:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":224:7:224:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":228:6:228:16|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":233:5:233:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":235:5:235:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":255:6:255:19|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":256:6:256:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":257:6:257:16|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":265:6:265:19|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":266:6:266:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":271:7:271:20|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":272:7:272:20|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":275:7:275:22|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":296:7:296:20|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":297:7:297:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":298:7:298:20|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":299:7:299:19|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":305:5:305:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":306:5:306:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":307:5:307:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":319:6:319:21|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":347:5:347:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":349:5:349:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":358:5:358:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":359:5:359:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":362:6:362:19|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":368:6:368:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":371:6:371:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":385:5:385:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":387:5:387:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":395:5:395:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":397:5:397:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":408:5:408:18|Removed redundant assignment~~

~~@W: CD604 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":415:4:415:17|OTHERS clause is not synthesized~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":471:4:471:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":514:5:514:16|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":518:4:518:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":525:6:525:17|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":528:5:528:16|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":536:4:536:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":537:4:537:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":574:4:574:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":597:4:597:9|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":645:4:645:13|Removed redundant assignment~~

~~Post processing for work.mem\_ctrl\_wr\_wbm.rtl\_mem\_ctrl\_wr\_wbm~~

~~@N: CL177 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":459:2:459:3|Sharing sequential element wr\_cnt\_en.~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbs.vhd":25:7:25:21|Synthesizing work.mem\_ctrl\_wr\_wbs.rtl\_mem\_ctrl\_wr\_wbs~~

~~@N: CD231 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbs.vhd":67:17:67:18|Using onehot encoding for type wbs\_states (wbs\_idle\_st="10000")~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbs.vhd":131:5:131:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbs.vhd":159:7:159:20|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbs.vhd":176:6:176:19|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbs.vhd":181:5:181:18|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbs.vhd":200:6:200:15|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbs.vhd":205:5:205:18|Removed redundant assignment~~

~~@W: CD604 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbs.vhd":207:4:207:17|OTHERS clause is not synthesized~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbs.vhd":228:4:228:14|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbs.vhd":306:4:306:11|Removed redundant assignment~~

~~Post processing for work.mem\_ctrl\_wr\_wbs.rtl\_mem\_ctrl\_wr\_wbs~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\altera\_8to16\_dc\_ram.vhd":42:7:42:25|Synthesizing work.altera\_8to16\_dc\_ram.syn~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\altera\_8to16\_dc\_ram.vhd":62:11:62:20|Synthesizing altera\_mf.altsyncram\_work\_top\_synthesis\_top\_synthesis\_rtl\_3.syn\_black\_box~~

~~Post processing for altera\_mf.altsyncram\_work\_top\_synthesis\_top\_synthesis\_rtl\_3.syn\_black\_box~~

~~Post processing for work.altera\_8to16\_dc\_ram.syn~~

~~Post processing for work.mem\_ctrl\_wr.rtl\_mem\_ctrl\_wr~~

@W: CL170 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr.vhd":355:2:355:3|Pruning bit <0> of type\_reg\_wbm\_d1(7 downto 0) - not in use ...

~~@W: CL111 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr.vhd":355:2:355:3|All reachable assignments to type\_reg\_wbm\_d2(0) assign '0', register removed by optimization~~

~~Post processing for work.mem\_mng\_top.rtl\_mem\_mng\_top~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon\_mux.vhd":24:7:24:18|Synthesizing work.intercon\_mux.intercon\_mux\_rtl~~

~~Post processing for work.intercon\_mux.intercon\_mux\_rtl~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon.vhd":35:7:35:14|Synthesizing work.intercon.intercon\_rtl~~

~~@N: CD233 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon.vhd":98:22:98:23|Using sequential encoding for type intercon\_states~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon.vhd":175:6:175:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon.vhd":184:6:184:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon.vhd":191:5:191:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon.vhd":192:5:192:11|Removed redundant assignment~~

~~@W: CD604 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon.vhd":194:4:194:19|OTHERS clause is not synthesized~~

~~Post processing for work.intercon.intercon\_rtl~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon.vhd":35:7:35:14|Synthesizing work.intercon.intercon\_rtl~~

~~@N: CD233 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon.vhd":98:22:98:23|Using sequential encoding for type intercon\_states~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon.vhd":175:6:175:12|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon.vhd":184:6:184:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon.vhd":191:5:191:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon.vhd":192:5:192:11|Removed redundant assignment~~

~~@W: CD604 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon.vhd":194:4:194:19|OTHERS clause is not synthesized~~

~~Post processing for work.intercon.intercon\_rtl~~

~~Post processing for work.mds\_top.rtl\_mds\_top~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\global\_nets\_top.vhd":37:7:37:21|Synthesizing work.global\_nets\_top.rtl\_global\_nets\_top~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\reset\_blk\_top.vhd":38:7:38:19|Synthesizing work.reset\_blk\_top.rtl\_reset\_blk\_top~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\sync\_rst\_gen.vhd":22:7:22:18|Synthesizing work.sync\_rst\_gen.rtl\_sync\_rst\_gen~~

~~Post processing for work.sync\_rst\_gen.rtl\_sync\_rst\_gen~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\reset\_debouncer.vhd":30:7:30:21|Synthesizing work.reset\_debouncer.rtl\_reset\_debouncer~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\reset\_debouncer.vhd":87:4:87:11|Removed redundant assignment~~

~~@N: CD364 :"H:\Project\SG\_synthesis\_proj\VHDL\reset\_debouncer.vhd":109:4:109:9|Removed redundant assignment~~

~~Post processing for work.reset\_debouncer.rtl\_reset\_debouncer~~

~~Post processing for work.reset\_blk\_top.rtl\_reset\_blk\_top~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\clk\_blk\_top.vhd":32:7:32:17|Synthesizing work.clk\_blk\_top.rtl\_clk\_blk\_top~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\pll.vhd":42:7:42:9|Synthesizing work.pll.syn~~

~~@N: CD630 :"H:\Project\SG\_synthesis\_proj\VHDL\pll.vhd":68:11:68:16|Synthesizing altera\_mf.altpll\_work\_top\_synthesis\_top\_synthesis\_rtl\_1.syn\_black\_box~~

~~Post processing for altera\_mf.altpll\_work\_top\_synthesis\_top\_synthesis\_rtl\_1.syn\_black\_box~~

~~Post processing for work.pll.syn~~

~~Post processing for work.clk\_blk\_top.rtl\_clk\_blk\_top~~

~~Post processing for work.global\_nets\_top.rtl\_global\_nets\_top~~

~~Post processing for work.top\_synthesis.top\_synthesis\_rtl~~

@W: CL138 :"H:\Project\SG\_synthesis\_proj\VHDL\intercon.vhd":167:2:167:3|Register 'wbs\_gnt' is only assigned 0 or its old value; the register will be removed

~~@N: CL201 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbs.vhd":119:2:119:3|Trying to extract state machine for register wbs\_cur\_st~~

~~Extracted state machine for register wbs\_cur\_st~~

~~State machine has 5 reachable states with original encodings of:~~

~~00001~~

~~00010~~

~~00100~~

~~01000~~

~~10000~~

~~@W: CL247 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbs.vhd":37:2:37:10|Input port bit 0 of wbs\_tga\_i(9 downto 0) is unused~~

~~@N: CL201 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":187:2:187:3|Trying to extract state machine for register wbm\_cur\_st~~

~~Extracted state machine for register wbm\_cur\_st~~

~~State machine has 10 reachable states with original encodings of:~~

~~0000000001~~

~~0000000010~~

~~0000000100~~

~~0000001000~~

~~0000010000~~

~~0000100000~~

~~0001000000~~

~~0010000000~~

~~0100000000~~

~~1000000000~~

~~@W: CL246 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr\_wbm.vhd":68:2:68:9|Input port bits 7 to 2 of type\_reg(7 downto 0) are unused~~

~~@N: CL135 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_wr.vhd":355:2:355:3|Found seqShift ram\_ready\_d3, depth=3, width=1~~

~~@N: CL201 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbs.vhd":136:2:136:3|Trying to extract state machine for register wbs\_cur\_st~~

~~Extracted state machine for register wbs\_cur\_st~~

~~State machine has 7 reachable states with original encodings of:~~

~~0000001~~

~~0000010~~

~~0000100~~

~~0001000~~

~~0010000~~

~~0100000~~

~~1000000~~

~~@W: CL247 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbs.vhd":49:2:49:10|Input port bit 0 of wbs\_tga\_i(9 downto 0) is unused~~

~~@N: CL201 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":188:2:188:3|Trying to extract state machine for register wbm\_cur\_st~~

~~Extracted state machine for register wbm\_cur\_st~~

~~State machine has 5 reachable states with original encodings of:~~

~~00001~~

~~00010~~

~~00100~~

~~01000~~

~~10000~~

~~@W: CL246 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd\_wbm.vhd":80:2:80:9|Input port bits 7 to 1 of type\_reg(7 downto 0) are unused~~

~~@N: CL135 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd.vhd":382:2:382:3|Found seqShift init\_rd\_d3, depth=3, width=1~~

~~@N: CL135 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd.vhd":382:2:382:3|Found seqShift restart\_rd\_d3, depth=3, width=1~~

~~@N: CL135 :"H:\Project\SG\_synthesis\_proj\VHDL\mem\_ctrl\_rd.vhd":456:2:456:3|Found seqShift ram\_ready\_d3, depth=3, width=1~~

~~@N: CL135 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":181:2:181:3|Found seqShift vsync\_sig, depth=3, width=1~~

~~@N: CL201 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":216:2:216:3|Trying to extract state machine for register cur\_st~~

~~Extracted state machine for register cur\_st~~

~~State machine has 6 reachable states with original encodings of:~~

~~000001~~

~~000010~~

~~000100~~

~~001000~~

~~010000~~

~~100000~~

@W: CL159 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":49:2:49:10|Input wbm\_dat\_i is unused

@W: CL159 :"H:\Project\SG\_synthesis\_proj\VHDL\pixel\_mng.vhd":61:2:61:9|Input term\_cyc is unused

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":109:2:109:3|Optimizing register bit vsync\_cnt(3) to a constant 0~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":109:2:109:3|Pruning Register bit 3 of vsync\_cnt(3 downto 0)~~

~~@N: CL201 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\SG\_WBM\_IF.vhd":160:2:160:3|Trying to extract state machine for register cur\_st~~

~~Extracted state machine for register cur\_st~~

~~State machine has 10 reachable states with original encodings of:~~

~~00000000001~~

~~00000000010~~

~~00000000100~~

~~00000001000~~

~~00000010000~~

~~00000100000~~

~~00001000000~~

~~00010000000~~

~~00100000000~~

~~01000000000~~

~~@N: CL201 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Trying to extract state machine for register frame\_state~~

~~Extracted state machine for register frame\_state~~

~~State machine has 5 reachable states with original encodings of:~~

~~000~~

~~001~~

~~010~~

~~011~~

~~100~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 7 of right\_frame(7 downto 4)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 6 of right\_frame(7 downto 4)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 5 of lower\_frame(6 downto 2)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 4 of lower\_frame(6 downto 2)~~

@W: CL159 :"H:\Project\SG\_synthesis\_proj\VHDL\wbs\_reg.vhd":33:3:33:5|Input rst is unused

@W: CL159 :"H:\Project\SG\_synthesis\_proj\VHDL\wbs\_reg.vhd":36:3:36:7|Input clk\_i is unused

~~@N: CL201 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\opcode\_unite.vhd":96:2:96:3|Trying to extract state machine for register current\_sm~~

~~Extracted state machine for register current\_sm~~

~~State machine has 3 reachable states with original encodings of:~~

~~00~~

~~01~~

~~10~~

@W: CL159 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\opcode\_store.vhd":37:4:37:9|Input op\_cnt is unused

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\manager.vhd":447:2:447:3|Pruning Register bit 3 of sdram\_addr\_rd(21 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\manager.vhd":447:2:447:3|Pruning Register bit 2 of sdram\_addr\_rd(21 downto 0)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\manager.vhd":447:2:447:3|Pruning Register bit 1 of sdram\_addr\_rd(21 downto 0)~~

~~@W: CL189 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\manager.vhd":447:2:447:3|Register bit sdram\_addr\_rd(0) is always 0, optimizing ...~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\manager.vhd":447:2:447:3|Pruning Register sdram\_addr\_rd(0)~~

~~@N: CL201 :"H:\Project\SG\_synthesis\_proj\VHDL\SG\manager.vhd":235:2:235:3|Trying to extract state machine for register current\_sm~~

~~Extracted state machine for register current\_sm~~

~~State machine has 5 reachable states with original encodings of:~~

~~00001~~

~~00010~~

~~00100~~

~~01000~~

~~10000~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register bit 6 of right\_frame\_rg\_d1(6 downto 5)~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register left\_frame\_rg\_d2(6)~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register right\_frame\_rg\_d2(6)~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\disp\_ctrl\_top.vhd":1305:1:1305:2|Pruning Register right\_frame\_rg\_d2(4)~~

~~@N: CL201 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_rx.vhd":119:2:119:3|Trying to extract state machine for register cur\_st~~

~~Extracted state machine for register cur\_st~~

~~State machine has 4 reachable states with original encodings of:~~

~~00001~~

~~00010~~

~~00100~~

~~10000~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_rx.vhd":119:2:119:3|Optimizing register bit parity\_err to a constant 0~~

~~@W: CL190 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_rx.vhd":119:2:119:3|Optimizing register bit parity\_err\_i to a constant 0~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_rx.vhd":119:2:119:3|Pruning Register parity\_err~~

~~@W: CL169 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_rx.vhd":119:2:119:3|Pruning Register parity\_err\_i~~

~~@N: CL201 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":180:2:180:3|Trying to extract state machine for register cur\_st~~

~~Extracted state machine for register cur\_st~~

~~State machine has 7 reachable states with original encodings of:~~

~~0000001~~

~~0000010~~

~~0000100~~

~~0001000~~

~~0010000~~

~~0100000~~

~~1000000~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_dec.vhd":328:2:328:3|Pruning Register bit 7 of eof\_blk(7 downto 6)~~

~~@N: CL201 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":420:2:420:3|Trying to extract state machine for register wbm\_cur\_st~~

~~Extracted state machine for register wbm\_cur\_st~~

~~State machine has 6 reachable states with original encodings of:~~

~~000001~~

~~000010~~

~~000100~~

~~001000~~

~~010000~~

~~100000~~

~~@W: CL159 :"H:\Project\SG\_synthesis\_proj\VHDL\rx\_path.vhd":67:4:67:12|Input wbm\_dat\_i is unused~~

~~@N: CL201 :"H:\Project\SG\_synthesis\_proj\VHDL\uart\_tx.vhd":111:2:111:3|Trying to extract state machine for register cur\_st~~

~~Extracted state machine for register cur\_st~~

~~State machine has 3 reachable states with original encodings of:~~

~~00~~

~~01~~

~~10~~

~~@N: CL201 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Trying to extract state machine for register cur\_st~~

~~Extracted state machine for register cur\_st~~

~~State machine has 9 reachable states with original encodings of:~~

~~000000001~~

~~000000010~~

~~000000100~~

~~000001000~~

~~000010000~~

~~000100000~~

~~001000000~~

~~010000000~~

~~100000000~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 7 of eof\_blk(7 downto 6)~~

~~@W: CL260 :"H:\Project\SG\_synthesis\_proj\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 6 of sof\_blk(6 downto 5)~~

@W: CL159 :"H:\Project\SG\_synthesis\_proj\VHDL\gen\_reg.vhd":62:3:62:7|Input rd\_en is unused

@W: CL159 :"H:\Project\SG\_synthesis\_proj\VHDL\wbs\_reg.vhd":33:3:33:5|Input rst is unused

@W: CL159 :"H:\Project\SG\_synthesis\_proj\VHDL\wbs\_reg.vhd":36:3:36:7|Input clk\_i is unused

~~@N: CL201 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path\_wbm.vhd":134:2:134:3|Trying to extract state machine for register wbm\_cur\_st~~

~~Extracted state machine for register wbm\_cur\_st~~

~~State machine has 3 reachable states with original encodings of:~~

~~00~~

~~01~~

~~10~~

~~@W: CL246 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path.vhd":90:4:90:12|Input port bits 9 to 4 of wbs\_adr\_i(9 downto 0) are unused~~

~~@W: CL159 :"H:\Project\SG\_synthesis\_proj\VHDL\tx\_path.vhd":91:4:91:12|Input wbs\_tga\_i is unused~~

@END