#Build: Synplify Pro D-2010.03-SP1, Build 079R, May 19 2010

#install: C:\Synopsys\fpga\_D201003SP1

#OS: 6.1

#Hostname: DIGLAB352-1-07

#Implementation: rev\_1

#Tue Apr 02 16:10:41 2013

$ Start of Compile

#Tue Apr 02 16:10:41 2013

Synopsys VHDL Compiler, version comp510rc, Build 073R, built May 14 2010

@N|Running in 32-bit mode

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@N: CD720 :"C:\Synopsys\fpga\_D201003SP1\lib\vhd\std.vhd":123:18:123:21|Setting time resolution to ns

@N:"H:\Project\SG\_Project\VHDL\top\_synthesis.vhd":23:7:23:19|Top entity is set to top\_synthesis.

VHDL syntax check successful!

Compiler output is up to date. No re-compile necessary

@N: CD231 :"C:\Synopsys\fpga\_D201003SP1\lib\vhd\std\_logic\_textio.vhd":79:15:79:16|Using onehot encoding for type mvl9plus ('U'="1000000000")

@N: CD630 :"H:\Project\SG\_Project\VHDL\top\_synthesis.vhd":23:7:23:19|Synthesizing work.top\_synthesis.top\_synthesis\_rtl

@N: CD630 :"H:\Project\SG\_Project\VHDL\Hexss.vhd":23:7:23:11|Synthesizing work.hexss.arc\_hexss

Post processing for work.hexss.arc\_hexss

@N: CD630 :"H:\Project\SG\_Project\VHDL\mds\_top.vhd":31:7:31:13|Synthesizing work.mds\_top.rtl\_mds\_top

@N: CD630 :"H:\Project\SG\_Project\VHDL\SG\led.vhd":26:7:26:9|Synthesizing work.led.led\_rtl

Post processing for work.led.led\_rtl

@N: CD630 :"H:\Project\SG\_Project\VHDL\tx\_path.vhd":25:7:25:13|Synthesizing work.tx\_path.arc\_tx\_path

@W: CD326 :"H:\Project\SG\_Project\VHDL\tx\_path.vhd":624:1:624:10|Port used of entity work.general\_fifo is unconnected

@W: CD326 :"H:\Project\SG\_Project\VHDL\tx\_path.vhd":624:1:624:10|Port aempty of entity work.general\_fifo is unconnected

@W: CD326 :"H:\Project\SG\_Project\VHDL\tx\_path.vhd":624:1:624:10|Port afull of entity work.general\_fifo is unconnected

@N: CD630 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":25:7:25:17|Synthesizing work.tx\_path\_wbm.rtl\_tx\_path\_wbm

@N: CD233 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":69:17:69:18|Using sequential encoding for type wbm\_states

@N: CD364 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":170:6:170:16|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":181:6:181:16|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":182:6:182:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":194:7:194:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":195:7:195:19|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":196:7:196:20|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":202:5:202:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":203:5:203:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":204:5:204:18|Removed redundant assignment

@W: CD604 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":221:4:221:17|OTHERS clause is not synthesized

@N: CD364 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":249:4:249:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":251:4:251:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":263:4:263:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":265:4:265:17|Removed redundant assignment

Post processing for work.tx\_path\_wbm.rtl\_tx\_path\_wbm

@N: CD630 :"H:\Project\SG\_Project\VHDL\wbs\_reg.vhd":26:7:26:13|Synthesizing work.wbs\_reg.rtl\_wbs\_reg

Post processing for work.wbs\_reg.rtl\_wbs\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment

Post processing for work.gen\_reg.rtl\_gen\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment

Post processing for work.gen\_reg.rtl\_gen\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment

Post processing for work.gen\_reg.rtl\_gen\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment

Post processing for work.gen\_reg.rtl\_gen\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment

Post processing for work.gen\_reg.rtl\_gen\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":61:7:61:18|Synthesizing work.general\_fifo.arc\_general\_fifo

@N: CD364 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":245:6:245:10|Removed redundant assignment

Post processing for work.general\_fifo.arc\_general\_fifo

@N: CL134 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":96:7:96:9|Found RAM mem, depth=9, width=8

@N: CL177 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":136:2:136:3|Sharing sequential element read\_addr\_dup.

@N: CD630 :"H:\Project\SG\_Project\VHDL\ram\_simple.vhd":45:7:45:16|Synthesizing work.ram\_simple.arc\_ram\_simple

Post processing for work.ram\_simple.arc\_ram\_simple

@N: CL134 :"H:\Project\SG\_Project\VHDL\ram\_simple.vhd":69:7:69:14|Found RAM ram\_data, depth=1024, width=8

@N: CD630 :"H:\Project\SG\_Project\VHDL\checksum\_calc.vhd":62:7:62:19|Synthesizing work.checksum\_calc.arc\_checksum\_calc

@W: CG296 :"H:\Project\SG\_Project\VHDL\checksum\_calc.vhd":120:24:120:30|Incomplete sensitivity list - assuming completeness

@W: CG290 :"H:\Project\SG\_Project\VHDL\checksum\_calc.vhd":123:15:123:31|Referenced variable checksum\_init\_val is not in sensitivity list

Post processing for work.checksum\_calc.arc\_checksum\_calc

@W: CL170 :"H:\Project\SG\_Project\VHDL\checksum\_calc.vhd":122:1:122:2|Pruning bit <8> of checksum\_i(8 downto 0) - not in use ...

@N: CD630 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":44:7:44:12|Synthesizing work.mp\_enc.rtl\_mp\_enc

@N: CD231 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":101:23:101:24|Using onehot encoding for type mp\_encoder\_states (idle\_st="100000000")

@N: CD364 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":327:7:327:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":329:7:329:16|Removed redundant assignment

@W: CD604 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":377:5:377:18|OTHERS clause is not synthesized

@N: CD364 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":384:4:384:9|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":386:4:386:13|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":387:4:387:10|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":450:5:450:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":451:5:451:13|Removed redundant assignment

Post processing for work.mp\_enc.rtl\_mp\_enc

@W: CL190 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit eof\_blk(0) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit eof\_blk(1) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit eof\_blk(2) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit eof\_blk(4) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit eof\_blk(5) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit sof\_blk(0) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit sof\_blk(1) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit sof\_blk(3) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit sof\_blk(4) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Optimizing register bit sof\_blk(7) to a constant 0

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 5 of eof\_blk(7 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 4 of eof\_blk(7 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 2 of eof\_blk(7 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 1 of eof\_blk(7 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 0 of eof\_blk(7 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 7 of sof\_blk(7 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 4 of sof\_blk(7 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 3 of sof\_blk(7 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 1 of sof\_blk(7 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 0 of sof\_blk(7 downto 0)

@N: CD630 :"H:\Project\SG\_Project\VHDL\uart\_tx.vhd":39:7:39:13|Synthesizing work.uart\_tx.arc\_uart\_tx

@N: CD233 :"H:\Project\SG\_Project\VHDL\uart\_tx.vhd":70:24:70:25|Using sequential encoding for type uart\_tx\_fsm\_states

@N: CD364 :"H:\Project\SG\_Project\VHDL\uart\_tx.vhd":157:7:157:13|Removed redundant assignment

@W: CD604 :"H:\Project\SG\_Project\VHDL\uart\_tx.vhd":162:5:162:18|OTHERS clause is not synthesized

Post processing for work.uart\_tx.arc\_uart\_tx

Post processing for work.tx\_path.arc\_tx\_path

@N: CD630 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":26:7:26:13|Synthesizing work.rx\_path.rtl\_rx\_path

@N: CD231 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":82:16:82:17|Using onehot encoding for type wbm\_states (wbm\_idle\_st="100000")

@W: CD326 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":270:1:270:9|Port parity\_err of entity work.uart\_rx is unconnected

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":457:5:457:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":466:6:466:21|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":472:7:472:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":473:7:473:22|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":474:7:474:20|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":481:7:481:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":487:6:487:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":488:6:488:21|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":490:6:490:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":494:5:494:20|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":495:5:495:16|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":496:5:496:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":500:6:500:21|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":519:5:519:20|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":526:6:526:20|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":527:6:527:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":535:6:535:21|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":548:6:548:21|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":549:6:549:15|Removed redundant assignment

@W: CD604 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":552:4:552:17|OTHERS clause is not synthesized

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":578:4:578:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":582:5:582:16|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":586:4:586:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":587:4:587:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":617:4:617:12|Removed redundant assignment

@N: CD630 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":52:7:52:12|Synthesizing work.mp\_dec.rtl\_mp\_dec

@N: CD231 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":108:19:108:20|Using onehot encoding for type mp\_dec\_states (sof\_st="1000000")

@W: CD604 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":310:5:310:18|OTHERS clause is not synthesized

@N: CD364 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":337:5:337:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":340:4:340:10|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":445:4:445:12|Removed redundant assignment

@W: CD638 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":152:7:152:12|Signal sof\_sr is undriven

@W: CD638 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":153:7:153:16|Signal sof\_sr\_cnt is undriven

Post processing for work.mp\_dec.rtl\_mp\_dec

@W: CL190 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":328:2:328:3|Optimizing register bit eof\_blk(0) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":328:2:328:3|Optimizing register bit eof\_blk(1) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":328:2:328:3|Optimizing register bit eof\_blk(2) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":328:2:328:3|Optimizing register bit eof\_blk(4) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":328:2:328:3|Optimizing register bit eof\_blk(5) to a constant 0

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":328:2:328:3|Pruning Register bit 5 of eof\_blk(7 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":328:2:328:3|Pruning Register bit 4 of eof\_blk(7 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":328:2:328:3|Pruning Register bit 2 of eof\_blk(7 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":328:2:328:3|Pruning Register bit 1 of eof\_blk(7 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":328:2:328:3|Pruning Register bit 0 of eof\_blk(7 downto 0)

@N: CD630 :"H:\Project\SG\_Project\VHDL\uart\_rx.vhd":46:7:46:13|Synthesizing work.uart\_rx.arc\_uart\_rx

@N: CD231 :"H:\Project\SG\_Project\VHDL\uart\_rx.vhd":74:24:74:25|Using onehot encoding for type uart\_rx\_fsm\_states (idle\_st="10000")

@N: CD364 :"H:\Project\SG\_Project\VHDL\uart\_rx.vhd":162:8:162:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\uart\_rx.vhd":231:7:231:16|Removed redundant assignment

@W: CD604 :"H:\Project\SG\_Project\VHDL\uart\_rx.vhd":302:4:302:17|OTHERS clause is not synthesized

Post processing for work.uart\_rx.arc\_uart\_rx

@W: CL190 :"H:\Project\SG\_Project\VHDL\uart\_rx.vhd":119:2:119:3|Optimizing register bit parity\_bit to a constant 0

@W: CL169 :"H:\Project\SG\_Project\VHDL\uart\_rx.vhd":119:2:119:3|Pruning Register parity\_bit

Post processing for work.rx\_path.rtl\_rx\_path

@N: CD630 :"H:\Project\SG\_Project\VHDL\sdram\_controller.vhd":42:7:42:22|Synthesizing work.sdram\_controller.rtl\_sdram\_controller

@N: CD231 :"H:\Project\SG\_Project\VHDL\sdram\_controller.vhd":127:18:127:19|Using onehot encoding for type main\_states (idle\_st="1000000000000000")

@N: CD231 :"H:\Project\SG\_Project\VHDL\sdram\_controller.vhd":116:18:116:19|Using onehot encoding for type init\_states (init\_idle\_st="10000000")

@N: CD364 :"H:\Project\SG\_Project\VHDL\sdram\_controller.vhd":456:4:456:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\sdram\_controller.vhd":559:3:559:16|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\sdram\_controller.vhd":592:4:592:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\sdram\_controller.vhd":597:4:597:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\sdram\_controller.vhd":603:4:603:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\sdram\_controller.vhd":633:4:633:14|Removed redundant assignment

Post processing for work.sdram\_controller.rtl\_sdram\_controller

@N: CD630 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":35:7:35:19|Synthesizing work.disp\_ctrl\_top.rtl\_disp\_ctrl\_top

@W: CD326 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":974:0:974:11|Port wrfull of entity work.dc\_fifo is unconnected

@W: CD326 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":996:0:996:11|Port used of entity work.general\_fifo is unconnected

@W: CD326 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":996:0:996:11|Port aempty of entity work.general\_fifo is unconnected

@W: CD326 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":996:0:996:11|Port afull of entity work.general\_fifo is unconnected

@W: CD638 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":157:7:157:23|Signal dc\_fifo\_wr\_en\_log is undriven

@W: CD638 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":178:7:178:19|Signal sc\_fifo\_rd\_en is undriven

@W: CD638 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":180:7:180:17|Signal dc\_fifo\_din is undriven

@W: CD638 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":181:7:181:19|Signal dc\_fifo\_wr\_en is undriven

@W: CD638 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":221:7:221:28|Signal left\_frame\_reg\_din\_ack is undriven

@W: CD638 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":223:7:223:31|Signal left\_frame\_reg\_dout\_valid is undriven

@W: CD638 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":224:7:224:29|Signal right\_frame\_reg\_din\_ack is undriven

@W: CD638 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":226:7:226:32|Signal right\_frame\_reg\_dout\_valid is undriven

@W: CD638 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":256:7:256:17|Signal opu\_data\_in is undriven

@W: CD638 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":257:7:257:23|Signal opu\_data\_in\_valid is undriven

@W: CD638 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":272:7:272:12|Signal zero\_s is undriven

@W: CD638 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":273:7:273:13|Signal zeros\_s is undriven

@N: CD630 :"H:\Project\SG\_Project\VHDL\SG\Symbol\_Generator\_Top.vhd":23:7:23:26|Synthesizing work.symbol\_generator\_top.rtl\_symbol\_generator\_top

@W: CD638 :"H:\Project\SG\_Project\VHDL\SG\Symbol\_Generator\_Top.vhd":208:8:208:22|Signal opu\_data\_in\_cnt is undriven

@W: CD638 :"H:\Project\SG\_Project\VHDL\SG\Symbol\_Generator\_Top.vhd":239:8:239:19|Signal fifo\_a\_flush is undriven

@W: CD638 :"H:\Project\SG\_Project\VHDL\SG\Symbol\_Generator\_Top.vhd":240:8:240:19|Signal fifo\_b\_flush is undriven

@N: CD630 :"H:\Project\SG\_Project\VHDL\SG\mux2.vhd":30:7:30:10|Synthesizing work.mux2.mux2\_rtl

Post processing for work.mux2.mux2\_rtl

@N: CD630 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":61:7:61:18|Synthesizing work.general\_fifo.arc\_general\_fifo

@N: CD364 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":245:6:245:10|Removed redundant assignment

Post processing for work.general\_fifo.arc\_general\_fifo

@N: CL134 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":96:7:96:9|Found RAM mem, depth=640, width=8

@N: CL177 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":136:2:136:3|Sharing sequential element read\_addr\_dup.

@N: CD630 :"H:\Project\SG\_Project\VHDL\SG\manager.vhd":45:7:45:13|Synthesizing work.manager.manager\_rtl

@N: CD231 :"H:\Project\SG\_Project\VHDL\SG\manager.vhd":108:14:108:15|Using onehot encoding for type state\_t (idle\_st="10000")

@W: CD604 :"H:\Project\SG\_Project\VHDL\SG\manager.vhd":331:4:331:17|OTHERS clause is not synthesized

Post processing for work.manager.manager\_rtl

@W: CL169 :"H:\Project\SG\_Project\VHDL\SG\manager.vhd":164:2:164:3|Pruning Register req\_in\_trg\_dev\_active

@W: CL169 :"H:\Project\SG\_Project\VHDL\SG\manager.vhd":164:2:164:3|Pruning Register req\_in\_trg\_counter(31 downto 0)

@W: CL190 :"H:\Project\SG\_Project\VHDL\SG\manager.vhd":447:2:447:3|Optimizing register bit sdram\_addr\_rd(22) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\SG\manager.vhd":447:2:447:3|Optimizing register bit sdram\_addr\_rd(23) to a constant 0

@W: CL260 :"H:\Project\SG\_Project\VHDL\SG\manager.vhd":447:2:447:3|Pruning Register bit 23 of sdram\_addr\_rd(23 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\SG\manager.vhd":447:2:447:3|Pruning Register bit 22 of sdram\_addr\_rd(23 downto 0)

@N: CD630 :"H:\Project\SG\_Project\VHDL\SG\RAM\_300.vhd":40:7:40:13|Synthesizing work.ram\_300.ram\_300\_rtl

Post processing for work.ram\_300.ram\_300\_rtl

@N: CL134 :"H:\Project\SG\_Project\VHDL\SG\RAM\_300.vhd":56:9:56:11|Found RAM mem, depth=300, width=13

@N: CD630 :"H:\Project\SG\_Project\VHDL\SG\opcode\_store.vhd":33:7:33:18|Synthesizing work.opcode\_store.opcode\_store\_rtl

@N: CD630 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":61:7:61:18|Synthesizing work.general\_fifo.arc\_general\_fifo

@N: CD364 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":245:6:245:10|Removed redundant assignment

Post processing for work.general\_fifo.arc\_general\_fifo

@N: CL134 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":96:7:96:9|Found RAM mem, depth=400, width=24

@N: CL177 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":136:2:136:3|Sharing sequential element read\_addr\_dup.

Post processing for work.opcode\_store.opcode\_store\_rtl

@W: CL169 :"H:\Project\SG\_Project\VHDL\SG\opcode\_store.vhd":183:2:183:3|Pruning Register op\_cnt\_i(9 downto 0)

@N: CD630 :"H:\Project\SG\_Project\VHDL\SG\opcode\_unite.vhd":37:7:37:18|Synthesizing work.opcode\_unite.opcode\_unite\_rtl

@N: CD233 :"H:\Project\SG\_Project\VHDL\SG\opcode\_unite.vhd":64:14:64:15|Using sequential encoding for type state\_t

@W: CD604 :"H:\Project\SG\_Project\VHDL\SG\opcode\_unite.vhd":151:6:151:19|OTHERS clause is not synthesized

Post processing for work.opcode\_unite.opcode\_unite\_rtl

@W: CL169 :"H:\Project\SG\_Project\VHDL\SG\opcode\_unite.vhd":96:2:96:3|Pruning Register counter\_i(9 downto 0)

Post processing for work.symbol\_generator\_top.rtl\_symbol\_generator\_top

@N: CD630 :"H:\Project\SG\_Project\VHDL\wbs\_reg.vhd":26:7:26:13|Synthesizing work.wbs\_reg.rtl\_wbs\_reg

Post processing for work.wbs\_reg.rtl\_wbs\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment

Post processing for work.gen\_reg.rtl\_gen\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment

Post processing for work.gen\_reg.rtl\_gen\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment

Post processing for work.gen\_reg.rtl\_gen\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment

Post processing for work.gen\_reg.rtl\_gen\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment

Post processing for work.gen\_reg.rtl\_gen\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":25:7:25:31|Synthesizing work.synthetic\_frame\_generator.rtl\_synthetic\_frame\_generator

@N: CD364 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":154:4:154:14|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":184:6:184:9|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":185:6:185:9|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":192:5:192:8|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":193:5:193:8|Removed redundant assignment

Post processing for work.synthetic\_frame\_generator.rtl\_synthetic\_frame\_generator

@W: CL190 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit lower\_frame(0) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit lower\_frame(1) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit lower\_frame(7) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit lower\_frame(8) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit lower\_frame(9) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit right\_frame(0) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit right\_frame(1) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit right\_frame(2) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit right\_frame(3) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit right\_frame(8) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Optimizing register bit right\_frame(9) to a constant 0

@W: CL260 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 9 of lower\_frame(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 8 of lower\_frame(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 7 of lower\_frame(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 1 of lower\_frame(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 0 of lower\_frame(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 9 of right\_frame(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 8 of right\_frame(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 3 of right\_frame(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 2 of right\_frame(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 1 of right\_frame(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 0 of right\_frame(9 downto 0)

@N: CD630 :"H:\Project\SG\_Project\VHDL\vesa\_gen\_ctrl.vhd":75:7:75:19|Synthesizing work.vesa\_gen\_ctrl.rtl\_vesa\_gen\_ctrl

@N: CD364 :"H:\Project\SG\_Project\VHDL\vesa\_gen\_ctrl.vhd":279:5:279:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\vesa\_gen\_ctrl.vhd":280:5:280:13|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\vesa\_gen\_ctrl.vhd":281:5:281:16|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\vesa\_gen\_ctrl.vhd":282:5:282:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\vesa\_gen\_ctrl.vhd":283:5:283:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\vesa\_gen\_ctrl.vhd":284:5:284:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\vesa\_gen\_ctrl.vhd":325:5:325:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\vesa\_gen\_ctrl.vhd":329:4:329:16|Removed redundant assignment

Post processing for work.vesa\_gen\_ctrl.rtl\_vesa\_gen\_ctrl

@N: CD630 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":61:7:61:18|Synthesizing work.general\_fifo.arc\_general\_fifo

@N: CD364 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":245:6:245:10|Removed redundant assignment

Post processing for work.general\_fifo.arc\_general\_fifo

@N: CL134 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":96:7:96:9|Found RAM mem, depth=4864, width=8

@N: CL177 :"H:\Project\SG\_Project\VHDL\SG\general\_fifo.vhd":136:2:136:3|Sharing sequential element read\_addr\_dup.

@N: CD630 :"H:\Project\SG\_Project\VHDL\dc\_fifo.vhd":42:7:42:13|Synthesizing work.dc\_fifo.syn

@N: CD630 :"H:\Project\SG\_Project\VHDL\dc\_fifo.vhd":68:11:68:16|Synthesizing altera\_mf.dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1.syn\_black\_box

Post processing for altera\_mf.dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1.syn\_black\_box

Post processing for work.dc\_fifo.syn

@N: CD630 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":30:7:30:15|Synthesizing work.sg\_wbm\_if.rtl\_sg\_wbm\_if

@N: CD231 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":74:17:74:18|Using onehot encoding for type wbm\_states (wbm\_idle\_st="10000000000")

@N: CD364 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":116:4:116:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":238:6:238:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":279:6:279:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":358:6:358:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":399:5:399:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":402:4:402:10|Removed redundant assignment

Post processing for work.sg\_wbm\_if.rtl\_sg\_wbm\_if

@W: CL169 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Pruning Register dbg\_cnt(30 downto 0)

@W: CL190 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Optimizing register bit wbm\_tga\_o(0) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Optimizing register bit wbm\_tga\_o(2) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Optimizing register bit wbm\_tga\_o(3) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Optimizing register bit wbm\_tga\_o(4) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Optimizing register bit wbm\_tga\_o(6) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Optimizing register bit wbm\_tga\_o(7) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Optimizing register bit wbm\_tga\_o(8) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Optimizing register bit wbm\_tga\_o(9) to a constant 0

@W: CL260 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Pruning Register bit 9 of wbm\_tga\_o(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Pruning Register bit 8 of wbm\_tga\_o(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Pruning Register bit 7 of wbm\_tga\_o(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Pruning Register bit 6 of wbm\_tga\_o(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Pruning Register bit 4 of wbm\_tga\_o(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Pruning Register bit 3 of wbm\_tga\_o(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Pruning Register bit 2 of wbm\_tga\_o(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Pruning Register bit 0 of wbm\_tga\_o(9 downto 0)

@N: CD630 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":30:7:30:15|Synthesizing work.pixel\_mng.rtl\_pixel\_mng

@N: CD231 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":77:17:77:18|Using onehot encoding for type wbm\_states (wbm\_idle\_st="100000")

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":237:6:237:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":264:7:264:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":280:6:280:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":298:6:298:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":318:6:318:11|Removed redundant assignment

@W: CD604 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":321:4:321:17|OTHERS clause is not synthesized

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":345:5:345:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":349:4:349:14|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":370:4:370:10|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":375:5:375:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":380:4:380:14|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":385:5:385:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":390:4:390:14|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":395:5:395:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":399:4:399:10|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":400:4:400:14|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":421:5:421:10|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":427:4:427:9|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":473:4:473:14|Removed redundant assignment

Post processing for work.pixel\_mng.rtl\_pixel\_mng

Post processing for work.disp\_ctrl\_top.rtl\_disp\_ctrl\_top

@W: CL240 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":226:7:226:32|right\_frame\_reg\_dout\_valid is not assigned a value (floating) - a simulation mismatch is possible

@W: CL240 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":224:7:224:29|right\_frame\_reg\_din\_ack is not assigned a value (floating) - a simulation mismatch is possible

@W: CL240 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":223:7:223:31|left\_frame\_reg\_dout\_valid is not assigned a value (floating) - a simulation mismatch is possible

@W: CL240 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":221:7:221:28|left\_frame\_reg\_din\_ack is not assigned a value (floating) - a simulation mismatch is possible

@W: CL168 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":996:0:996:11|Pruning instance sc\_fifo\_inst - not in use ...

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to upper\_frame\_rg\_d1(8) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to upper\_frame\_rg\_d1(9) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to right\_frame\_rg\_d1(0) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to right\_frame\_rg\_d1(1) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to right\_frame\_rg\_d1(2) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to right\_frame\_rg\_d1(3) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to right\_frame\_rg\_d1(5) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to right\_frame\_rg\_d1(7) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to right\_frame\_rg\_d1(8) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to right\_frame\_rg\_d1(9) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to lower\_frame\_rg\_d1(8) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to lower\_frame\_rg\_d1(9) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to left\_frame\_rg\_d1(0) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to left\_frame\_rg\_d1(1) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to left\_frame\_rg\_d1(2) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to left\_frame\_rg\_d1(3) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to left\_frame\_rg\_d1(5) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to left\_frame\_rg\_d1(7) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to left\_frame\_rg\_d1(8) assign '0', register removed by optimization

@W: CL111 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|All reachable assignments to left\_frame\_rg\_d1(9) assign '0', register removed by optimization

@N: CL177 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Sharing sequential element left\_frame\_rg\_d1.

@N: CL177 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Sharing sequential element left\_frame\_rg\_d1.

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit left\_frame\_rg\_d2(0) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit left\_frame\_rg\_d2(1) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit left\_frame\_rg\_d2(2) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit left\_frame\_rg\_d2(3) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit left\_frame\_rg\_d2(5) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit left\_frame\_rg\_d2(7) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit left\_frame\_rg\_d2(8) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit left\_frame\_rg\_d2(9) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit lower\_frame\_rg\_d2(8) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit lower\_frame\_rg\_d2(9) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit right\_frame\_rg\_d2(0) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit right\_frame\_rg\_d2(1) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit right\_frame\_rg\_d2(2) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit right\_frame\_rg\_d2(3) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit right\_frame\_rg\_d2(5) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit right\_frame\_rg\_d2(7) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit right\_frame\_rg\_d2(8) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit right\_frame\_rg\_d2(9) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit upper\_frame\_rg\_d2(8) to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Optimizing register bit upper\_frame\_rg\_d2(9) to a constant 0

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 9 of left\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 8 of left\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 7 of left\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 5 of left\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 3 of left\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 2 of left\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 1 of left\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 0 of left\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 9 of lower\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 8 of lower\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 9 of right\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 8 of right\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 7 of right\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 5 of right\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 3 of right\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 2 of right\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 1 of right\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 0 of right\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 9 of upper\_frame\_rg\_d2(9 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 8 of upper\_frame\_rg\_d2(9 downto 0)

@N: CD630 :"H:\Project\SG\_Project\VHDL\mem\_mng\_top.vhd":29:7:29:17|Synthesizing work.mem\_mng\_top.rtl\_mem\_mng\_top

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_mng\_top.vhd":505:4:505:14|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_mng\_top.vhd":506:4:506:14|Removed redundant assignment

@N: CD630 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment

Post processing for work.gen\_reg.rtl\_gen\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment

Post processing for work.gen\_reg.rtl\_gen\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment

Post processing for work.gen\_reg.rtl\_gen\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":34:7:34:13|Synthesizing work.gen\_reg.rtl\_gen\_reg

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":102:5:102:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":106:4:106:11|Removed redundant assignment

Post processing for work.gen\_reg.rtl\_gen\_reg

@N: CD630 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd.vhd":36:7:36:17|Synthesizing work.mem\_ctrl\_rd.rtl\_mem\_ctrl\_rd

@N: CD630 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":35:7:35:21|Synthesizing work.mem\_ctrl\_rd\_wbm.rtl\_mem\_ctrl\_rd\_wbm

@N: CD231 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":97:17:97:18|Using onehot encoding for type wbm\_states (wbm\_idle\_st="10000")

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":219:7:219:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":226:6:226:16|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":231:5:231:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":232:5:232:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":233:5:233:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":266:6:266:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":267:6:267:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":268:6:268:16|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":279:6:279:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":284:7:284:20|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":298:8:298:20|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":308:7:308:19|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":309:7:309:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":310:7:310:20|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":311:7:311:19|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":317:5:317:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":318:5:318:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":323:6:323:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":347:6:347:21|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":386:5:386:18|Removed redundant assignment

@W: CD604 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":394:4:394:17|OTHERS clause is not synthesized

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":419:4:419:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":473:4:473:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":492:4:492:9|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":530:5:530:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":594:4:594:16|Removed redundant assignment

Post processing for work.mem\_ctrl\_rd\_wbm.rtl\_mem\_ctrl\_rd\_wbm

@N: CD630 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbs.vhd":37:7:37:21|Synthesizing work.mem\_ctrl\_rd\_wbs.rtl\_mem\_ctrl\_rd\_wbs

@N: CD231 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbs.vhd":83:17:83:18|Using onehot encoding for type wbs\_states (wbs\_idle\_st="1000000")

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbs.vhd":149:7:149:16|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbs.vhd":152:6:152:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbs.vhd":171:6:171:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbs.vhd":188:7:188:16|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbs.vhd":196:6:196:15|Removed redundant assignment

@W: CD604 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbs.vhd":204:4:204:17|OTHERS clause is not synthesized

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbs.vhd":309:5:309:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbs.vhd":314:4:314:17|Removed redundant assignment

Post processing for work.mem\_ctrl\_rd\_wbs.rtl\_mem\_ctrl\_rd\_wbs

@N: CD630 :"H:\Project\SG\_Project\VHDL\altera\_16to8\_dc\_ram.vhd":42:7:42:25|Synthesizing work.altera\_16to8\_dc\_ram.syn

@N: CD630 :"H:\Project\SG\_Project\VHDL\altera\_16to8\_dc\_ram.vhd":62:11:62:20|Synthesizing altera\_mf.altsyncram\_work\_top\_synthesis\_top\_synthesis\_rtl\_1.syn\_black\_box

Post processing for altera\_mf.altsyncram\_work\_top\_synthesis\_top\_synthesis\_rtl\_1.syn\_black\_box

Post processing for work.altera\_16to8\_dc\_ram.syn

Post processing for work.mem\_ctrl\_rd.rtl\_mem\_ctrl\_rd

@W: CL169 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd.vhd":382:2:382:3|Pruning Register rd\_addr\_reg\_d2(21 downto 0)

@W: CL169 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd.vhd":382:2:382:3|Pruning Register type\_reg\_d2(7 downto 0)

@W: CL169 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd.vhd":382:2:382:3|Pruning Register rd\_addr\_reg\_d1(21 downto 0)

@W: CL169 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd.vhd":382:2:382:3|Pruning Register type\_reg\_d1(7 downto 0)

@N: CD630 :"H:\Project\SG\_Project\VHDL\mem\_mng\_arbiter.vhd":30:7:30:21|Synthesizing work.mem\_mng\_arbiter.rtl\_mem\_mng\_arbiter

Post processing for work.mem\_mng\_arbiter.rtl\_mem\_mng\_arbiter

@N: CD630 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr.vhd":41:7:41:17|Synthesizing work.mem\_ctrl\_wr.rtl\_mem\_ctrl\_wr

@N: CD630 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":34:7:34:21|Synthesizing work.mem\_ctrl\_wr\_wbm.rtl\_mem\_ctrl\_wr\_wbm

@N: CD231 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":93:17:93:18|Using onehot encoding for type wbm\_states (wbm\_idle\_st="1000000000")

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":217:8:217:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":224:7:224:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":228:6:228:16|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":233:5:233:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":235:5:235:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":255:6:255:19|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":256:6:256:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":257:6:257:16|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":265:6:265:19|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":266:6:266:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":271:7:271:20|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":272:7:272:20|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":275:7:275:22|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":296:7:296:20|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":297:7:297:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":298:7:298:20|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":299:7:299:19|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":305:5:305:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":306:5:306:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":307:5:307:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":319:6:319:21|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":347:5:347:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":349:5:349:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":358:5:358:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":359:5:359:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":362:6:362:19|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":368:6:368:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":371:6:371:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":385:5:385:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":387:5:387:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":395:5:395:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":397:5:397:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":408:5:408:18|Removed redundant assignment

@W: CD604 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":415:4:415:17|OTHERS clause is not synthesized

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":471:4:471:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":514:5:514:16|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":518:4:518:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":525:6:525:17|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":528:5:528:16|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":536:4:536:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":537:4:537:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":574:4:574:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":597:4:597:9|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":645:4:645:13|Removed redundant assignment

Post processing for work.mem\_ctrl\_wr\_wbm.rtl\_mem\_ctrl\_wr\_wbm

@N: CL177 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":459:2:459:3|Sharing sequential element wr\_cnt\_en.

@N: CD630 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbs.vhd":25:7:25:21|Synthesizing work.mem\_ctrl\_wr\_wbs.rtl\_mem\_ctrl\_wr\_wbs

@N: CD231 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbs.vhd":67:17:67:18|Using onehot encoding for type wbs\_states (wbs\_idle\_st="10000")

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbs.vhd":131:5:131:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbs.vhd":159:7:159:20|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbs.vhd":176:6:176:19|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbs.vhd":181:5:181:18|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbs.vhd":200:6:200:15|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbs.vhd":205:5:205:18|Removed redundant assignment

@W: CD604 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbs.vhd":207:4:207:17|OTHERS clause is not synthesized

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbs.vhd":228:4:228:14|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbs.vhd":306:4:306:11|Removed redundant assignment

Post processing for work.mem\_ctrl\_wr\_wbs.rtl\_mem\_ctrl\_wr\_wbs

@N: CD630 :"H:\Project\SG\_Project\VHDL\altera\_8to16\_dc\_ram.vhd":42:7:42:25|Synthesizing work.altera\_8to16\_dc\_ram.syn

@N: CD630 :"H:\Project\SG\_Project\VHDL\altera\_8to16\_dc\_ram.vhd":62:11:62:20|Synthesizing altera\_mf.altsyncram\_work\_top\_synthesis\_top\_synthesis\_rtl\_3.syn\_black\_box

Post processing for altera\_mf.altsyncram\_work\_top\_synthesis\_top\_synthesis\_rtl\_3.syn\_black\_box

Post processing for work.altera\_8to16\_dc\_ram.syn

Post processing for work.mem\_ctrl\_wr.rtl\_mem\_ctrl\_wr

@W: CL170 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr.vhd":355:2:355:3|Pruning bit <0> of type\_reg\_wbm\_d1(7 downto 0) - not in use ...

@W: CL111 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr.vhd":355:2:355:3|All reachable assignments to type\_reg\_wbm\_d2(0) assign '0', register removed by optimization

Post processing for work.mem\_mng\_top.rtl\_mem\_mng\_top

@N: CD630 :"H:\Project\SG\_Project\VHDL\intercon\_mux.vhd":24:7:24:18|Synthesizing work.intercon\_mux.intercon\_mux\_rtl

Post processing for work.intercon\_mux.intercon\_mux\_rtl

@N: CD630 :"H:\Project\SG\_Project\VHDL\intercon.vhd":35:7:35:14|Synthesizing work.intercon.intercon\_rtl

@N: CD233 :"H:\Project\SG\_Project\VHDL\intercon.vhd":98:22:98:23|Using sequential encoding for type intercon\_states

@N: CD364 :"H:\Project\SG\_Project\VHDL\intercon.vhd":175:6:175:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\intercon.vhd":184:6:184:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\intercon.vhd":191:5:191:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\intercon.vhd":192:5:192:11|Removed redundant assignment

@W: CD604 :"H:\Project\SG\_Project\VHDL\intercon.vhd":194:4:194:19|OTHERS clause is not synthesized

Post processing for work.intercon.intercon\_rtl

@N: CD630 :"H:\Project\SG\_Project\VHDL\intercon.vhd":35:7:35:14|Synthesizing work.intercon.intercon\_rtl

@N: CD233 :"H:\Project\SG\_Project\VHDL\intercon.vhd":98:22:98:23|Using sequential encoding for type intercon\_states

@N: CD364 :"H:\Project\SG\_Project\VHDL\intercon.vhd":175:6:175:12|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\intercon.vhd":184:6:184:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\intercon.vhd":191:5:191:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\intercon.vhd":192:5:192:11|Removed redundant assignment

@W: CD604 :"H:\Project\SG\_Project\VHDL\intercon.vhd":194:4:194:19|OTHERS clause is not synthesized

Post processing for work.intercon.intercon\_rtl

Post processing for work.mds\_top.rtl\_mds\_top

@N: CD630 :"H:\Project\SG\_Project\VHDL\global\_nets\_top.vhd":37:7:37:21|Synthesizing work.global\_nets\_top.rtl\_global\_nets\_top

@N: CD630 :"H:\Project\SG\_Project\VHDL\reset\_blk\_top.vhd":38:7:38:19|Synthesizing work.reset\_blk\_top.rtl\_reset\_blk\_top

@N: CD630 :"H:\Project\SG\_Project\VHDL\sync\_rst\_gen.vhd":22:7:22:18|Synthesizing work.sync\_rst\_gen.rtl\_sync\_rst\_gen

Post processing for work.sync\_rst\_gen.rtl\_sync\_rst\_gen

@N: CD630 :"H:\Project\SG\_Project\VHDL\reset\_debouncer.vhd":30:7:30:21|Synthesizing work.reset\_debouncer.rtl\_reset\_debouncer

@N: CD364 :"H:\Project\SG\_Project\VHDL\reset\_debouncer.vhd":87:4:87:11|Removed redundant assignment

@N: CD364 :"H:\Project\SG\_Project\VHDL\reset\_debouncer.vhd":109:4:109:9|Removed redundant assignment

Post processing for work.reset\_debouncer.rtl\_reset\_debouncer

Post processing for work.reset\_blk\_top.rtl\_reset\_blk\_top

@N: CD630 :"H:\Project\SG\_Project\VHDL\clk\_blk\_top.vhd":32:7:32:17|Synthesizing work.clk\_blk\_top.rtl\_clk\_blk\_top

@N: CD630 :"H:\Project\SG\_Project\VHDL\pll.vhd":42:7:42:9|Synthesizing work.pll.syn

@N: CD630 :"H:\Project\SG\_Project\VHDL\pll.vhd":68:11:68:16|Synthesizing altera\_mf.altpll\_work\_top\_synthesis\_top\_synthesis\_rtl\_1.syn\_black\_box

Post processing for altera\_mf.altpll\_work\_top\_synthesis\_top\_synthesis\_rtl\_1.syn\_black\_box

Post processing for work.pll.syn

Post processing for work.clk\_blk\_top.rtl\_clk\_blk\_top

Post processing for work.global\_nets\_top.rtl\_global\_nets\_top

Post processing for work.top\_synthesis.top\_synthesis\_rtl

@W: CL138 :"H:\Project\SG\_Project\VHDL\intercon.vhd":167:2:167:3|Register 'wbs\_gnt' is only assigned 0 or its old value; the register will be removed

@N: CL201 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbs.vhd":119:2:119:3|Trying to extract state machine for register wbs\_cur\_st

Extracted state machine for register wbs\_cur\_st

State machine has 5 reachable states with original encodings of:

00001

00010

00100

01000

10000

@W: CL247 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbs.vhd":37:2:37:10|Input port bit 0 of wbs\_tga\_i(9 downto 0) is unused

@N: CL201 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":187:2:187:3|Trying to extract state machine for register wbm\_cur\_st

Extracted state machine for register wbm\_cur\_st

State machine has 10 reachable states with original encodings of:

0000000001

0000000010

0000000100

0000001000

0000010000

0000100000

0001000000

0010000000

0100000000

1000000000

@W: CL246 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr\_wbm.vhd":68:2:68:9|Input port bits 7 to 2 of type\_reg(7 downto 0) are unused

@N: CL135 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_wr.vhd":355:2:355:3|Found seqShift ram\_ready\_d3, depth=3, width=1

@N: CL201 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbs.vhd":136:2:136:3|Trying to extract state machine for register wbs\_cur\_st

Extracted state machine for register wbs\_cur\_st

State machine has 7 reachable states with original encodings of:

0000001

0000010

0000100

0001000

0010000

0100000

1000000

@W: CL247 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbs.vhd":49:2:49:10|Input port bit 0 of wbs\_tga\_i(9 downto 0) is unused

@N: CL201 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":188:2:188:3|Trying to extract state machine for register wbm\_cur\_st

Extracted state machine for register wbm\_cur\_st

State machine has 5 reachable states with original encodings of:

00001

00010

00100

01000

10000

@W: CL246 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd\_wbm.vhd":80:2:80:9|Input port bits 7 to 1 of type\_reg(7 downto 0) are unused

@N: CL135 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd.vhd":382:2:382:3|Found seqShift init\_rd\_d3, depth=3, width=1

@N: CL135 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd.vhd":382:2:382:3|Found seqShift restart\_rd\_d3, depth=3, width=1

@N: CL135 :"H:\Project\SG\_Project\VHDL\mem\_ctrl\_rd.vhd":456:2:456:3|Found seqShift ram\_ready\_d3, depth=3, width=1

@N: CL135 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":181:2:181:3|Found seqShift vsync\_sig, depth=3, width=1

@N: CL201 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":216:2:216:3|Trying to extract state machine for register cur\_st

Extracted state machine for register cur\_st

State machine has 6 reachable states with original encodings of:

000001

000010

000100

001000

010000

100000

@W: CL159 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":49:2:49:10|Input wbm\_dat\_i is unused

@W: CL159 :"H:\Project\SG\_Project\VHDL\pixel\_mng.vhd":61:2:61:9|Input term\_cyc is unused

@N: CL201 :"H:\Project\SG\_Project\VHDL\SG\SG\_WBM\_IF.vhd":161:2:161:3|Trying to extract state machine for register cur\_st

Extracted state machine for register cur\_st

State machine has 10 reachable states with original encodings of:

00000000001

00000000010

00000000100

00000001000

00000010000

00000100000

00001000000

00010000000

00100000000

01000000000

@N: CL201 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Trying to extract state machine for register frame\_state

Extracted state machine for register frame\_state

State machine has 5 reachable states with original encodings of:

000

001

010

011

100

@W: CL260 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 7 of right\_frame(7 downto 4)

@W: CL260 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 6 of right\_frame(7 downto 4)

@W: CL260 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 5 of lower\_frame(6 downto 2)

@W: CL260 :"H:\Project\SG\_Project\VHDL\synthetic\_frame\_generator.vhd":107:2:107:3|Pruning Register bit 4 of lower\_frame(6 downto 2)

@W: CL159 :"H:\Project\SG\_Project\VHDL\wbs\_reg.vhd":33:3:33:5|Input rst is unused

@W: CL159 :"H:\Project\SG\_Project\VHDL\wbs\_reg.vhd":36:3:36:7|Input clk\_i is unused

@N: CL201 :"H:\Project\SG\_Project\VHDL\SG\opcode\_unite.vhd":96:2:96:3|Trying to extract state machine for register current\_sm

Extracted state machine for register current\_sm

State machine has 3 reachable states with original encodings of:

00

01

10

@W: CL159 :"H:\Project\SG\_Project\VHDL\SG\opcode\_store.vhd":37:4:37:9|Input op\_cnt is unused

@W: CL260 :"H:\Project\SG\_Project\VHDL\SG\manager.vhd":447:2:447:3|Pruning Register bit 3 of sdram\_addr\_rd(21 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\SG\manager.vhd":447:2:447:3|Pruning Register bit 2 of sdram\_addr\_rd(21 downto 0)

@W: CL260 :"H:\Project\SG\_Project\VHDL\SG\manager.vhd":447:2:447:3|Pruning Register bit 1 of sdram\_addr\_rd(21 downto 0)

@W: CL189 :"H:\Project\SG\_Project\VHDL\SG\manager.vhd":447:2:447:3|Register bit sdram\_addr\_rd(0) is always 0, optimizing ...

@W: CL169 :"H:\Project\SG\_Project\VHDL\SG\manager.vhd":447:2:447:3|Pruning Register sdram\_addr\_rd(0)

@N: CL201 :"H:\Project\SG\_Project\VHDL\SG\manager.vhd":235:2:235:3|Trying to extract state machine for register current\_sm

Extracted state machine for register current\_sm

State machine has 5 reachable states with original encodings of:

00001

00010

00100

01000

10000

@W: CL260 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register bit 6 of right\_frame\_rg\_d1(6 downto 5)

@W: CL169 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register left\_frame\_rg\_d2(6)

@W: CL169 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register right\_frame\_rg\_d2(6)

@W: CL169 :"H:\Project\SG\_Project\VHDL\disp\_ctrl\_top.vhd":1307:1:1307:2|Pruning Register right\_frame\_rg\_d2(4)

@N: CL201 :"H:\Project\SG\_Project\VHDL\uart\_rx.vhd":119:2:119:3|Trying to extract state machine for register cur\_st

Extracted state machine for register cur\_st

State machine has 4 reachable states with original encodings of:

00001

00010

00100

10000

@W: CL190 :"H:\Project\SG\_Project\VHDL\uart\_rx.vhd":119:2:119:3|Optimizing register bit parity\_err to a constant 0

@W: CL190 :"H:\Project\SG\_Project\VHDL\uart\_rx.vhd":119:2:119:3|Optimizing register bit parity\_err\_i to a constant 0

@W: CL169 :"H:\Project\SG\_Project\VHDL\uart\_rx.vhd":119:2:119:3|Pruning Register parity\_err

@W: CL169 :"H:\Project\SG\_Project\VHDL\uart\_rx.vhd":119:2:119:3|Pruning Register parity\_err\_i

@N: CL201 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":180:2:180:3|Trying to extract state machine for register cur\_st

Extracted state machine for register cur\_st

State machine has 7 reachable states with original encodings of:

0000001

0000010

0000100

0001000

0010000

0100000

1000000

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_dec.vhd":328:2:328:3|Pruning Register bit 7 of eof\_blk(7 downto 6)

@N: CL201 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":420:2:420:3|Trying to extract state machine for register wbm\_cur\_st

Extracted state machine for register wbm\_cur\_st

State machine has 6 reachable states with original encodings of:

000001

000010

000100

001000

010000

100000

@W: CL159 :"H:\Project\SG\_Project\VHDL\rx\_path.vhd":67:4:67:12|Input wbm\_dat\_i is unused

@N: CL201 :"H:\Project\SG\_Project\VHDL\uart\_tx.vhd":111:2:111:3|Trying to extract state machine for register cur\_st

Extracted state machine for register cur\_st

State machine has 3 reachable states with original encodings of:

00

01

10

@N: CL201 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Trying to extract state machine for register cur\_st

Extracted state machine for register cur\_st

State machine has 9 reachable states with original encodings of:

000000001

000000010

000000100

000001000

000010000

000100000

001000000

010000000

100000000

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 7 of eof\_blk(7 downto 6)

@W: CL260 :"H:\Project\SG\_Project\VHDL\mp\_enc.vhd":174:2:174:3|Pruning Register bit 6 of sof\_blk(6 downto 5)

@W: CL159 :"H:\Project\SG\_Project\VHDL\gen\_reg.vhd":62:3:62:7|Input rd\_en is unused

@W: CL159 :"H:\Project\SG\_Project\VHDL\wbs\_reg.vhd":33:3:33:5|Input rst is unused

@W: CL159 :"H:\Project\SG\_Project\VHDL\wbs\_reg.vhd":36:3:36:7|Input clk\_i is unused

@N: CL201 :"H:\Project\SG\_Project\VHDL\tx\_path\_wbm.vhd":134:2:134:3|Trying to extract state machine for register wbm\_cur\_st

Extracted state machine for register wbm\_cur\_st

State machine has 3 reachable states with original encodings of:

00

01

10

@W: CL246 :"H:\Project\SG\_Project\VHDL\tx\_path.vhd":90:4:90:12|Input port bits 9 to 4 of wbs\_adr\_i(9 downto 0) are unused

@W: CL159 :"H:\Project\SG\_Project\VHDL\tx\_path.vhd":91:4:91:12|Input wbs\_tga\_i is unused

@END

Process took 0h:00m:01s realtime, 0h:00m:01s cputime

# Tue Apr 02 16:10:42 2013

###########################################################]

Synopsys Altera Technology Mapper, Version map520rc, Build 069R, Built May 14 2010 21:31:02

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Product Version D-2010.03-SP1

Reading constraint file: H:\Project\SG\_synthesis\_proj\SG.sdc

@N: MF249 |Running in 64-bit mode.

@N: MF257 |Gated clock conversion enabled

@N|Running in logic synthesis mode without enhanced optimization

@W: BN132 :"h:\project\sg\_project\vhdl\sg\sg\_wbm\_if.vhd":161:2:161:3|Removing sequential instance wbm\_tgc\_o, because it is equivalent to instance we\_internal

@W: BN132 :"h:\project\sg\_project\vhdl\sdram\_controller.vhd":642:1:642:2|Removing sequential instance dram\_ldqm, because it is equivalent to instance dram\_udqm

@W: BN132 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":328:2:328:3|Removing sequential instance eof\_blk[3], because it is equivalent to instance eof\_blk[6]

@W: BN132 :"h:\project\sg\_project\vhdl\mp\_enc.vhd":174:2:174:3|Removing sequential instance sof\_blk[5], because it is equivalent to instance eof\_blk[6]

@W: BN132 :"h:\project\sg\_project\vhdl\mp\_enc.vhd":174:2:174:3|Removing sequential instance eof\_blk[3], because it is equivalent to instance eof\_blk[6]

@W: BN132 :"h:\project\sg\_project\vhdl\mp\_enc.vhd":174:2:174:3|Removing sequential instance sof\_blk[2], because it is equivalent to instance eof\_blk[6]

Finished Timing Extraction Phase. (Time elapsed 0h:00m:00s; Memory used current: 111MB peak: 113MB)

Automatic dissolve during optimization of view:work.clk\_blk\_top(rtl\_clk\_blk\_top) of pll\_inst(pll)

Automatic dissolve during optimization of view:work.global\_nets\_top(rtl\_global\_nets\_top) of clk\_blk\_inst(clk\_blk\_top)

Automatic dissolve during optimization of view:work.mem\_ctrl\_wr(rtl\_mem\_ctrl\_wr) of ram1\_inst(altera\_8to16\_dc\_ram)

Automatic dissolve during optimization of view:work.mem\_ctrl\_rd(rtl\_mem\_ctrl\_rd) of ram1\_inst(altera\_16to8\_dc\_ram)

Automatic dissolve during optimization of view:work.disp\_ctrl\_top(rtl\_disp\_ctrl\_top) of dc\_fifo\_inst(dc\_fifo)

Automatic dissolve during optimization of view:work.top\_synthesis(top\_synthesis\_rtl) of msb\_version\_hexss\_inst(hexss)

Automatic dissolve during optimization of view:work.top\_synthesis(top\_synthesis\_rtl) of lsb\_version\_hexss\_inst(hexss)

Automatic dissolve during optimization of view:work.top\_synthesis(top\_synthesis\_rtl) of msb\_tx\_hexss\_inst(hexss)

Automatic dissolve during optimization of view:work.top\_synthesis(top\_synthesis\_rtl) of lsb\_tx\_hexss\_inst(hexss)

Automatic dissolve during optimization of view:work.top\_synthesis(top\_synthesis\_rtl) of msb\_disp\_hexss\_inst(hexss)

Automatic dissolve during optimization of view:work.top\_synthesis(top\_synthesis\_rtl) of lsb\_disp\_hexss\_inst(hexss)

Automatic dissolve during optimization of view:work.top\_synthesis(top\_synthesis\_rtl) of msb\_mem\_hexss\_inst(hexss)

Automatic dissolve during optimization of view:work.top\_synthesis(top\_synthesis\_rtl) of lsb\_mem\_hexss\_inst(hexss)

Automatic dissolve at startup in view:work.reset\_blk\_top(rtl\_reset\_blk\_top) of sync\_rst\_vesa\_inst(sync\_rst\_gen)

Automatic dissolve at startup in view:work.reset\_blk\_top(rtl\_reset\_blk\_top) of sync\_rst\_sys\_inst(sync\_rst\_gen)

Automatic dissolve at startup in view:work.reset\_blk\_top(rtl\_reset\_blk\_top) of sync\_rst\_sdram\_inst(sync\_rst\_gen)

Automatic dissolve at startup in view:work.mem\_mng\_top(rtl\_mem\_mng\_top) of wbs\_reg\_inst(wbs\_regZ1)

Automatic dissolve at startup in view:work.mem\_mng\_top(rtl\_mem\_mng\_top) of dbg\_reg\_generate\.0\.gen\_reg\_dbg\_inst(gen\_regZ0)

Automatic dissolve at startup in view:work.mem\_mng\_top(rtl\_mem\_mng\_top) of dbg\_reg\_generate\.1\.gen\_reg\_dbg\_inst(gen\_regZ1)

Automatic dissolve at startup in view:work.mem\_mng\_top(rtl\_mem\_mng\_top) of dbg\_reg\_generate\.2\.gen\_reg\_dbg\_inst(gen\_regZ2)

Automatic dissolve at startup in view:work.mem\_mng\_top(rtl\_mem\_mng\_top) of gen\_reg\_type\_inst(gen\_regZ3)

Automatic dissolve at startup in view:work.mem\_mng\_top(rtl\_mem\_mng\_top) of arbiter\_inst(mem\_mng\_arbiter)

Automatic dissolve at startup in view:work.opcode\_store(opcode\_store\_rtl) of general\_fifo\_inst(general\_fifoZ0)

@N: BN116 :"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":116:2:116:3|Removing sequential instance general\_fifo\_inst.dout\_valid of view:PrimLib.dffr(prim) because there are no references to its outputs

Automatic dissolve at startup in view:work.Symbol\_Generator\_Top(rtl\_symbol\_generator\_top) of mux2\_inst(mux2)

Automatic dissolve at startup in view:work.Symbol\_Generator\_Top(rtl\_symbol\_generator\_top) of RAM\_300\_inst(RAM\_300)

Automatic dissolve at startup in view:work.disp\_ctrl\_top(rtl\_disp\_ctrl\_top) of gen\_reg\_version\_inst(gen\_regZ4)

Automatic dissolve at startup in view:work.disp\_ctrl\_top(rtl\_disp\_ctrl\_top) of gen\_reg\_opcode\_unite\_inst(gen\_regZ5)

Automatic dissolve at startup in view:work.disp\_ctrl\_top(rtl\_disp\_ctrl\_top) of gen\_reg\_lower\_frame\_inst(gen\_regZ6)

Automatic dissolve at startup in view:work.disp\_ctrl\_top(rtl\_disp\_ctrl\_top) of gen\_reg\_upper\_frame\_inst(gen\_regZ7)

Automatic dissolve at startup in view:work.disp\_ctrl\_top(rtl\_disp\_ctrl\_top) of gen\_reg\_type\_inst(gen\_regZ8)

@N: BN116 :"h:\project\sg\_project\vhdl\gen\_reg.vhd":86:2:86:3|Removing sequential instance gen\_reg\_version\_inst.din\_ack of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\gen\_reg.vhd":86:2:86:3|Removing sequential instance gen\_reg\_lower\_frame\_inst.din\_ack of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\gen\_reg.vhd":86:2:86:3|Removing sequential instance gen\_reg\_upper\_frame\_inst.din\_ack of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\gen\_reg.vhd":86:2:86:3|Removing sequential instance gen\_reg\_type\_inst.din\_ack of view:PrimLib.dffr(prim) because there are no references to its outputs

Automatic dissolve at startup in view:work.rx\_path(rtl\_rx\_path) of checksum\_inst\_dec(checksum\_calc)

Automatic dissolve at startup in view:work.rx\_path(rtl\_rx\_path) of ram\_inst1(ram\_simple)

@N: BN116 :"h:\project\sg\_project\vhdl\ram\_simple.vhd":113:2:113:3|Removing sequential instance ram\_inst1.dout\_valid of view:PrimLib.dffr(prim) because there are no references to its outputs

Automatic dissolve at startup in view:work.tx\_path(arc\_tx\_path) of wbs\_reg\_inst(wbs\_regZ1)

Automatic dissolve at startup in view:work.tx\_path(arc\_tx\_path) of rd\_burst\_reg\_generate\.1\.gen\_rd\_burst\_reg\_inst(gen\_regZ10)

Automatic dissolve at startup in view:work.tx\_path(arc\_tx\_path) of rd\_burst\_reg\_generate\.0\.gen\_rd\_burst\_reg\_inst(gen\_regZ9)

Automatic dissolve at startup in view:work.tx\_path(arc\_tx\_path) of gen\_reg\_addr\_reg\_inst(gen\_regZ11)

Automatic dissolve at startup in view:work.tx\_path(arc\_tx\_path) of gen\_dbg\_cmd\_reg\_inst(gen\_regZ12)

Automatic dissolve at startup in view:work.tx\_path(arc\_tx\_path) of gen\_reg\_type\_inst(gen\_regZ13)

Automatic dissolve at startup in view:work.tx\_path(arc\_tx\_path) of fifo\_inst1(general\_fifoZ3)

Automatic dissolve at startup in view:work.tx\_path(arc\_tx\_path) of ram\_inst1(ram\_simple)

Automatic dissolve at startup in view:work.tx\_path(arc\_tx\_path) of checksum\_inst\_enc(checksum\_calc)

Automatic dissolve at startup in view:work.mds\_top(rtl\_mds\_top) of intercon\_x\_inst(intercon\_mux)

Automatic dissolve at startup in view:work.mds\_top(rtl\_mds\_top) of intercon\_y\_inst(interconZ0)

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":453:2:453:3|Removing sequential instance pix\_max\_b of view:PrimLib.dffr(prim) because there are no references to its outputs

Available hyper\_sources - for debug and ip models

None Found

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom msb\_version\_hexss\_inst.ss\_1[6:0] mapped in logic.

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom lsb\_version\_hexss\_inst.ss\_1[6:0] mapped in logic.

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom msb\_tx\_hexss\_inst.ss\_1[6:0] mapped in logic.

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom lsb\_tx\_hexss\_inst.ss\_1[6:0] mapped in logic.

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom msb\_disp\_hexss\_inst.ss\_1[6:0] mapped in logic.

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom lsb\_disp\_hexss\_inst.ss\_1[6:0] mapped in logic.

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom msb\_mem\_hexss\_inst.ss\_1[6:0] mapped in logic.

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom lsb\_mem\_hexss\_inst.ss\_1[6:0] mapped in logic.

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom msb\_version\_hexss\_inst.ss\_1[6:0] mapped in logic.

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom lsb\_version\_hexss\_inst.ss\_1[6:0] mapped in logic.

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom msb\_tx\_hexss\_inst.ss\_1[6:0] mapped in logic.

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom lsb\_tx\_hexss\_inst.ss\_1[6:0] mapped in logic.

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom msb\_disp\_hexss\_inst.ss\_1[6:0] mapped in logic.

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom lsb\_disp\_hexss\_inst.ss\_1[6:0] mapped in logic.

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom msb\_mem\_hexss\_inst.ss\_1[6:0] mapped in logic.

@N: FA239 :"h:\project\sg\_project\vhdl\hexss.vhd":48:3:48:11|Rom lsb\_mem\_hexss\_inst.ss\_1[6:0] mapped in logic.

Finished RTL optimizations (Time elapsed 0h:00m:00s; Memory used current: 113MB peak: 114MB)

@N:"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":119:2:119:3|Found counter in view:work.mem\_ctrl\_wr\_wbs(rtl\_mem\_ctrl\_wr\_wbs) inst ram\_expect\_adr[9:0]

@N:"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":298:2:298:3|Found counter in view:work.mem\_ctrl\_wr\_wbs(rtl\_mem\_ctrl\_wr\_wbs) inst done\_cnt[2:0]

Encoding state machine work.mem\_ctrl\_wr\_wbs(rtl\_mem\_ctrl\_wr\_wbs)-wbs\_cur\_st[0:4]

original code -> new code

00001 -> 00001

00010 -> 00010

00100 -> 00100

01000 -> 01000

10000 -> 10000

@N:"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbm.vhd":187:2:187:3|Found counter in view:work.mem\_ctrl\_wr\_wbm(rtl\_mem\_ctrl\_wr\_wbm) inst ram\_words\_left[8:0]

@N:"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbm.vhd":187:2:187:3|Found counter in view:work.mem\_ctrl\_wr\_wbm(rtl\_mem\_ctrl\_wr\_wbm) inst ram\_addr\_out\_i[8:0]

@N:"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbm.vhd":588:2:588:3|Found counter in view:work.mem\_ctrl\_wr\_wbm(rtl\_mem\_ctrl\_wr\_wbm) inst wr\_cnt[18:0]

@N:"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbm.vhd":550:2:550:3|Found counter in view:work.mem\_ctrl\_wr\_wbm(rtl\_mem\_ctrl\_wr\_wbm) inst ack\_i\_cnt[8:0]

Encoding state machine work.mem\_ctrl\_wr\_wbm(rtl\_mem\_ctrl\_wr\_wbm)-wbm\_cur\_st[0:9]

original code -> new code

0000000001 -> 0000000001

0000000010 -> 0000000010

0000000100 -> 0000000100

0000001000 -> 0000001000

0000010000 -> 0000010000

0000100000 -> 0000100000

0001000000 -> 0001000000

0010000000 -> 0010000000

0100000000 -> 0100000000

1000000000 -> 1000000000

@N:"h:\project\sg\_project\vhdl\mem\_ctrl\_rd\_wbs.vhd":300:2:300:3|Found counter in view:work.mem\_ctrl\_rd\_wbs(rtl\_mem\_ctrl\_rd\_wbs) inst ram\_expect\_adr[9:0]

Encoding state machine work.mem\_ctrl\_rd\_wbs(rtl\_mem\_ctrl\_rd\_wbs)-wbs\_cur\_st[0:6]

original code -> new code

0000001 -> 0000001

0000010 -> 0000010

0000100 -> 0000100

0001000 -> 0001000

0010000 -> 0010000

0100000 -> 0100000

1000000 -> 1000000

@N:"h:\project\sg\_project\vhdl\mem\_ctrl\_rd\_wbm.vhd":188:2:188:3|Found counter in view:work.mem\_ctrl\_rd\_wbm(rtl\_mem\_ctrl\_rd\_wbm) inst ram\_words\_left[8:0]

@N:"h:\project\sg\_project\vhdl\mem\_ctrl\_rd\_wbm.vhd":409:2:409:3|Found counter in view:work.mem\_ctrl\_rd\_wbm(rtl\_mem\_ctrl\_rd\_wbm) inst rd\_cnt\_i[18:0]

@N:"h:\project\sg\_project\vhdl\mem\_ctrl\_rd\_wbm.vhd":188:2:188:3|Found counter in view:work.mem\_ctrl\_rd\_wbm(rtl\_mem\_ctrl\_rd\_wbm) inst cur\_rd\_addr[21:0]

@N:"h:\project\sg\_project\vhdl\mem\_ctrl\_rd\_wbm.vhd":188:2:188:3|Found counter in view:work.mem\_ctrl\_rd\_wbm(rtl\_mem\_ctrl\_rd\_wbm) inst ram\_addr\_in\_i[8:0]

@N:"h:\project\sg\_project\vhdl\mem\_ctrl\_rd\_wbm.vhd":625:2:625:3|Found counter in view:work.mem\_ctrl\_rd\_wbm(rtl\_mem\_ctrl\_rd\_wbm) inst release\_arb\_cnt[12:0]

@N:"h:\project\sg\_project\vhdl\mem\_ctrl\_rd\_wbm.vhd":522:2:522:3|Found counter in view:work.mem\_ctrl\_rd\_wbm(rtl\_mem\_ctrl\_rd\_wbm) inst ram\_delay\_cnt[3:0]

Encoding state machine work.mem\_ctrl\_rd\_wbm(rtl\_mem\_ctrl\_rd\_wbm)-wbm\_cur\_st[0:4]

original code -> new code

00001 -> 00001

00010 -> 00010

00100 -> 00100

01000 -> 01000

10000 -> 10000

@N:"h:\project\sg\_project\vhdl\pixel\_mng.vhd":412:2:412:3|Found counter in view:work.pixel\_mng(rtl\_pixel\_mng) inst rd\_adr[9:0]

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":335:2:335:3|Register bit ack\_err\_cnt[10] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":335:2:335:3|Register bit ack\_err\_cnt[9] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":335:2:335:3|Register bit ack\_err\_cnt[8] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":335:2:335:3|Register bit ack\_err\_cnt[7] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":335:2:335:3|Register bit ack\_err\_cnt[6] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":335:2:335:3|Register bit ack\_err\_cnt[5] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":335:2:335:3|Register bit ack\_err\_cnt[4] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":335:2:335:3|Register bit ack\_err\_cnt[3] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":335:2:335:3|Register bit ack\_err\_cnt[2] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":335:2:335:3|Register bit ack\_err\_cnt[1] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":335:2:335:3|Register bit ack\_err\_cnt[0] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[18] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[17] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[16] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[15] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[14] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[13] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[12] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[11] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[10] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[9] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[8] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[7] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[6] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[5] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[4] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[3] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[2] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[1] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Register bit pix\_cnt[0] is always 0, optimizing ...

Encoding state machine work.pixel\_mng(rtl\_pixel\_mng)-cur\_st[0:5]

original code -> new code

000001 -> 000001

000010 -> 000010

000100 -> 000100

001000 -> 001000

010000 -> 010000

100000 -> 100000

@W: MO161 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":283:4:283:21|Register bit cur\_st[2] is always 0, optimizing ...

@N:"h:\project\sg\_project\vhdl\sg\sg\_wbm\_if.vhd":110:2:110:3|Found counter in view:work.SG\_WBM\_IF(rtl\_sg\_wbm\_if) inst vsync\_cnt[11:0]

@N:"h:\project\sg\_project\vhdl\sg\sg\_wbm\_if.vhd":389:2:389:3|Found counter in view:work.SG\_WBM\_IF(rtl\_sg\_wbm\_if) inst ack\_cnt[10:0]

Encoding state machine work.SG\_WBM\_IF(rtl\_sg\_wbm\_if)-cur\_st[0:9]

original code -> new code

00000000001 -> 0000000001

00000000010 -> 0000000010

00000000100 -> 0000000100

00000001000 -> 0000001000

00000010000 -> 0000010000

00000100000 -> 0000100000

00001000000 -> 0001000000

00010000000 -> 0010000000

00100000000 -> 0100000000

01000000000 -> 1000000000

@N:"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":166:2:166:3|Found counter in view:work.synthetic\_frame\_generator(rtl\_synthetic\_frame\_generator) inst hcnt[9:0]

@N:"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":166:2:166:3|Found counter in view:work.synthetic\_frame\_generator(rtl\_synthetic\_frame\_generator) inst vcnt[8:0]

Encoding state machine work.synthetic\_frame\_generator(rtl\_synthetic\_frame\_generator)-frame\_state[0:4]

original code -> new code

000 -> 000

001 -> 001

010 -> 010

011 -> 011

100 -> 100

@W: MO161 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Register bit upper\_frame[9] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Register bit upper\_frame[8] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Register bit upper\_frame[7] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Register bit upper\_frame[1] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Register bit upper\_frame[0] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Register bit left\_frame[9] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Register bit left\_frame[8] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Register bit left\_frame[3] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Register bit left\_frame[2] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Register bit left\_frame[1] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Register bit left\_frame[0] is always 0, optimizing ...

Encoding state machine work.opcode\_unite(opcode\_unite\_rtl)-current\_sm[0:2]

original code -> new code

00 -> 00

01 -> 01

10 -> 10

@N:"h:\project\sg\_project\vhdl\sg\opcode\_store.vhd":203:2:203:3|Found counter in view:work.opcode\_store(opcode\_store\_rtl) inst counter[9:0]

@N:"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":235:2:235:3|Found updn counter in view:work.opcode\_store(opcode\_store\_rtl) inst general\_fifo\_inst.count[8:0]

@N: BN116 :"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":182:2:182:3|Removing sequential instance general\_fifo\_inst.dout[23] of view:PrimLib.dff(prim) because there are no references to its outputs

@N:"h:\project\sg\_project\vhdl\sg\manager.vhd":361:2:361:3|Found counter in view:work.manager(manager\_rtl) inst sdram\_wait\_counter[7:0]

@N:"h:\project\sg\_project\vhdl\sg\manager.vhd":361:2:361:3|Found counter in view:work.manager(manager\_rtl) inst sdram\_wait\_counter\_tmp[7:0]

@N:"h:\project\sg\_project\vhdl\sg\manager.vhd":394:2:394:3|Found counter in view:work.manager(manager\_rtl) inst row\_count[10:0]

Encoding state machine work.manager(manager\_rtl)-current\_sm[0:4]

original code -> new code

00001 -> 00001

00010 -> 00010

00100 -> 00100

01000 -> 01000

10000 -> 10000

@N:"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":235:2:235:3|Found updn counter in view:work.general\_fifoZ1\_fifo\_A(arc\_general\_fifo) inst count[9:0]

@N:"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":235:2:235:3|Found updn counter in view:work.general\_fifoZ1\_fifo\_B\_0(arc\_general\_fifo) inst count[9:0]

@N:"h:\project\sg\_project\vhdl\rx\_path.vhd":420:2:420:3|Found counter in view:work.rx\_path(rtl\_rx\_path) inst ram\_bytes\_left[9:0]

Encoding state machine work.rx\_path(rtl\_rx\_path)-wbm\_cur\_st[0:5]

original code -> new code

000001 -> 000001

000010 -> 000010

000100 -> 000100

001000 -> 001000

010000 -> 010000

100000 -> 100000

@N:"h:\project\sg\_project\vhdl\uart\_rx.vhd":119:2:119:3|Found counter in view:work.uart\_rx(arc\_uart\_rx) inst pos\_cnt[3:0]

Encoding state machine work.uart\_rx(arc\_uart\_rx)-cur\_st[0:3]

original code -> new code

00001 -> 00

00010 -> 01

00100 -> 10

10000 -> 11

Encoding state machine work.mp\_dec(rtl\_mp\_dec)-cur\_st[0:6]

original code -> new code

0000001 -> 0000001

0000010 -> 0000010

0000100 -> 0000100

0001000 -> 0001000

0010000 -> 0010000

0100000 -> 0100000

1000000 -> 1000000

@N:"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":235:2:235:3|Found updn counter in view:work.tx\_path(arc\_tx\_path) inst fifo\_inst1.count[3:0]

@N:"h:\project\sg\_project\vhdl\uart\_tx.vhd":111:2:111:3|Found counter in view:work.uart\_tx(arc\_uart\_tx) inst pos\_cnt[3:0]

Encoding state machine work.uart\_tx(arc\_uart\_tx)-cur\_st[0:2]

original code -> new code

00 -> 00

01 -> 01

10 -> 10

Encoding state machine work.mp\_enc(rtl\_mp\_enc)-cur\_st[0:8]

original code -> new code

000000001 -> 000000001

000000010 -> 000000010

000000100 -> 000000100

000001000 -> 000001000

000010000 -> 000010000

000100000 -> 000100000

001000000 -> 001000000

010000000 -> 010000000

100000000 -> 100000000

@N:"h:\project\sg\_project\vhdl\tx\_path\_wbm.vhd":134:2:134:3|Found counter in view:work.tx\_path\_wbm(rtl\_tx\_path\_wbm) inst ram\_words\_left[10:0]

@N:"h:\project\sg\_project\vhdl\tx\_path\_wbm.vhd":134:2:134:3|Found counter in view:work.tx\_path\_wbm(rtl\_tx\_path\_wbm) inst ram\_in\_addr\_i[9:0]

Encoding state machine work.tx\_path\_wbm(rtl\_tx\_path\_wbm)-wbm\_cur\_st[0:2]

original code -> new code

00 -> 00

01 -> 01

10 -> 10

@N:"h:\project\sg\_project\vhdl\sg\led.vhd":62:2:62:3|Found counter in view:work.led(led\_rtl) inst timer\_counter[26:0]

@N:"h:\project\sg\_project\vhdl\sdram\_controller.vhd":224:1:224:2|Found counter in view:work.sdram\_controller(rtl\_sdram\_controller) inst rfsh\_int\_cntr[11:0]

@N:"h:\project\sg\_project\vhdl\sdram\_controller.vhd":224:1:224:2|Found counter in view:work.sdram\_controller(rtl\_sdram\_controller) inst wait\_200us\_cntr[14:0]

@N:"h:\project\sg\_project\vhdl\sdram\_controller.vhd":224:1:224:2|Found counter in view:work.sdram\_controller(rtl\_sdram\_controller) inst tRC\_cntr[3:0]

@N:"h:\project\sg\_project\vhdl\sdram\_controller.vhd":296:1:296:2|Found counter in view:work.sdram\_controller(rtl\_sdram\_controller) inst init\_pre\_cntr[3:0]

Starting Early Timing Optimization (Time elapsed 0h:00m:01s; Memory used current: 121MB peak: 122MB)

Finished Early Timing Optimization (Time elapsed 0h:00m:02s; Memory used current: 122MB peak: 122MB)

@W: MF244 :"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":96:7:96:9|Glue logic is created around ram "general\_fifo\_inst.mem[23:0]" to avoid read write conflict.

@W: MF245 :"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":96:7:96:9|To avoid this glue logic you can use syn\_ramstyle = "no\_rw\_check" attribute.

@W: MF244 :"h:\project\sg\_project\vhdl\ram\_simple.vhd":69:7:69:14|Glue logic is created around ram "ram\_inst1.ram\_data[7:0]" to avoid read write conflict.

@W: MF245 :"h:\project\sg\_project\vhdl\ram\_simple.vhd":69:7:69:14|To avoid this glue logic you can use syn\_ramstyle = "no\_rw\_check" attribute.

@W: MF244 :"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":96:7:96:9|Glue logic is created around ram "mem[7:0]" to avoid read write conflict.

@W: MF245 :"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":96:7:96:9|To avoid this glue logic you can use syn\_ramstyle = "no\_rw\_check" attribute.

@W: MF244 :"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":96:7:96:9|Glue logic is created around ram "mem[7:0]" to avoid read write conflict.

@W: MF245 :"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":96:7:96:9|To avoid this glue logic you can use syn\_ramstyle = "no\_rw\_check" attribute.

@W: MF244 :"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":96:7:96:9|Glue logic is created around ram "fifo\_inst1.mem[7:0]" to avoid read write conflict.

@W: MF245 :"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":96:7:96:9|To avoid this glue logic you can use syn\_ramstyle = "no\_rw\_check" attribute.

@W: BN132 :"h:\project\sg\_project\vhdl\ram\_simple.vhd":98:2:98:3|Removing sequential instance mds\_top\_inst.tx\_path\_inst.ram\_inst1.data\_out\_3[6], because it is equivalent to instance mds\_top\_inst.tx\_path\_inst.ram\_inst1.data\_out\_3[7]

@W: BN132 :"h:\project\sg\_project\vhdl\ram\_simple.vhd":98:2:98:3|Removing sequential instance mds\_top\_inst.tx\_path\_inst.ram\_inst1.data\_out\_3[5], because it is equivalent to instance mds\_top\_inst.tx\_path\_inst.ram\_inst1.data\_out\_3[7]

@W: BN132 :"h:\project\sg\_project\vhdl\ram\_simple.vhd":98:2:98:3|Removing sequential instance mds\_top\_inst.tx\_path\_inst.ram\_inst1.data\_out\_3[4], because it is equivalent to instance mds\_top\_inst.tx\_path\_inst.ram\_inst1.data\_out\_3[7]

@W: BN132 :"h:\project\sg\_project\vhdl\ram\_simple.vhd":98:2:98:3|Removing sequential instance mds\_top\_inst.tx\_path\_inst.ram\_inst1.data\_out\_3[3], because it is equivalent to instance mds\_top\_inst.tx\_path\_inst.ram\_inst1.data\_out\_3[7]

@W: BN132 :"h:\project\sg\_project\vhdl\ram\_simple.vhd":98:2:98:3|Removing sequential instance mds\_top\_inst.tx\_path\_inst.ram\_inst1.data\_out\_3[2], because it is equivalent to instance mds\_top\_inst.tx\_path\_inst.ram\_inst1.data\_out\_3[7]

@W: BN132 :"h:\project\sg\_project\vhdl\ram\_simple.vhd":98:2:98:3|Removing sequential instance mds\_top\_inst.tx\_path\_inst.ram\_inst1.data\_out\_3[1], because it is equivalent to instance mds\_top\_inst.tx\_path\_inst.ram\_inst1.data\_out\_3[7]

@W: BN132 :"h:\project\sg\_project\vhdl\ram\_simple.vhd":98:2:98:3|Removing sequential instance mds\_top\_inst.tx\_path\_inst.ram\_inst1.data\_out\_3[0], because it is equivalent to instance mds\_top\_inst.tx\_path\_inst.ram\_inst1.data\_out\_3[7]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[11], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[10], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[9], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[8], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[7], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[6], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[5], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[4], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[3], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[2], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[1], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[0], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_3[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[11], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[10], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[9], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[8], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[7], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[6], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[5], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[4], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[3], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[2], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[1], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[12]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\ram\_300.vhd":88:2:88:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[0], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.RAM\_300\_inst.ram\_data\_out\_0\_0[12]

@W: MO161 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Register bit right\_frame\_i[3] is always 1, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Register bit right\_frame\_i[2] is always 1, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Register bit right\_frame\_i[1] is always 1, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Register bit right\_frame\_i[0] is always 1, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Register bit upper\_frame\_i[9] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Register bit upper\_frame\_i[8] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Register bit left\_frame\_i[9] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Register bit left\_frame\_i[8] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Register bit left\_frame\_i[3] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Register bit left\_frame\_i[2] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Register bit left\_frame\_i[1] is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Register bit left\_frame\_i[0] is always 0, optimizing ...

Auto Dissolve of wbs\_inst (inst of view:work.mem\_ctrl\_wr\_wbs(rtl\_mem\_ctrl\_wr\_wbs))

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance wbs\_inst.type\_reg\_wbm[0] of view:PrimLib.dffr(prim) because there are no references to its outputs

Auto Dissolve of wbs\_inst (inst of view:work.mem\_ctrl\_rd\_wbs(rtl\_mem\_ctrl\_rd\_wbs))

Automatic dissolve during optimization of view:work.SG\_WBM\_IF(rtl\_sg\_wbm\_if) of fsm\_proc\.un42\_wbm\_dat\_o(PM\_top\_synthesis\_LSH\_\_24\_24\_5\_0000uuuuuuuuuuuuuuuuuu00\_ep2c35)

Automatic dissolve during optimization of view:work.SG\_WBM\_IF(rtl\_sg\_wbm\_if) of fsm\_proc\.un43\_wbm\_dat\_o(PM\_top\_synthesis\_RSH\_\_24\_24\_5\_0000uuuuuuuuuuuuuuuuuu00\_ep2c35)

Automatic dissolve during optimization of view:work.SG\_WBM\_IF(rtl\_sg\_wbm\_if) of fsm\_proc\.un19\_wbm\_dat\_o(PM\_top\_synthesis\_LSH\_\_24\_24\_5\_0000uuuuuuuuuuuuuuuuuu00\_ep2c35)

Automatic dissolve during optimization of view:work.SG\_WBM\_IF(rtl\_sg\_wbm\_if) of fsm\_proc\.un20\_wbm\_dat\_o(PM\_top\_synthesis\_RSH\_\_24\_24\_5\_0000uuuuuuuuuuuuuuuuuu00\_ep2c35)

Auto Dissolve of general\_fifo\_inst.mem\_98 (inst of view:VhdlGenLib.RAM\_R\_W\_400\_24\_TFFF\_NOSTYLE\_ygr1(block\_ram))

Automatic dissolve during optimization of view:work.general\_fifoZ1(arc\_general\_fifo) of mem\_34(RAM\_R\_W\_640\_8\_TFFF\_NOSTYLE\_ygr1\_0)

Automatic dissolve during optimization of view:work.disp\_ctrl\_top(rtl\_disp\_ctrl\_top) of wbs\_reg\_inst(wbs\_regZ0)

Auto Dissolve of Symbol\_Generator\_Top\_inst (inst of view:work.Symbol\_Generator\_Top(rtl\_symbol\_generator\_top))

Auto Dissolve of pixel\_mng\_inst (inst of view:work.pixel\_mng(rtl\_pixel\_mng))

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":308:4:308:26|Removing sequential instance pixel\_mng\_inst.cur\_st[0] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":302:4:302:24|Removing sequential instance pixel\_mng\_inst.cur\_st[1] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":252:4:252:20|Removing sequential instance pixel\_mng\_inst.cur\_st[3] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":243:4:243:25|Removing sequential instance pixel\_mng\_inst.cur\_st[4] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":223:4:223:22|Removing sequential instance pixel\_mng\_inst.cur\_st[5] of view:PrimLib.dffs(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[18] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[17] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[16] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[15] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[14] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[13] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[12] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[11] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[10] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[9] of view:PrimLib.dffs(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[8] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[7] of view:PrimLib.dffs(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[6] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[5] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[4] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[3] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[2] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[1] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":361:2:361:3|Removing sequential instance pixel\_mng\_inst.tot\_req\_pix[0] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":467:2:467:3|Removing sequential instance pixel\_mng\_inst.pix\_req\_add[9] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":467:2:467:3|Removing sequential instance pixel\_mng\_inst.pix\_req\_add[8] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":467:2:467:3|Removing sequential instance pixel\_mng\_inst.pix\_req\_add[7] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":467:2:467:3|Removing sequential instance pixel\_mng\_inst.pix\_req\_add[6] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":467:2:467:3|Removing sequential instance pixel\_mng\_inst.pix\_req\_add[5] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":467:2:467:3|Removing sequential instance pixel\_mng\_inst.pix\_req\_add[4] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":467:2:467:3|Removing sequential instance pixel\_mng\_inst.pix\_req\_add[3] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":467:2:467:3|Removing sequential instance pixel\_mng\_inst.pix\_req\_add[2] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":467:2:467:3|Removing sequential instance pixel\_mng\_inst.pix\_req\_add[1] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":467:2:467:3|Removing sequential instance pixel\_mng\_inst.pix\_req\_add[0] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":216:2:216:3|Removing sequential instance pixel\_mng\_inst.wbm\_tgc\_o of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":216:2:216:3|Removing sequential instance pixel\_mng\_inst.wbm\_stb\_o of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":216:2:216:3|Removing sequential instance pixel\_mng\_inst.cyc\_internal of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":439:2:439:3|Removing sequential instance pixel\_mng\_inst.end\_burst\_b of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":158:2:158:3|Removing sequential instance pixel\_mng\_inst.req\_trig\_sig of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":158:2:158:3|Removing sequential instance pixel\_mng\_inst.req\_trig\_d3 of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":158:2:158:3|Removing sequential instance pixel\_mng\_inst.req\_trig\_d2 of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":202:2:202:3|Removing sequential instance pixel\_mng\_inst.req\_trig\_b of view:PrimLib.dffs(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":158:2:158:3|Removing sequential instance pixel\_mng\_inst.req\_trig\_d1 of view:PrimLib.dffr(prim) because there are no references to its outputs

Automatic dissolve during optimization of view:work.rx\_path(rtl\_rx\_path) of ram\_inst1.ram\_data\_34(RAM\_R\_W\_1024\_8\_TFFF\_NOSTYLE\_ygr1)

Auto Dissolve of mp\_dec1 (inst of view:work.mp\_dec(rtl\_mp\_dec))

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":353:2:353:3|Removing sequential instance mp\_dec1.write\_addr[15] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":353:2:353:3|Removing sequential instance mp\_dec1.write\_addr[14] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":353:2:353:3|Removing sequential instance mp\_dec1.write\_addr[13] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":353:2:353:3|Removing sequential instance mp\_dec1.write\_addr[12] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":353:2:353:3|Removing sequential instance mp\_dec1.write\_addr[11] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":353:2:353:3|Removing sequential instance mp\_dec1.write\_addr[10] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":459:2:459:3|Removing sequential instance mp\_dec1.len\_reg[15] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":459:2:459:3|Removing sequential instance mp\_dec1.len\_reg[14] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":459:2:459:3|Removing sequential instance mp\_dec1.len\_reg[13] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":459:2:459:3|Removing sequential instance mp\_dec1.len\_reg[12] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":459:2:459:3|Removing sequential instance mp\_dec1.len\_reg[11] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":459:2:459:3|Removing sequential instance mp\_dec1.len\_reg[10] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":459:2:459:3|Removing sequential instance mp\_dec1.addr\_reg[15] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":459:2:459:3|Removing sequential instance mp\_dec1.addr\_reg[14] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":459:2:459:3|Removing sequential instance mp\_dec1.addr\_reg[13] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":459:2:459:3|Removing sequential instance mp\_dec1.addr\_reg[12] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":459:2:459:3|Removing sequential instance mp\_dec1.addr\_reg[11] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":459:2:459:3|Removing sequential instance mp\_dec1.addr\_reg[10] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":180:2:180:3|Removing sequential instance mp\_dec1.addr\_blk[15] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":180:2:180:3|Removing sequential instance mp\_dec1.addr\_blk[14] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":180:2:180:3|Removing sequential instance mp\_dec1.addr\_blk[13] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":180:2:180:3|Removing sequential instance mp\_dec1.addr\_blk[12] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":180:2:180:3|Removing sequential instance mp\_dec1.addr\_blk[11] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_dec.vhd":180:2:180:3|Removing sequential instance mp\_dec1.addr\_blk[10] of view:PrimLib.dffr(prim) because there are no references to its outputs

Automatic dissolve during optimization of view:work.tx\_path(arc\_tx\_path) of fifo\_inst1.mem\_34(RAM\_R\_W\_9\_8\_TFFF\_NOSTYLE\_ygr1)

Auto Dissolve of intercon\_z\_inst (inst of view:work.interconZ1(intercon\_rtl))

Finished factoring (Time elapsed 0h:00m:05s; Memory used current: 132MB peak: 133MB)

@N: BN116 :"h:\project\sg\_project\vhdl\tx\_path\_wbm.vhd":134:2:134:3|Removing sequential instance mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.wbm\_tga\_o[0] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mp\_enc.vhd":400:2:400:3|Removing sequential instance mds\_top\_inst.tx\_path\_inst.mp\_enc1.mp\_done of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\rx\_path.vhd":420:2:420:3|Removing sequential instance mds\_top\_inst.rx\_path\_inst.wbm\_tga\_o[0] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":307:2:307:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.pixels\_req[9] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":307:2:307:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.pixels\_req[8] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":307:2:307:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.pixels\_req[7] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":307:2:307:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.pixels\_req[6] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":307:2:307:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.pixels\_req[5] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":307:2:307:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.pixels\_req[4] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":307:2:307:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.pixels\_req[3] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":307:2:307:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.pixels\_req[2] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":307:2:307:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.pixels\_req[1] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":307:2:307:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.pixels\_req[0] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd.vhd":382:2:382:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.type\_reg\_wbm\_d1[7] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd.vhd":382:2:382:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.type\_reg\_wbm\_d1[6] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd.vhd":382:2:382:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.type\_reg\_wbm\_d1[5] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd.vhd":382:2:382:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.type\_reg\_wbm\_d1[4] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd.vhd":382:2:382:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.type\_reg\_wbm\_d1[3] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd.vhd":382:2:382:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.type\_reg\_wbm\_d1[2] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd.vhd":382:2:382:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.type\_reg\_wbm\_d1[1] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd.vhd":382:2:382:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.type\_reg\_wbm\_d2[7] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd.vhd":382:2:382:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.type\_reg\_wbm\_d2[6] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd.vhd":382:2:382:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.type\_reg\_wbm\_d2[5] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd.vhd":382:2:382:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.type\_reg\_wbm\_d2[4] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd.vhd":382:2:382:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.type\_reg\_wbm\_d2[3] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd.vhd":382:2:382:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.type\_reg\_wbm\_d2[2] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd.vhd":382:2:382:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.type\_reg\_wbm\_d2[1] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd\_wbs.vhd":384:2:384:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbs\_inst.type\_reg\_wbm[7] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd\_wbs.vhd":384:2:384:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbs\_inst.type\_reg\_wbm[6] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd\_wbs.vhd":384:2:384:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbs\_inst.type\_reg\_wbm[5] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd\_wbs.vhd":384:2:384:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbs\_inst.type\_reg\_wbm[4] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd\_wbs.vhd":384:2:384:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbs\_inst.type\_reg\_wbm[3] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd\_wbs.vhd":384:2:384:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbs\_inst.type\_reg\_wbm[2] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd\_wbs.vhd":384:2:384:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbs\_inst.type\_reg\_wbm[1] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.type\_reg\_wbm\_d1[7] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.type\_reg\_wbm\_d1[6] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.type\_reg\_wbm\_d1[5] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.type\_reg\_wbm\_d1[4] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.type\_reg\_wbm\_d1[3] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.type\_reg\_wbm\_d1[2] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[21] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[20] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[19] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[18] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[17] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[16] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[15] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[14] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[13] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[12] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[11] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[10] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[9] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[8] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[7] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[6] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[5] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[4] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[3] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[2] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[1] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d1[0] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.type\_reg\_wbm\_d2[7] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.type\_reg\_wbm\_d2[6] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.type\_reg\_wbm\_d2[5] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.type\_reg\_wbm\_d2[4] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.type\_reg\_wbm\_d2[3] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.type\_reg\_wbm\_d2[2] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[21] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[20] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[19] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[18] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[17] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[16] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[15] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[14] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[13] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[12] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[11] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[10] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[9] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[8] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[7] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[6] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[5] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[4] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[3] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[2] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[1] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr.vhd":355:2:355:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wr\_addr\_reg\_wbm\_d2[0] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[21] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[20] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[19] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[18] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[17] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[16] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[15] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[14] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[13] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[12] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[11] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[10] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[9] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[8] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[7] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[6] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[5] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[4] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[3] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[2] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[1] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.wr\_addr\_reg\_wbm[0] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.type\_reg\_wbm[7] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.type\_reg\_wbm[6] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.type\_reg\_wbm[5] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.type\_reg\_wbm[4] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.type\_reg\_wbm[3] of view:PrimLib.dffr(prim) because there are no references to its outputs

@N: BN116 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbs.vhd":318:2:318:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbs\_inst.type\_reg\_wbm[2] of view:PrimLib.dffr(prim) because there are no references to its outputs

@W: BN132 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":181:2:181:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.pixel\_mng\_inst.vsync\_d1, because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.opcode\_store\_inst.start\_trigger\_1

@W: BN132 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.vesa\_en\_i, because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.right\_frame\_rg\_d1[5]

@W: BN132 :"h:\project\sg\_project\vhdl\disp\_ctrl\_top.vhd":766:2:766:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.right\_frame[6], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.right\_frame[4]

@W: BN132 :"h:\project\sg\_project\vhdl\disp\_ctrl\_top.vhd":766:2:766:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.right\_frame[7], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.right\_frame[5]

@W: BN132 :"h:\project\sg\_project\vhdl\sg\opcode\_store.vhd":138:2:138:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.opcode\_store\_inst.start\_trigger\_2, because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.pixel\_mng\_inst.vsync\_d2

@W: BN132 :"h:\project\sg\_project\vhdl\pixel\_mng.vhd":181:2:181:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.pixel\_mng\_inst.vsync\_sig\_0, because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.opcode\_store\_inst.start\_trigger\_3

@W: BN132 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.frame\_state[1], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.lower\_frame\_1[6]

@W: BN132 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.left\_frame[7], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.left\_frame[5]

@W: BN132 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.left\_frame[6], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.left\_frame[4]

@W: BN132 :"h:\project\sg\_project\vhdl\disp\_ctrl\_top.vhd":766:2:766:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.left\_frame[7], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.left\_frame[5]

@W: BN132 :"h:\project\sg\_project\vhdl\disp\_ctrl\_top.vhd":766:2:766:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.left\_frame[6], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.left\_frame[4]

@W: BN132 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.upper\_frame[5], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.upper\_frame[4]

@W: BN132 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.left\_frame[4], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.right\_frame\_1[4]

@W: BN132 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.upper\_frame[2], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.right\_frame\_1[4]

@W: BN132 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.lower\_frame\_1[2], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.right\_frame\_1[4]

@W: BN132 :"h:\project\sg\_project\vhdl\disp\_ctrl\_top.vhd":766:2:766:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.left\_frame[4], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.right\_frame[4]

@W: BN132 :"h:\project\sg\_project\vhdl\synthetic\_frame\_generator.vhd":107:2:107:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.upper\_frame[4], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.synth\_pic\_gen\_inst.upper\_frame[3]

@W: BN132 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.left\_frame\_i[6], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.left\_frame\_i[4]

@W: BN132 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Removing sequential instance mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.left\_frame\_i[7], because it is equivalent to instance mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.left\_frame\_i[5]

@N:"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":198:2:198:3|Found counter in view:work.top\_synthesis(top\_synthesis\_rtl) inst mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.opcode\_store\_inst.general\_fifo\_inst.write\_addr[8:0]

@N:"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":198:2:198:3|Found counter in view:work.top\_synthesis(top\_synthesis\_rtl) inst mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.fifo\_A.read\_addr[9:0]

@N:"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":198:2:198:3|Found counter in view:work.top\_synthesis(top\_synthesis\_rtl) inst mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.fifo\_A.write\_addr[9:0]

@N:"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":198:2:198:3|Found counter in view:work.top\_synthesis(top\_synthesis\_rtl) inst mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.fifo\_B.read\_addr[9:0]

@N:"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":198:2:198:3|Found counter in view:work.top\_synthesis(top\_synthesis\_rtl) inst mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.fifo\_B.write\_addr[9:0]

@N:"h:\project\sg\_project\vhdl\rx\_path.vhd":420:2:420:3|Found counter in view:work.top\_synthesis(top\_synthesis\_rtl) inst mds\_top\_inst.rx\_path\_inst.ram\_addr\_out[9:0]

@N:"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":198:2:198:3|Found counter in view:work.top\_synthesis(top\_synthesis\_rtl) inst mds\_top\_inst.tx\_path\_inst.fifo\_inst1.read\_addr[3:0]

@N:"h:\project\sg\_project\vhdl\sg\general\_fifo.vhd":198:2:198:3|Found counter in view:work.top\_synthesis(top\_synthesis\_rtl) inst mds\_top\_inst.tx\_path\_inst.fifo\_inst1.write\_addr[3:0]

@W: MO161 :|Register bit false\_5 is always 0, optimizing ...

@W: MO161 :|Register bit false\_4 is always 0, optimizing ...

@W: MO161 :|Register bit false\_3 is always 0, optimizing ...

@W: MO161 :|Register bit false\_2 is always 0, optimizing ...

@W: MO161 :|Register bit false\_1 is always 0, optimizing ...

@W: MO161 :|Register bit false\_0 is always 0, optimizing ...

@W: MO161 :"h:\project\sg\_project\vhdl\vesa\_gen\_ctrl.vhd":255:2:255:3|Register bit mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.right\_frame\_i[9] is always 1, optimizing ...

@W: FA160 :"h:\project\sg\_project\vhdl\mem\_ctrl\_wr\_wbm.vhd":459:2:459:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbm\_inst.wr\_cnt\_to\_rd[18] of view:ALTERA\_APEX.S\_DFFE\_P(PRIM) because its output is stuck at constant value

@W: FA160 :"h:\project\sg\_project\vhdl\mem\_ctrl\_rd\_wbm.vhd":486:2:486:3|Removing sequential instance mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.rd\_cnt[18] of view:ALTERA\_APEX.S\_DFFE\_P(PRIM) because its output is stuck at constant value

#################### START OF GENERATED CLOCK OPTIMIZATION REPORT ####################[

======================================================================================

Instance:Pin Generated Clock Optimization Status

======================================================================================

mds\_top\_inst.rx\_path\_inst.wbm\_tga\_o[9]:CLK Not Done

mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.left\_frame\_i\_0[5]:CLK Not Done

global\_nets\_inst.reset\_blk\_inst.sync\_rst\_sdram\_inst.sync\_rst\_out:CLK Not Done

##################### END OF GENERATED CLOCK OPTIMIZATION REPORT #####################]

Finished gated-clock and generated-clock conversion (Time elapsed 0h:00m:08s; Memory used current: 142MB peak: 144MB)

Finished generic timing optimizations - Pass 1 (Time elapsed 0h:00m:09s; Memory used current: 138MB peak: 147MB)

Starting Early Timing Optimization (Time elapsed 0h:00m:09s; Memory used current: 140MB peak: 147MB)

Finished Early Timing Optimization (Time elapsed 0h:00m:15s; Memory used current: 143MB peak: 147MB)

Finished generic timing optimizations - Pass 2 (Time elapsed 0h:00m:15s; Memory used current: 142MB peak: 147MB)

Starting Early Timing Optimization (Time elapsed 0h:00m:16s; Memory used current: 143MB peak: 147MB)

Finished Early Timing Optimization (Time elapsed 0h:00m:17s; Memory used current: 143MB peak: 147MB)

Finished preparing to map (Time elapsed 0h:00m:18s; Memory used current: 143MB peak: 147MB)

Finished technology mapping (Time elapsed 0h:00m:24s; Memory used current: 204MB peak: 214MB)

Finished technology timing optimizations and critical path resynthesis (Time elapsed 0h:00m:27s; Memory used current: 208MB peak: 214MB)

Finished restoring hierarchy (Time elapsed 0h:00m:27s; Memory used current: 212MB peak: 214MB)

Writing Analyst data base H:\Project\SG\_synthesis\_proj\rev\_1\SG\_synthesis\_proj.srm

Finished Writing Netlist Databases (Time elapsed 0h:00m:29s; Memory used current: 205MB peak: 214MB)

Writing Verilog Netlist and constraint files

Writing .vqm output for Quartus

Finished Writing Verilog Netlist and constraint files (Time elapsed 0h:00m:35s; Memory used current: 206MB peak: 214MB)

Starting Writing Gated Clock Conversion Report (Time elapsed 0h:00m:35s; Memory used current: 201MB peak: 214MB)

@N: MF276 |Gated clock conversion enabled, but no gated clocks found in design

Finished Writing Gated Clock Conversion Report (Time elapsed 0h:00m:35s; Memory used current: 201MB peak: 214MB)

Starting Writing Generated Clock Conversion Report (Time elapsed 0h:00m:35s; Memory used current: 201MB peak: 214MB)

@N: MF333 |Generated clock conversion enabled, but no generated clocks found in design

Finished Writing Generated Clock Conversion Report (Time elapsed 0h:00m:35s; Memory used current: 201MB peak: 214MB)

Found clock fpga\_clk with period 20.00ns

Found clock global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock with period 25.00ns

Found clock global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock with period 10.00ns

Found clock global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock with period 7.50ns

@W: MT246 :"h:\project\sg\_project\vhdl\dc\_fifo.vhd":104:1:104:16|Blackbox dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1 is missing a user supplied timing model. This may have a negative effect on timing analysis and optimizations (Quality of Results)

##### START OF TIMING REPORT #####[

# Timing Report written on Tue Apr 02 16:12:47 2013

#

Top view: top\_synthesis

Requested Frequency: 40.0 MHz

Wire load mode: top

Paths requested: 5

Constraint File(s): H:\Project\SG\_synthesis\_proj\SG.sdc

@N: MT320 |This timing report estimates place and route data. Please look at the place and route timing report for final timing..

@N: MT322 |Clock constraints cover only FF-to-FF paths associated with the clock..

Performance Summary

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Worst slack in design: -0.023

Requested Estimated Requested Estimated Clock Clock

Starting Clock Frequency Frequency Period Period Slack Type Group

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fpga\_clk 50.0 MHz 615.0 MHz 20.000 1.626 18.374 declared default\_clkgroup\_0

global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock 133.3 MHz 134.0 MHz 7.500 7.465 0.035 derived (from fpga\_clk) default\_clkgroup\_0

global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock 100.0 MHz 99.8 MHz 10.000 10.023 -0.023 derived (from fpga\_clk) default\_clkgroup\_0

global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock 40.0 MHz 45.3 MHz 25.000 22.063 0.587 derived (from fpga\_clk) default\_clkgroup\_0

System 133.0 MHz 934.6 MHz 7.519 1.070 6.449 system default\_clkgroup5

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Clock Relationships

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Clocks | rise to rise | fall to fall | rise to fall | fall to rise

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Starting Ending | constraint slack | constraint slack | constraint slack | constraint slack

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fpga\_clk fpga\_clk | 20.000 18.374 | No paths - | No paths - | No paths -

global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock | 7.500 0.035 | No paths - | No paths - | No paths -

global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock | 2.500 1.740 | No paths - | No paths - | No paths -

global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock | 2.500 0.672 | No paths - | No paths - | No paths -

global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock | 10.000 -0.023 | No paths - | No paths - | No paths -

global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock | 5.000 3.794 | No paths - | No paths - | No paths -

global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock | 5.000 0.587 | No paths - | No paths - | No paths -

global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock | 25.000 19.174 | No paths - | No paths - | No paths -

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Note: 'No paths' indicates there are no paths in the design for that pair of clock edges.

'Diff grp' indicates that paths exist but the starting clock and ending clock are in different clock groups.

Interface Information

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

No IO constraint found

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Detailed Report for Clock: fpga\_clk

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Starting Points with Worst Slack

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Starting Arrival

Instance Reference Type Pin Net Time Slack

Clock

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global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.pll\_d3 fpga\_clk cycloneii\_lcell\_ff regout pll\_d3 0.250 18.374

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.reset\_d3 fpga\_clk cycloneii\_lcell\_ff regout reset\_d3 0.250 18.374

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.sync\_rst\_d2 fpga\_clk cycloneii\_lcell\_ff regout sync\_rst\_d2 0.250 18.374

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.pll\_d2 fpga\_clk cycloneii\_lcell\_ff regout pll\_d2 0.250 18.519

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.reset\_d2 fpga\_clk cycloneii\_lcell\_ff regout reset\_d2 0.250 18.519

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.pll\_db fpga\_clk cycloneii\_lcell\_ff regout pll\_db 0.250 18.644

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.reset\_db fpga\_clk cycloneii\_lcell\_ff regout reset\_db 0.250 18.644

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.pll\_d4 fpga\_clk cycloneii\_lcell\_ff regout pll\_d4 0.250 18.802

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.reset\_d4 fpga\_clk cycloneii\_lcell\_ff regout reset\_d4 0.250 18.802

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.sync\_rst\_d3 fpga\_clk cycloneii\_lcell\_ff regout sync\_rst\_d3 0.250 18.802

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Ending Points with Worst Slack

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Starting Required

Instance Reference Type Pin Net Time Slack

Clock

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global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.pll\_db fpga\_clk cycloneii\_lcell\_ff datain pll\_db\_1\_0\_g0 19.952 18.374

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.reset\_db fpga\_clk cycloneii\_lcell\_ff datain reset\_db\_1\_0\_g0 19.952 18.374

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.sync\_rst\_out fpga\_clk cycloneii\_lcell\_ff datain un3\_sync\_rst\_d2 19.952 18.374

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.pll\_d3 fpga\_clk cycloneii\_lcell\_ff datain pll\_d2 19.952 18.794

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.pll\_d4 fpga\_clk cycloneii\_lcell\_ff datain pll\_d3 19.952 18.794

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.reset\_d3 fpga\_clk cycloneii\_lcell\_ff datain reset\_d2 19.952 18.794

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.reset\_d4 fpga\_clk cycloneii\_lcell\_ff datain reset\_d3 19.952 18.794

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.sync\_rst\_d3 fpga\_clk cycloneii\_lcell\_ff datain sync\_rst\_d2 19.952 18.794

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.pll\_d2 fpga\_clk cycloneii\_lcell\_ff datain pll\_d1 19.952 19.240

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.reset\_d2 fpga\_clk cycloneii\_lcell\_ff datain reset\_d1 19.952 19.240

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Worst Path Information

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Path information for path number 1:

Requested Period: 20.000

- Setup time: 0.048

+ Clock delay at ending point: 0.000 (ideal)

= Required time: 19.952

- Propagation time: 1.578

- Clock delay at starting point: 0.000 (ideal)

= Slack (non-critical) : 18.374

Number of logic level(s): 1

Starting point: global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.pll\_d3 / regout

Ending point: global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.pll\_db / datain

The start point is clocked by fpga\_clk [rising] on pin clk

The end point is clocked by fpga\_clk [rising] on pin clk

Instance / Net Pin Pin Arrival No. of

Name Type Name Dir Delay Time Fan Out(s)

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global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.pll\_d3 cycloneii\_lcell\_ff regout Out 0.250 0.250 -

pll\_d3 Net - - 0.908 - 2

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.pll\_db\_RNO cycloneii\_lcell\_comb datab In - 1.158 -

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.pll\_db\_RNO cycloneii\_lcell\_comb combout Out 0.420 1.578 -

pll\_db\_1\_0\_g0 Net - - 0.000 - 1

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.pll\_db cycloneii\_lcell\_ff datain In - 1.578 -

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Total path delay (propagation time + setup) of 1.626 is 0.718(44.2%) logic and 0.908(55.8%) route.

Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value

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Detailed Report for Clock: global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock

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Starting Points with Worst Slack

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Starting Arrival

Instance Reference Type Pin Net Time Slack

Clock

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mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbm\_inst.wbm\_cyc\_internal global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff regout wbm\_cyc\_internal 0.250 0.035

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbm\_inst.neg\_cyc\_bool global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff regout neg\_cyc\_bool 0.250 0.053

mds\_top\_inst.mem\_mng\_inst.arbiter\_inst.wr\_gnt\_i\_i global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff regout wr\_gnt\_i\_i 0.250 0.172

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.ram\_words\_left[0] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff regout ram\_words\_left[0] 0.250 0.417

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.rd\_cnt\_i[0] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff regout rd\_cnt\_i[0] 0.250 0.421

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.cur\_rd\_addr[0] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff regout cur\_rd\_addr\_0 0.250 0.438

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.addr\_pipe[0] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff regout addr\_pipe[0] 0.250 0.522

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.ram\_words\_in\_d2[0] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff regout ram\_words\_in\_d2[0] 0.250 0.543

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.ram\_words\_left[1] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff regout ram\_words\_left[1] 0.250 0.546

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.rd\_cnt\_i[1] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff regout rd\_cnt\_i[1] 0.250 0.550

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Ending Points with Worst Slack

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Starting Required

Instance Reference Type Pin Net Time Slack

Clock

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mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.ram\_words\_cnt[7] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff sdata ram\_words\_cnt\_15\_m4[7] 7.170 0.035

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.ram\_words\_cnt[8] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff sdata ram\_words\_cnt\_15\_m4[8] 7.170 0.051

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.ram\_words\_cnt[6] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff sdata ram\_words\_cnt\_15\_m4[6] 7.170 0.164

mds\_top\_inst.sdr\_ctrl.blen\_cnt[8] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff datain un1\_blen\_cnt\_1\_sqmuxa\_2\_add8 7.452 0.172

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.ram\_words\_cnt[5] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff sdata ram\_words\_cnt\_15\_m4[5] 7.170 0.293

mds\_top\_inst.sdr\_ctrl.blen\_cnt[7] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff datain un1\_blen\_cnt\_1\_sqmuxa\_2\_add7 7.452 0.301

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.ram\_words\_cnt[0] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff sdata ram\_words\_cnt\_15\_m4[0] 7.170 0.417

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.ram\_words\_cnt[1] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff sdata ram\_words\_cnt\_15\_m4[1] 7.170 0.417

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.ram\_words\_cnt[2] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff sdata ram\_words\_cnt\_15\_m4[2] 7.170 0.417

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.ram\_words\_cnt[3] global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock cycloneii\_lcell\_ff sdata ram\_words\_cnt\_15\_m4[3] 7.170 0.417

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Worst Path Information

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Path information for path number 1:

Requested Period: 7.500

- Setup time: 0.330

+ Clock delay at ending point: 0.000 (ideal)

= Required time: 7.170

- Propagation time: 7.135

- Clock delay at starting point: 0.000 (ideal)

= Slack (non-critical) : 0.035

Number of logic level(s): 14

Starting point: mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbm\_inst.wbm\_cyc\_internal / regout

Ending point: mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.ram\_words\_cnt[7] / sdata

The start point is clocked by global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock [rising] on pin clk

The end point is clocked by global\_nets\_top|clk\_blk\_inst.pll\_inst.sdram\_clk\_derived\_clock [rising] on pin clk

Instance / Net Pin Pin Arrival No. of

Name Type Name Dir Delay Time Fan Out(s)

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mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbm\_inst.wbm\_cyc\_internal cycloneii\_lcell\_ff regout Out 0.250 0.250 -

wbm\_cyc\_internal Net - - 0.462 - 1

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbm\_inst.wbm\_cyc\_o cycloneii\_lcell\_comb dataa In - 0.712 -

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_wr\_inst.wbm\_inst.wbm\_cyc\_o cycloneii\_lcell\_comb combout Out 0.438 1.150 -

wbm\_cyc\_o Net - - 0.355 - 1

mds\_top\_inst.sdr\_ctrl.next\_state\_1\_sqmuxa\_7\_0\_a6\_0\_g2 cycloneii\_lcell\_comb datac In - 1.505 -

mds\_top\_inst.sdr\_ctrl.next\_state\_1\_sqmuxa\_7\_0\_a6\_0\_g2 cycloneii\_lcell\_comb combout Out 0.275 1.780 -

next\_state\_1\_sqmuxa\_7\_0\_a6\_0\_g2 Net - - 1.148 - 34

mds\_top\_inst.sdr\_ctrl.wbs\_stall\_o\_i cycloneii\_lcell\_comb datad In - 2.928 -

mds\_top\_inst.sdr\_ctrl.wbs\_stall\_o\_i cycloneii\_lcell\_comb combout Out 0.150 3.078 -

wbs\_stall\_o\_i Net - - 0.328 - 6

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.dat\_1st\_bool\_0\_sqmuxa cycloneii\_lcell\_comb datad In - 3.405 -

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.dat\_1st\_bool\_0\_sqmuxa cycloneii\_lcell\_comb combout Out 0.150 3.555 -

dat\_1st\_bool\_0\_sqmuxa Net - - 0.355 - 1

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_2 cycloneii\_lcell\_comb datad In - 3.910 -

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_2 cycloneii\_lcell\_comb combout Out 0.150 4.060 -

un1\_dat\_1st\_bool\_0\_sqmuxa\_2 Net - - 0.367 - 9

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add0 cycloneii\_lcell\_comb datab In - 4.427 -

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add0 cycloneii\_lcell\_comb cout Out 0.393 4.820 -

un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_carry\_0 Net - - 0.000 - 1

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add1 cycloneii\_lcell\_comb cin In - 4.820 -

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add1 cycloneii\_lcell\_comb cout Out 0.129 4.949 -

un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_carry\_1 Net - - 0.000 - 1

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add2 cycloneii\_lcell\_comb cin In - 4.949 -

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add2 cycloneii\_lcell\_comb cout Out 0.129 5.078 -

un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_carry\_2 Net - - 0.000 - 1

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add3 cycloneii\_lcell\_comb cin In - 5.078 -

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add3 cycloneii\_lcell\_comb cout Out 0.129 5.207 -

un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_carry\_3 Net - - 0.000 - 1

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add4 cycloneii\_lcell\_comb cin In - 5.207 -

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add4 cycloneii\_lcell\_comb cout Out 0.129 5.336 -

un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_carry\_4 Net - - 0.000 - 1

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add5 cycloneii\_lcell\_comb cin In - 5.336 -

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add5 cycloneii\_lcell\_comb cout Out 0.129 5.465 -

un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_carry\_5 Net - - 0.000 - 1

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add6 cycloneii\_lcell\_comb cin In - 5.465 -

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add6 cycloneii\_lcell\_comb cout Out 0.129 5.594 -

un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_carry\_6 Net - - 0.000 - 1

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add7 cycloneii\_lcell\_comb cin In - 5.594 -

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add7 cycloneii\_lcell\_comb combout Out 0.410 6.004 -

un1\_dat\_1st\_bool\_0\_sqmuxa\_5\_add7 Net - - 0.355 - 1

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.wbm\_fsm\_proc\.ram\_words\_cnt\_15\_m4[7] cycloneii\_lcell\_comb datab In - 6.359 -

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.wbm\_fsm\_proc\.ram\_words\_cnt\_15\_m4[7] cycloneii\_lcell\_comb combout Out 0.420 6.779 -

ram\_words\_cnt\_15\_m4[7] Net - - 0.355 - 1

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.ram\_words\_cnt[7] cycloneii\_lcell\_ff sdata In - 7.135 -

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Total path delay (propagation time + setup) of 7.465 is 3.740(50.1%) logic and 3.725(49.9%) route.

Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value

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Detailed Report for Clock: global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock

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Starting Points with Worst Slack

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Starting Arrival

Instance Reference Type Pin Net Time Slack

Clock

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mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.wbm\_tgc\_o global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff regout wbm\_tgc\_o 0.250 -0.023

mds\_top\_inst.intercon\_z\_inst.wbm\_gnt\_i\_0[0] global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff regout wbm\_gnt\_i\_0\_0 0.250 0.169

mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.cur\_rd\_addr[1] global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff regout cur\_rd\_addr\_1 0.250 0.342

mds\_top\_inst.rx\_path\_inst.wbm\_adr\_internal[1] global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff regout wbm\_adr\_internal\_1 0.250 0.360

mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.cur\_rd\_addr[2] global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff regout cur\_rd\_addr\_2 0.250 0.548

mds\_top\_inst.rx\_path\_inst.wbm\_adr\_internal[2] global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff regout wbm\_adr\_internal\_2 0.250 0.566

mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.cur\_rd\_addr[0] global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff regout cur\_rd\_addr\_0 0.250 0.629

mds\_top\_inst.rx\_path\_inst.wbm\_adr\_internal[0] global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff regout wbm\_adr\_internal\_0 0.250 0.647

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.rd\_addr\_reg\_wbm\_d2[21] global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff regout rd\_addr\_reg\_wbm\_d2[21] 0.250 0.672

mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.wbm\_cyc\_internal global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff regout wbm\_cyc\_internal 0.250 0.679

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Ending Points with Worst Slack

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Starting Required

Instance Reference Type Pin Net Time Slack

Clock

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mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5 global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff datain I\_3\_NE\_i\_0\_g0 9.952 -0.023

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.I\_1 global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock synplicity\_altsyncram5\_r\_w\_rx\_path address\_b[9] ram\_addr\_out\_4\_9 9.858 0.663

mds\_top\_inst.mem\_mng\_inst.mem\_ctrl\_rd\_inst.wbm\_inst.cur\_rd\_addr[21] global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff datain cur\_rd\_addr\_lm21 2.452 0.672

mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.cur\_rd\_addr[9] global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff datain cur\_rd\_addr\_8\_9\_0\_a2\_0\_g0 9.952 0.780

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.I\_1 global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock synplicity\_altsyncram5\_r\_w\_rx\_path address\_b[7] ram\_addr\_out\_4\_7 9.858 0.792

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.I\_1 global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock synplicity\_altsyncram5\_r\_w\_rx\_path address\_b[8] ram\_addr\_out\_4\_8 9.858 0.792

mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.ack\_i\_cnt[0] global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff sload inc\_wbm\_ack\_i 9.377 0.810

mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.ack\_i\_cnt[1] global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff sload inc\_wbm\_ack\_i 9.377 0.810

mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.ack\_i\_cnt[2] global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff sload inc\_wbm\_ack\_i 9.377 0.810

mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.ack\_i\_cnt[3] global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock cycloneii\_lcell\_ff sload inc\_wbm\_ack\_i 9.377 0.810

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Worst Path Information

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Path information for path number 1:

Requested Period: 10.000

- Setup time: 0.048

+ Clock delay at ending point: 0.000 (ideal)

= Required time: 9.952

- Propagation time: 9.975

- Clock delay at starting point: 0.000 (ideal)

= Slack (critical) : -0.023

Number of logic level(s): 17

Starting point: mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.wbm\_tgc\_o / regout

Ending point: mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5 / datain

The start point is clocked by global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock [rising] on pin clk

The end point is clocked by global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock [rising] on pin clk

Instance / Net Pin Pin Arrival No. of

Name Type Name Dir Delay Time Fan Out(s)

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mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.wbm\_tgc\_o cycloneii\_lcell\_ff regout Out 0.250 0.250 -

wbm\_tgc\_o Net - - 1.561 - 55

mds\_top\_inst.intercon\_z\_inst.fsm\_proc\.get\_wbs\.adrint\_i\_m3\_i\_m3[1] cycloneii\_lcell\_comb datad In - 1.811 -

mds\_top\_inst.intercon\_z\_inst.fsm\_proc\.get\_wbs\.adrint\_i\_m3\_i\_m3[1] cycloneii\_lcell\_comb combout Out 0.150 1.961 -

adrint\_i\_m3\_i\_m3\_1 Net - - 1.180 - 35

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_0 cycloneii\_lcell\_comb datad In - 3.140 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_0 cycloneii\_lcell\_comb combout Out 0.150 3.290 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_0 Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_1 cycloneii\_lcell\_comb datad In - 3.645 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_1 cycloneii\_lcell\_comb combout Out 0.150 3.795 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_1 Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c cycloneii\_lcell\_comb datab In - 4.151 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c cycloneii\_lcell\_comb combout Out 0.420 4.571 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_c Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_0 cycloneii\_lcell\_comb datad In - 4.926 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_0 cycloneii\_lcell\_comb combout Out 0.150 5.076 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_0 Net - - 0.301 - 3

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_a[0] cycloneii\_lcell\_comb datad In - 5.377 -

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_a[0] cycloneii\_lcell\_comb combout Out 0.150 5.527 -

ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_a[0] Net - - 0.355 - 1

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3[0] cycloneii\_lcell\_comb datad In - 5.882 -

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3[0] cycloneii\_lcell\_comb combout Out 0.150 6.032 -

ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_0 Net - - 0.301 - 3

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_19\_i cycloneii\_lcell\_comb datad In - 6.334 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_19\_i cycloneii\_lcell\_comb combout Out 0.150 6.484 -

un1\_wbm\_cur\_st\_19\_i Net - - 0.301 - 3

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22\_a[1] cycloneii\_lcell\_comb dataa In - 6.785 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22\_a[1] cycloneii\_lcell\_comb cout Out 0.414 7.199 -

un1\_wbm\_cur\_st\_22\_a\_cout[1] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[2] cycloneii\_lcell\_comb cin In - 7.199 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[2] cycloneii\_lcell\_comb cout Out 0.129 7.328 -

un1\_wbm\_cur\_st\_22\_cout[2] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[4] cycloneii\_lcell\_comb cin In - 7.328 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[4] cycloneii\_lcell\_comb cout Out 0.129 7.457 -

un1\_wbm\_cur\_st\_22\_cout[4] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[6] cycloneii\_lcell\_comb cin In - 7.457 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[6] cycloneii\_lcell\_comb cout Out 0.129 7.586 -

un1\_wbm\_cur\_st\_22\_cout[6] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[8] cycloneii\_lcell\_comb cin In - 7.586 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[8] cycloneii\_lcell\_comb cout Out 0.129 7.715 -

un1\_wbm\_cur\_st\_22\_cout[8] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[10] cycloneii\_lcell\_comb cin In - 7.715 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[10] cycloneii\_lcell\_comb combout Out 0.410 8.125 -

un1\_wbm\_cur\_st\_22\_combout[10] Net - - 0.355 - 1

mds\_top\_inst.rx\_path\_inst.wbm\_fsm\_proc\.ram\_addr\_out\_4[9] cycloneii\_lcell\_comb datab In - 8.480 -

mds\_top\_inst.rx\_path\_inst.wbm\_fsm\_proc\.ram\_addr\_out\_4[9] cycloneii\_lcell\_comb combout Out 0.420 8.900 -

ram\_addr\_out\_4[9] Net - - 0.295 - 2

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO\_3 cycloneii\_lcell\_comb datac In - 9.195 -

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO\_3 cycloneii\_lcell\_comb combout Out 0.275 9.470 -

I\_3\_NE\_i\_0\_g0\_a Net - - 0.355 - 1

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO cycloneii\_lcell\_comb datad In - 9.825 -

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO cycloneii\_lcell\_comb combout Out 0.150 9.975 -

I\_3\_NE\_i\_0\_g0 Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5 cycloneii\_lcell\_ff datain In - 9.975 -

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Total path delay (propagation time + setup) of 10.023 is 3.953(39.4%) logic and 6.070(60.6%) route.

Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value

Path information for path number 2:

Requested Period: 10.000

- Setup time: 0.048

+ Clock delay at ending point: 0.000 (ideal)

= Required time: 9.952

- Propagation time: 9.862

- Clock delay at starting point: 0.000 (ideal)

= Slack (non-critical) : 0.090

Number of logic level(s): 15

Starting point: mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.wbm\_tgc\_o / regout

Ending point: mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5 / datain

The start point is clocked by global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock [rising] on pin clk

The end point is clocked by global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock [rising] on pin clk

Instance / Net Pin Pin Arrival No. of

Name Type Name Dir Delay Time Fan Out(s)

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mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.wbm\_tgc\_o cycloneii\_lcell\_ff regout Out 0.250 0.250 -

wbm\_tgc\_o Net - - 1.561 - 55

mds\_top\_inst.intercon\_z\_inst.fsm\_proc\.get\_wbs\.adrint\_i\_m3\_i\_m3[1] cycloneii\_lcell\_comb datad In - 1.811 -

mds\_top\_inst.intercon\_z\_inst.fsm\_proc\.get\_wbs\.adrint\_i\_m3\_i\_m3[1] cycloneii\_lcell\_comb combout Out 0.150 1.961 -

adrint\_i\_m3\_i\_m3\_1 Net - - 1.180 - 35

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_0 cycloneii\_lcell\_comb datad In - 3.140 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_0 cycloneii\_lcell\_comb combout Out 0.150 3.290 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_0 Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_1 cycloneii\_lcell\_comb datad In - 3.645 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_1 cycloneii\_lcell\_comb combout Out 0.150 3.795 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_1 Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c cycloneii\_lcell\_comb datab In - 4.151 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c cycloneii\_lcell\_comb combout Out 0.420 4.571 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_c Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_0 cycloneii\_lcell\_comb datad In - 4.926 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_0 cycloneii\_lcell\_comb combout Out 0.150 5.076 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_0 Net - - 0.301 - 3

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_a[0] cycloneii\_lcell\_comb datad In - 5.377 -

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_a[0] cycloneii\_lcell\_comb combout Out 0.150 5.527 -

ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_a[0] Net - - 0.355 - 1

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3[0] cycloneii\_lcell\_comb datad In - 5.882 -

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3[0] cycloneii\_lcell\_comb combout Out 0.150 6.032 -

ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_0 Net - - 0.301 - 3

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_19\_i cycloneii\_lcell\_comb datad In - 6.334 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_19\_i cycloneii\_lcell\_comb combout Out 0.150 6.484 -

un1\_wbm\_cur\_st\_19\_i Net - - 0.301 - 3

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22\_a[1] cycloneii\_lcell\_comb dataa In - 6.785 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22\_a[1] cycloneii\_lcell\_comb cout Out 0.414 7.199 -

un1\_wbm\_cur\_st\_22\_a\_cout[1] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[2] cycloneii\_lcell\_comb cin In - 7.199 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[2] cycloneii\_lcell\_comb cout Out 0.129 7.328 -

un1\_wbm\_cur\_st\_22\_cout[2] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[4] cycloneii\_lcell\_comb cin In - 7.328 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[4] cycloneii\_lcell\_comb cout Out 0.129 7.457 -

un1\_wbm\_cur\_st\_22\_cout[4] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[6] cycloneii\_lcell\_comb cin In - 7.457 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[6] cycloneii\_lcell\_comb combout Out 0.410 7.867 -

un1\_wbm\_cur\_st\_22\_combout[6] Net - - 0.355 - 1

mds\_top\_inst.rx\_path\_inst.wbm\_fsm\_proc\.ram\_addr\_out\_4[5] cycloneii\_lcell\_comb datab In - 8.222 -

mds\_top\_inst.rx\_path\_inst.wbm\_fsm\_proc\.ram\_addr\_out\_4[5] cycloneii\_lcell\_comb combout Out 0.420 8.642 -

ram\_addr\_out\_4[5] Net - - 0.295 - 2

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO\_1 cycloneii\_lcell\_comb datad In - 8.937 -

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO\_1 cycloneii\_lcell\_comb combout Out 0.150 9.087 -

I\_3\_NE\_i\_0\_g0\_2 Net - - 0.355 - 1

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO cycloneii\_lcell\_comb datab In - 9.442 -

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO cycloneii\_lcell\_comb combout Out 0.420 9.862 -

I\_3\_NE\_i\_0\_g0 Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5 cycloneii\_lcell\_ff datain In - 9.862 -

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Total path delay (propagation time + setup) of 9.910 is 3.840(38.7%) logic and 6.070(61.3%) route.

Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value

Path information for path number 3:

Requested Period: 10.000

- Setup time: 0.048

+ Clock delay at ending point: 0.000 (ideal)

= Required time: 9.952

- Propagation time: 9.858

- Clock delay at starting point: 0.000 (ideal)

= Slack (non-critical) : 0.094

Number of logic level(s): 14

Starting point: mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.wbm\_tgc\_o / regout

Ending point: mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5 / datain

The start point is clocked by global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock [rising] on pin clk

The end point is clocked by global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock [rising] on pin clk

Instance / Net Pin Pin Arrival No. of

Name Type Name Dir Delay Time Fan Out(s)

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mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.wbm\_tgc\_o cycloneii\_lcell\_ff regout Out 0.250 0.250 -

wbm\_tgc\_o Net - - 1.561 - 55

mds\_top\_inst.intercon\_z\_inst.fsm\_proc\.get\_wbs\.adrint\_i\_m3\_i\_m3[1] cycloneii\_lcell\_comb datad In - 1.811 -

mds\_top\_inst.intercon\_z\_inst.fsm\_proc\.get\_wbs\.adrint\_i\_m3\_i\_m3[1] cycloneii\_lcell\_comb combout Out 0.150 1.961 -

adrint\_i\_m3\_i\_m3\_1 Net - - 1.180 - 35

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_0 cycloneii\_lcell\_comb datad In - 3.140 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_0 cycloneii\_lcell\_comb combout Out 0.150 3.290 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_0 Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_1 cycloneii\_lcell\_comb datad In - 3.645 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_1 cycloneii\_lcell\_comb combout Out 0.150 3.795 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_1 Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c cycloneii\_lcell\_comb datab In - 4.151 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c cycloneii\_lcell\_comb combout Out 0.420 4.571 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_c Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_0 cycloneii\_lcell\_comb datad In - 4.926 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_0 cycloneii\_lcell\_comb combout Out 0.150 5.076 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_0 Net - - 0.301 - 3

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_a[0] cycloneii\_lcell\_comb datad In - 5.377 -

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_a[0] cycloneii\_lcell\_comb combout Out 0.150 5.527 -

ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_a[0] Net - - 0.355 - 1

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3[0] cycloneii\_lcell\_comb datad In - 5.882 -

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3[0] cycloneii\_lcell\_comb combout Out 0.150 6.032 -

ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_0 Net - - 0.301 - 3

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_19\_i cycloneii\_lcell\_comb datad In - 6.334 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_19\_i cycloneii\_lcell\_comb combout Out 0.150 6.484 -

un1\_wbm\_cur\_st\_19\_i Net - - 0.301 - 3

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[1] cycloneii\_lcell\_comb dataa In - 6.785 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[1] cycloneii\_lcell\_comb cout Out 0.414 7.199 -

un1\_wbm\_cur\_st\_22\_cout[1] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[3] cycloneii\_lcell\_comb cin In - 7.199 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[3] cycloneii\_lcell\_comb cout Out 0.129 7.328 -

un1\_wbm\_cur\_st\_22\_cout[3] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[5] cycloneii\_lcell\_comb cin In - 7.328 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[5] cycloneii\_lcell\_comb combout Out 0.410 7.738 -

un1\_wbm\_cur\_st\_22\_combout[5] Net - - 0.355 - 1

mds\_top\_inst.rx\_path\_inst.wbm\_fsm\_proc\.ram\_addr\_out\_4[4] cycloneii\_lcell\_comb datab In - 8.093 -

mds\_top\_inst.rx\_path\_inst.wbm\_fsm\_proc\.ram\_addr\_out\_4[4] cycloneii\_lcell\_comb combout Out 0.420 8.513 -

ram\_addr\_out\_4[4] Net - - 0.295 - 2

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO\_1 cycloneii\_lcell\_comb datac In - 8.808 -

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO\_1 cycloneii\_lcell\_comb combout Out 0.275 9.083 -

I\_3\_NE\_i\_0\_g0\_2 Net - - 0.355 - 1

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO cycloneii\_lcell\_comb datab In - 9.438 -

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO cycloneii\_lcell\_comb combout Out 0.420 9.858 -

I\_3\_NE\_i\_0\_g0 Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5 cycloneii\_lcell\_ff datain In - 9.858 -

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Total path delay (propagation time + setup) of 9.906 is 3.836(38.7%) logic and 6.070(61.3%) route.

Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value

Path information for path number 4:

Requested Period: 10.000

- Setup time: 0.048

+ Clock delay at ending point: 0.000 (ideal)

= Required time: 9.952

- Propagation time: 9.846

- Clock delay at starting point: 0.000 (ideal)

= Slack (non-critical) : 0.106

Number of logic level(s): 16

Starting point: mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.wbm\_tgc\_o / regout

Ending point: mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5 / datain

The start point is clocked by global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock [rising] on pin clk

The end point is clocked by global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock [rising] on pin clk

Instance / Net Pin Pin Arrival No. of

Name Type Name Dir Delay Time Fan Out(s)

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mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.wbm\_tgc\_o cycloneii\_lcell\_ff regout Out 0.250 0.250 -

wbm\_tgc\_o Net - - 1.561 - 55

mds\_top\_inst.intercon\_z\_inst.fsm\_proc\.get\_wbs\.adrint\_i\_m3\_i\_m3[1] cycloneii\_lcell\_comb datad In - 1.811 -

mds\_top\_inst.intercon\_z\_inst.fsm\_proc\.get\_wbs\.adrint\_i\_m3\_i\_m3[1] cycloneii\_lcell\_comb combout Out 0.150 1.961 -

adrint\_i\_m3\_i\_m3\_1 Net - - 1.180 - 35

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_0 cycloneii\_lcell\_comb datad In - 3.140 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_0 cycloneii\_lcell\_comb combout Out 0.150 3.290 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_0 Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_1 cycloneii\_lcell\_comb datad In - 3.645 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_1 cycloneii\_lcell\_comb combout Out 0.150 3.795 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_1 Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c cycloneii\_lcell\_comb datab In - 4.151 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c cycloneii\_lcell\_comb combout Out 0.420 4.571 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_c Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_0 cycloneii\_lcell\_comb datad In - 4.926 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_0 cycloneii\_lcell\_comb combout Out 0.150 5.076 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_0 Net - - 0.301 - 3

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_a[0] cycloneii\_lcell\_comb datad In - 5.377 -

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_a[0] cycloneii\_lcell\_comb combout Out 0.150 5.527 -

ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_a[0] Net - - 0.355 - 1

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3[0] cycloneii\_lcell\_comb datad In - 5.882 -

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3[0] cycloneii\_lcell\_comb combout Out 0.150 6.032 -

ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_0 Net - - 0.301 - 3

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_19\_i cycloneii\_lcell\_comb datad In - 6.334 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_19\_i cycloneii\_lcell\_comb combout Out 0.150 6.484 -

un1\_wbm\_cur\_st\_19\_i Net - - 0.301 - 3

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22\_a[1] cycloneii\_lcell\_comb dataa In - 6.785 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22\_a[1] cycloneii\_lcell\_comb cout Out 0.414 7.199 -

un1\_wbm\_cur\_st\_22\_a\_cout[1] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[2] cycloneii\_lcell\_comb cin In - 7.199 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[2] cycloneii\_lcell\_comb cout Out 0.129 7.328 -

un1\_wbm\_cur\_st\_22\_cout[2] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[4] cycloneii\_lcell\_comb cin In - 7.328 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[4] cycloneii\_lcell\_comb cout Out 0.129 7.457 -

un1\_wbm\_cur\_st\_22\_cout[4] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[6] cycloneii\_lcell\_comb cin In - 7.457 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[6] cycloneii\_lcell\_comb cout Out 0.129 7.586 -

un1\_wbm\_cur\_st\_22\_cout[6] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[8] cycloneii\_lcell\_comb cin In - 7.586 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[8] cycloneii\_lcell\_comb combout Out 0.410 7.996 -

un1\_wbm\_cur\_st\_22\_combout[8] Net - - 0.355 - 1

mds\_top\_inst.rx\_path\_inst.wbm\_fsm\_proc\.ram\_addr\_out\_4[7] cycloneii\_lcell\_comb datab In - 8.351 -

mds\_top\_inst.rx\_path\_inst.wbm\_fsm\_proc\.ram\_addr\_out\_4[7] cycloneii\_lcell\_comb combout Out 0.420 8.771 -

ram\_addr\_out\_4[7] Net - - 0.295 - 2

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO\_2 cycloneii\_lcell\_comb datad In - 9.066 -

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO\_2 cycloneii\_lcell\_comb combout Out 0.150 9.216 -

I\_3\_NE\_i\_0\_g0\_3 Net - - 0.355 - 1

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO cycloneii\_lcell\_comb datac In - 9.571 -

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO cycloneii\_lcell\_comb combout Out 0.275 9.846 -

I\_3\_NE\_i\_0\_g0 Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5 cycloneii\_lcell\_ff datain In - 9.846 -

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Total path delay (propagation time + setup) of 9.894 is 3.824(38.6%) logic and 6.070(61.4%) route.

Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value

Path information for path number 5:

Requested Period: 10.000

- Setup time: 0.048

+ Clock delay at ending point: 0.000 (ideal)

= Required time: 9.952

- Propagation time: 9.846

- Clock delay at starting point: 0.000 (ideal)

= Slack (non-critical) : 0.106

Number of logic level(s): 16

Starting point: mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.wbm\_tgc\_o / regout

Ending point: mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5 / datain

The start point is clocked by global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock [rising] on pin clk

The end point is clocked by global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock [rising] on pin clk

Instance / Net Pin Pin Arrival No. of

Name Type Name Dir Delay Time Fan Out(s)

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mds\_top\_inst.tx\_path\_inst.tx\_wbm\_inst.wbm\_tgc\_o cycloneii\_lcell\_ff regout Out 0.250 0.250 -

wbm\_tgc\_o Net - - 1.561 - 55

mds\_top\_inst.intercon\_z\_inst.fsm\_proc\.get\_wbs\.adrint\_i\_m3\_i\_m3[1] cycloneii\_lcell\_comb datad In - 1.811 -

mds\_top\_inst.intercon\_z\_inst.fsm\_proc\.get\_wbs\.adrint\_i\_m3\_i\_m3[1] cycloneii\_lcell\_comb combout Out 0.150 1.961 -

adrint\_i\_m3\_i\_m3\_1 Net - - 1.180 - 35

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_0 cycloneii\_lcell\_comb datad In - 3.140 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_0 cycloneii\_lcell\_comb combout Out 0.150 3.290 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_0 Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_1 cycloneii\_lcell\_comb datad In - 3.645 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_1 cycloneii\_lcell\_comb combout Out 0.150 3.795 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_c\_1 Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c cycloneii\_lcell\_comb datab In - 4.151 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_c cycloneii\_lcell\_comb combout Out 0.420 4.571 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_c Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_0 cycloneii\_lcell\_comb datad In - 4.926 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_cyc\_i\_o2\_0\_0\_0 cycloneii\_lcell\_comb combout Out 0.150 5.076 -

wbs\_reg\_cyc\_i\_o2\_0\_0\_0 Net - - 0.301 - 3

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_a[0] cycloneii\_lcell\_comb datad In - 5.377 -

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_a[0] cycloneii\_lcell\_comb combout Out 0.150 5.527 -

ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_a[0] Net - - 0.355 - 1

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3[0] cycloneii\_lcell\_comb datad In - 5.882 -

mds\_top\_inst.intercon\_z\_inst.wbm\_stall\_comb\_proc\.0\.ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3[0] cycloneii\_lcell\_comb combout Out 0.150 6.032 -

ic\_wbm\_stall\_i\_11\_u\_i\_m3\_i\_m3\_0 Net - - 0.301 - 3

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_19\_i cycloneii\_lcell\_comb datad In - 6.334 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_19\_i cycloneii\_lcell\_comb combout Out 0.150 6.484 -

un1\_wbm\_cur\_st\_19\_i Net - - 0.301 - 3

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[1] cycloneii\_lcell\_comb dataa In - 6.785 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[1] cycloneii\_lcell\_comb cout Out 0.414 7.199 -

un1\_wbm\_cur\_st\_22\_cout[1] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[3] cycloneii\_lcell\_comb cin In - 7.199 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[3] cycloneii\_lcell\_comb cout Out 0.129 7.328 -

un1\_wbm\_cur\_st\_22\_cout[3] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[5] cycloneii\_lcell\_comb cin In - 7.328 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[5] cycloneii\_lcell\_comb cout Out 0.129 7.457 -

un1\_wbm\_cur\_st\_22\_cout[5] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[7] cycloneii\_lcell\_comb cin In - 7.457 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[7] cycloneii\_lcell\_comb cout Out 0.129 7.586 -

un1\_wbm\_cur\_st\_22\_cout[7] Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[9] cycloneii\_lcell\_comb cin In - 7.586 -

mds\_top\_inst.rx\_path\_inst.un1\_wbm\_cur\_st\_22[9] cycloneii\_lcell\_comb combout Out 0.410 7.996 -

un1\_wbm\_cur\_st\_22\_combout[9] Net - - 0.295 - 2

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO\_4 cycloneii\_lcell\_comb datac In - 8.291 -

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO\_4 cycloneii\_lcell\_comb combout Out 0.275 8.566 -

I\_3\_8\_0\_0 Net - - 0.355 - 1

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO\_3 cycloneii\_lcell\_comb datab In - 8.921 -

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO\_3 cycloneii\_lcell\_comb combout Out 0.420 9.341 -

I\_3\_NE\_i\_0\_g0\_a Net - - 0.355 - 1

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO cycloneii\_lcell\_comb datad In - 9.696 -

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5\_RNO cycloneii\_lcell\_comb combout Out 0.150 9.846 -

I\_3\_NE\_i\_0\_g0 Net - - 0.000 - 1

mds\_top\_inst.rx\_path\_inst.ram\_inst1.ram\_data\_34.G\_5 cycloneii\_lcell\_ff datain In - 9.846 -

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Total path delay (propagation time + setup) of 9.894 is 3.824(38.6%) logic and 6.070(61.4%) route.

Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value

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Detailed Report for Clock: global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock

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Starting Points with Worst Slack

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Starting Arrival

Instance Reference Type Pin Net Time Slack

Clock

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mds\_top\_inst.disp\_ctrl\_inst.right\_frame[4] global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock cycloneii\_lcell\_ff regout right\_frame[4] 0.250 0.587

mds\_top\_inst.disp\_ctrl\_inst.right\_frame[5] global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock cycloneii\_lcell\_ff regout right\_frame\_1 0.250 0.587

mds\_top\_inst.disp\_ctrl\_inst.lower\_frame[5] global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock cycloneii\_lcell\_ff regout lower\_frame\_5 0.250 0.797

mds\_top\_inst.disp\_ctrl\_inst.lower\_frame[6] global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock cycloneii\_lcell\_ff regout lower\_frame[6] 0.250 0.922

mds\_top\_inst.disp\_ctrl\_inst.left\_frame[5] global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock cycloneii\_lcell\_ff regout left\_frame\_0 0.250 1.195

mds\_top\_inst.disp\_ctrl\_inst.lower\_frame[0] global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock cycloneii\_lcell\_ff regout lower\_frame[0] 0.250 1.195

mds\_top\_inst.disp\_ctrl\_inst.lower\_frame[1] global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock cycloneii\_lcell\_ff regout lower\_frame[1] 0.250 1.195

mds\_top\_inst.disp\_ctrl\_inst.lower\_frame[2] global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock cycloneii\_lcell\_ff regout lower\_frame[2] 0.250 1.195

mds\_top\_inst.disp\_ctrl\_inst.lower\_frame[3] global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock cycloneii\_lcell\_ff regout lower\_frame[3] 0.250 1.195

mds\_top\_inst.disp\_ctrl\_inst.lower\_frame[4] global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock cycloneii\_lcell\_ff regout lower\_frame[4] 0.250 1.302

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Ending Points with Worst Slack

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Starting Required

Instance Reference Type Pin Net Time Slack

Clock

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mds\_top\_inst.tx\_path\_inst.ram\_inst1.ram\_data global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock synplicity\_altsyncram4\_r\_w\_tx\_path data\_a[4] inc\_wbm\_dat\_i\_4 4.894 0.587

mds\_top\_inst.tx\_path\_inst.ram\_inst1.ram\_data global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock synplicity\_altsyncram4\_r\_w\_tx\_path data\_a[7] inc\_wbm\_dat\_i\_7 4.894 0.587

mds\_top\_inst.tx\_path\_inst.ram\_inst1.ram\_data global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock synplicity\_altsyncram4\_r\_w\_tx\_path data\_a[5] inc\_wbm\_dat\_i\_5 4.894 0.732

mds\_top\_inst.tx\_path\_inst.ram\_inst1.ram\_data global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock synplicity\_altsyncram4\_r\_w\_tx\_path data\_a[6] inc\_wbm\_dat\_i\_6 4.894 0.857

mds\_top\_inst.tx\_path\_inst.ram\_inst1.ram\_data global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock synplicity\_altsyncram4\_r\_w\_tx\_path data\_a[0] inc\_wbm\_dat\_i\_0 4.894 1.195

mds\_top\_inst.tx\_path\_inst.ram\_inst1.ram\_data global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock synplicity\_altsyncram4\_r\_w\_tx\_path data\_a[1] inc\_wbm\_dat\_i\_1 4.894 1.195

mds\_top\_inst.tx\_path\_inst.ram\_inst1.ram\_data global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock synplicity\_altsyncram4\_r\_w\_tx\_path data\_a[2] inc\_wbm\_dat\_i\_2 4.894 1.195

mds\_top\_inst.tx\_path\_inst.ram\_inst1.ram\_data global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock synplicity\_altsyncram4\_r\_w\_tx\_path data\_a[3] inc\_wbm\_dat\_i\_3 4.894 1.195

mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.opcode\_store\_inst.start\_trigger\_1 global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock cycloneii\_lcell\_ff datain vsync\_i 4.952 3.794

mds\_top\_inst.disp\_ctrl\_inst.Symbol\_Generator\_Top\_inst.manager\_inst.req\_in\_trg\_1 global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock cycloneii\_lcell\_ff datain req\_ln\_trig 4.952 4.240

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Worst Path Information

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Path information for path number 1:

Requested Period: 5.000

- Setup time: 0.106

+ Clock delay at ending point: 0.000 (ideal)

= Required time: 4.894

- Propagation time: 4.307

- Clock delay at starting point: 0.000 (ideal)

= Slack (non-critical) : 0.587

Number of logic level(s): 5

Starting point: mds\_top\_inst.disp\_ctrl\_inst.right\_frame[4] / regout

Ending point: mds\_top\_inst.tx\_path\_inst.ram\_inst1.ram\_data / data\_a[4]

The start point is clocked by global\_nets\_top|clk\_blk\_inst.pll\_inst.vesa\_clk\_derived\_clock [rising] on pin clk

The end point is clocked by global\_nets\_top|clk\_blk\_inst.pll\_inst.system\_clk\_derived\_clock [rising] on pin clock0

Instance / Net Pin Pin Arrival No. of

Name Type Name Dir Delay Time Fan Out(s)

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mds\_top\_inst.disp\_ctrl\_inst.right\_frame[4] cycloneii\_lcell\_ff regout Out 0.250 0.250 -

right\_frame[4] Net - - 0.908 - 9

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_dout\_m\_0\_0\_a2\_2[6] cycloneii\_lcell\_comb dataa In - 1.158 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_dout\_m\_0\_0\_a2\_2[6] cycloneii\_lcell\_comb combout Out 0.438 1.596 -

wbs\_reg\_dout\_m\_0\_0\_a2\_2[6] Net - - 0.295 - 2

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_dout\_m\_0\_0\_1[4] cycloneii\_lcell\_comb datab In - 1.891 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_dout\_m\_0\_0\_1[4] cycloneii\_lcell\_comb combout Out 0.420 2.311 -

wbs\_reg\_dout\_m\_0\_0\_1[4] Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_dout\_m\_0\_0[4] cycloneii\_lcell\_comb datac In - 2.666 -

mds\_top\_inst.disp\_ctrl\_inst.wbs\_reg\_dout\_m\_0\_0[4] cycloneii\_lcell\_comb combout Out 0.275 2.941 -

wbs\_reg\_dout\_m\_0\_0\_0 Net - - 0.355 - 1

mds\_top\_inst.intercon\_z\_inst.wbm\_dat\_comb\_proc\.0\.ic\_wbm\_dat\_i\_11[4] cycloneii\_lcell\_comb datad In - 3.296 -

mds\_top\_inst.intercon\_z\_inst.wbm\_dat\_comb\_proc\.0\.ic\_wbm\_dat\_i\_11[4] cycloneii\_lcell\_comb combout Out 0.150 3.446 -

ic\_wbm\_dat\_i\_11\_4 Net - - 0.355 - 1

mds\_top\_inst.intercon\_x\_inst.inc\_wbm\_dat\_i[4] cycloneii\_lcell\_comb datad In - 3.801 -

mds\_top\_inst.intercon\_x\_inst.inc\_wbm\_dat\_i[4] cycloneii\_lcell\_comb combout Out 0.150 3.951 -

inc\_wbm\_dat\_i\_4 Net - - 0.355 - 1

mds\_top\_inst.tx\_path\_inst.ram\_inst1.ram\_data synplicity\_altsyncram4\_r\_w\_tx\_path data\_a[4] In - 4.307 -

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Total path delay (propagation time + setup) of 4.413 is 1.789(40.5%) logic and 2.624(59.5%) route.

Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value

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Detailed Report for Clock: System

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Starting Points with Worst Slack

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Starting Arrival

Instance Reference Type Pin Net Time Slack

Clock

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mds\_top\_inst.disp\_ctrl\_inst.dc\_fifo\_inst.dcfifo\_component System dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1 rdempty dc\_fifo\_empty 0.000 6.449

global\_nets\_inst.clk\_blk\_inst.pll\_inst.altpll\_component System altpll\_work\_top\_synthesis\_top\_synthesis\_rtl\_1 locked pll\_locked\_i 0.000 19.597

mds\_top\_inst.disp\_ctrl\_inst.dc\_fifo\_inst.dcfifo\_component System dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1 q[0] dc\_fifo\_dout\_0 0.000 24.213

mds\_top\_inst.disp\_ctrl\_inst.dc\_fifo\_inst.dcfifo\_component System dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1 q[1] dc\_fifo\_dout\_1 0.000 24.213

mds\_top\_inst.disp\_ctrl\_inst.dc\_fifo\_inst.dcfifo\_component System dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1 q[2] dc\_fifo\_dout\_2 0.000 24.213

mds\_top\_inst.disp\_ctrl\_inst.dc\_fifo\_inst.dcfifo\_component System dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1 q[3] dc\_fifo\_dout\_3 0.000 24.213

mds\_top\_inst.disp\_ctrl\_inst.dc\_fifo\_inst.dcfifo\_component System dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1 q[4] dc\_fifo\_dout\_4 0.000 24.213

mds\_top\_inst.disp\_ctrl\_inst.dc\_fifo\_inst.dcfifo\_component System dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1 q[5] dc\_fifo\_dout\_5 0.000 24.213

mds\_top\_inst.disp\_ctrl\_inst.dc\_fifo\_inst.dcfifo\_component System dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1 q[6] dc\_fifo\_dout\_6 0.000 24.213

mds\_top\_inst.disp\_ctrl\_inst.dc\_fifo\_inst.dcfifo\_component System dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1 q[7] dc\_fifo\_dout\_7 0.000 24.213

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Ending Points with Worst Slack

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Starting Required

Instance Reference Type Pin Net Time Slack

Clock

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mds\_top\_inst.disp\_ctrl\_inst.dc\_fifo\_inst.dcfifo\_component System dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1 rdreq dc\_rd\_req 7.519 6.449

global\_nets\_inst.reset\_blk\_inst.rst\_deb\_inst.pll\_d1 System cycloneii\_lcell\_ff datain pll\_locked\_i 19.952 19.597

mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.b\_out[0] System cycloneii\_lcell\_ff sclr b\_out\_1\_sqmuxa\_9 24.526 22.180

mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.b\_out[1] System cycloneii\_lcell\_ff sclr b\_out\_1\_sqmuxa\_9 24.526 22.180

mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.b\_out[2] System cycloneii\_lcell\_ff sclr b\_out\_1\_sqmuxa\_9 24.526 22.180

mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.b\_out[3] System cycloneii\_lcell\_ff sclr b\_out\_1\_sqmuxa\_9 24.526 22.180

mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.b\_out[4] System cycloneii\_lcell\_ff sclr b\_out\_1\_sqmuxa\_9 24.526 22.180

mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.b\_out[5] System cycloneii\_lcell\_ff sclr b\_out\_1\_sqmuxa\_9 24.526 22.180

mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.b\_out[6] System cycloneii\_lcell\_ff sclr b\_out\_1\_sqmuxa\_9 24.526 22.180

mds\_top\_inst.disp\_ctrl\_inst.vesa\_gen\_ctrl\_inst.b\_out[7] System cycloneii\_lcell\_ff sclr b\_out\_1\_sqmuxa\_9 24.526 22.180

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Worst Path Information

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Path information for path number 1:

Requested Period: 7.519

- Setup time: 0.000

+ Clock delay at ending point: 0.000 (ideal)

+ Estimated clock delay at ending point: 0.000

= Required time: 7.519

- Propagation time: 1.070

- Clock delay at starting point: 0.000 (ideal)

- Estimated clock delay at start point: -0.000

= Slack (non-critical) : 6.449

Number of logic level(s): 1

Starting point: mds\_top\_inst.disp\_ctrl\_inst.dc\_fifo\_inst.dcfifo\_component / rdempty

Ending point: mds\_top\_inst.disp\_ctrl\_inst.dc\_fifo\_inst.dcfifo\_component / rdreq

The start point is clocked by System [rising]

The end point is clocked by System [rising]

Instance / Net Pin Pin Arrival No. of

Name Type Name Dir Delay Time Fan Out(s)

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mds\_top\_inst.disp\_ctrl\_inst.dc\_fifo\_inst.dcfifo\_component dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1 rdempty Out 0.000 0.000 -

dc\_fifo\_empty Net - - 0.295 - 2

mds\_top\_inst.disp\_ctrl\_inst.dc\_rd\_req cycloneii\_lcell\_comb datab In - 0.295 -

mds\_top\_inst.disp\_ctrl\_inst.dc\_rd\_req cycloneii\_lcell\_comb combout Out 0.420 0.715 -

dc\_rd\_req Net - - 0.355 - 1

mds\_top\_inst.disp\_ctrl\_inst.dc\_fifo\_inst.dcfifo\_component dcfifo\_work\_top\_synthesis\_top\_synthesis\_rtl\_1 rdreq In - 1.070 -

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Total path delay (propagation time + setup) of 1.070 is 0.420(39.3%) logic and 0.650(60.7%) route.

Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value

##### END OF TIMING REPORT #####]

##### START OF AREA REPORT #####[

Design view:work.top\_synthesis(top\_synthesis\_rtl)

Selecting part EP2C35F672C6

@N: FA174 |The following device usage report estimates place and route data. Please look at the place and route report for final resource usage..

Total combinational functions 3468

Logic element usage by number of inputs

4 input functions 1126

3 input functions 603

<=2 input functions 1739

Logic elements by mode

normal mode 2381

arithmetic mode 1087

Total registers 2230 of 33216 ( 6%)

I/O pins 142 of 475 (29%), total I/O based on largest package of this part.

Number of I/O registers

Output DDRs :0

Total user instantiated Altsyncrams: 2

DSP.Simple\_Multipliers\_9\_bit: 2

DSP Blocks: 1 (2 nine-bit DSP elements).

DSP Utilization: 2.86% of available 35 blocks (70 nine-bit).

ShiftTap: 0 (0 registers)

Total ESB: 40196 bits

##### END OF AREA REPORT #####]

Mapper successful!

Process took 0h:02m:03s realtime, 0h:00m:35s cputime

# Tue Apr 02 16:12:47 2013

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